WP-1004 Designing an Accurate SPICE Macromodel for Ultra-Low Power, Rail-to-Rail CMOS Op Amps

SPICE modelling is an integral part of designing complex electronic devices, because it allows engineers to eliminate many mistakes when building working prototypes, thus reducing time-to-market. Operational amplifiers (op amps) are the most widely used analog integrated circuits (IC). Accurate and fast models can be extremely helpful in the design process.

Using macromodels instead of micromodels greatly reduces simulation time, especially when simulating circuits containing several op amps. However, designing an accurate and fast macromodel with minimum convergence problems is quite a challenge.

Most op amp macromodels are based on work by Boyle, Cohn, Pederson, Solomon [1] and Alexander and Bowers [2]. However, these topologies have some limitations and inaccuracies, especially for ultra-low power op amps with high open loop output impedance.

Designing an Accurate SPICE Macromodel

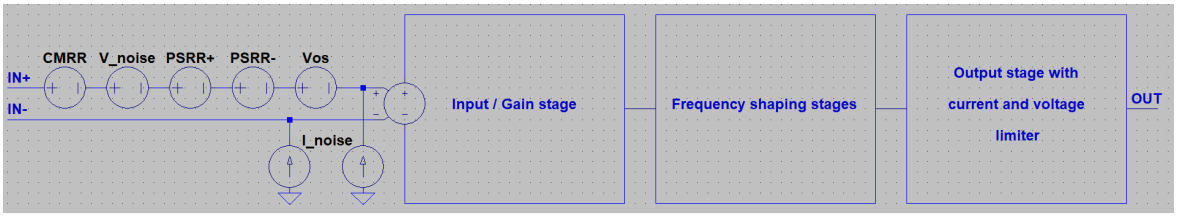

Figure 1. Op amp macromodel simplified schematic

A simplified schematic of the proposed macromodel is shown in Figure 1. It consists of several cascaded sections: an Input/Gain stage, with input referred error sources (CMRR, voltage noise, current noise, PSRR+, PSRR-, Vos); frequency shaping stages; and an output stage with a current and voltage limiter.

The following parameters are modeled:

- Open loop gain and phase with RL and CL effects
- AC/DC common mode rejection ratio
- AC/DC power supply rejection ratio
- Positive and negative slew rate
- Input common mode voltage range
- Input voltage noise with 1/f
- Input current noise with 1/f
- Input bias current with common mode and temperature effects
- Input offset current with temperature effects
- Input offset voltage with temperature effects
- Input impedance
- Output current through the supply rails
- Output current limit with temperature effects
- Output voltage swing from rails with RL effects
- Output impedance
- Quiescent current vs supply voltage with temperature effects
- Maximum supply voltage breakdown

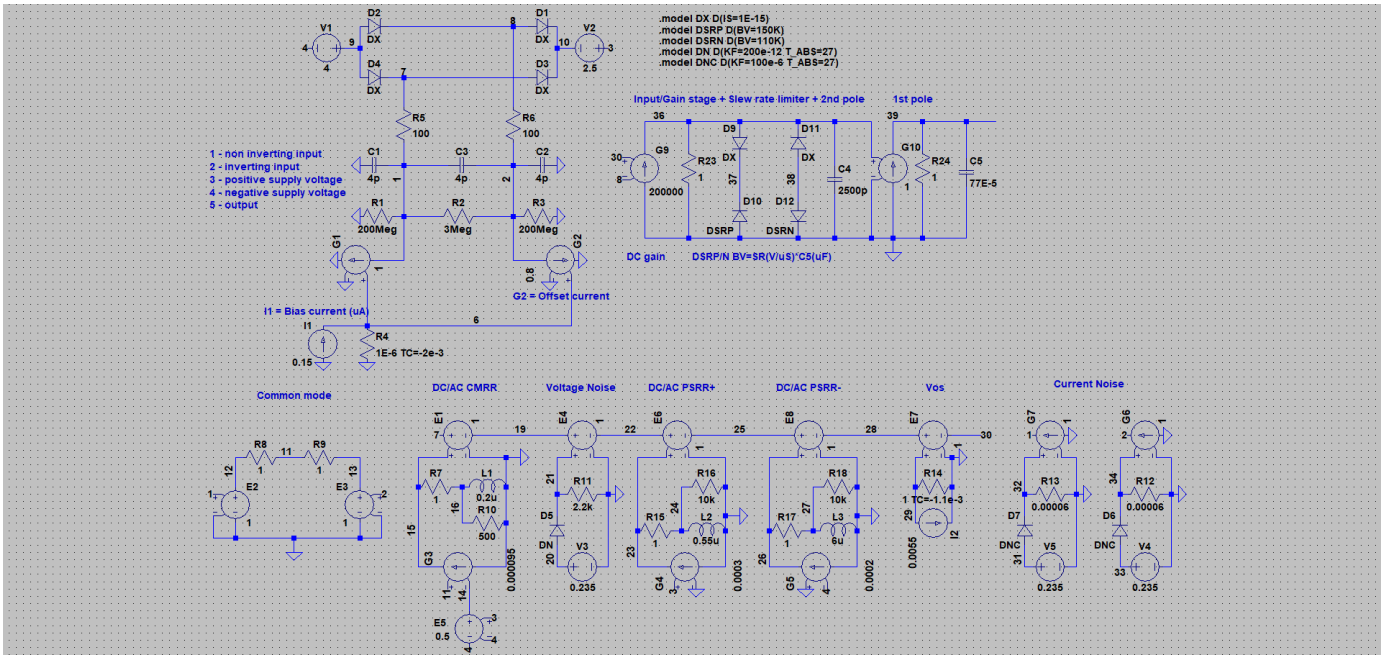

Figure 2. Input stage done only with diodes, passive components, and fixed and dependent current and voltage sources (e.g., BJT input op amp)

Boyle and Alexander use a gain normalized input differential transistor stage that doesn't represent the real input stage of an op amp. Therefore, input parameters like common mode input range, offset voltage, offset current, bias current, CMRR, PSRR, input impedance, voltage noise, current noise, and temperature performance are not accurately modelled.

A simpler, faster, and more accurate input stage can be modelled without transistors. One can instead use only diodes, passive components, and fixed and dependent current and voltage sources. An example of such a stage for a BJT input op amp is shown in Figure 2. The notation is as follows:

C1, C2, C3, R1, R2, R3 - represent input common mode and differential capacitance and resistance.

I1, R4, G1, G2 - input bias and offset current with temperature dependencies.

D1-D4, V1, V2, R5, R6 - input common mode voltage range.

I2, R14, E7 - offset voltage with temperature effects.

E5, G3, R7, L1, R10, E1 - DC/AC CMRR.

G4, R15, L2, R16, E6 - DC/AC positive PSRR.

G5, R17, L3, R18, E8 - DC/AC negative PSRR.

V3, D5, R11, E4 - voltage noise spectral density, where R11 represents the white noise portion and V3, D5 - 1/f noise portion.

V5, D7, R13, G7, V4, D6, R12, G6 - current noise spectral density, where R12 and R13 represent the white noise portion and V5, D7, V4, D6 - 1/f noise portion.

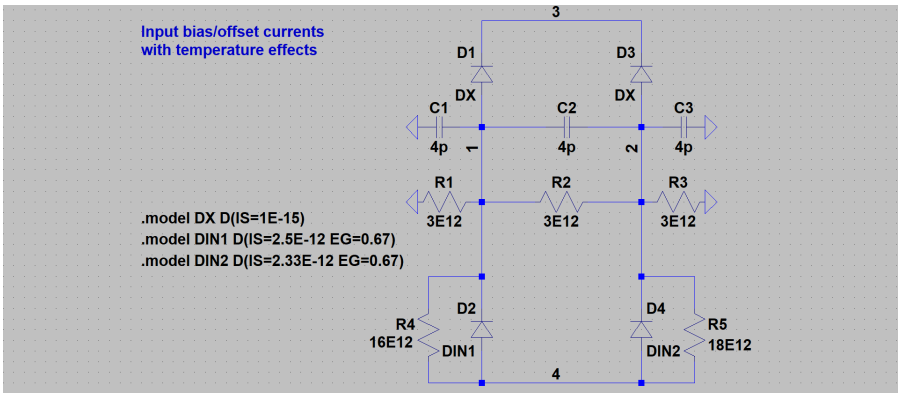

Figure 3. CMOS rail-to-rail input stage with very low input offset and bias currents

Figure 3 shows the input stage for a rail-to-rail CMOS op amp with very low input offset and bias currents. Such low currents and temperature dependencies are modelled with different diodes D1-D4 and resistors R4 and R5. The difference between the saturation current (IS) of diodes DX and DIN1 defines the bias current, while the difference between the saturation currents (IS) of diodes DIN1 and DIN2 defines the op amp offset current. The temperature dependence of the diode's saturation current is defined by the parameters EG (the band gap energy) and XTI (the saturation current temperature exponent).

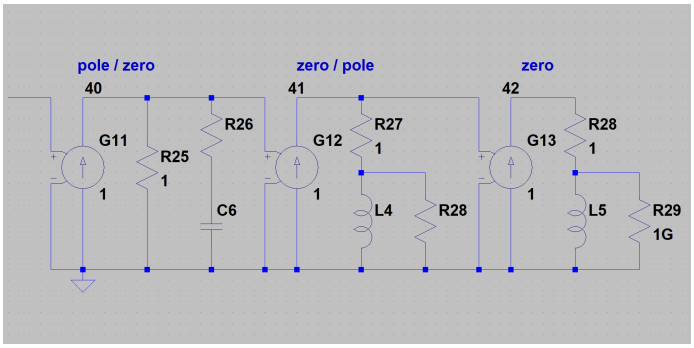

Figure 4. Three types of frequency shaping stages

In Figure 2, the op amp DC open loop gain is determined by G9. Diodes D9-D12 form the slew rate limiting circuit, where the reverse breakdown voltage (BV) of diodes DSRP and DSRN defines the positive and negative slew rate limit (BV=SR(V/µs)*C5(µF)). Resistor R23 and capacitor C4 form the second pole, and resistor R24 and capacitor C5 form the dominant pole of the op amp. Different types of op amps need more than two poles to accurately simulate open loop gain and phase. In this case, more frequency shaping stages can be added as shown in Figure 4. In gain/frequency shaping stages, all gain resistors were selected to be 1 Ohm for almost noiseless operation.

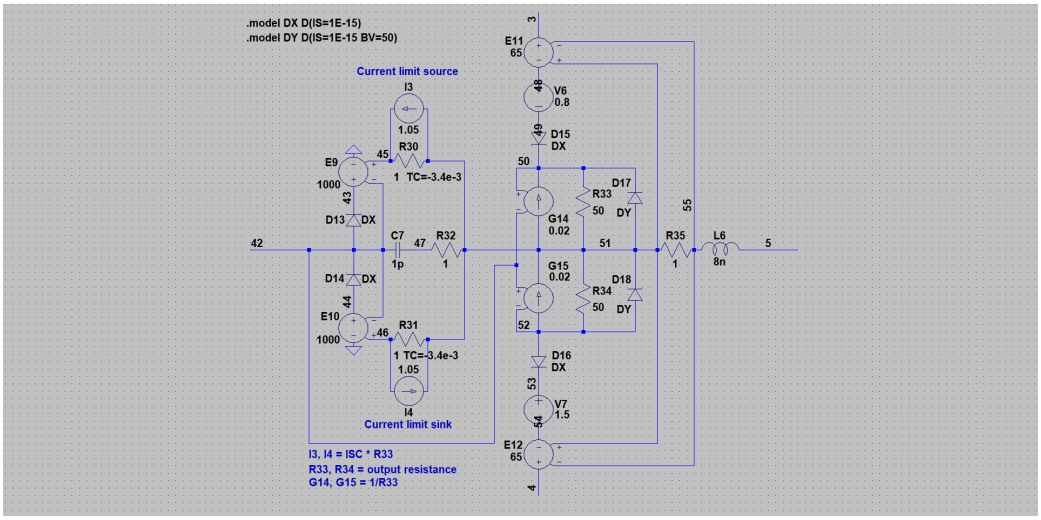

Figure 5. Universal output stage for SPICE macromodel (e.g., low open loop output resistance)

Compared with [2], the proposed output stage (see Figure 5) can simulate not only the output stage output impedance and output current through the supply rails, but also the maximum output voltage swings with RL effects. Also, the short-circuit current limiter with temperature dependencies works not only with low impedance output stages, but with high impedance output stages too.

G14, R33, G15, R34, L6 and D15-D18 represent the output stage with proper output impedance and output current through the supply rails. R33, R34 = output resistance; G14, G15 = 1/R33.

E9, E10, D13, D14, I3, R30, I4, R31 - temperature dependent short-circuit current limiter.

I3, I4 = Isc * R33.

E11, V6, V7, E12 - maximum output voltage swings with RL effects. V6, V7 = output swings from rails without load; E11, E12 = load dependent output swings from rails.

R32, C7 - load dependent frequency shaping (if needed by op amp design).

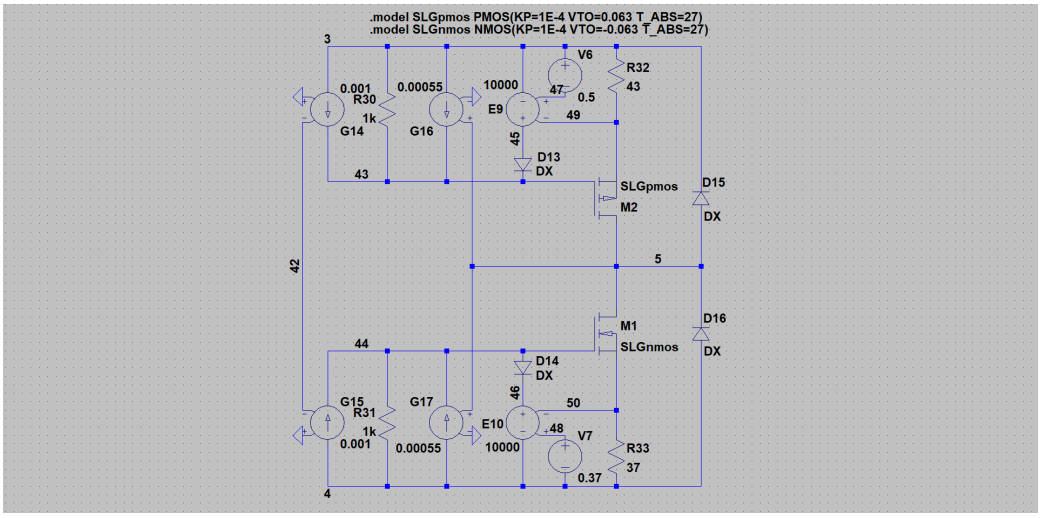

Figure 6. CMOS ultra-low power rail-to-rail output stage

In ultra-low power rail-to-rail op amps such as the SLG88103V/SLG88104V, the common source output stage works with a tiny bias current around 100 nA. In the case proposed above, the universal output stage for the SPICE macromodel is not completely right, because it doesn't simulate the output stage transistors' transconductance (gm) variations when external DC bias current is applied. A new output stage for the SPICE macromodel was designed as shown in Figure 6.

M1 and M2 form the rail-to-rail output stage. Parameters KP and VTO determine the output stage bias current, and with G16, G17 - output resistance.

R32, R33 - load dependent output swing from rails.

E9, E10, D13, D14, V6, V7, R32, R33 - short-circuit current limiter.

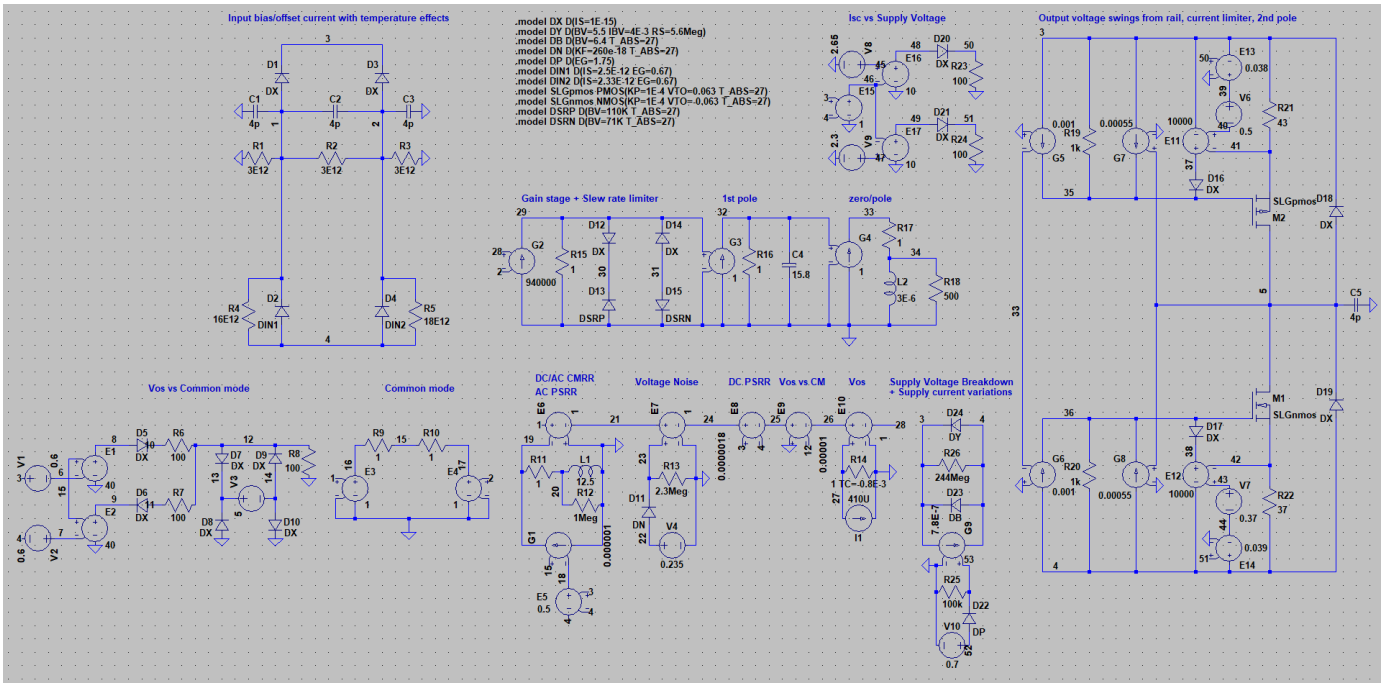

Figure 7. SLG88103V/SLG88104V complete SPICE macromodel

Figure 7 shows the complete SLG88103V/SLG88104V SPICE macromodel. Some additional elements were added to further increase simulation accuracy:

D24, R26, D23, G9, R25, D22, V10 - Quiescent current vs supply voltage with temperature effects and supply voltage breakdown.

V1, V2, E1, E2, D5, D6, R6, R7, D7-D10, V3, R8, E9 - Vos vs. common mode variations.

V8, V9, E15, E16, E17, D20, D21, R23, R24, E13, E14 - Short circuit current vs. supply voltage.

Simulation accuracy comparison

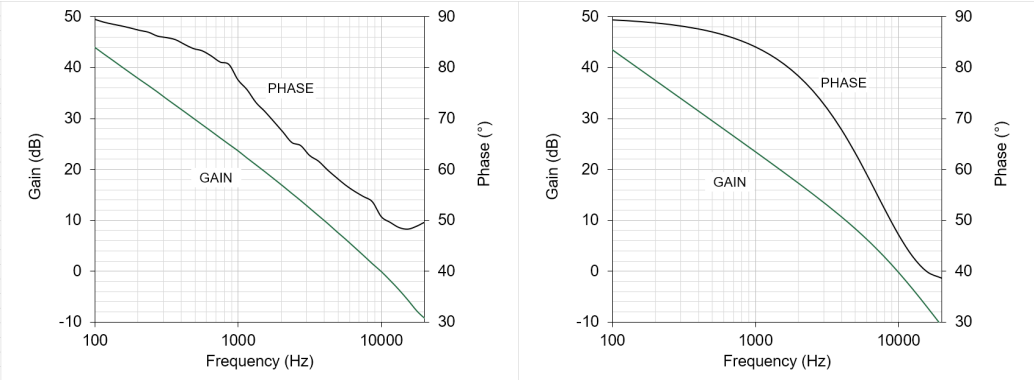

Figure 8. Measured (left) and simulated (right) Gain and Phase response

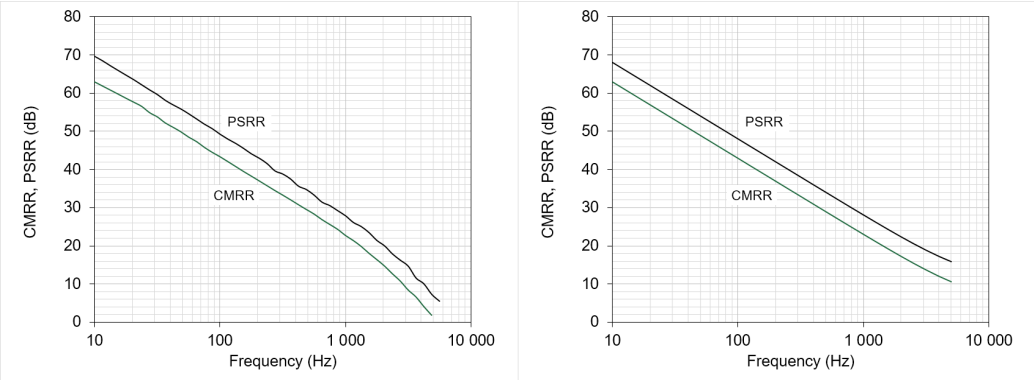

Figure 9. Measured (left) and simulated (right) CMRR and PSRR

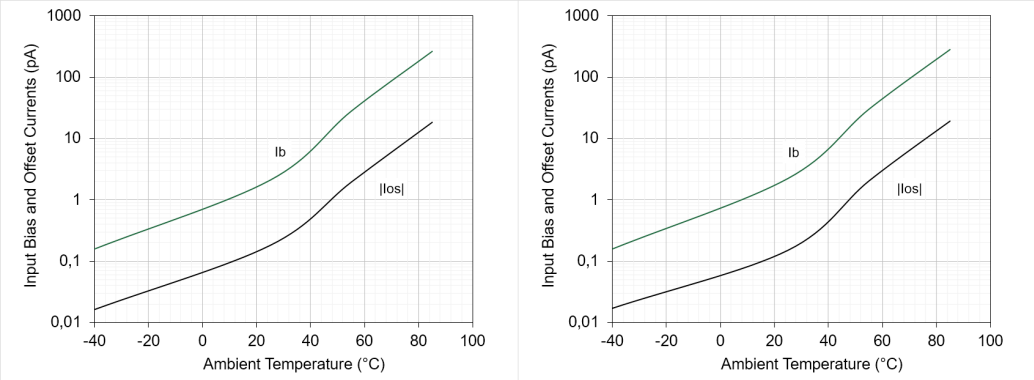

Figure 10. Measured (left) and simulated (right) input bias and offset currents vs. ambient temperature

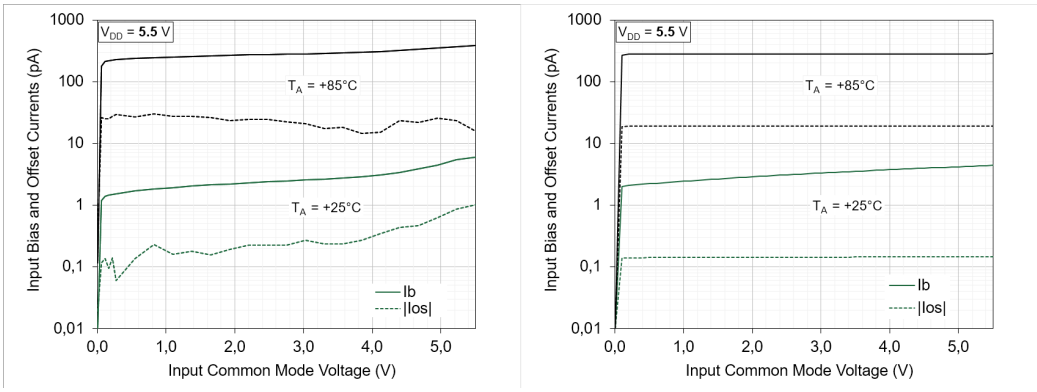

Figure 11. Measured (left) and simulated (right) input bias and offset currents vs. common mode voltage

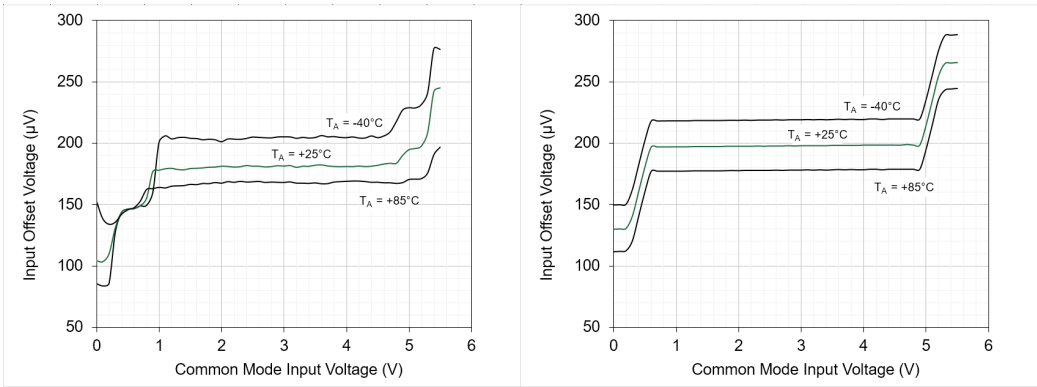

Figure 12. Measured (left) and simulated (right) input offset voltage vs. common mode input voltage (VDD=5.5 V)

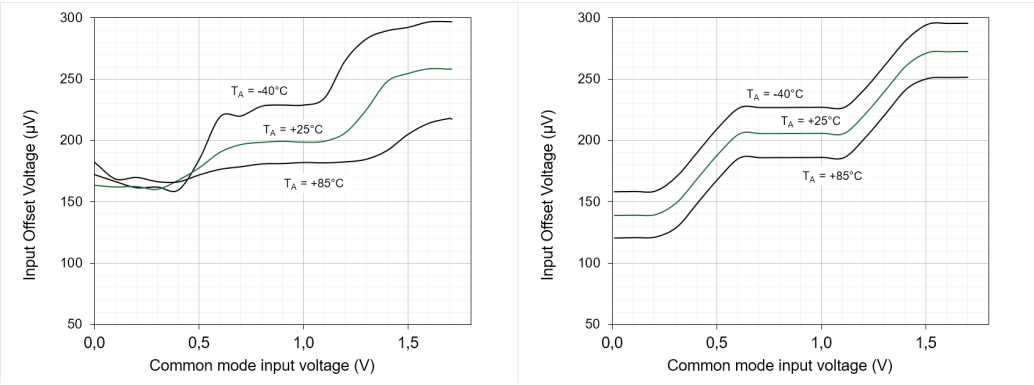

Figure 13. Measured (left) and simulated (right) input offset voltage vs. common mode input voltage (VDD=1.71 V)

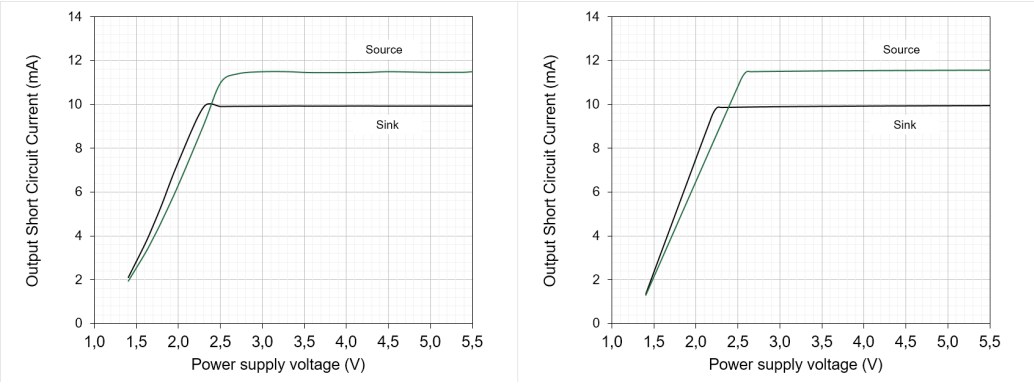

Figure 14. Measured (left) and simulated (right) output short circuit current vs. power supply voltage

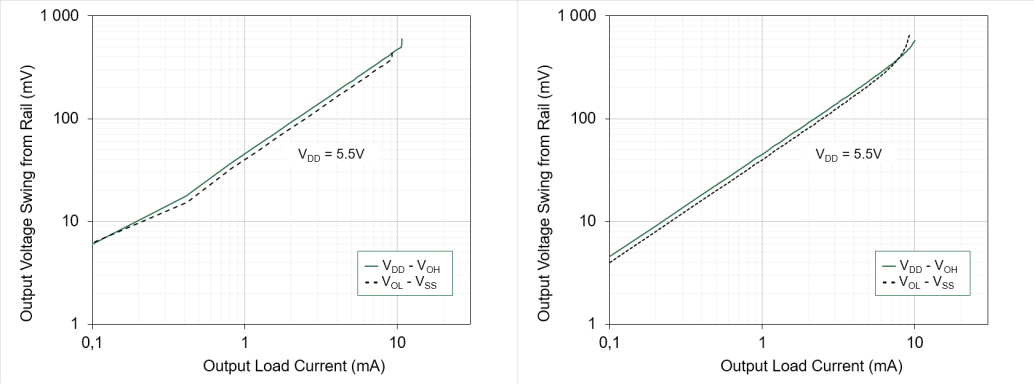

Figure 15. Measured (left) and simulated (right) output voltage swing from rail vs. output load current

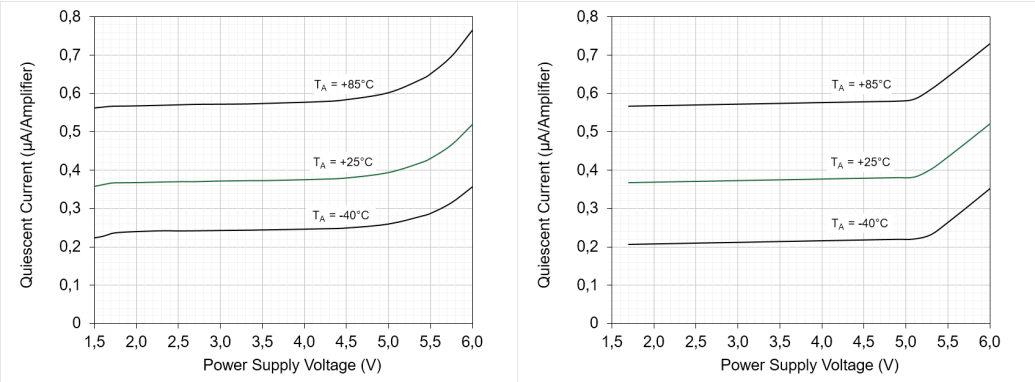

Figure 16. Measured (left) and simulated (right) quiescent current vs. power supply voltage

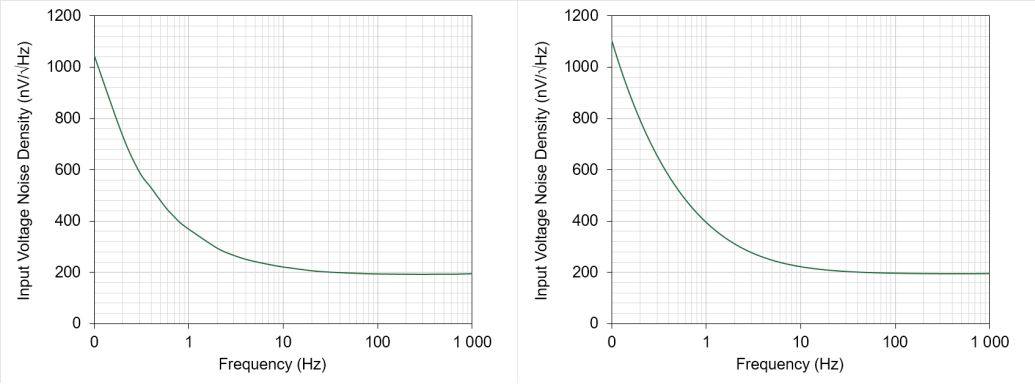

Figure 17. Measured (left) and simulated (right) input noise voltage density vs. frequency

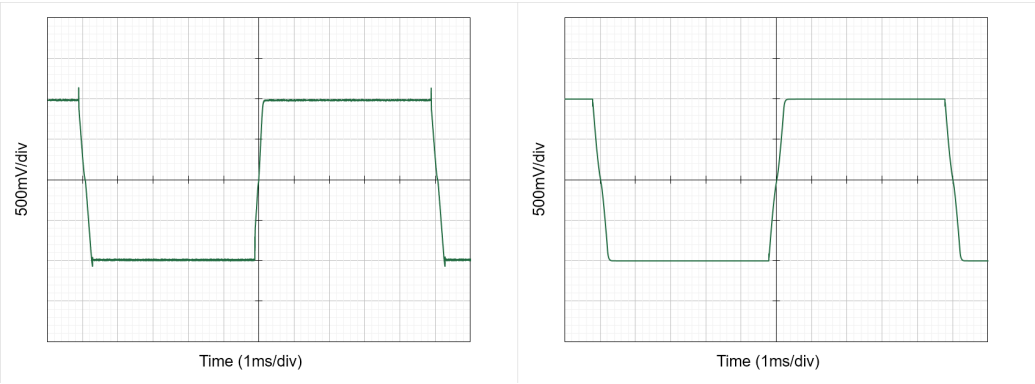

Figure 18. Measured (left) and simulated (right) large signal non-inverting step response

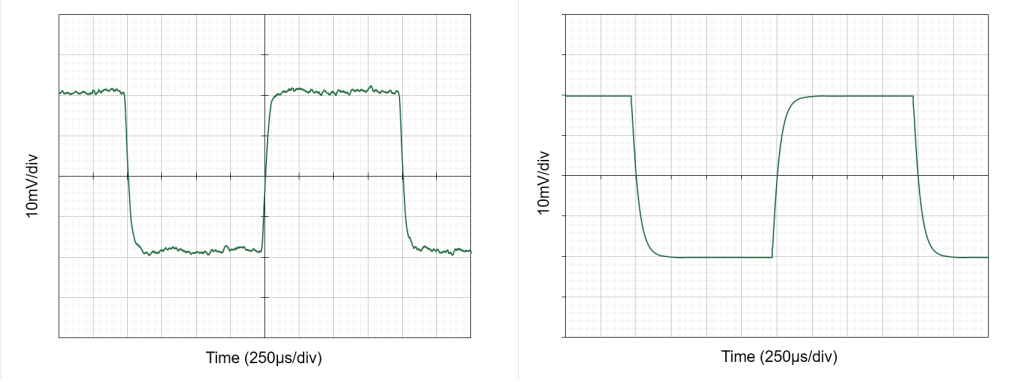

Figure 19. Measured (left) and simulated (right) small signal non-inverting step response

Conclusion

An accurate, fast, and comprehensive SPICE macromodel for a voltage feedback op amp was developed. It can be very easily adopted for other voltage feedback amplifiers.

References

↑ 1. Boyle, Cohn, Pederson, Solomon "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid State Circuits, Vol. SC-9, No. 6, December 1974

↑ 2. Alexander, Bowers "SPICE-Compatible Op Amp Macro-Models", Precision Monolithics Inc., AN-138, March 1990

About the Author

Name: Nazar Shtybel

Background: Nazar Shtybel graduated from Lviv Polytechnic National University in 2007 studying at the Department of Telecommunications, Radio electronics & Electronic Engineering. He has more than 10 years of experience in analog and mixed signal circuit design.

Contact: appnotes@silego.com

Files

- WP-1004 Designing an Accurate SPICE Macromodel for Ultra-Low Power, Rail-to-Rail CMOS Op Amps.pdf- (1.2 MB)
- WP-1004.zip- (902 KB)

See full list of Application Notes