HIGH PERFORMANCE DUAL DOLBY B-TYPE NOISE REDUCTION IC FOR LOW VOLTAGE APPLICATIONS

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1. Introduction

Recent advances in tape transport mechanism, tape head, and headset design have led to significant fidelity improvements of personal portable stereo playback and record/play systems using only two 1.5V battery cells.

Although new types of magnetic tape materials show improved high frequency, high level characteristics (metal alloy tapes) and improved noise characteristics (low noise tapes), the dynamic range of compact cassette tapes remains fundamentally limited, thus application of noise reduction systems remains attractive.

The most popular complementary noise reduction system for medium quality HI-FI record-play machines is undoubtedly the Dolby* B-type, yielding nearly 10dB dynamic range improvement. Since a large selection of prerecorded program material is available, this system is ideally suited for the predominantly playback only personal portable models. Low voltage B-type integrated circuit processors only recently became available. The objective of the present design was to develop an IC with superior performance and versatility.

2. System Description

The block diagram of a B-type Dolby noise reduction system is shown in Figure 1.

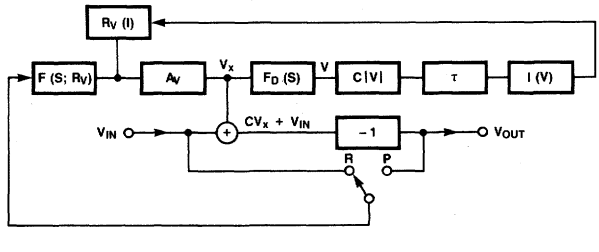

Figure 1. B-Type Dolby Noise Reduction System

In record mode, the input signal is fed to a high-pass filter, with a transfer function of F (s; R_V), where s is the complex frequency variable and R_V is the variable resistance termination of the filter. The value of R_V is controlled by the current I, generated in a control loop.

The output signal of the variable high-pass filter is amplified and fed to the control loop input, x, and the summing circuit, where it is combined with the original input, V_{IN}. The output voltage is

$$V_{OUT} = -V_{IN}\,[F\,(s;\,R_V)\,cA_V + 1] \qquad (1)$$

where c is the side chain summing constant. The amplitude response a (w) may be written as

$$a\,(w) = 20\,\log\,|V_{OUT}/V_{IN}| = 20\,\log|F\,(s;\,R_V)\,cA_V + 1| \qquad (2)$$

Although it is not shown explicitly in this equation, a (w) is both frequency and level dependent. The level dependence is caused by the side chain control loop and it is incorporated into this equation through R_V. More details are given in the Appendix.

The system of Figure 1 boosts low level/high frequency components of the input signal sufficiently ABOVE the tape noise BEFORE it is recorded. In order not to alter the signal composition by this compression, it is processed complementarily during playback.

3. The Steady State Equations

Since Dolby Laboratories defines the frequency and level dependent steady state response in form of a specification table and transient response in form of a hardware standard, a mathematical representation of the static characteristics suitable for analytical approach was developed. First, the transfer equation for the side chain filter of Figure 2 is determined (Appendix 1):

$$F\,(jw;\,R_V) = \frac{-w^2T_1T_2R_V}{R_V\,(1 - w^2T_1T_2) + R_1R_2 + \cdots} \cdots \frac{+jwT_1R_V}{+jw\,[R_V\,(T_1 + T_2) + R_1R_2\,(C_1 + C_2)]}$$

where $T_1 = R_1C_1$ and $T_2 = R_2C_2$

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Substituting this into equation (1) yields a quadratic equation (Appendix 2) in the form of

$$R_V^2[D(R^2+T^2)-(V^2+W^2)]-$$
$$-2R_V[S(DR-V)+(DT-W)]+$$
$$+(D-1)(S^2+U^2)=0$$

where parameter D represents the frequency dependency for a given input level as it is defined by equation (A2-2) of the Appendix. Solution of this equation for variable R_V, for any combination of input level and frequency provides a two-variable function, $R_V(V_{IN}; f)$. Regardless of the type of control loop used, it always has to generate R_V according to this equation, so long as the high-pass filter configuration of Figure 2 is used in conjunction with a variable resistance.

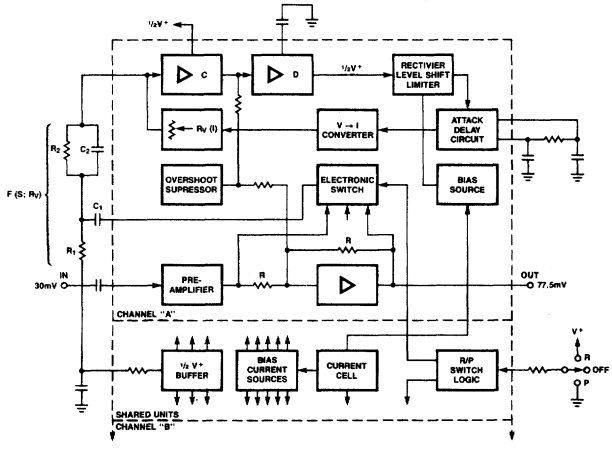


Figure 2. Block Diagram of the Dual Record/Play IC

4. Computer Modeling

In order to analyze the system of Figure 1 and its integrated circuit implementation of Figure 2, an interactive simulator has been developed, using an HP 9845B desktop computer. The main elements of the simulator are shown in Figure 3.

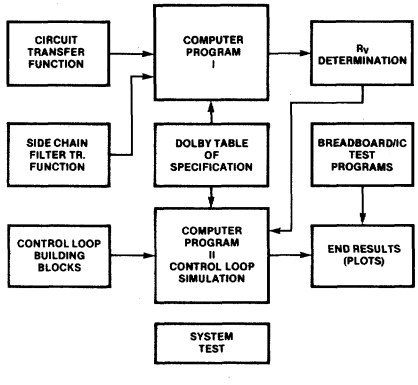


Figure 3. The Interactive Dolby B-Type Simulator

The focus is on providing a flexible and efficient means of modeling hardware, performing experiments on error sensitivity and exploring ways of improving circuit performance. An interesting by-product of the selected method is the ability to deduce the ideal transfer curves for the voltage-to-resistance converter in the side chain (in the present case it is a voltage to current-to-resistance converter system) from the ideal Dolby-specified transfer curves. It is also possible to compute the required curves with a given error from the ideal specified gains (Figure 4). This feature can be useful in providing a better view of the performance trade-offs and sensitivities in the voltage to current converters.

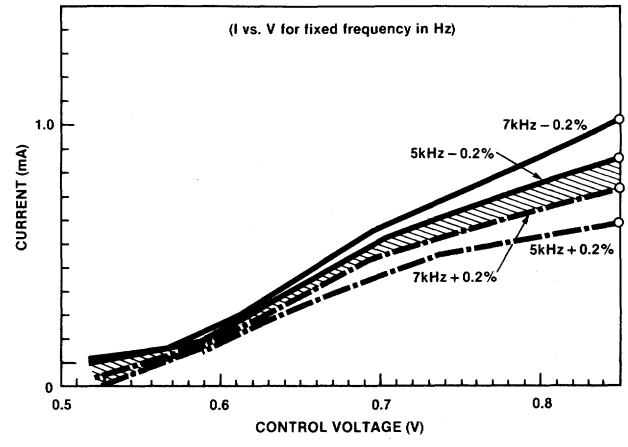


Figure 4. I (V) Converter Curve Variations Causing ±2% Dolby Transfer Curve Error

The modeling system has been designed to be modular (the system is divided into subcircuits such as op amps and filters) and provides information on the input and output signals of each hardware block or subcircuit.

Some applications of these features were: assessing how to decrease circuit voltage for a low voltage power supply system, examine the effect of transistor and resistor variations, and check voltage-to-current converter characteristic sensitivities and certain threshold and bias sensitivities. In some cases, where it was impractical to derive standard equations for a particular hardware solution, the circuit was sampled by computer and fitted by polynomials with a high degree of accuracy. Once this was done, the effects of component parameter variations were examined.

Since there is a feedback loop in the side chain from the variable filter output (Figure 2) through the voltage converter, an iterative method was used. This was preferred because it is adaptable for different circuits and because the nonlinear rectifiers and voltage converters would make an exact equation difficult to derive.

The method is to find the input signal to the side chain filter by assuming an initial value for R_V, then open the feedback loop at some convenient point (such as variable resistance) and iteratively find the relevant feedback characteristic at that point by comparing guesses at the value with the value obtained while traversing the loop until they match within a certain tolerance.

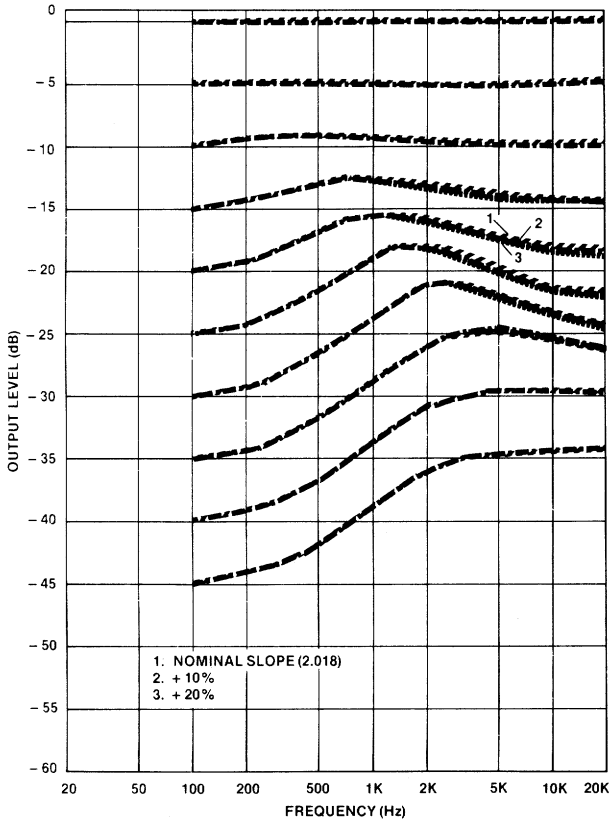


Figure 5. Computed Transfer Curves of the System of Figure 2

We can consider the guess and the returned value as X and F (x), respectively. Since the circuit is stable, X = F (x) somewhere, or G (x) = F (x) – X = 0, and assuming there is a "zero crossing" of G (x), we can find a $X_a = F(X_a)$ and $X_b = F(X_b)$. We fine two such points, then split the interval between them and retain the subinterval that contains the zero as our new interval, stopping when we find an answer which is close enough.

After the iteration has converged, the output can be calculated from the state of the side chain and the input signal to the circuit. A sample plot showing the effect of slope (resistance) variations of the rectifier is shown in Figure 5.

The derivation of the ideal voltage-to-current-to-resistance characteristic is accomplished by first finding the necessary filter resistance R_V. The output of each stage from the constant gain amplifier, A_V (Figure 1), depends on the main input and the side chain input to the output amplifier. The main input is independent of the side chain and depends solely on the input to the stage, while the side chain input comes from the filter and is thus a function of the stage input and the filter resistance. Therefore, at a given input and specified stage output, the filter resistance is uniquely defined.

5. Integrated Circuit Implementation

Dolby B-type noise reduction systems designed for 8–20V supply voltage have a rectifier output control voltage range of about four volts. In a low voltage system, designed for a minimum supply voltage of 1.5V, the control voltage range must be reduced by over a factor of 3. Since system accuracy heavily depends on control voltage accuracy, the lower the control voltage range, the more difficult it is to maintain specified accuracy.

The objective of the present design was to achieve low voltage operation without compromising system accuracy. In order to accomplish this:

a. new subcircuit blocks able to handle input and output signal swings near the supply voltage have been developed,

b. error correction schemes, and process-insensitive design techniques were used,

c. noise sources were minimized in order to maintain signal-to-noise ratio equal to or better than what is available in previous designs.

One channel and the shared units are shown in Figure 2. The main signal path spans through the pre-amplifier and the summing amplifier to the output.

Depending on the setting of the electronic record/play switch, the side chain receives its input signal either from the pre-amplifier or the summing amplifier output. The amplified side chain signal is added to the main path through suming resistors R_a, R_b and R_f, in-phase in record mode, opposite phase in play mode.

The control loop begins with amplifier D and continues through the rectifier, attack/decay circuit, to the variable resistance block.

The shared units provide the various bias voltages and currents. All bias currents are derived from a cascaded peaking current source [1], which provides relatively supply-independent current with about 2800 ppm/degree temperature coefficient to compensate for the temperature dependence of the op amp transconductances. Except for diode forward voltage biases, stable voltage references are not needed for this design.

The present design uses a Dolby reference level of 77.5mV and a corresponding input level of 30mV, giving a typical signal-to-noise ratio (CCIR ARM) of 69/72/81dB in record/noise reduction off/and play modes, respectively, when the input is terminated by 10kΩ. The relatively low reference level and the use of rail-to-ground output swing op amps provide an unusually large headroom: 17dB at 1.8 volt supply voltage. The schematic diagram of the new op amp is shown in Figure 6 [2].

The input stage consists of a PNP/NPN differential pair and the current combiner. The input devices are arranged as thermally balanced quads. Since the PNP and NPN base currents have opposite polarity, a first order bias current cancellation will occur.

The output stage is a simplified Widlar-scheme. It has two distinct signal paths for the positive and

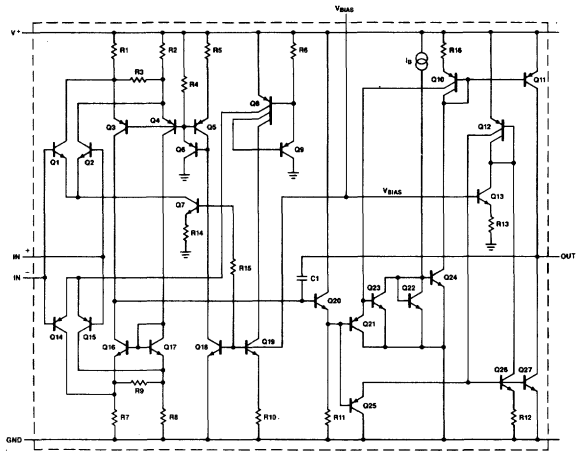


Figure 6. Operational Amplifier with Rail to Ground Input/Output Swing

negative half cycles, respectively. Each path has its own local feedback loop to achieve approximate matching of the open loop gains.

The pre-amplifier and amplifiers C and D use the same basic op amp cell with minor modifications, depending on the particular requirements.

The electronic record/play switch has three input quads, all connected to the same current combiner. Their tail currents are switched by the logic circuitry. A conceptual schematic is shown in Figure 7.

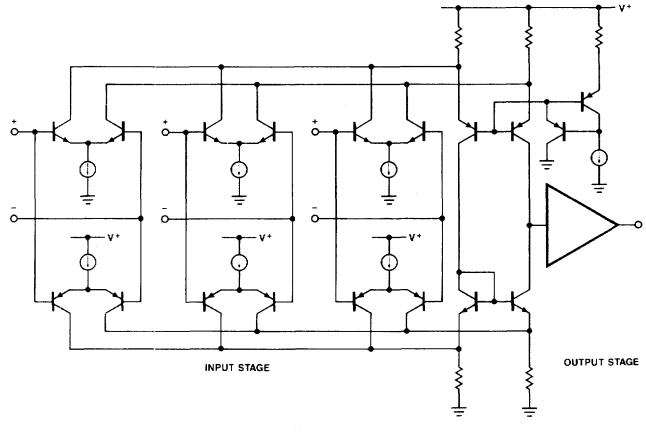


Figure 7. Electronic Switch

Amplifier D has a high-pass characteristic as specified by Dolby Laboratories. The input and output are Schottky diode clamped to prevent excessive overdrive of the rectifier under extreme transient conditions.

The conceptual schematic of the full wave rectifier and the attack/decay circuit is shown in Figure 8. The rectifier has current inut and output. The gain is controlled by the internal mirror ratios. Rectifier threshold of conduction is set by the current sink, I_{TH}. The output stage is an inverting configuration with a V_{be} multiplier in the feedback acting as a limiter. The circuit is biased by 500mV reference voltage that has

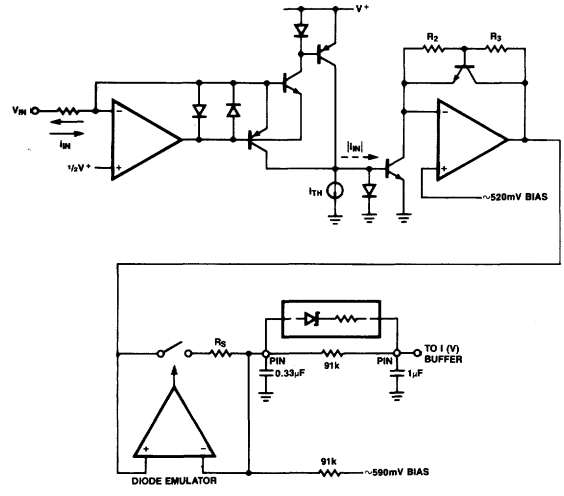


Figure 8. Full Wave Rectifier and Attack/Decay Circuit Concept

V_{be} tracking temperature coefficient. In order to maintain large control range even at low power supply voltages, the germanium diode used in the original discrete circuit has been replaced by a one directional switch with only a few millivolts voltage drop in the conducting direction. The switch is driven by a comparator that senses the voltage polarity across its input and output. Q23 and Q24 of Figure 9 do the actual switching. Each device has its own base current drive in the "on" mode to allow rail to ground signal range. Since this switch doesn't have the smoothness of a germanium diode, those characteristics were provided in the rectifier and voltage-to-current converter.

The "speed-up" diode of the attack/decay circuit has been implemented by a Schottky diode-resistor network.

Compared to the discrete implementation, the values of the external capacitors in the attack/decay circuit have been increased, and the associated resistors decreased by a factor three to minimize dc error due to I(V) converter buffer bias currents flowing through large value resistors. Bias current errors in the buffer have been minimized.

The voltage-to-current-to-resistance converter is shown in Figure 10. The core of the variable resistance is a differential quad driven by the control current of Q13. The loop around the quad is closed by the PNP mirrors Q3-4, creating a floating resistance of $4V_t/I_C$ where I_C is the control current. To prevent imbalances causing audible dc level shift under tone burst conditions, the quad core and the top mirrors were arranged to minimize thermal effects. The PNP mirror, Q3-4 and the NPN mirror, Q12-17 were base current error compensated. Q7-9 and Q15 provide alpha error compensation for the core.

The circuit is driven by a low impedance buffer biased to 500mV under no control signal condition, therefore the current through R231 is very small. Due to dc errors propagating through previous stages, however, some current could flow, decreasing the variable resistance value below the one megohm

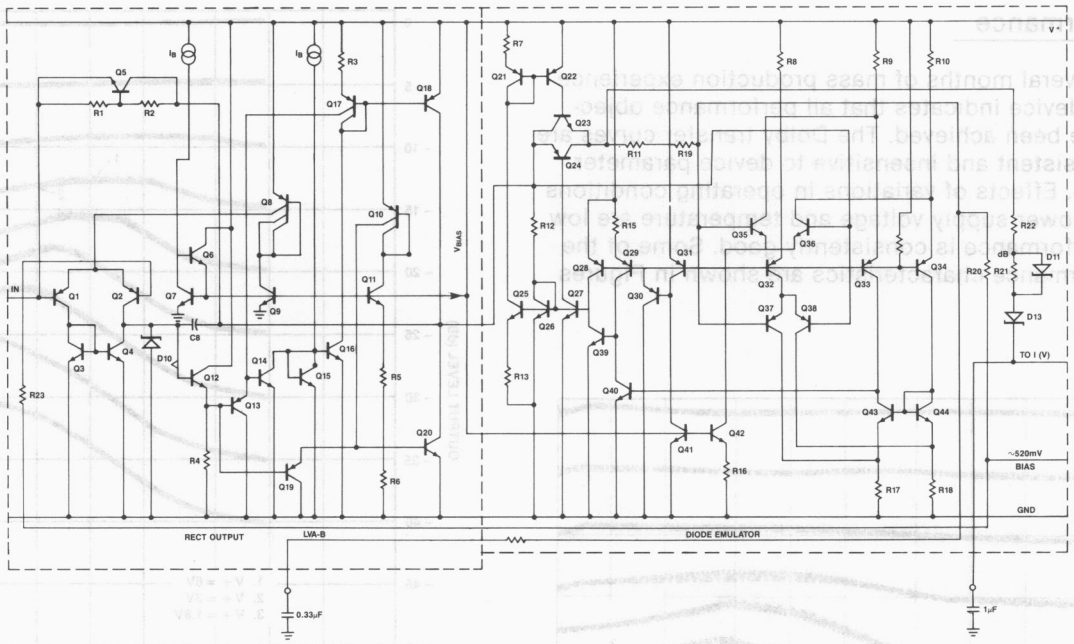


Figure 9. Full Wave Rectifier and the One Directional Switch

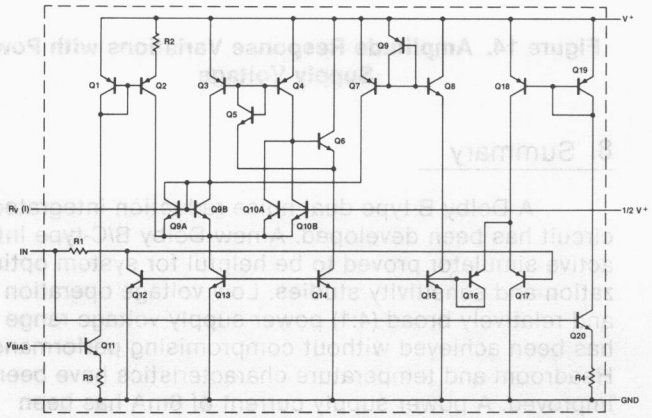


Figure 10. Voltage-to-Current-to-Resistance Converter

minimum required to obtain the specified 10.3dB boost at weak high frequency input signals. To desensitize the system to this type of error, an auxiliary current of about 250nA is subtracted from the quad core tail current (Q2).

The control current of Q13 varies over four decades within the dynamic range of the audio signal, therefore the mirror bias currents of Q14 and Q18 were designed to track the control current. The alpha correction is also dynamic.

6. Device Fabrication

High density dual layer metal, low noise fabrication process was used with ion implantation. Some of the subcircuit blocks such as the op amps and the peaking current source were pre-fabricated to shorten the development cycle. The main characteristics of these units (for example: the quiescent current, peak output current and compensation capacitances of the op amps) were set by a few external components to provide maximum flexibility. The device is housed in a 20-pin plastic SO package. Die photograph is shown in Figure 11.

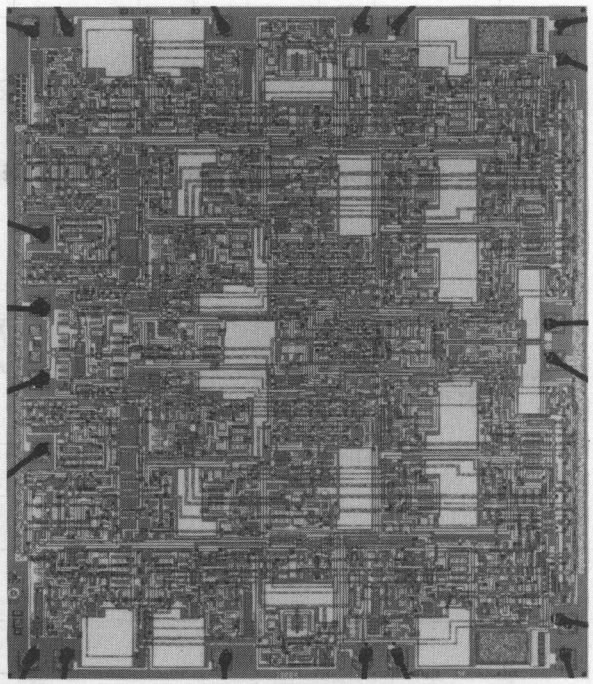


Figure 11. Die Photograph of the Noise Reduction Circuit

7. Performance

Several months of mass production experience with the device indicates that all performance objectives have been achieved. The Dolby transfer curves are quite consistent and insensitive to device parameter variations. Effects of variations in operating conditions such as power supply voltage and temperature are low. Noise performance is consistently good. Some of the key performance characteristics are shown in Figures 12-14.

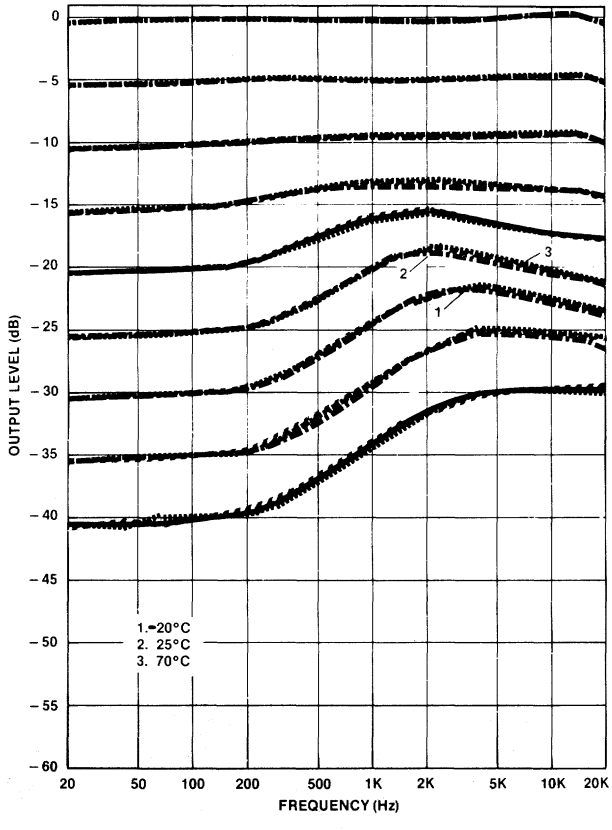


Figure 12. Amplitude Response Variations with Temperature

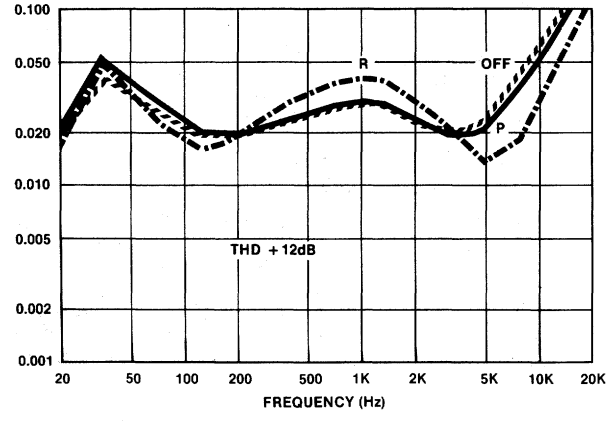


Figure 13. Distortion Plus Noise at +12dB Input

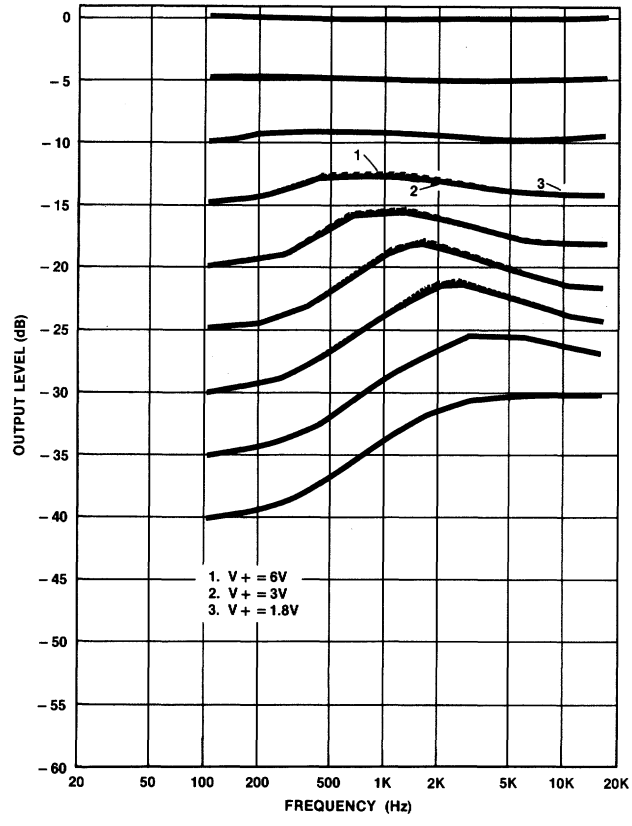


Figure 14. Amplitude Response Variations with Power Supply Voltage

8. Summary

A Dolby B-type dual noise reduction integrated circuit has been developed. A new Dolby B/C-type interactive simulator proved to be helpful for system optimization and sensitivity studies. Low voltage operation and relatively broad (4:1) power supply voltage range has been achieved without compromising performance. Headroom and temperature characteristics have been improved. A power supply current of 6mA has been achieved. Schottky diodes were used successfully to achieve over 3:1 down-scaling of the control voltage range. A modular circuit design concept using subcircuit library cells has contributed to the reduction of development cycle.

Acknowledgements

The authors wish to express their appreciation to R. A. Blauschild who contributed the rail to ground op amp input stage with the current combiner, Derluen Pan and Brian Conte for the Dolby simulator program development, Janet Larson for the layout and William D. Mack for the superb device/process characterization support.

References:

[1] V. Gheorghiu A. A. Vild-Maior: Optimum Design of Two Cascaded Peaking Current Sources. IEEE Solid-State Circuits, Vol. SC-16, pp 415-417.

[2] R. A. Blauschild, L. Burgyan: Patent Applications.

Appendix 1. Derivation of the Side Chain Transfer Function, F (s; R_V)

The side chain filter configuration is shown in Figure 15, where R_V represents the variable resistance determined by the control loop.

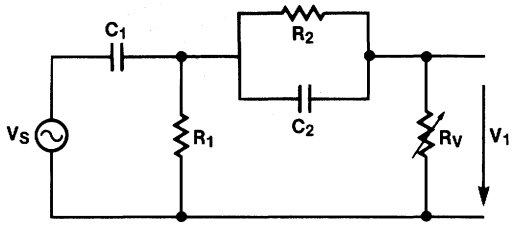


Figure 15. Side Chain Filter

The Thevenin equivalent of V_S, R_1 and C_1 can be determined as

$$I_{s.c.} = V_S/(1/sC_1) = V_S sC_1$$

$$V_{o.c.} = V_S [R_1/(R_1 + 1/sC_1)] = V_S [sT_1/(1 + sT_1)]$$

where $T_1 = R_1C_1$

$$Z_{eq} = V_{o.c.}/I_{s.c.} = sT_1/(1 + sT_1)sC_1 = R_1/(1 + sT_1)$$

Replacing R_2 and C_2 with Z_2:

$$Z_2 = R_2 (1/sC_2)/R_2 + 1/(sC_2) = R_2/(1 + sT_2)$$

where $T_2 = R_2C_2$

The new equivalent circuit is shown in Figure 16.

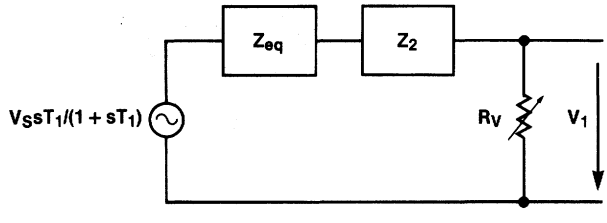


Figure 16. Equivalent Circuit

From the figure

$$V_1 = V_S [sT_1/(1 + sT_1)] [R_V/R_V + Z_2 + R_{eq})]$$

and

$$\frac{V_1}{V_S} = \frac{sR_VT_1 (1 + T_2)}{R_V (1 + sT_1) (1 + sT_2) + R_2 (1 + sT_1) + R_1 (1 + sT_2)}$$

Substituting s = jw, we obtain

$$F (jw; R_V) = \frac{V_1}{V_S} = \frac{-w^2T_1T_2R_V}{R_V(1 - w^2T_1T_2) + R_1 + R_2 + \cdots} \cdots$$

$$\cdots \frac{+ jwT_1R_V}{+ jw [R_V (T_1 + T_2) + R_1R_2 (C_1 + C_2)]}$$

Let

$$P = -w^2T_1T_2$$
$$Q = wT_1$$
$$R = 1 - w^2T_1T_2 = 1 + P$$
$$S = R_1 + R_2$$
$$T = w (T_1 + T_2)$$
$$U = w (R_2T_1 + R_1T_2)$$

Then,

$$F (jw; R_V) = \frac{R_V (P + jQ)}{S + R_VR + j (U + R_VT)} \quad \text{(A1-1)}$$

Appendix 2. Derivation of the Variable Resistance, R_V

Starting from the block diagram of Figure 1 and equation (1), in record mode:

$$V_{OUT} = -V_{IN} [F (s; R_V) A_{VC} + 1] \quad \text{(A2-1)}$$

The amplitude response of the system is

$$a (w) = 20\log|V_{OUT}/V_{IN}|$$

Let $$|V_{OUT}/V_{IN}|^2 = 10 (a (w)/10) = D \quad \text{(A2-2)}$$

where a (w) is the input level dependent transfer function, defined by Dolby Laboratories, Inc., for B and C type systems, respectively. From (A2-1):

$$|V_{OUT}/V_{IN}|^2 = |1 + A_{VC}F (s; R_V)|^2 \quad \text{(A2-3)}$$

Combining (A1-1, (A2-2) and (A2-3):

$$D = \frac{S + R_VR + j (U + R_VT) + A_{VC}R_V (P + jQ)^2}{(S + R_VR)^2 + (U + R_VT)^2}$$

Let $V = R + A_{VC}P$ and $W = TA_{VC}Q$

$$D = \frac{(S + R_VV)^2 + (U + R_VW)^2}{(S + R_VR)^2 + (U + R_VT)^2}$$

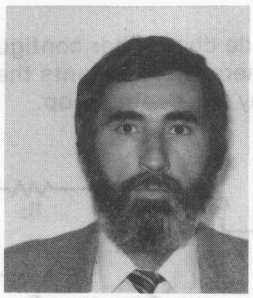
$$D [(S + R_VR)^2 + (U + R_VT)^2 -$$
$$- (S + R_VV)^2 - (U + R_VW)^2 = 0$$

Reorganizing this in the familiar form of a quadratic equation:

$$R_V^2 [D (R^2 + T^2) - (V^2 + W^2)] -$$
$$- 2R_V [S (DR - V) + U (DT - W)] + \quad \text{(A2-4)}$$
$$+ (D - 1) (S^2 + U^2) = 0$$

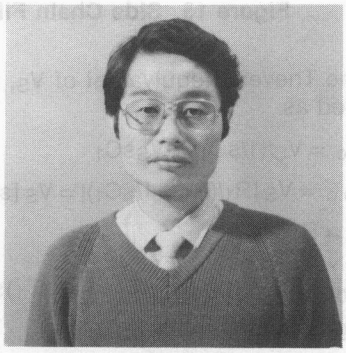
Solution of this equation provides the value of R_V by substituting the constants as defined by the circuit configuration and the required output data from the Dolby-tables, for any combination of input levels and frequencies.

Biography

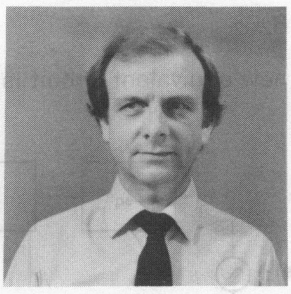


LAJOS BURGYAN was born in Hungary on November 23, 1942. He received degree from the Tivadar Puskas Institute of Telecommunication and diploma in electrical engineering from the Polytechnikal University of Budapest. In 1972 he joined the Circuits and Communication Systems Research Group of Zenith Radio Corporation in Chicago, Illinois, where he was involved in various integrated circuit development projects for consumer audio. In January 1977 he joined Fairchild Semiconductor where worked on consumer and industrial IC design projects.

In 1980 he became Manager of the Japan Design Center of Signetics Corporation in Tokyo. Since January 1983 he has been Manager of the Japan Products Design Group of Signetics in Sunnyvale, California.



FUMIMARU OKAMURA was born in Japan on October 15, 1947. He received B.S. degree from University of Electro-Communications in Japan. From 1971 to 1981 he worked for Toko Inc., Japan, where he was involved in memory systems development projects and various MOS LSI project developments. In 1981, he joined the Japan Design Center of Signetics Corporation in Tokyo, Japan.



PHILIP A. DARLINGTON was born in Seattle, WA, on November 16, 1941. He was a communication technician with Aeronautical Radio Incorporated until he joined Fairchild Semiconductor in 1978. He received BSEE degree from San Jose State University in 1980 and became an Analog Circuit Design Engineer at Fairchild in 1980, where he was involved with the development of various consumer audio and industrial development projects. In 1981 he joined the Japan Design Center of Signetics Corporation in Tokyo and worked on consumer audio projects. Since January 1983 he has been with the Analog Division of Signetics Corporation in Sunnyvale, CA.