# Application Note AN-1071

## Class D Audio Amplifier Basics

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A Class D audio amplifier is basically a switching amplifier or PWM amplifier. There are a number of different classes of amplifiers. This application note takes a look at the definitions for the main classifications.

## What is a Class D Audio Amplifier - Theory of Operation

A Class D audio amplifier is basically a switching amplifier or PWM amplifier. There are a number of different classes of amplifiers. We will take a look at the definitions for the main classifications as an introduction:

Class A – In a Class A amplifier, the output devices are continuously conducting for the entire cycle, or in other words there is always bias current flowing in the output devices. This topology has the least distortion and is the most linear, but at the same time is the least efficient at about 20%. The design is typically not complementary with a high and low side output devices.

Class B – This type of amplifier operates in the opposite way to Class A amplifiers. The output devices only conduct for half the sinusoidal cycle (one conducts in the positive region, and one conducts in the negative region), or in other words, if there is no input signal then there is no current flow in the output devices. This class of amplifier is obviously more efficient than Class A, at about 50%, but has some issue with linearity at the crossover point, due to the time it takes to turn one device off and turn the other device on.

Class AB – This type of amplifier is a combination of the above two types, and is currently one of the most common types of power amplifier in existence. Here both devices are allowed to conduct at the same time, but just a small amount near the crossover point. Hence each device is conducting for more than half a cycle but less than the whole cycle, so the inherent non-linearity of Class B designs is overcome, without the inefficiencies of a Class A design. Efficiencies for Class AB amplifiers is about 50%.

Class D – This class of amplifier is a switching or PWM amplifier as mentioned above. This class of amplifier is the main focus of this application note. In this type of amplifier, the switches are either fully on or fully off, significantly reducing the power losses in the output devices. Efficiencies of 90-95% are possible. The audio signal is used to modulate a PWM carrier signal which drives the output devices, with the last stage being a low pass filter to remove the high frequency PWM carrier frequency.

From the above amplifier classifications, classes A, B and AB are all what is termed linear amplifiers. We will discuss the differences between Linear and Class D amplifiers in the next section. The block diagram of a linear amplifier is shown below in fig 1. In a linear amplifier the signals always remain in the analog domain, and the output transistors act as linear regulators to modulate the output voltage. This results in a voltage drop across the output devices, which reduces efficiency.

Class D amplifiers take on many different forms, some can have digital inputs and some can have analog inputs. Here we will focus on the type which have analog inputs.
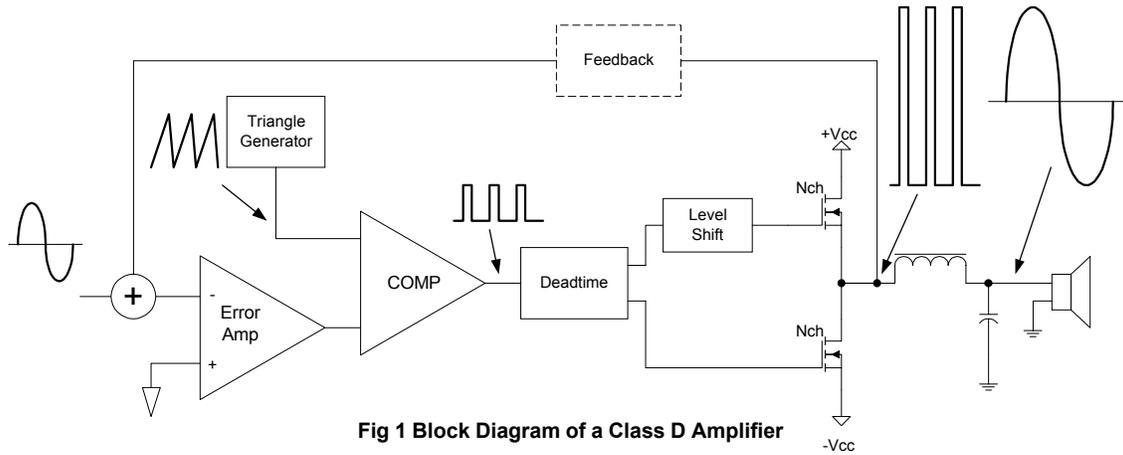
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**Fig 1 Block Diagram of a Class D Amplifier**

Fig 1 above shows the basic block diagram for a Half Bridge Class D amplifier, with the waveforms at each stage. This circuit uses feedback from the output of the half-bridge to help compensate for variations in the bus voltages.

So how does a Class D amplifier work? A Class D amplifier works in very much the same way as a PWM power supply (we will show the analogy later). Let's start with an assumption that

the input signal is a standard audio line level signal. This audio line level signal is sinusoidal with a frequency ranging from 20Hz to 20kHz typically. This signal is compared with a high frequency triangle or sawtooth waveform to create the PWM signal as seen in fig 2a below. This PWM signal is then used to drive the power stage, creating the amplified digital signal, and finally a low pass filter is applied to the signal to filter out the PWM carrier frequency and retrieve the sinusoidal audio signal (also seen in fig 2b).
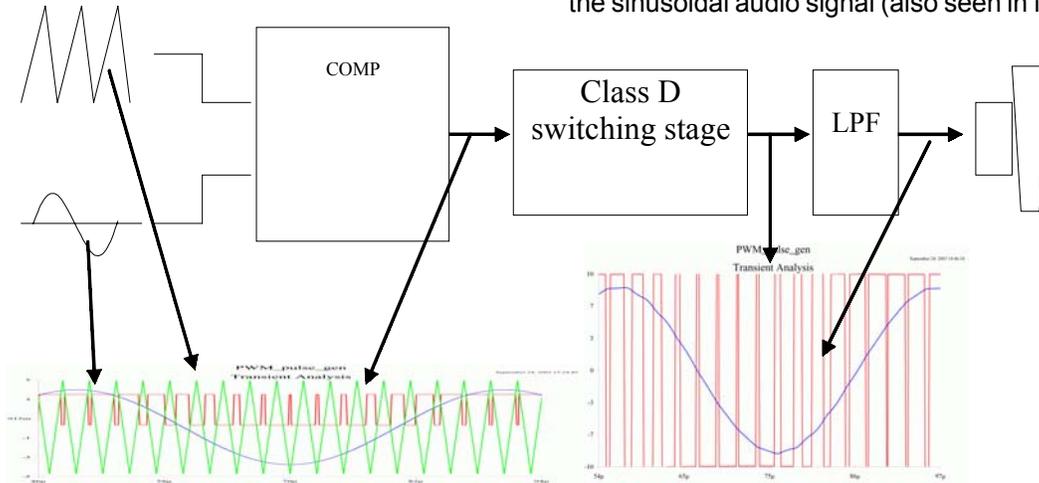


Fig 2a PWM Signal Generation

Fig 2b Output Filtering

**Fig 2) Class D Amplifier Waveforms**

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**Topology Comparison – Linear vs. Class D**

In this section we will discuss the differences between linear (Class A and Class AB) amplifiers, and Class D digital power amplifiers. The primary and main difference between linear and Class D amplifiers is the efficiency. This is the whole reason for the invention of Class D amplifiers. The Linear amplifiers is inherently very linear in terms of its performance, but it is also very inefficient at about 50% typically for a Class AB amplifier, whereas a Class D amplifier is much more efficient, with values in the order of 90% in practical designs. Fig 3 below shows typical efficiency curves for linear and Class D amplifiers.



Linear Amplifier



Class D Amplifier

**Fig 3 Linear and Class D Amplifier Efficiencies**

Gain – With Linear amplifiers the gain is constant irrespective of bus voltage variations, however with Class D amplifiers the gain is proportional to the bus voltage. This means that the power supply rejection ratio (PSRR) of a Class D amplifier is 0dB, whereas the PSRR of a linear amplifier is very good. It is common in Class D amplifiers to use feedback to compensate for the bus voltage variations.

Energy Flow – In linear amplifiers the energy flow is always from supply to the load, and in Full bridge Class D amplifiers this is also true. A half-bridge Class D amplifier however is different, as the energy flow can be bi-directional, which leads to the "Bus pumping" phenomena, which causes the bus capacitors to be charged up by the energy flow from the load back to the supply. This occurs mainly at the low audio frequencies i.e. below 100Hz.
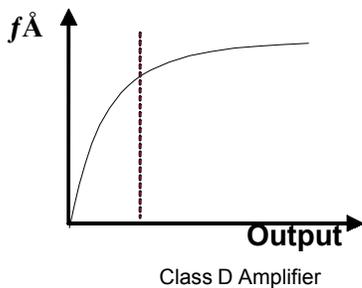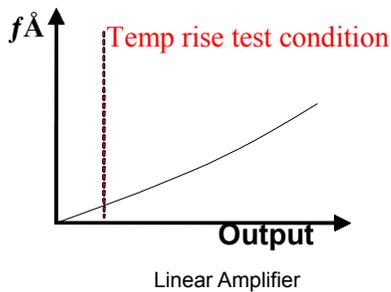
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## Analogy to a Synchronous Buck Converter

A simple analogy can be made between a Class D amplifier and a synchronous buck converter. The topologies are essentially the same as can be seen below in fig 4.
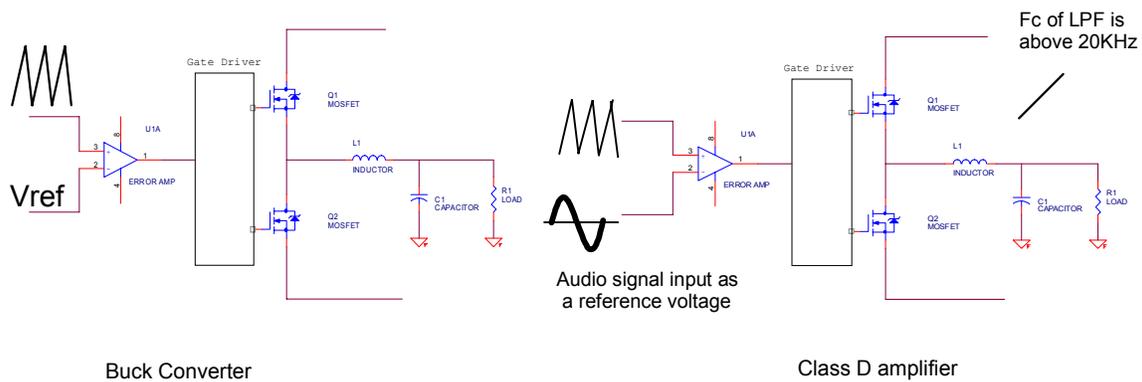


Buck Converter

Class D amplifier

**Fig 4 Topologies for Synchronous Buck Converter and a Class D amplifier**

The main difference between the two circuits is that the reference signal for the synchronous buck converter is a slow changing signal from the feedback circuit(➔a fixed voltage), in the case of the Class D amplifier the reference signal is an audio signal which is continuously changing. This means that the duty cycle is relatively fixed in the synch buck converter, whereas the duty is continuously changing in the Class D amplifier with an average duty of 50%.

In the synch buck converter the load current direction is always towards the load, but in Class D the current flows in both directions.

The final difference is in the way the MOSFETs are optimized. The Synch buck converter is optimized differently for the high and low side MOSFETs, with lower $R_{DS(on)}$ for longer duty and low Qg for short duty. The Class D amplifier has the same optimization for both of the MOSFETs, with the same $R_{DS(on)}$ for high and low side.

## Power Losses in the MOSFETs

The losses in the power switches are very different between linear amplifiers and Class D amplifiers. First lets look at the losses in a linear Class AB amplifier. The losses can be defined as:

$$P_C = \frac{1}{2 \cdot \pi} \cdot \int_0^{\pi} \frac{Vcc}{2} (1 - K \sin \omega \cdot t) \frac{Vcc}{2 \cdot R_L} K \sin \omega \cdot t \bullet d\omega \cdot t$$

Where K is the ratio of $V_{bus}$ to output voltage.

This can then be simplified down to the following equation for the linear amplifier Power switch losses:

$$P_{tot} = \frac{Vcc^2}{8\pi \cdot R_L} \cdot \left( \frac{2K}{\pi} - \frac{K^2}{2} \right)$$

Note that the power loss is not related to the output device parameters. Fig 5) below shows the power loss vs K.
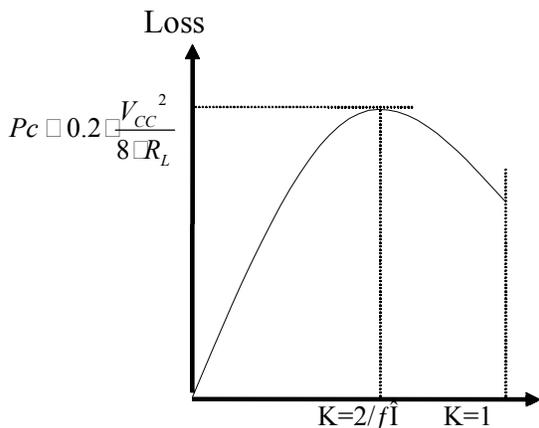


$$Pc \square 0.2 \square \frac{V_{CC}^2}{8 \square R_L}$$

K=2/$f\hat{1}$    K=1

**Fig 5) Power Loss vs. K for Linear Class AB Amplifier**

Now lets look at the losses for a Class D amplifier. The total power loss in the output devices for a Class D amplifier are given by:

$$P_{TOTAL} = Psw + Pcond + Pgd$$

Psw are the switching losses and are given by the equation:

$$Psw = C_{OSS} \cdot V_{BUS}^2 \cdot f_{PWM} + I_D \cdot V_{DS} \cdot t_f \cdot f_{PWM}$$

Pcond are the conduction losses and are given by the equation:

$$Pcond = \frac{R_{DS(ON)}}{R_L} \cdot Po$$

Pgd are the gate drive losses and are given by the equation:

$$Pgd = 2 \cdot Qg \cdot Vgs \cdot f_{PWM}$$

As can be seen in a Class D amplifier the output losses are dependant on the parameters of the device used, so optimization is needed to have the most effective device, based on Qg, $R_{DS(on)}$, $C_{OSS}$, and $t_f$ . Fig 6 below shows the power losses vs K for the Class D amplifier.



Loss

**Efficiency can be improved further!**

K=1

**Fig 6  Power Loss vs. K for Class D Amplifie**

## Half Bridge    v.s.    Full Bridge

| | Half Bridge | Full Bridge |
|---|---|---|
| **Supply voltage** | 0.5 x 2ch | 1 |
| **Current ratings** | 1 | 2 |
| **MOSFET** | 2 MOSFETs/CH | 4 MOSFETs/CH |
| **Gate Driver** | 1 Gate Driver/CH | 2 Gate Drivers/CH |
| **Linearity** | | Superior (No even order HD) |
| **DC Offset** | Adjustment is needed | Can be cancelled out |
| **PWM pattern** | 2 level | 3 level PWM can be implemented |
| **Notes** | Pumping effect<br>Need a help of feed back | Suitable for open loop design |
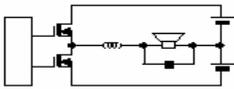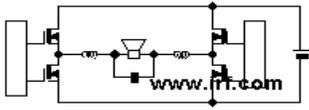
Table 1: Topology Comparison (Half-bridge vs. Full-bridge)

Similar to conventional Class AB amplifiers, Class D amplifiers can be categorized into two topologies, half-bridge and full-bridge configurations. Each topology has pros and cons. In brief, a half-bridge is potentially simpler, while a full-bridge is better in audio performance. The full-bridge topology requires two half-bridge amplifiers, and thus, more components. However, the differential output structure of the bridge topology inherently can cancel even the order of harmonic distortion components and DC offsets, as in Class AB amplifiers. A full-bridge topology allows of the use of a better PWM modulation scheme, such as the three level PWM which essentially has fewer errors due to quantization.

In the half-bridge topology, the power supply might suffer from the energy being pumped back from the amplifier, resulting in severe bus voltage fluctuations when the amplifier outputs low frequency audio signals to the load. This kickback energy to the power supply is a fundamental characteristic of Class D amplification. Complementary switching legs in the full-bridge tend to consume energy from the other side of the leg, so there is no energy being pumped back towards the power supply.

Table 1 shows the summary of the comparison.
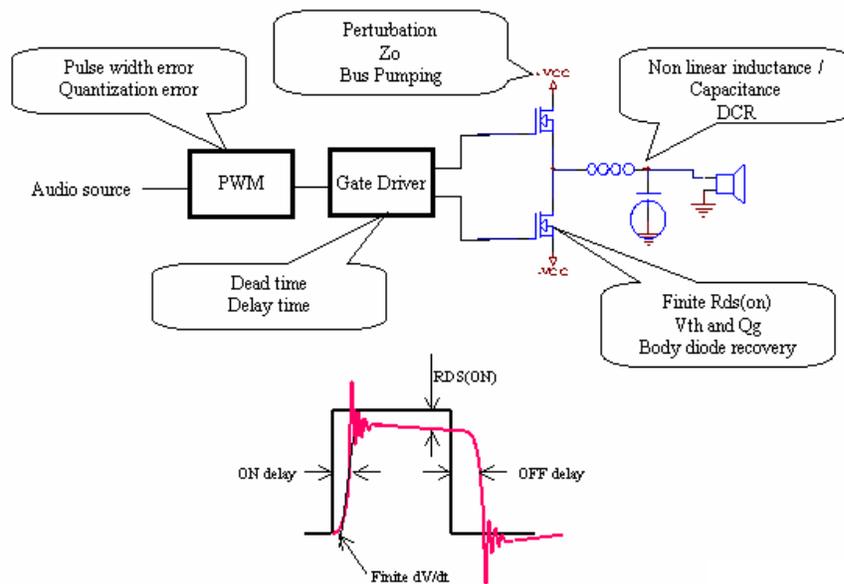
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**Fig 7: Major Cause of Degradation**

An ideal Class D amplifying stage has no distortion and no noise generation in the audible band, along with providing 100% efficiency. However, as shown in Fig 7, practical Class D amplifiers have imperfections that generate distortions and noise. The imperfections are caused by the distorted switching waveform being generated by the Class D stage. The causes are:

1. Nonlinearity in the PWM signal from modulator to switching stage due to limited resolution and/or jitter in timing
2. Timing errors added by the gate drivers, such as dead-time, ton/toff, and tr/tf
3. Unwanted characteristics in the switching devices, such as finite ON resistance, finite switching speed or body

diode characteristics.
4. Parasitic components that cause ringing on transient edges
5. Power supply voltage fluctuations due to its finite output impedance and reactive power flowing through the DC bus
6. Non-linearity in the output LPF.

In general, switching timing error in a gate signal is the primary cause of the nonlinearity. The timing error due to dead-time in particular has the most significant contribution of nonlinearity in a Class D stage. A small amount of dead-time in the tens of nano-seconds can easily generate more than 1% of THD (Total Harmonic Distortion). Accurate switching timing is always a primary concern.

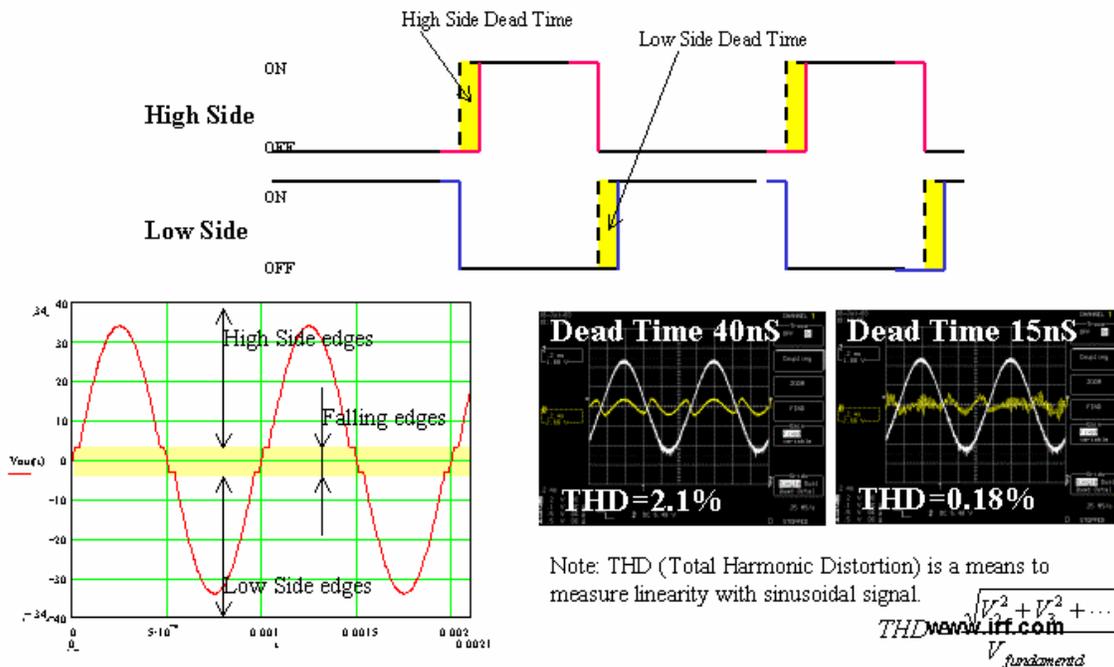Let us take a look at how the dead-time affects nonlinearity.



**Fig 8: THD and Dead-time**

The operation mode in a Class D output stage can be categorized into three different regions based on how the output waveform follows the input timing. In those three different operation regions, the output waveform follows different edges in high side and low side input signals.

Let's examine the first operating region where the output current flows from the Class D stage to the load when the amount of the current is larger than the inductor ripple current. At the instant of high side turn-off and prior to low side turn-on, the output node is driven to the nega-

tive DC bus. This action is automatically caused by the commutation current from the demodulation inductor, regardless of low side turn-on timing. Therefore the timing in the output waveform is not influenced by the dead-time inserted into the turn-on edge of low side, and always follows the high side input timing. Consequently, the PWM waveform is shortened only by the dead-time inserted into the high side gate signal, resulting in slightly lower voltage gain as expected from the input duty cycle.

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A similar situation happens to the negative operation region where the output current flows from the load to the Class D stage. The amount of the current is larger than the inductor ripple current. In this case, the timing in the output waveform is not influenced by the dead-time inserted into the turn-on edge of the high side, and always follows the low side input timing. Consequently, the PWM waveform is shortened only by the dead-time inserted into the low side gate signal.

There is a region between the two operation modes described earlier where the output timing is independent of the dead-time. When the output current is smaller than the inductor ripple current, the output timing follows the turn-off edge of each input because, in this region, turn-on is made by ZVS (Zero Voltage Switching) operation. Hence, there is no distortion in this middle region.

As the output current varies according to the audio input signal, the Class D stage changes its operation regions, which each have a slightly

different gain. The output waveform will be distorted by these three different gain regions in a cycle of the audio signal.

Fig. 8 shows how significantly dead time affects THD performance. A 40nS dead time can create 2% THD. This can be improved to 0.2% by tightening the dead time down to 15nS. This punctuates the significance of seamless high side and low side switching for better linearity.

**Audio Performance Measurement**

Audio measuring equipment with an AES17 brick wall filter, such as Audio Precision AP2, are necessary. However a classic audio analyzer like the HP8903B can be used with appropriate pre-stage low pass filter is applied. The important consideration here is that the output signal of a Class D amplifier still contains substantial amount of switching frequency carrier on its waveform, which causes a wrong reading, and those analyzers might not be immune enough to the carrier leak from a Class D amplifier. Fig. 9 shows an example of a filter.
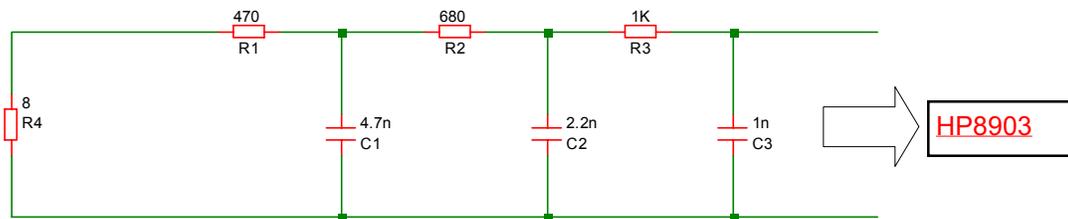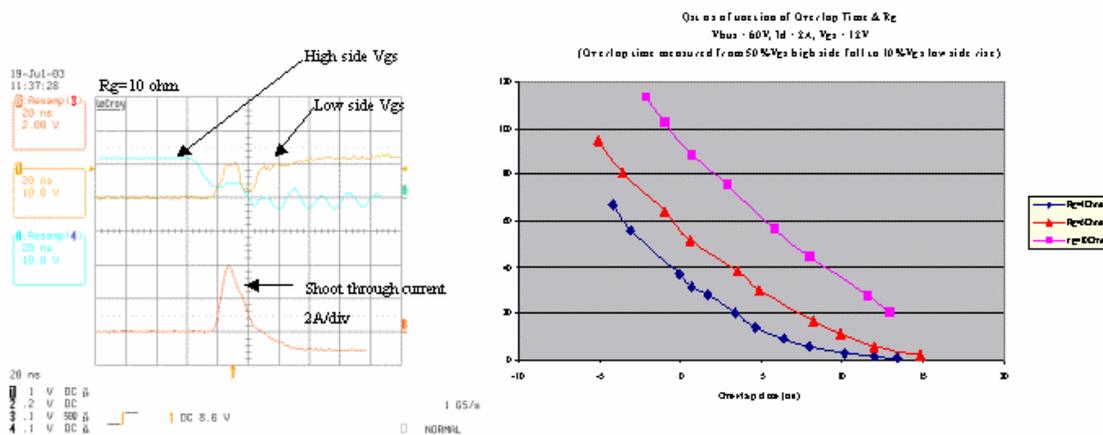


Fig 9: Example of an output filter

**Fig 10: Shoot-through prevention**

However, a narrow dead-time can be very risky in mass production. Because once both high and low side MOSFETs are turned on simultaneously, the DC bus voltage will be short circuited by the MOSFETs. A huge amount of shoot-through current starts to flow, which will result in device destruction. It should be noticed that the effective dead-time can be vary from unit to unit variation of component values and its die tempera-ture. Fig. 10 shows the relationship between the length of the dead time and the amount of shoot-through charge. It is extremely important for a reliable design of a Class D amplifier to ensure that the dead-time is always positive and never negative to prevent MOSFETs from en-tering the shoot through condition.

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## Power Supply Pumping

Load Current

Commutation current

**Half Bridge**
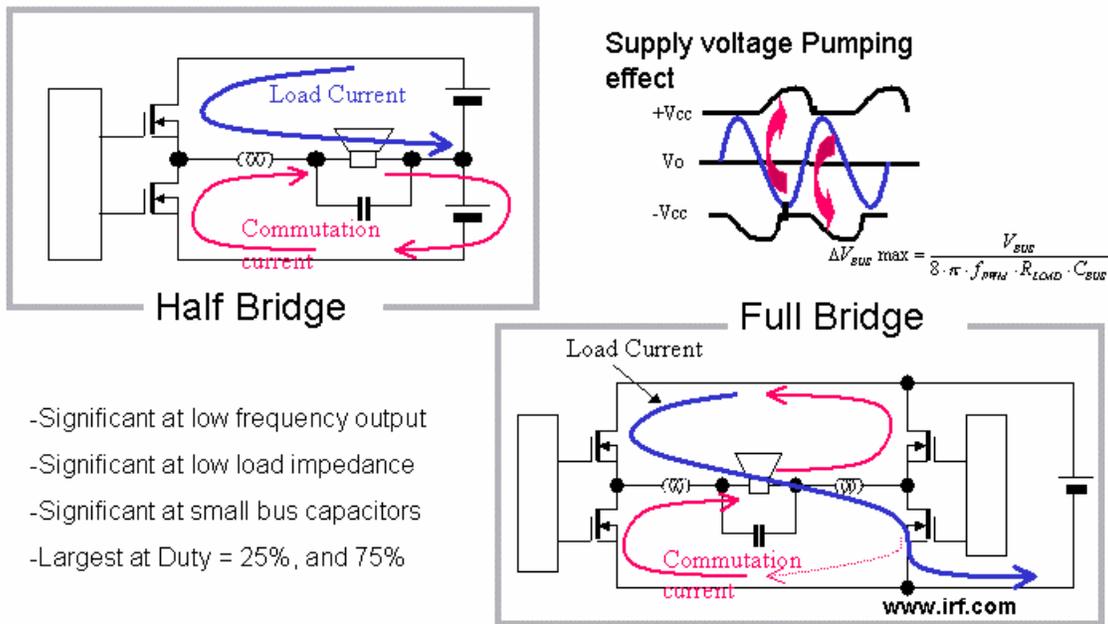
-Significant at low frequency output
-Significant at low load impedance
-Significant at small bus capacitors
-Largest at Duty = 25%, and 75%

**Supply voltage Pumping effect**

+Vcc

Vo

-Vcc

$$\Delta V_{BUS}\max = \frac{V_{BUS}}{8 \cdot \pi \cdot f_{PWM} \cdot R_{LOAD} \cdot C_{BUS}}$$

**Full Bridge**

Load Current

Commutation current

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**Fig 11: Power Supply Pumping**

Another marked cause of degradation in Class D amplifiers is bus pumping, which can be seen when the half bridge topology is powering a low frequency output to the load. Always keep in mind that the gain of a Class D amplifier stage is directly proportional to the bus voltage. Therefore, bus fluctuation creates distortion. Since the energy flowing in the Class D switching stage is bi-directional, there is a period where the Class D amplifier feeds energy back to the power supply. The majority of the energy flowing back to the supply is from the energy stored in the inductor in the output LPF. Usually, the power supply has no way to absorb the energy coming back from the load. Consequently the bus voltage is pumped up, creating bus voltage fluctuations.

Bus pumping does not occur in full bridge topologies because the energy kicked back to the power supply from one side of the switching leg will be consumed in the other side of the switching leg.

**EMI consideration: Qrr in Body Diode**
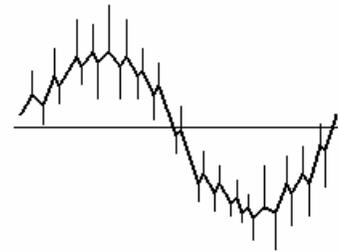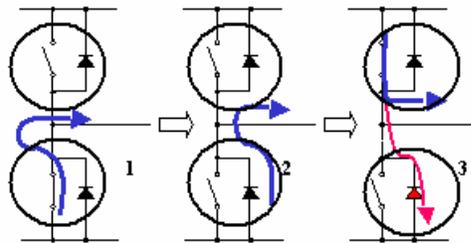
1. Low side drains inductor current

2. During dead time body diode of low side conducts and keep inductor current flow

3. At the moment high side is turned ON after dead time, the body diode is still conducting to wipe away minority carrier charge stored in the duration of forward conduction.

➔ This current generates large high frequency current waveform and causes EMI noises.
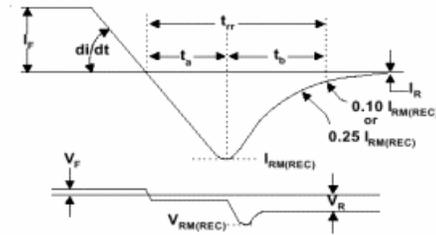
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**Fig 12: EMI Considerations**

EMI (Electro-Magnetic Interference) in Class D amplifier design is troublesome like in other switching applications. One of the major sources of EMI comes from the reverse recovery charge of the MOSFET body diode flowing from the top rail to the bottom, similar to the shoot-through current. During the dead-time inserted to prevent shoot through current, the inductor current in the output LPF turns on the body diode. In the next phase when the other side of the MOSFET starts to turn on at the end of the dead-time, the body diode stays in a conducting state unless the stored minority carrier is fully discharged. This reverse recovery current tends to have a sharp spiky shape and leads to unwanted ringing from stray inductances in PCB traces and the package. Therefore, PCB layout is crucial for both ruggedness of the design and reduction of EMI.

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## Conclusion

Highly efficient Class D amplifiers now provide similar performances to conventional Class AB amplifier if key components are carefully selected and the layout takes into account the subtle, yet significant impact of parasitic components.

Constant innovations in semiconductor technologies are increasing the use of Class D amplifiers usage due to improvements in higher efficiency, increased power density and better audio performance.

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