A 113dB SNR OVERSAMPLING SIGMA-DELTA DAC FOR CD/DVD APPLICATION

Khiem Nguyen, Robert Adams, Karl Sweetland
Analog Devices Inc., Wilmington, MA USA

***Abstract*— A sigma-delta (ΣΔ) audio digital-to-analog converter (DAC) for CD and digital versatile disk (DVD) application is presented. The converter uses a 6-bit modulator and a segmented noise-shaped scrambling technique to achieve a 113dB dynamic-range over a 20kHz bandwidth. A continuous-time output stage is used to achieve high signal-to-noise (SNR) in a small die area. This output stage employs a dual return-to-zero scheme to eliminate errors caused by inter-symbol interference (ISI). The converter is fabricated in a 0.6μm double-poly double-metal CMOS process. The chip occupies 3.1x3.2 squared mm and operates from a single 5V supply.**

I. INTRODUCTION

Sigma-delta (ΣΔ) digital-to-analog converters (DACs) offer a way to achieve high resolution and low distortion with relaxed post-analog filter requirements at a relatively low cost compared to conventional Nyquist converters. A typical ΣΔ DAC as in Fig. 1 consists of a digital interpolation filter to bring the input sample rate up to the modulator rate, a modulator to reduce the word width by trading off the out-of-band noise, a switched-capacitor filter for out-of-band noise filtering and analog signal reconstruction. To achieve perfect linearity in analog signal reconstruction, the modulator output is usually 1-bit. This type of architecture has several drawbacks. Modulators with 1-bit quantizers create large step sizes at the discrete-to-continuous boundary and hence require a tight clock jitter specification. For example, to achieve +100dB SNR over the audio band, it would need a master clock with jitter of less than 10ps. One approach to reduce the clock jitter sensitivity is to use a multi-bit quantizer. Multi-bit DACs' suffer from distortion problem caused by the analog element mismatch. Techniques such as those presented in [1] or [2] can be used to dynamically swap the elements so that on average the mismatch error is zero. One drawback is that the swapping circuitry becomes large when the word width is greater than four.

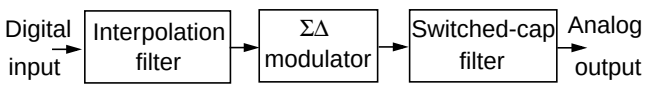

Fig. 1 Block diagram of a typical ΣΔ DAC

The major disadvantage of ΣΔ DACs with switched-capacitor filters is the relationship between the noise power and the capacitor area. The noise power each capacitor accumulates is described by the equation $P_N = kT/C$. It follows that each additional bit of resolution increases the capacitor area by four times. Since the capacitors are larger, they will need higher slew rate, faster on-chip opamps, and larger switches for settling to the desired accuracy. These requirements make the design very expensive.

This paper presents a multi-bit ΣΔ DAC with a continuous-time output stage. The continuous-time output stage enables the design to achieve high SNR while occupying much less area than normal switched-capacitor circuits. To reduce the out-of-band noise energy, a multi-bit modulator is used. A new noise-shaped segmentation technique is used in conjunction with scrambling to achieve low distortion at a very small hardware cost. The output stage uses a dual return-to-zero switching scheme which yields an output current pulse that is free of inter-symbol interference. High performance on-chip opamps are used for I-to-V conversion. The chip architecture and design will be discussed in section II. Section III will discuss about the circuit design issues. Section IV will show some of the measured results.

II. ARCHITECTURE

Fig. 2 shows the block diagram of one DAC channel. The chip consists of a serial port to receive the 3-wire input, a selectable 4x/8x interpolator, a 16x sample-and-hold register, a second-order 6-bit modulator operating at $128f_s$, and a continuous-time output stage. The selectable interpolation factor allows the input sample rate to be either 44.1kHz or 88.2kHz. The digital filter engine also includes a digital volume control circuit and an IIR filter that performs the required de-emphasis filtering found in some CDs. The continuous-time output stage is used since its output noise power is dominated by the thermal noise of the MOS current sources which can be optimized. Hence, a high SNR design can be achieved in a smaller area compared to that of a switched capacitor filter output stage.

A. Multi-bit modulator

For single-bit ΣΔ DACs, the sample-to-sample step size at the discrete-to-continuous time boundary will swing from rail to rail. Hence, the output waveform is very sensitive to clock jitter. In addition, the continuous-time output stage relies on the external analog filter to remove the out-of-band

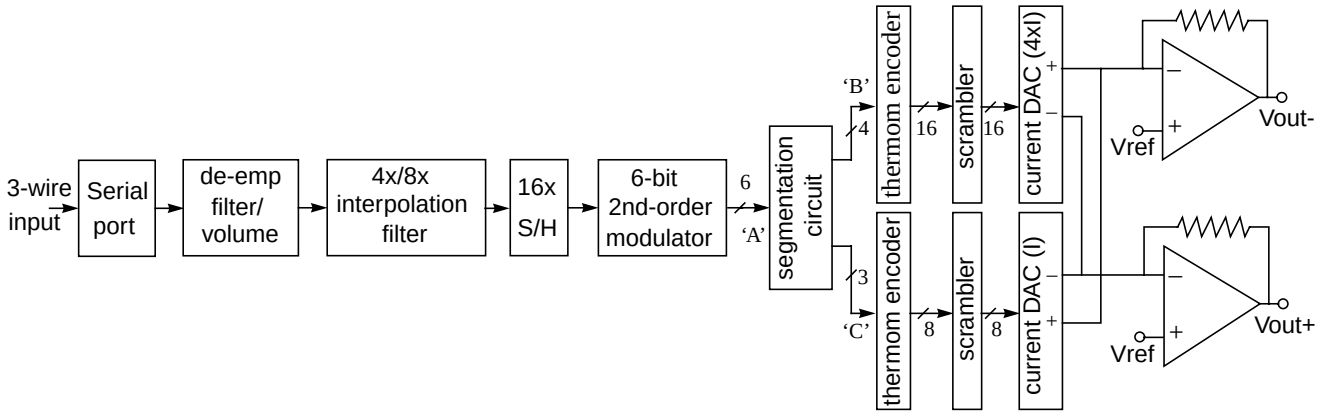

Fig. 2: Block diagram of 1 DAC channel

quantization noise, having a single-bit modulator will require a high performance and expensive post-analog filter. The modulator in this design is a conventional second-order with 6-bit quantization. The finer quantization levels greatly reduce the clock jitter sensitivity requirement to a practical level specified by commercially available ICs. At the same time, the lower out-of-band noise energy allows the use of a more relaxed post analog filter. Multi-bit modulators also offer other benefits such as larger usable input range and higher SNR. The theoretical SNR of the modulator in this design is 125dB.

B. Noise-shaped segmentation

The use of the multi-bit quantization scheme, however, does have a disadvantage. To achieve a guaranteed monotonicity and low DNL in the DAC, the thermometer encoding scheme is commonly used before the analog reconstruction. Due to the mismatch between the analog unit elements, distortion is introduced into the output waveform and degrades the overall linearity of the DAC.

This design uses the scrambling scheme presented in [2] to convert the harmonics resulting from element mismatch into spectrally shaped noise, thus preserving the high dynamic range. Since the area of the swapping circuitry is proportional to $N \log N$, where N is the number of input levels, the approach is more suitable for inputs with equal to or less than 16 levels. With a 6-bit input, or equivalently 64 levels, straight application of the scrambling scheme leads to a significant increase in chip area. To alleviate this problem, a new noise-shaped segmentation technique in Fig. 3 is used. A first-order modulator converts the 6-bit word 'A' into a 4-bit word 'B'. This 4-bit word 'B' is then subtracted from the input word 'A' to produce the 3-bit word 'C'. Both 'B' and 'C' are then thermometer encoded and scrambled. A 16-level DAC with weight 4I and an 8-level DAC with weight I then convert the thermometer codes to current pulses which are summed together by on-chip I-V converters. Since 'A' and 'B' both contain the inband signal, the difference "C" is the quantization noise of the first-order modulator. Any gain mismatch between the 'B' and the 'C' DACs will therefore also be spectrally shaped and contribute little inband noise energy. The first-order modulator is a conventional-type

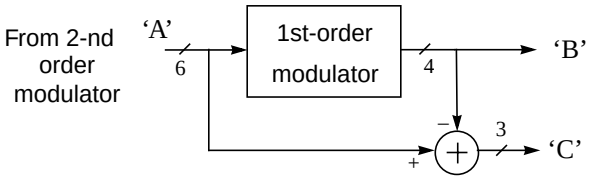

Fig. 3: Noise-shaped segmentation circuit

which adds very little hardware. One interesting point to note here is that although the 6-bit word is segmented, the signal content is only present in one subword. Hence, the mismatch between the two DACs does not result in any spectral leakage.

C. Dual return-to-zero

A classic problem in continuous-time output stage is inter-symbol interference (ISI). This interference occurs because the output pulse does not have equal rise and fall times, and hence each output level is affected by the previous ones. ISI results in inband harmonics and thus degrades the linearity of the converter. One solution is to use the return-to-zero (RTZ) scheme so that the circuit does not have any memory of its previous output levels. However, this approach has several disadvantages such as the presence of high frequency components, large output step sizes and half the signal strength. The large step sizes cause the output to be more sensitive to clock jitter and also makes it difficult to filter the waveform.

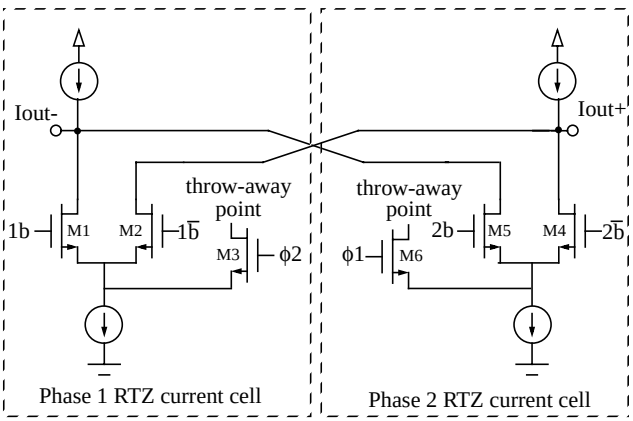

Fig. 4: Dual return-to-zero current DAC cell

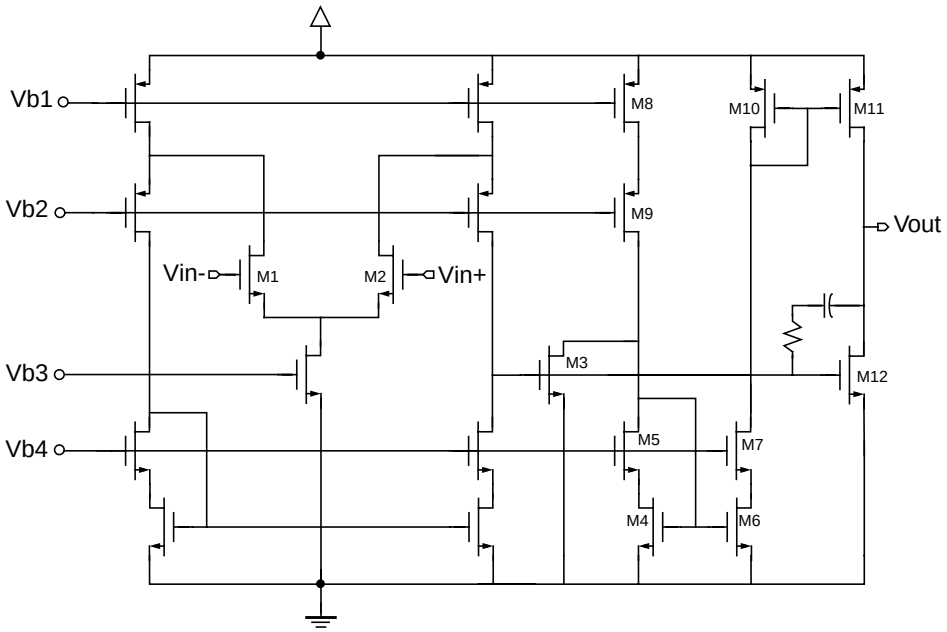

Fig. 5 On-chip I-to-V opamp

To eliminate the inter-symbol interference in the output waveform, the dual return-to-zero switching scheme in Fig. 4 is used. This new scheme avoids the large DAC output step size and reduces high frequency energy in the output waveform which would appear in a single RTZ scheme. Nonlinearities resulting from large voltage step sizes in the output circuit will also be reduced. Since the step size is now much smaller, a more relaxed I-to-V converter design with smaller slew rate and gain bandwidth can be used. The dual RTZ DAC cell in Fig. 4 consists of two identical current sources, each active in one-half of the clock period. The data bit is gated with the proper clock phase to drive the current source. The total current pulse delivered to the I-to-V converter by this scheme is therefore similar to that of the non-RTZ scheme except it is free of ISI. The dual RTZ scheme can also be explained using the superposition theorem. Since each individual RTZ cell is free of ISI, by the principle of superposition, the summation of two RTZ cells must also be free of ISI. To avoid long switching transient time, the unused cell is switched to a throw-away node during its inactive phase (via M3 and M6) to keep its drain at a constant voltage.

III. Circuit Designs

To convert the current output to voltage, each DAC channel uses a pair of I-to-V converters consisting of on-chip resistors and very low-noise, low-distortion opamps. The opamp is a classic two-stage single-ended opamp and has a g_m-stabilizing circuit in its output stage to drive a 1KΩ load. The first stage is a folded cascode which provides most of the overall DC gain. The high DC gain is needed to suppress any voltage modulation at the drain of the current sources. The second stage is a class AB-like output circuit to provide a high driving capability and low-distortion. In a normal class-A output stage, the NMOS driver may suffer from bias current starvation when driving a heavy resistive load and may lead to instability. The g_m-stabilizing circuit M3-M10 is added in to provide a constant bias current for the NMOS driver M12. When the gate voltage of the NMOS driver drops due to lack of bias current, the loop will increase the bias current in M6. This increment will be mirrored to M11 in attempt to keep the NMOS driver bias current at the correct level. For optimal distortion, the transconductance of the g_m-stabilize loop should match with that of the NMOS driver. The opamp measured separately achieves -108dB THD+N with a 1Vrms output voltage over the audio frequency band.

Fig. 6 shows the on-chip low noise current generator. To ensure low gain drifting, the reference resistor is of the same type as the feedback resistor in the I-to-V converters. To achieve the required noise figure, all MOS devices are optimized for low thermal noise. An additional opamp, A2, is also used to enhance the matching between the current sources and reduce the output dc offset voltage.

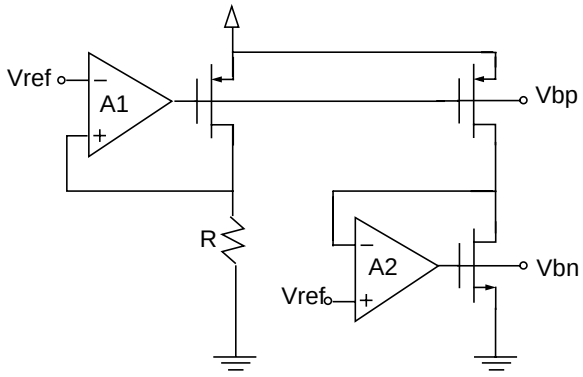

Fig. 6 Low noise reference current generator

IV. Measured Results

The converter is fabricated in a 0.6μm double-poly double metal CMOS process. The total die size is 3.1x3.2 squared mm. The power consumption is 250mW. Fig. 9 shows the micro photograph of the IC. Fig. 7 shows the measured spectral plot of a 1kHz, 0dBFS (2Vrms differential) sine-wave input. Fig. 8 shows the THD+N plot versus input amplitude for a 1kHz input sine-wave. Table I summarizes some of the measured results from the Audio Precision System Two.

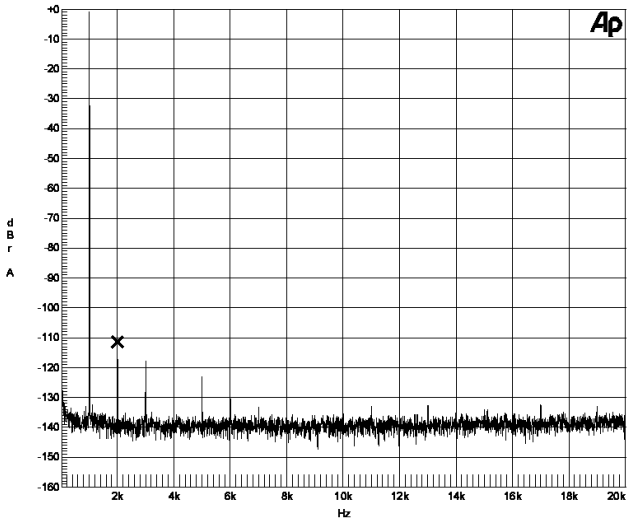

Fig. 7: 8K-FFT plot of a 1 kHz, 0dBFS input

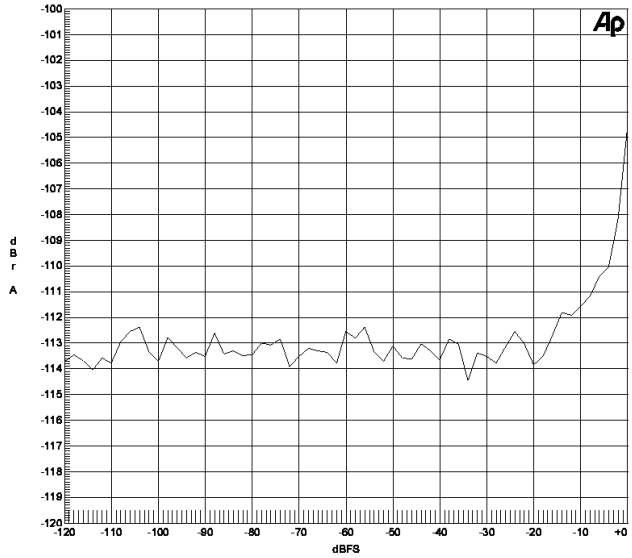

Fig. 8: THD+N vs. amplitude of a 1kHz sine wave

Table I**:**
Chip summary

SNR (20-20kHz), unweighted	111dB
SNR (20-20kHz), A-weighted	113dB
D-range, -60dBFS, A-weighted	113dB
THD+N (0dBFS)	-102dB
Digital filter passband ripple	±0.04 dB

V. Conclusion

This paper presents an audio D-to-A converter for CD/DVD application. The design uses a continuous-time output stage to achieve high SNR in a small are. A new dual return-to-zero scheme is used to eliminate the errors from inter-symbol interference in the output waveform. The design uses a 6-bit ΣΔ modulator and a new noise-shaped segmentation technique to lower the out-of-band noise and clock jitter sensitivity.

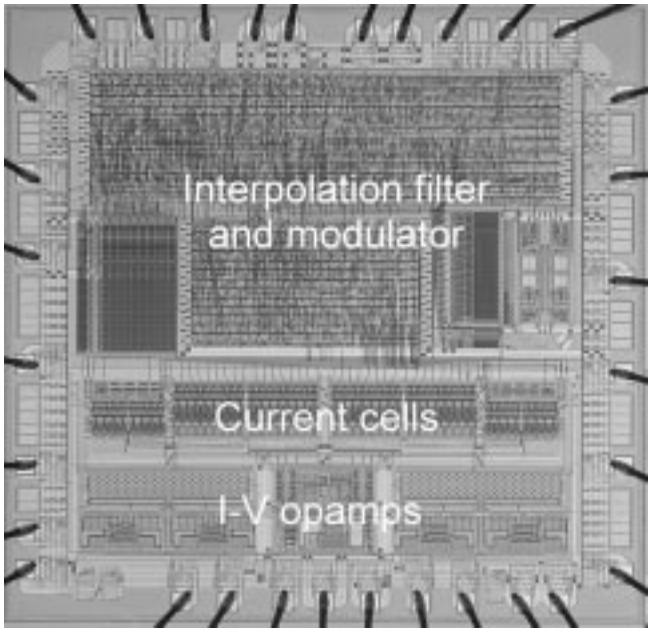

Fig. 9 Chip photograph

References

[1] L. R. Carley, J. Kenney, "A 16-bit 4th-order noise-shaping D/A converter", in Proc. 1988 *CICC*, pp.21.7.1-21.7.4.

[2] T. Kwan, R. Adams, "A Stereo Multi-bit ΣΔ D/A with Asynchronous Master-clock Interface," ISSCC Digest of Technical Papers, Feb., 1996.