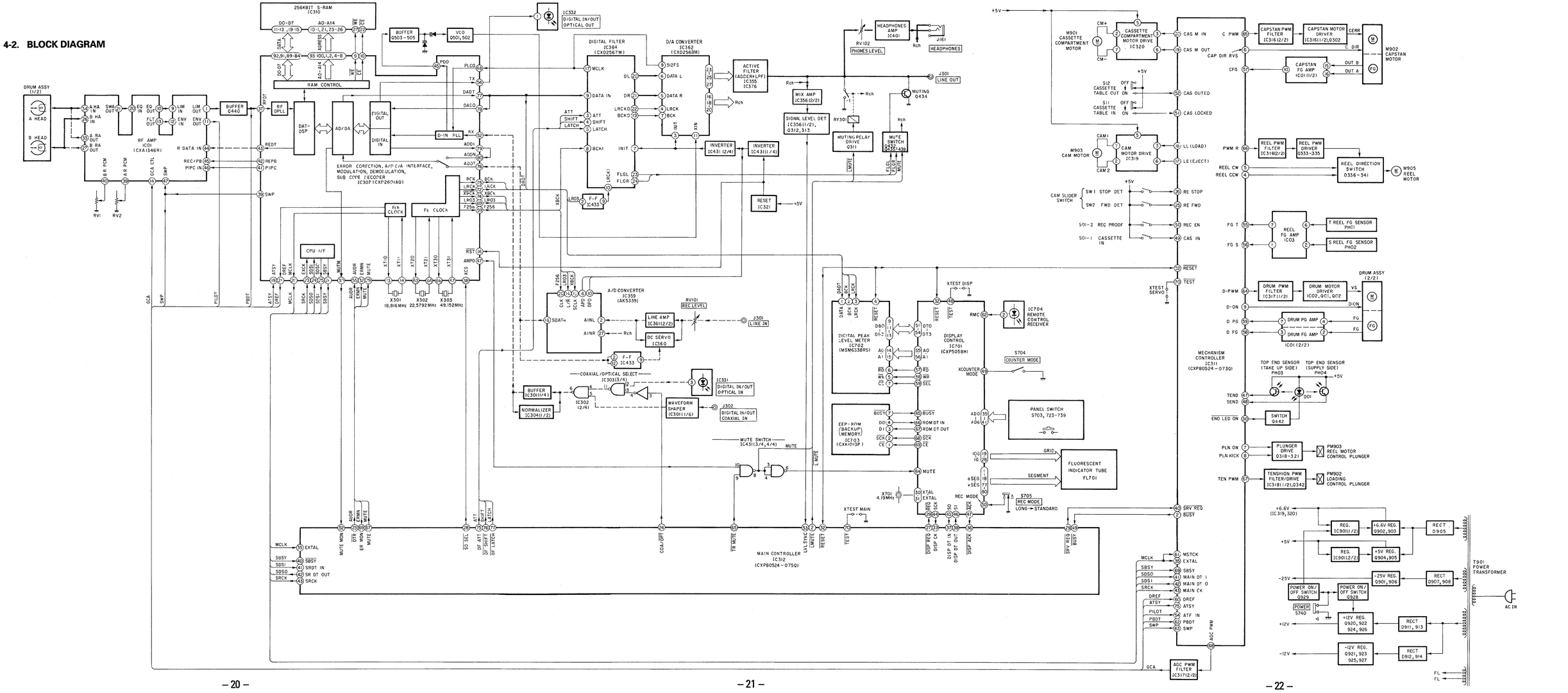
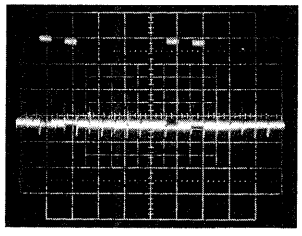
4-2. BLOCK DIAGRAM

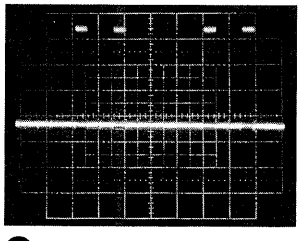


4-3. WAVEFORMS

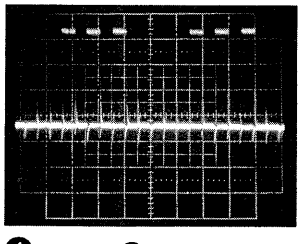
❶ FL701 ⑤-⑭pin (1G-10G)
32Vp-p, 2.5ms



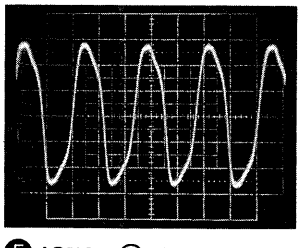
❷ IC701 ⑲-㉘pin (10G-1G)
34Vp-p, 2.45ms



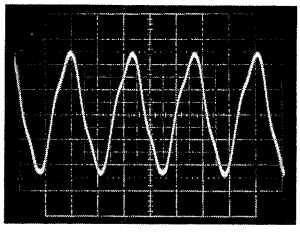
❸ IC701 ㊼-㊿pin, ①-⑱pin (a-v)
38Vp-p, 1.2ms



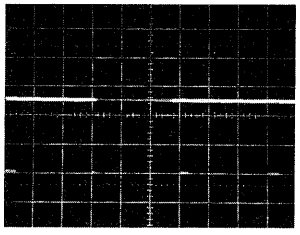
❹ IC701 ㉚piN (XTAL)
5.5Vp-p, 2.5µs



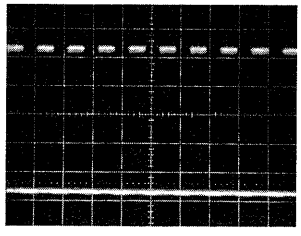
❺ IC701 ㉛pin (EXTAL)
5Vp-p, 2.5µs



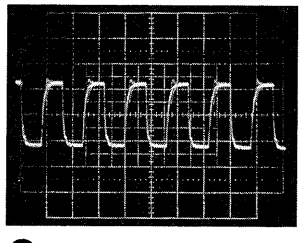
❻ IC701 ㊻pin, IC312 ㊳pin (SI)
5.2Vp-p, 30ms



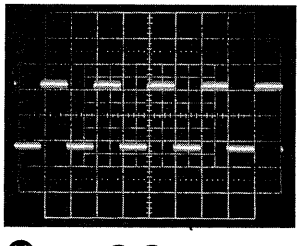
❼ IC702 ①pin (DATA)
5Vp-p, 10µs



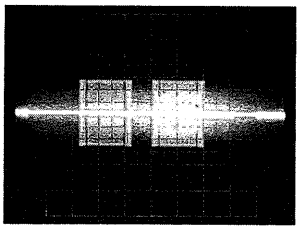
❽ IC702 ②pin (BCK)
5Vp-p, 0.35µs



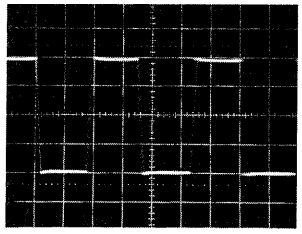
❾ IC702 ③pin (LRCK)
5Vp-p, 20µs



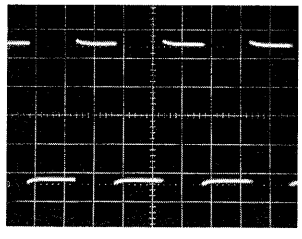
❿ IC01 ㉗,㉝pin (HEAD) REC mode
4.2Vp-p



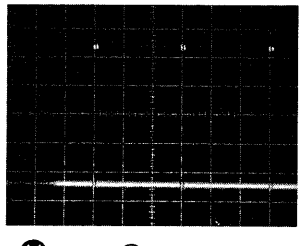
⓫ IC01 ①,⑦pin,IC311 ㊺,㊻pin(FGT,FGS) FF,REW mode
4Vp-p, 2ms



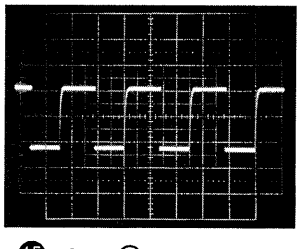
⓬ IC01 ⑩pin, IC311 ㊼pin (CFG) PLAY mode
5Vp-p, 1.5ms



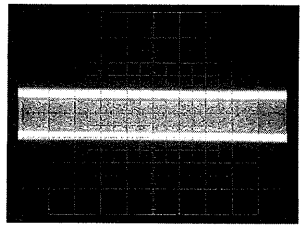
⓭ IC01 ⑦pin, IC311 ㊾pin (DPG) PLAY mode
5Vp-p, 30ms



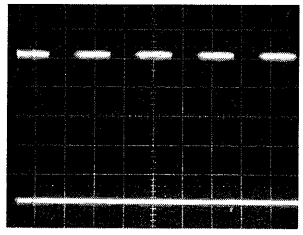
⓮ IC01 ③pin, IC311 ㊽pin (DFG) PLAY mode
5Vp-p, 1.5ms



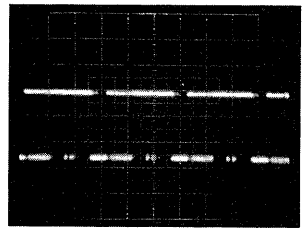
⓯ IC01 ①pin,Q440 Base (PBDT) PLAY mode
1Vp-p



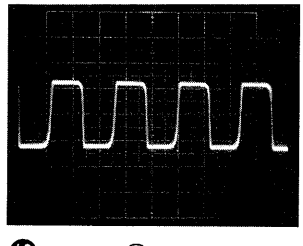
⓰ IC307 ㊽pin (DADO)
5Vp-p, 5µs



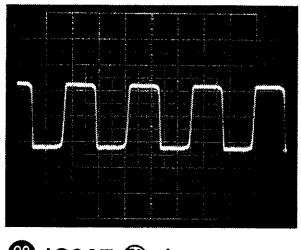
⓱ IC307 ㊻pin, IC359 ⑯pin (ADDT) REC mode
5.6Vp-p, 1µs



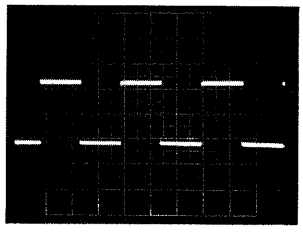
⓲ IC307 ㊺pin (BCK)
5.2Vp-p, 0.3µs



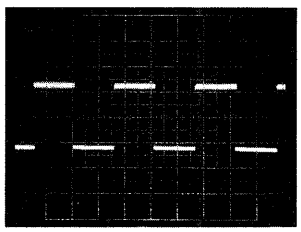
⓳ IC307 ㊹pin, IC359 ⑮pin (XBCK)
5Vp-p, 0.48µs



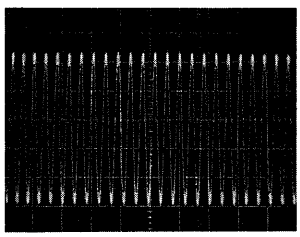
⓴ IC307 ㊷pin (LRCK)
5Vp-p, 32µs



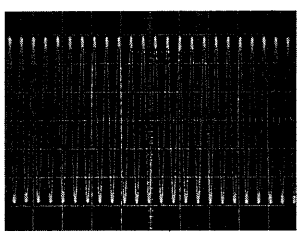
㉑ IC307 ㊾pin,IC359 ⑭pin (LR03)
5Vp-p, 20µs



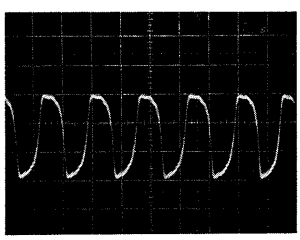
㉒ IC307 ㊼pin (XT3I)
1.4Vp-p, 0.12µs



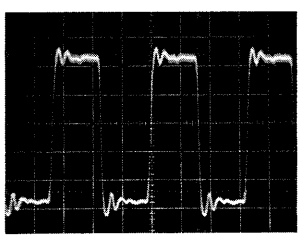
㉓ IC307 ㊻pin (XT3O)
6Vp-p, 0.2µs



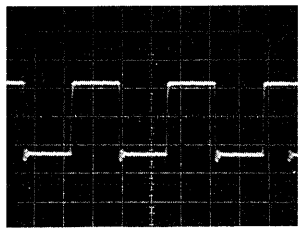
㉔ IC307 ㊾pin, IC359 ⑳pin
5Vp-p, 0.05µs



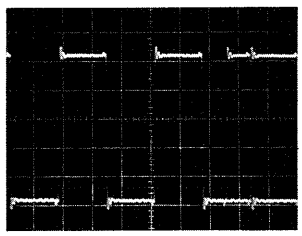
㉕ IC307 ㊽pin (F128)
5.8Vp-p, 0.17µs



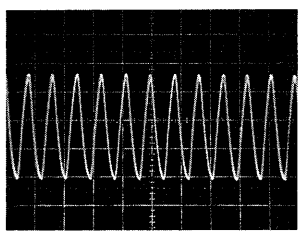
㉖ IC307 ㊹pin (TX)
PLAY mode
5Vp-p, 0.64µs



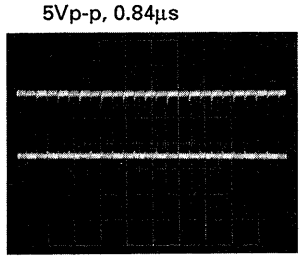
㉗ IC307 ㊷pin (RX)
5.2Vp-p, 0.64ms



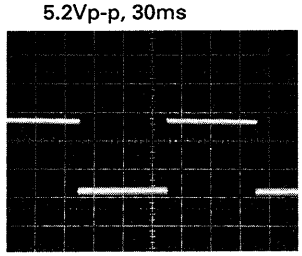
㉘ IC307 ㊽pin (PLCO)
3.7Vp-p, 0.052ms



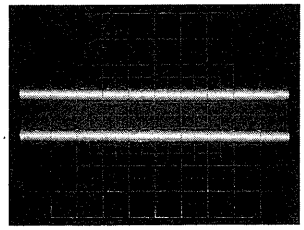
㉙ IC307 ㊸pin (REDT)
REC mode
5Vp-p, 0.84µs



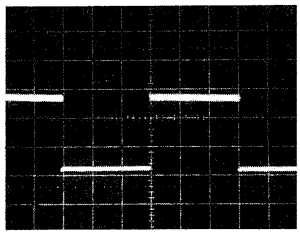
㉚ IC307 ㊾pin, IC311 ㊸pin (SWP)
PLAY mode
5.2Vp-p, 30ms



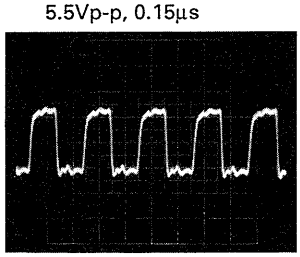
㉛ IC307 ㊲pin, IC311 ㊷pin (RFDT)
PLAY mode
1mVp-p, 2ms



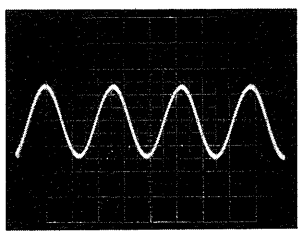
㉜ IC307 ㉑pin, IC311 ㊵pin (DREF)
5Vp-p, 30ms



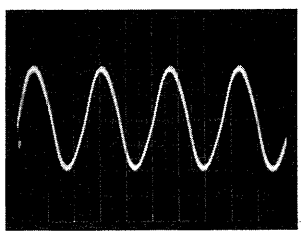
㉝ IC307 ⑳pin, IC311 ㉟,㊶pin IC312 ㉟pin (MCLK)
5.5Vp-p, 0.15µs



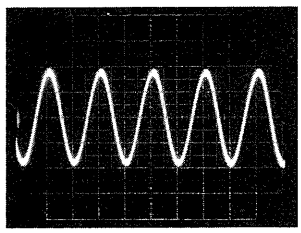
㉞ IC307 ⑭pin (XT1I)
2.8Vp-p, 18.816MHz



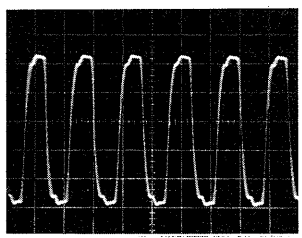
㉟ IC307 ⑬pin (XT1O)
4.4Vp-p, 18.816MHz



㊱ IC362 ⑪pin, IC502 ①,⑥pin (XIN)
3Vp-p, 0.5µs

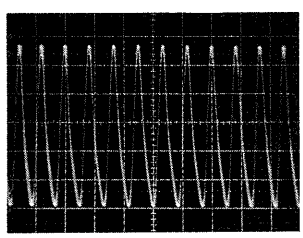


㊲ IC362 ⑦pin (BCK)
5.4Vp-p, 80ns

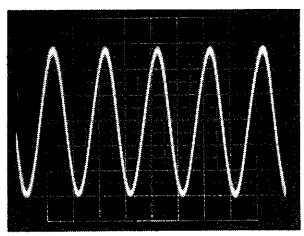


㊳ IC362 ⑥,⑤pin (DATAL, DATAR)
5.4Vp-p, 0.18µs

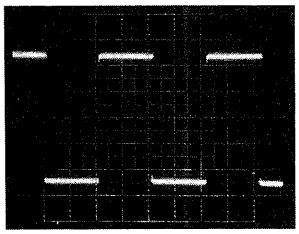
㊴ IC362 ④pin (LRCK)
5.6Vp-p, 0.52µs



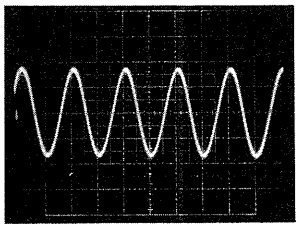
㊵ IC364 ⑰pin (MCLK)
3.6Vp-p, 52ns



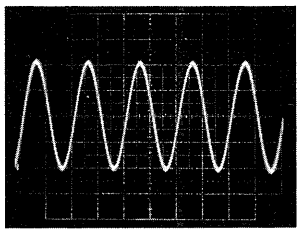
㊶ IC364 ⑩pin (LRCKI)
5Vp-p, 21μs



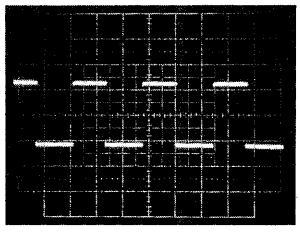
㊷ IC501 CATHODE (VCO)
3Vp-p, 0.75μs



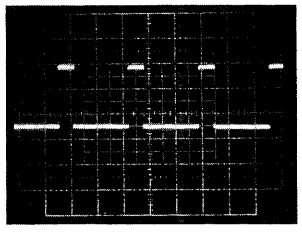
㊸ Q502 SOURCE (VCO)
3Vp-p, 0.52μs



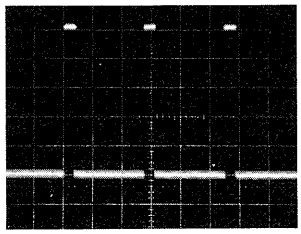
㊹ IC311 ㊹pin (D PWM) PLAYmode
5Vp-p, 28μs



㊺IC311 ㊺,㊻pin (CPWM, PWMR) PLAY mode
5.2Vp-p, 28μs

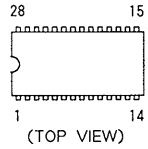


㊻ IC311 ㊼,㊽pin (TEN PWM, AGC PWM) PLAY mode
5Vp-p, 28μs

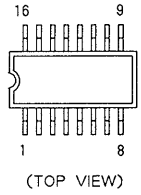


4-4. SEMICONDUCTOR LEAD LAYOUTS

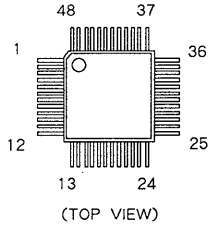
AK5339



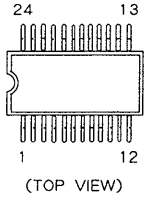
CX20115A



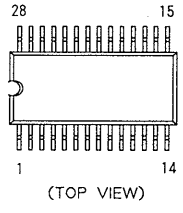
CXA1364R



CXD2560M



CXD2561BM-1
CXK58257AM-12L



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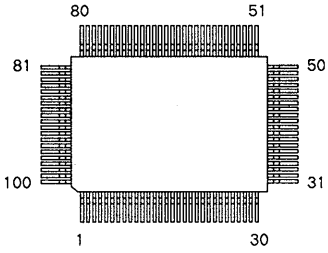

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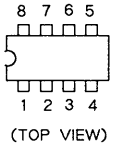
M5238P
NE5532P
μPC358C



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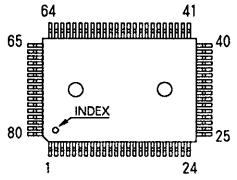
CXP80524-073Q
CXP80524-075Q



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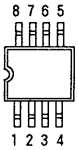

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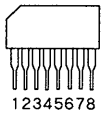
M54641L



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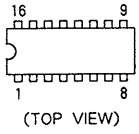

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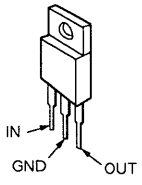

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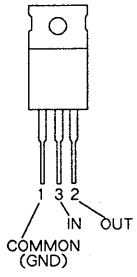

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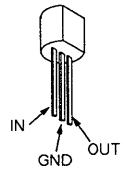

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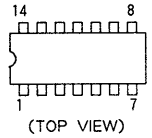

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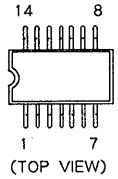

DTA114ES
DTC114ES
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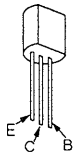
2SD1387



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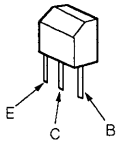

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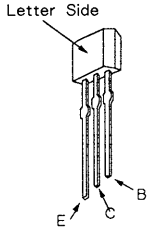

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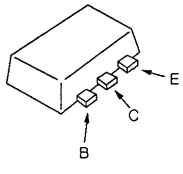
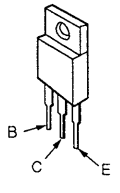
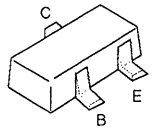


2SB1094-LK
2SD2012



2SC1623



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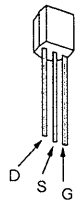

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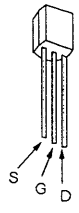
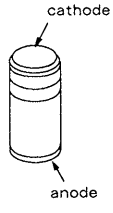
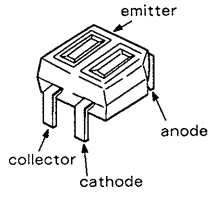


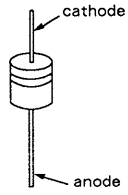
GL-453



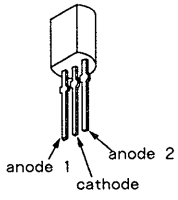
GP2S09-C



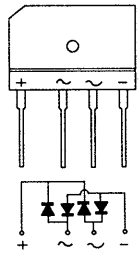
HZS6A1L
UZ-7L2
10E2N
11ES2



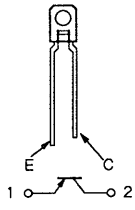
KV1260



RBA406B



PT4850F



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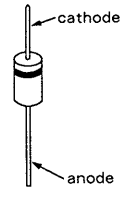


4-5. PRINTED WIRING BOARDS

– MD/POWER SUPPLY/DISPLAY SECTION –

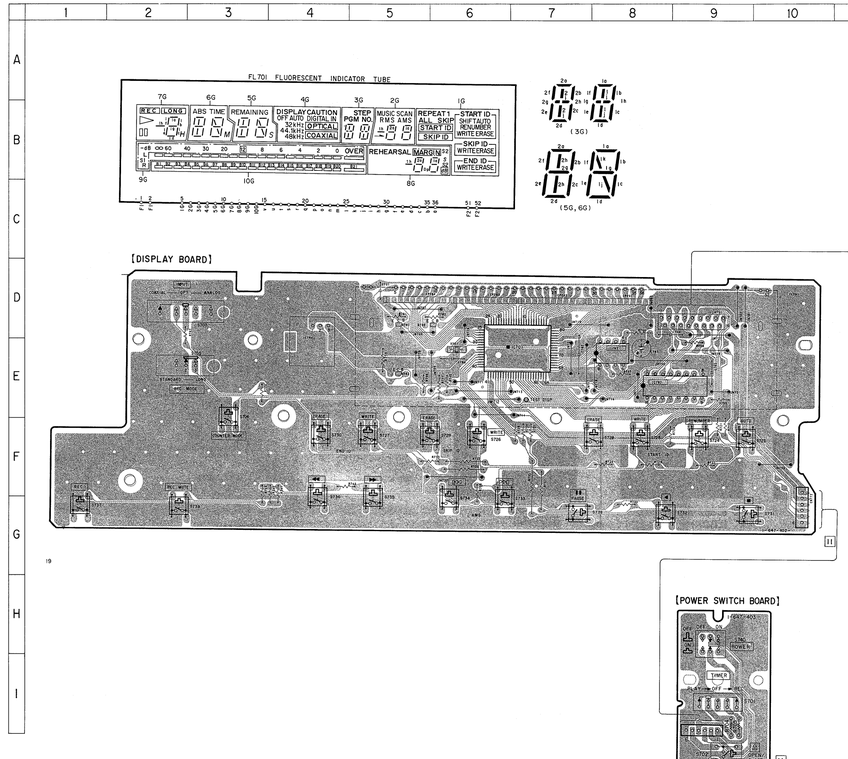
• See page 19 for circuit boards location and 26 for semiconductor lead layouts.

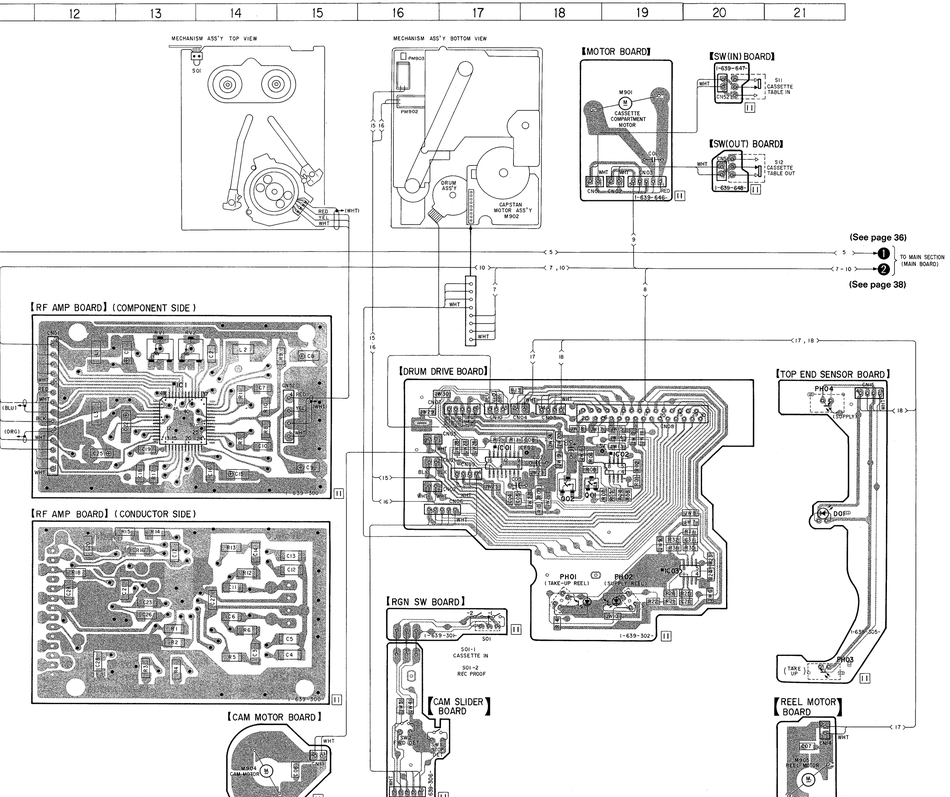
● SEMICONDUCTOR LOCATION

Ref. No.	Location
D01	G – 21
IC1	E – 13
IC01	F – 17
IC02	F – 19
IC03	G – 19
IC701	E – 6
IC702	E – 8
IC703	E – 8
IC704	D – 4
PH01	H – 18
PH02	H – 18
PH03	I – 21
PH04	E – 21
Q01	F – 18
Q02	G – 18
Q701	D – 5
Q702	D – 6
Q703	E – 5

Notes on printed wiring board:

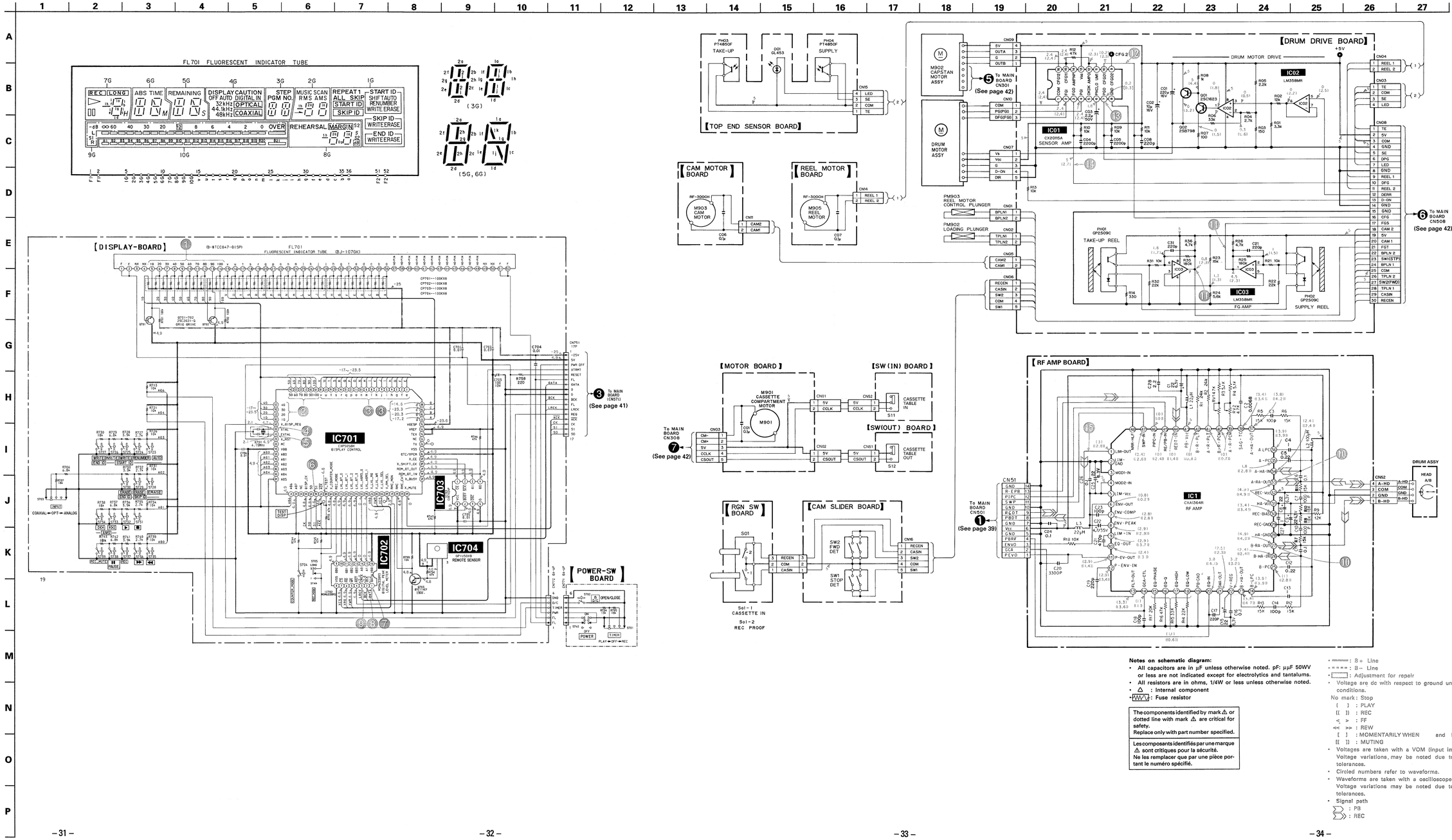
- ○——: Indicated a lead wire mounted on the component side
- ■ : Parts mounted on the conductor side
- ● : Through hole
- ▒▒▒ : Pattern from the side which enables seeing
- ▒▒▒ : Pattern of the rear side





4-6. SCHEMATIC DIAGRAM – MD/POWER SUPPLY/DISPLAY SECTION –

• See page 23 for waveforms, 43 for IC block diagrams and 47 for pin functions.



Notes on schematic diagram:

- All capacitors are in μF unless otherwise noted. pF: μμF 50WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in ohms, 1/4W or less unless otherwise noted.
- △ : Internal component
- ⊣WW⊢ : Fuse resistor

The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

Les composants identifiés par une marque ⚠ sont critiques pour la sécurité.
Ne les remplacer que par une pièce portant le numéro spécifié.

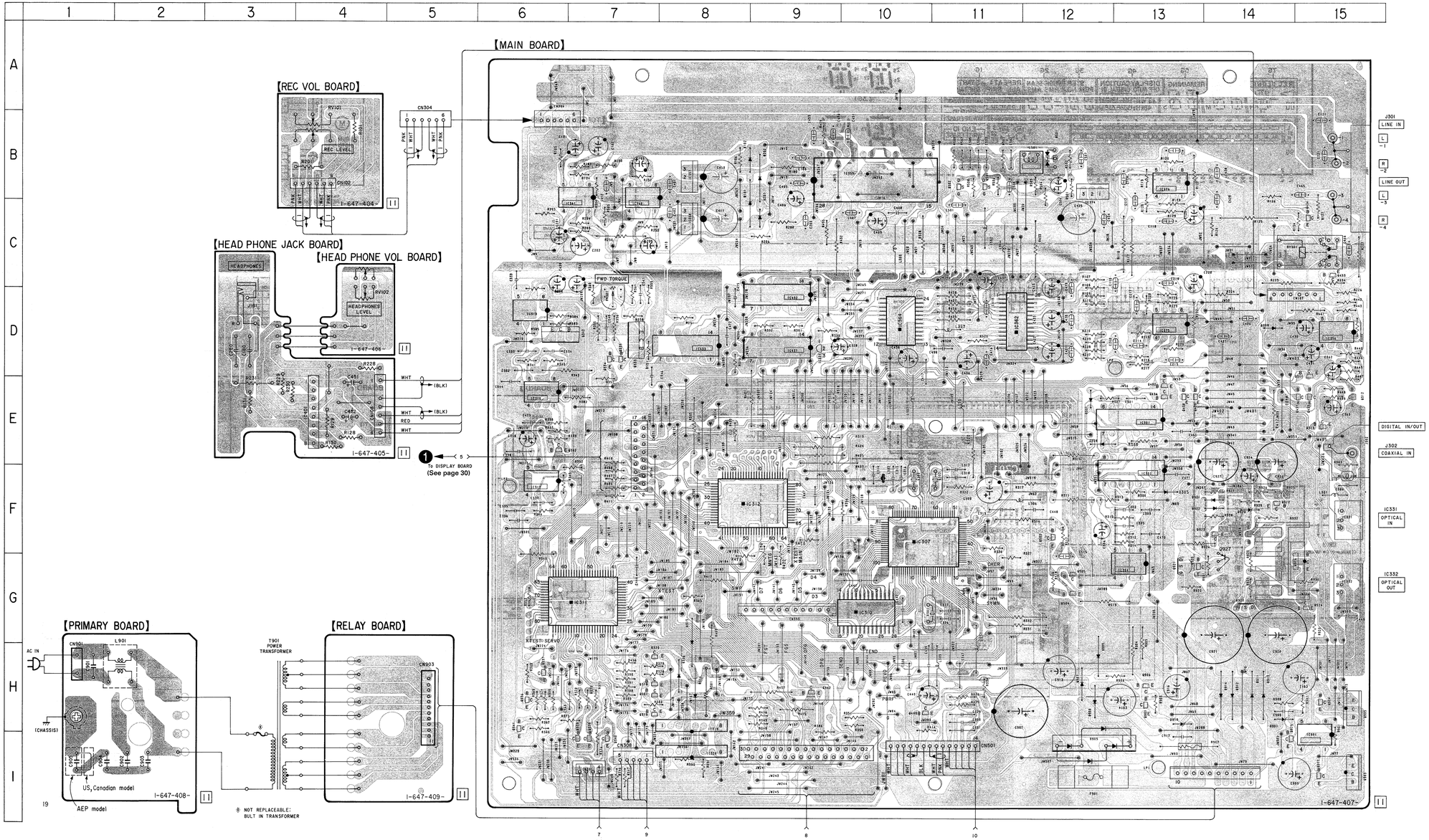
- ═══ : B+ Line
- ═ ═ ═ : B− Line
- ▭ : Adjustment for repair
- Voltage are dc with respect to ground under no-signal (STOP) conditions.
  No mark : Stop
  ( ) : PLAY
  (( )) : REC
  > : FF
  << >> : REW
  [ ] : MOMENTARILY WHEN and BUTTON IS PRESSED.
  [[ ]] : MUTING
- Voltages are taken with a VOM (input impedance 10MΩ). Voltage variations may be noted due to normal production tolerances.
- Circled numbers refer to waveforms.
- Waveforms are taken with a oscilloscope. Voltage variations may be noted due to normal production tolerances.
- Signal path
  ▷▷ : PB
  ▷▷ : REC

4-7. PRINTED WIRING BOARDS – MAIN SECTION –

• See page 19 for circuit boards location and 26 for semiconductor lead layouts.

● SEMICONDUCTOR LOCATION

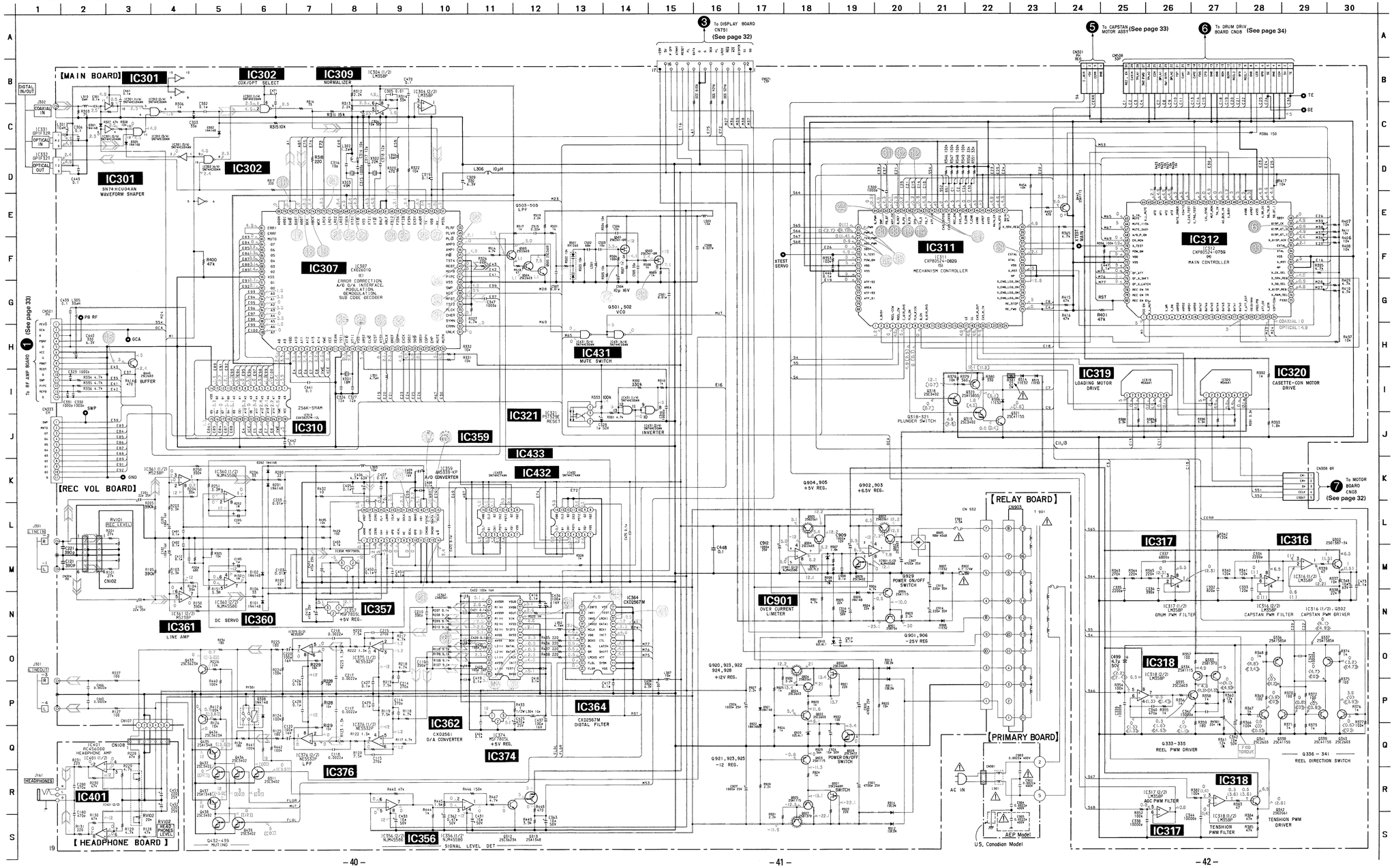
Ref. No.	Location	Ref. No.	Location
D101	C – 8	IC432	D – 9
D102	B – 8	IC433	D – 8
D201	C – 9	IC901	I – 15
D202	B – 9		
D301	E – 11	Q302	E – 6
		Q311	D – 15
D302	E – 12	Q312	E – 15
D305	F – 13	Q313	E – 15
D306	H – 7	Q318	H – 7
D308	D – 14		
D314	H – 7	Q319	H – 7
		Q320	H – 7
D315	G – 7	Q321	H – 7
D501	B – 12	Q333	D – 8
D901	H – 14	Q334	D – 7
D905	I – 12		
D907	H – 11	Q335	D – 7
		Q336	H – 6
D908	H – 11	Q337	H – 6
D909	H – 11	Q338	I – 7
D910	H – 13	Q339	I – 7
D911	H – 14		
D912	H – 14	Q340	I – 7
		Q341	H – 6
D913	H – 14	Q342	D – 6
D914	H – 14	Q432	E – 13
D920	F – 14	Q433	C – 15
D921	F – 14		
D922	F – 14	Q434	C – 15
		Q435	E – 15
IC301	E – 13	Q436	E – 13
IC302	F – 13	Q437	E – 15
IC304	G – 13	Q438	E – 13
IC307	F – 10		
IC310	G – 10	Q439	E – 13
		Q440	H – 10
IC311	G – 6	Q442	H – 8
IC312	F – 8	Q501	B – 11
IC316	E – 6	Q502	B – 11
IC317	F – 6		
IC318	D – 6	Q503	F – 11
		Q504	G – 12
IC319	H – 7	Q505	G – 12
IC320	I – 8	Q901	H – 13
IC321	D – 9	Q902	I – 15
IC331	F – 14		
IC332	G – 14	Q903	I – 15
		Q904	H – 15
IC356	D – 15	Q905	H – 15
IC357	B – 8	Q906	H – 13
IC358	C – 8	Q920	G – 14
IC359	B – 10		
IC360	B – 7	Q921	G – 13
		Q922	F – 14
IC361	B – 7	Q923	F – 14
IC362	D – 10	Q924	G – 15
IC364	D – 10	Q925	G – 13
IC374	B – 12		
IC375	D – 13	Q926	G – 14
		Q927	G – 13
IC376	B – 13	Q928	F – 14
IC401	E – 4	Q929	I – 14
IC431	D – 9		



Notes on printed wiring board:
- ○——: Indicated a lead wire mounted on the component side.
- ■ : Parts mounted on the conductor side
- ▒▒ : Pattern from the side which enables seeing

4-8. SCHEMATIC DIAGRAM – MAIN SECTION –

• See page 19 for waveforms, 39 for IC block diagrams and 43 for pin functions.



Notes on schematic diagram:

- All capacitors are in µF unless otherwise noted. pF: µµF 50WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in ohms, 1/4W or less unless otherwise noted.
- FWV : Fuse resistor

The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

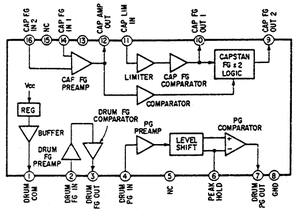
Les composants identifiés par une marque ⚠ sont critiques pour la sécurité.
Ne les remplacer que par une pièce portant le numéro spécifié.

- B+ Line
- B– Line
- Voltage are dc with respect to ground under no-signal (STOP) conditions.
  No mark : Stop
  [ ] : PLAY
  (( )) : REC
  > : FF
  >> : REW
  ( ) : MOMENTARILY WHEN and BUTTON IS PRESSED.
  [[ ]] : MUTING
- Voltages are taken with a VOM (Input Impedance 10MΩ). Voltage variations may be noted due to normal production tolerances.
- Circled numbers refer to waveforms.
- Waveforms are taken with a oscilloscope. Voltage variations may be noted due to normal production tolerances.
- Signal path
  : PB
  : REC

4-9. IC BLOCK DIAGRAMS

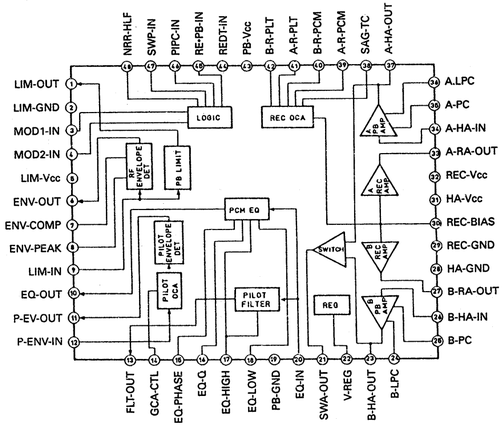
- **DRUM DRIVE BOARD**

IC01 CX20115A



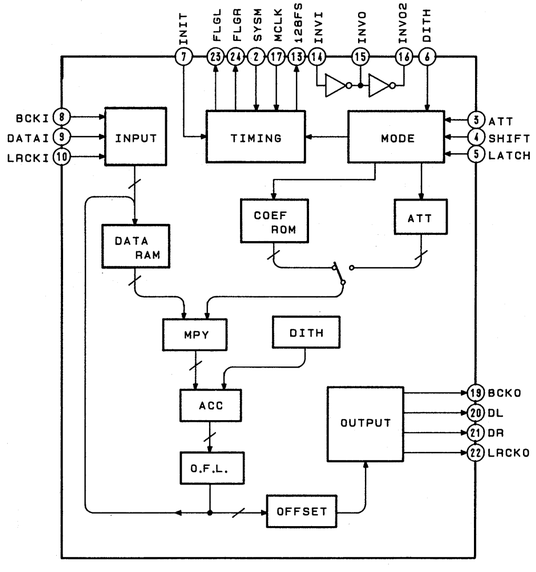
- **RF AMP BOARD**

IC1 CXA1364R

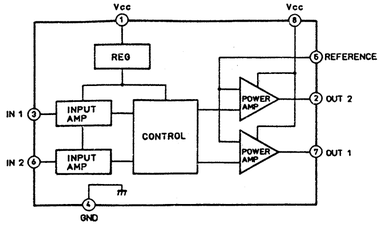


- **MAIN BOARD**

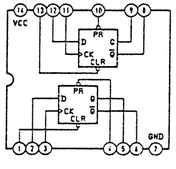
IC364 CXD2567M



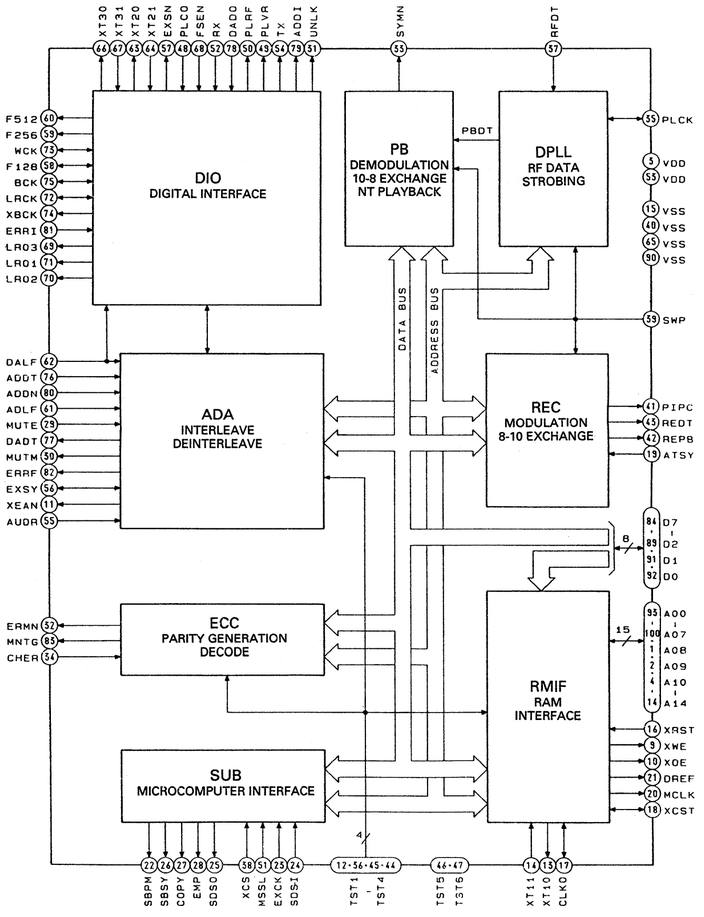
IC319,320 M54641L



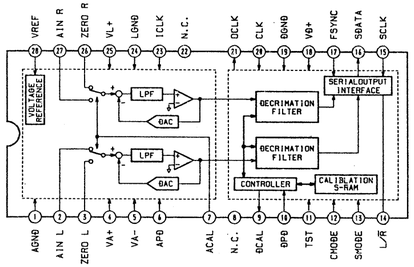
IC309 SN74HC74ANS



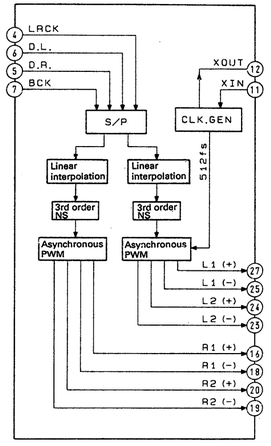
IC307 CXD2601AQ



IC359 AK5339



IC362 CXD2561M



4-10. PIN FUNCTIONS

IC307 DAT Signal Processor (CXD2601AQ)

This processor is an LSI to process recording and playback signals of the R-DAT system, in a single chip and provided with digital PLL, modem, error correction circuit, digital I/O, RAM control circuit, etc.

Pin No.	Pin Name	I/O	Description
1, 2	A08, A09	I/O	RAM address A08, A09
3	VDD	—	5 V
4-6	A10-A12	I/O	RAM address A10-A12
7, 8	A13, A14	O	RAM address A13, A14
9	XWE	O	RAM write enable signal
10	XOE	O	RAM output enable signal
11	XEAN	O	External addressing bus interrupt enable signal (Not in use)
12	TST1	I	Test pin (normally "L")
13	XT1O	O	18.816 MHz crystal oscillator output
14	XT1I	I	18.816 MHz crystal oscillator input
15	VSS	—	GND
16	XRST	I	Reset pin (normally"H")
17	CLKO	I/O	18.816 MHz clock output (Not in use)
18	XCST	I/O	SYEK (internal system clock) generation CLKO division timing signal (Not in use)
19	ATSY	I	ATF sync signal input
20	MCLK	O	9.408 MHz clock output
21	DREF	O	Drum servo reference signal
22	SBPM	O	Discrimination signal determining whether the subcode I/O clock (EXCK) is accepted ("L": accept, "H": ignore) (Not in use)
23	EXCK	I	Subcode I/O data transfer clock (DUTY50)
24	SDSI	I	Subcode serial data input
25	SDSO	O	Subcode serial data output
26	SBSY	O	Subcode I/O sync signal
27	COPY	O	Copy data output (Not in use)
28	EMP	O	Emphasis data output (Not in use)
29	MUTE	I	Mute pin
30	MUTM	O	Mute discrimination signal ("H": muted)
31	UNLK	O	RX PLL lock discrimination signal ("H": locked)
32	ERMN	O	Detects presence or absence of RF ("H": RF present, "L" during REC)
33	SYMN	O	C1 check result for RF ("H": OK) (Not in use)
34	CHER	I	Signal for discriminating whether C2 is 1 or 2 times (C2 → C1 → C2 or C1 → C2) ("H": 1 time, "L": 2 times) (Not in use)
35	PLCK	I/O	RF PLL clock output (Not in use)
36	TST2	I	Test pin (normally "L")
37	RFDT	I	RF signal input
38	XCS	I	Subcode I/O chip select ("L": select)
39	SWP	I	RF switching pulse ("L": A-CH, "H": B-CH)
40	VSS	—	GND
41	PIPC	O	REC data PILOT/PCM discrimination signal ("H": PILOT, during playback: always "L")
42	REPB	O	Record/playback switching signal ("H": record)
43	REDT	O	Recording signal output, fixed "L" during playback
44	TST4	I	Test pin (normally "L")
45	PDO	O	RX APLL PD output (comparator output)
46	AMPI	I	RX APLL oscillator cell amp input
47	AMPO	O	RX APLL oscillator cell amp inverted output
48	PLCO	I	RX APLL external VCO clock input

Pin No.	Pin Name	I/O	Description
49	PLVR	O	RX APLL comparison signal when external comparator is active (Vin) Not in use
50	PLVF	O	RX APLL comparison signal when external comparator is active (Rin) Not in use
51	MSSL	I	Master/slave setting ("H": master (fixed with the equipment), "L": slave)
52	RX	I	Digital input
53	VDD	—	5 V
54	TX	O	Digital output
55	AUDR	I	Audio mode/data recorder mode setting ("H": audio mode, "L": data recorder mode)
56	EXSY	I/O	Complete copy sync signal (25/3 - 100/3 Hz)
57	EXSN	I/O	Complete copy sync signal (25/3 - 100/3 Hz)
58	F128	I/O	128fsCK (normal)/256fsCK (×2) (DUTY50)
59	F256	O	256fsCK (normal)/512fsCK (×2) (DUTY50)
60	F512	O	512fsCK (normal)/512fsCK (×2) (DUTY50)
61	ADLF	I	Signal for discriminating whether ADDT serial data is MSB first or LSB first ("H": LSB first)
62	DALF	I	Signal for discriminating whether DADT serial data is MSB first or LSB first ("H": LSB first)
63	XT20	O	22.5792 MHz crystal oscillator output
64	XT21	I	22.5792 MHz crystal oscillator input
65	VSS	—	GND
66	XT30	O	49.152 MHz crystal oscillator output (24.576 MHz in B mode)
67	XT31	I	49.152 MHz crystal oscillator input (24.576 MHz in B mode)
68	FSEN	I	F128, BCK, LRCK input/output switch ("H": output)
69	LR03	O	LR02 inversion
70	LR02	O	LRCK 16BCK delay signal
71	LR01	O	LRCK 15BCK delay signal
72	LRCK	I/O	fs (normal)/2fs (×2) ("L": L-CH, "H": R-CH)
73	WCK	I/O	2fs (normal)/4fs (×2) (input mode only for testing)
74	XBCK	O	BCK inversion
75	BCK	I/O	64fs (normal)/128fs (×2)
76	ADDT	I	Serial AD data (complement of 2)
77	DADT	O	Serial DA data (complement of 2)
78	DADO	I	Digital output (DA) data input (normally connected to DADT)
79	ADDI	O	Digital input (AD) data output (normally connected to ADDN)
80	ADDN	I	Digital input (DA) data input
81	ERRI	I	Digital output V-FLAG data input (normally connected to ERRF)
82	ERRF	O	Signal output for discriminating whether or not DADT has interpolated data ("H": interpolated data)
83	MUTG	O	Error correction status monitor trigger
84-89	D7-D2	I/O	RAM data bus D7-D2
90	VSS	—	GND
91, 92	D1, D0	I/O	RAM data bus D1, D0
93-100	A00-A07	I/O	RAM address A00-A07

IC311 Mechanism/Servo Micon (CXP80524-073Q)

The mechanical deck servo systems are controlled by the captioned micon according to instructions from the main micon (IC312).

Pin No.	Pin Name	I/O	Connected to	Description
1		O		Not in use
2	$\overline{\text{BUSY}}$	O	Main Micon	Busy (Active "L") to the Main Micon
3		O		Not in use
4	REEL_CCW	O	Mechanism	Reel motor CCW ("L": RVS direction) } *1
5	REEL_CW	O	Mechanism	Reel motor CW ("H": FWD direction) } *1
6	C_DIR_RVS	O	Mechanism	Capstan Direction ("L": FWD, "H": RVS)
7	PLN_ON	O	Mechanism	Plunger On
8	PLN_KICK	O	Mechanism	Plunger Kick
9	D_ON	O	Mechanism	Drum On ("H": The drum is revolving)
10	D_DIR_RVS	O	Mechanism	Not in use
11-16		O		Not in use
17	LE	O	Mechanism	Loading Motor Eject } *2
18	LL	O	Mechanism	Loading Motor Load } *2
19	CAS_M_OUT	O	Mechanism	Cassette control motor Out } *3
20	CAS_M_IN	O	Mechanism	Cassette control motor In } *3
21-24		—		Not in use
25	RE_FWD	I	Mechanism	Encoder SW2 } *4
26	RE_STOP	I	Mechanism	Encoder SW1 } *4
27-30	$\overline{\text{END\_LED\_ON}}$	O	Mechanism	End sensor ON Illuminated upon "L" (rectangular wave of about 500kHz). It is not output unless a cassette is mounted ("H").
31	$\overline{\text{MP}}$	I		Microprocessor mode selected (the equipment is fixed at "L").
32	$\overline{\text{RST}}$	I		System Reset (low active)
33	Vss	—		Power terminal (GND)
34	XTAL	O		System Clock Output (Not in use)
35	EXTAL	I	CXD2601AQ	System Clock Input (9.408 MHz)
36-39		—		Not in use
40	X_SRV_REQ	I	Main Micon	Request for communication from the Main Micon
41	MAIN_DT_I	I	Main Micon	Serial Input from the Main Micon
42	MAIN_DT_O	O	Main Micon	Serial Output to the Main Micon
43	MAIN_CK	I	Main Micon	Serial Clock with the Main Micon
44	AVss	—		GND for A/D
45	AVref	—		Reference Voltage for A/D (+5 V)
46	AVdd	—		Power Supply for A/D (+5 V)
47	T_END	I	Mechanism	Take-up side end sensor input (analog) } Magnetic matter: 0V,
48	S_END	I	Mechanism	Supply side end sensor input (analog) } Leader tape: AC (*5)
49	CAS_IN	I	Mechanism	Cassette-in switch (S01). "H": Cassette is mounted.
50	REC_EN	I	Mechanism	Rec-enable switch (S01). "H": REC enabled.
51	CAS_LCKed	I	Mechanism	Casecon locked Upon completion of loading: "H"
52	CAS_OUTed	I	Mechanism	Casecon outed Upon completion of loading OUT: "H"
53		I		Not in use
54	ATF_IN	I	RF Amp	ATF PILOT input
55	FG_T	I	Mechanism	Reel FG (T Side) } 6/24Hz (Small reel diameter) -
56	FG_S	I	Mechanism	Reel FG (S Side) } 15/24Hz (Large reel diameter) (In SP FWD)
57	C_FG	I	Mechanism	Capstan FG SP: 674 Hz, LP: 337 Hz
58	D_FG	I	Mechanism	Drum FG 400 Hz: LP REC, 800 Hz: Other modes
59	D_PG	I	Mechanism	Drum PG } Other than LP REC: 800/24Hz
60	D_REF	I	CXD2601AQ	Drum Reference } In LP REC: 400/24Hz

Pin No.	Pin Name	I/O	Connected to	Description
61	MST_CK	I	CXD2601AQ	Master clock (9.408MHz)
62	PB_DT	I	RF Amp	PB Data input to create ATF Sync
63	SWP	O	CXD2601AQ	Switching Pulse "L": Ach, "H": Bch
64	D_PWM	O	Mechanism	PWM Out for Drum
65	C_PWM	O	Mechanism	PWM Out for Capstan
66	PWM_R	O	Mechanism	PWM Out for Reel
67	TEN_PWM	O	Mechanism	PWM Out for Tension Regulator Plunger
68	AGC_PWM	O	RF Amp	PWM Out for AGC
69	SBSY	I	CXD2601AQ	↓ of subsync is detected (XINT2).
70	TEST	I	Pull-up	Test Mode (active "L")
71	POW_DN	I		Not in use
72	Vdd	—		Power terminal (+5 V)
73	Vss	—		Power terminal (GND)
74		—		Not in use
75	ATF_S2	O	CXD2601AQ	ATF Sampling Pulse
76-80		—		Not in use

* 1 Reel motor control

	CCW (counterclockwise)	CW (clockwise)
STOP (only in POWER ON)	L	L
FWD	L	H
RVS	H	L
Prohibit	H	H

*2 Loading motor control

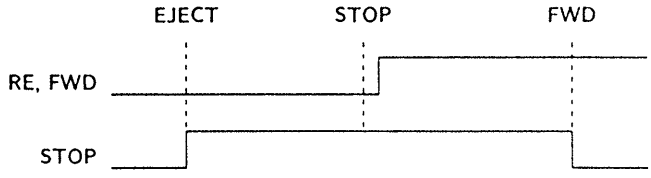
	LE	LL
—	L	L
LOAD	L	H
EJECT	H	L
Brake	H	H

*3 Casecon motor control

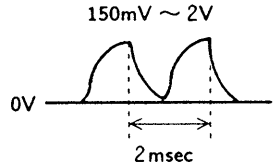
	OUT	IN
—	L	L
IN	L	H
OUT	H	L
Brake	H	H

*4 Encoder

RF-FWD	RE_STOP	Position
L	L	EJECT
L	H	STOP UNLD-STOP
H	L	FWD
H	H	STOP-FWD



*5 End sensor



With leader tape

IC312 Main Micon (CXP80524-075Q)

This Micon generally controls the operation of the equipment while exchanging data with the display micon (IC701) and mechanism/servo micon (IC311) in serial communications, including the DAT signal processor (IC307), digital filter (IC363) and other IC.

Pin No.	Pin Name	I/O	Connected to	Description
1		O		Not in use
2	L_MUTE	O	Line Out	Line Mute (Active "L")
3		O		Not in use
4		O		Not in use
5	WRT	O	Clock IC	Write request (Active "L")
6	RD	O	Clock IC	Read request (Active "L")
7-10	ADRS_3-0	O	Clock IC	Address 3-0 (Address BUS)
11-14	DATA_7-4	I/O		DATA 7-4 (DATA BUS). Not in use with the equipment
15-18	DATA_3-0	I/O	Clock IC	DATA 3-0 (DATA BUS)
19	ATT_EXT	O	CXD1136Q	Fade attenuator ck externally selected (Active "L")
20	DIG/ANA	O	CXD1136Q	Fade In/Out switching for DIG ("L")/ANA ("H")
21	REC/PB	O	CXD1136Q	Fade In/Out REC switching for ("L")/PB ("H")
22	ATT_CK	O	CXD1136Q	Clock for fade In/Out
23	DTR	O	CXD2601AQ	Audio use ("H")/Data Recorder use ("L). Becomes "L" in after-recording and searching.
24	OPT/COA	O	Digital I/O	Switching for Optical ("L")/Coaxial ("H")
25	FS32	O	1Bit DAC	"H" upon Fs = 32kHz. "L" for others.
26	RAM_SEL	O		Not in use
27	DISP_REQ	O	Display Micon	Request for communication with the Display Micon ("L" Active)
28	SD_SEL	O	CXD2601AQ	Request for communication with CXD2601 ("L" Active)
29	SRV_REQ	O	Mechanism Micon	Request for communication with the Mechanism Micon ("L" Active)
30	CLOCK_SEL	O	Clock IC	Clock IC chip selected
31	MP	I		Microprocessor mode selected (fixed at "L" with the equipment)
32	RST	I		System Reset ("L" Active)
33	Vss	—		Power terminal (GND)
34	XTAL	O		System Clock Output (Not in use)
35	EXTAL	I	CXD2601AQ	System Clock Input (9.048 MHz)
36	DISP_ACK	I	Display Micon	ACKnowledge (Active "L")
37	DISP_DT_I	I	Display Micon	Serial Input
38	DISP_DT_O	O	Display Micon	Serial Output
39	DISP_CK	I	Display Micon	Serial clock
40	SBSY	I	CXD2601AQ	Subcode sync
41	SR_DT_IN	I	CXD2601AQ & Mechanism Micon	Serial Data In
42	SR_DT_OUT	O		Serial Data Out
43	SR_CK	I/O		Serial clock (In/Out) to Sub Code Interface
44	AVss	—		GND for A/D
45	AVref	—		Reference Voltage for A/D (+5 V)
46	AVdd	—		Power Supply for A/D (+5 V)
47		I		Not in use
48		I		Not in use
49	BUSY	I	Mechanism Micon	Mechanism servo micon Busy (Active "L")
50	AU_BUS_IN	I	Audio Bus	Not in use

Pin No.	Pin Name	I/O	Connected to	Description
51	TM_IN	I	Clock IC	TM_OUT for clock IC
52	MUT_MON	I	CXD2601AQ	Mute monitor (Active "H")
53	LVL_SYNC	I	Audio Block	Start ID is written by entering Level Sync Input audio.
54		I		Not in use
55	$\overline{\text{TRQ\_TEST}}$	I	Pull-up	Not in use
56	$\overline{\text{NO\_CAS\_TEST}}$	I	Pull-up	Not in use
57	TIME_$\overline{24}$/12	I	Pull-up	Time indication "H": 12 hours (AM, PM) "L": 24 hours display
58	DATE_ORDER	I	Pull-up	Order of DATA display "H": Year, month and day "L": Month, day and year
59-62	AF_3-0	I	Pull-up	Not in use
63		O	Pull-up	Not in use
64	$\overline{\text{L\_MUTE}}$	O		Line Mute (Active "L"). Not in use with the equipment (Not in use)
65	$\overline{\text{TR\_MUTE}}$	O	Line Out	Transistor Mute (Active "L")
66	MUTE_1136	O		Not in use
67	MUTE_2601	O	CXD2601AQ	Mute for CXD2601 (Active "H")
68	A_D_PWR_DWN	O	CS5339	A/D Converter Power Down Mode (Active "H"). The AD converter is turned OFF upon digital input/output.
69	ER_MON	I	CXD2601AQ	Error Monitor (Data Valid)
70	$\overline{\text{TEST}}$	I	Pull-up	Test Mode (Active "L")
71	POW_DN	I	+5 V	Not in use
72	Vdd	—		Power terminal (+5V)
73	Vss	—		Power terminal (GND)
74		—		Not in use
75	D_F_ATT	O	CXD2560M	Communication line (Serial Data) with Digital Filter
76	D_F_$\overline{\text{SHIFT}}$	O	CXD2560M	Communication line with Digital Filter (Shift Clock; shifted by ↓ and taken in by ↑)
77	D_F_$\overline{\text{LATCH}}$	O	CXD2560M	Communication line (Latch Pulse) with Digital Filter
78, 79	MODE2, 1	O		Mode Control of the RF amplifier (Not in use)
80		O		Not in use

IC362 Pulse D/A Converter (CXD2561M-1)

The Converter is a small, high-performance 1 bit pulse D/A converter that provides 4 asymmetrical PWM wave outputs in each ch of L/R.

Pin No.	Pin Name	I/O	Description
1	DV_{DD}	—	Digital power supply
2	TEST	I	Test terminal. Normally fixed at "L."
3	INIT	I	Again synchronized at the buildup edge of the signal.
4	LRCKI	I	LRCK input
5	DRI	I	Rch data input
6	DLI	I	Lch data input
7	BCKI	I	BCK input
8	DVss	—	Digital GND
9	512Fs	O	512Fs output
10	XVss	—	Clock GND
11	XIN	I	X'tal oscillator input terminal (512Fs)
12	XOUT	O	X'tal oscillator output terminal
13	XV_{DD}	—	Clock power supply
14	VSUB	—	Substrate. Connected to GND.
15	$AV_{DD}R$	—	Analog power supply
16	R1 (+)	O	Rch PLM output 1 (normal phase)
17	AVssR	—	Analog GND
18	R1 (–)	O	Rch PLM output 1 (reverse phase)
19	R2 (+)	O	Rch PLM output 2 (normal phase)
20	R2 (–)	O	Rch PLM output 2 (reverse phase)
21	AV_{DD}	—	Analog power supply
22	AVss	—	Analog GND
23	L2 (–)	O	Lch PLM output 2 (reverse phase)
24	L2 (+)	O	Lch PLM output 2 (normal phase)
25	L1 (–)	O	Lch PLM output 1 (reverse phase)
26	AVssL	—	Analog GND
27	L1 (+)	O	Lch PLM output 1 (normal phase)
28	$AV_{DD}L$	—	Analog power supply