8/1/2005

Errata: CS8416 Rev. B

Rev. B Silicon (Reference CS8416 Datasheet revision DS578F1)

- For revision B, bi-phase encoded signals with F_S < 48 kHz AND less than 24-bit audio data can cause the PLL to take more time to lock. To shorten the lock time under these conditions use the external PLL component values listed in Table 1:

Range (kHz)	R_{FLT}	C_{FLT}	C_{RIP}
32-96	1 kΩ	220 nF	10 nF

Table 1

Systems using bi-phase encoded signals with F_S ≥ 48 kHz OR 24-bit audio data should use the external PLL component values listed in the datasheet and repeated in below in Table 2:

Range (kHz)	R_{FLT}	C_{FLT}	C_{RIP}
32-192	3 kΩ	22 nF	1 nF

Table 2

For revision D, the external PLL component values listed in the datasheet (and repeated here in Table 2) should be used for all conditions.

- In Software mode, the PDUR bit (bit 3 of the Control0 register) is not available in revision B and should not be used. This function will be added in revision D. This register bit should be written with a '0' for revision B.
- In Hardware mode, the TX pin startup option for PDUR is not available in revision B and should not be used. This function will be added in revision D. This pin should be pulled low for revision B.
- The Power Supply Voltage specification for VA should be:
  - Min=3.2 V
  - Max=3.46 V
- When the PLL loses lock and OMCK is set to output on RMCK (always enabled in Hardware mode), with RMCK set to 256*Fs, RMCK will equal the clock on OMCK. However, when the PLL loses lock and OMCK is set to output on RMCK, with RMCK set to 128*Fs, RMCK will be indeterminate. In both modes, when LRCK and SCLK are set as master, they will be divided down from OMCK, where LRCK=OMCK/256 and SCLK=OMCK/(4 or 2).

- OMCK System Clock Mode does not function properly at sample rates above 96 kHz. As a result, when OMCK System Clock Mode is enabled and the sample rate is above 96 kHz the part may indicate an unlock condition and may not drive the RMCK signal onto the pin. Also, invalid serial audio output data and clocks may result.

  In software mode, OMCK System Clock Mode is disabled on startup, allowing the part to operate at sampling frequencies up to 200 kHz. Should this function become enabled by setting the SWCLK bit in the Control1 register (01h) to '1', it may be disabled by setting it to '0', once again allowing the part to operate at sampling frequencies up to 200 kHz.

  In hardware mode, OMCK System Clock Mode is permanently enabled, and therefore the part will not function properly at sample rates above 96 kHz.

- In Software mode, GPOxSEL[3:0] = 0000 selects the TX passthrough and GPOxSEL[3:0] = 1011 selects GND.

- In Software mode, the FSWCLK bit (bit 6 of Control0 register) is not available in revision B and should not be used. This function will be added in revision D. This register bit should be written with a '0' for revision B.