EMC Improvement Guidelines

1. Introduction

High-speed digital Integrated Circuits operate in frequency bands where passif components (PCB, decoupling capacitors, PCB connexions, packages, ...) can not be considered as ideal but with parasitic elements (inductance, resistance, ..). Because their impedances depend on the frequency, the emission levels generated by voltage and current drops may not be compliant to the different EMC standards. It is impossible to predict the compliance of a system but it is possible to reduce the risk by implementing some rules and design technics in most applications. This application note gives a brief checklist of major points which can degrade EMC and then demonstrates how some basic technics can help to reduce emission levels and harden the electronic system.

2. EMC Definitions

Some following basic terms are used in this application note and are explained hereafter:

- **EMC**: *Electromagnetic Compatibility*, the ability of a product to coexist in its intended electromagnetic environment without causing or suffering functional degradation or damage.

- **EMI**: *Electromagnetic Interference*, a process by which disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths (or both).

- **Radiated**: Energy transmitted by the air via antenna or loops.

- **Conducted**: Energy transmitted via solid medium like cables, PCB connexions, packages, ...

They are three elements in the EMC model to analyse and understand an EMC problem:

- A **Noise source**, a source that generates a electromagnetic perturbation,

- A **victim**, an electronic device that receives a perturbation which causes dysfunctionalities,

- A **coupling path**, a medium that transmit energy from the noise source to the victim.

Figure 1 shows the topology of an EMC environment. A noise source drives a current *i(t)*. This current flows through the left coupling path (PCB connexion for example) and causes voltage drops. This voltage perturbation is transmitted to the victim through the right coupling path and can cause a dysfonctionnality if the level is high enough.
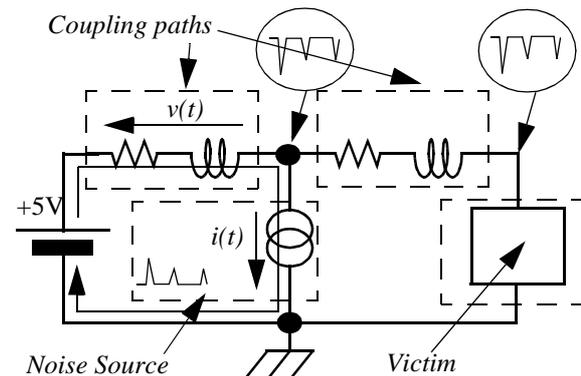

Figure 1. Elements of EMC environment

To significaly improve the EMC quality of the design the EMC environment through these elements have to be analysed.

3. Basic Ckecklist to be Compliant with EMC

The basic rules to decrease the conducted and radiated emissions through the power-supply are to:

- Reduce the speed of the system:
  - *Choose the lowest system clock frequency,*
  - *Adapt the technology to the system constraints.*
- Reduce all the magnetic loops of the Printed Circuit Board:
  - *Decrease the surface of the magnetic loops,*
  - *Maintain the signal trace closed to the ground,*
  - *Shorten the loops around the oscillator and crystal.*
- Cancel H field:
  - *Opposite magnetic loops,*
  - *Choose a package with a VCC adn VSS pins close together,*

- *Choose a package with several VSS and VCC pins connected in opposite side.*
- Reduce the parasitic inductance of all devices (PCB traces, package, capacitors, ...):
  - *Increase the PCB connection widths,*
  - *Use ground and power planes,*
  - *Adapt the decoupling capacitors to the working frequency of IC's,*
  - *Shorten the capacitor connexion length,*
  - *Select the smaller package.*
- Reduce the Equivalent Serie Resistance (ESR):
  - *Put identical capacitors in parallel to reduce the ESR,*
  - *Choose COG and NPO dielectrique types.*

All theses rules are detailled in the following sections.

4. Reduce the Speed of the System

4.1. Maintain the System Clock Frequency as low as Possible

A key parameter to improve EMC is to reduce the working frequency of the system. The system clock frequency is defined by evaluating the following guidelines:

- the realtime events such as interrupts, serial link, ...
- the CPU time to process all the tasks attached to these events,
- the most critical window where the CPU has to process a sequence of realtime events,
- the clock frequency to achieve this window time.

and then increase the clock frequency by 20 to 30% to have a good margin.

4.2. Adapt the Technology to the System Constraints

Another key parameter to reduce EMI is to select the slowest technology of the components used in the system (address latch, memories, buffers, ...). Indeed the spectral envelop has two cut-off frequencies and is shown on Figure 2. The first one (FC1) depends on the pulse width of the signal and the second (FC2) depend on the sharpness of the transition mainly due to the technology. Slower the technology lower the EMI.
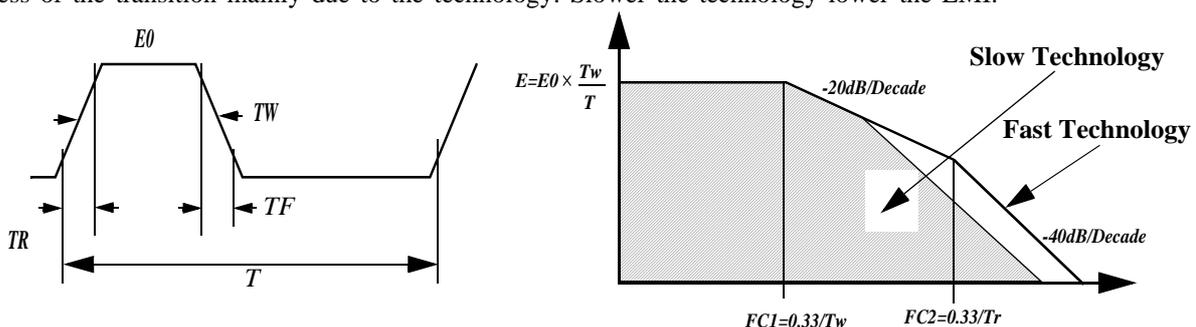

Figure 2. Spectrum of the trapezoïdal signal for a fast and slow technlogy

A timing analysis of the system has to be done to choose the slowest technology of the components to determine the electrical characteristics of such devices. When the maximum operation frequency limit is divided by two EMI is reduced by 12dB.

5. Reduce all the magnetic loops of the Printed Circuit Board

5.1. Decrease the Magnetic Loop Surface

A current flowing around a loop generates a magnetic field (H) proportionnal to the area of the loop. The next equations give the mathematical expressions when the observation distance is in the near and far field conditions:

$$Hnear_{A/m} = I \times \frac{S}{4 \times \pi \times D^3}, \quad Hfar_{A/m} = \pi \times I \times \frac{S}{\lambda^2 \times D}$$

where,

$I(A)$:loop current, $S(m^2)$:loop surface, $D(m)$: observation distance, $\lambda(m)$: current wavelength.

The near field and far condition is expressed by the following formula:

$$\frac{D}{\lambda} = \frac{1}{2 \times \pi}$$

This ratio indicates the transition where the emission is in far field or in near field conditions (see Figure 3). The far field condition is a specific distance where the electrical and magnetic fields are coupled and perpendicular. In that condition the ratio E/H is the intrinsic impedance of free space equal to 300 Ω. In the near field condition the nature of the fiels depends on the connection impedance. For an high impedance (Z >>300 Ω) the field is electric and magnetic if impedance is low (Z << 300 Ω).

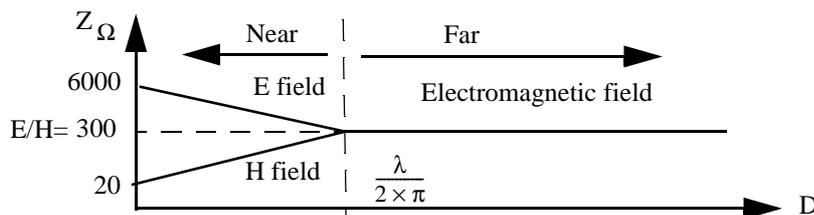**Figure 3. Far and near field conditions**

For example at 3 meters, F=30Mhz and I=0.1A, the magnetic field intensity is -19.6dbµA for a 1cm² surface loop and -13.6dbµA when the loop surface is doubled. So reducing the surface by a factor of two leads to decrease H field by a factor of 6dB. This can be achieved by carefully checking the PCB lay-out.

The decoupling capacitor acts in this way as well. It supplies locally the fast transient current and reduces the length of the current discharging path. It contributes to reduce the closed contour taken by the current and finally the radiation surface as shown in Figure 4.
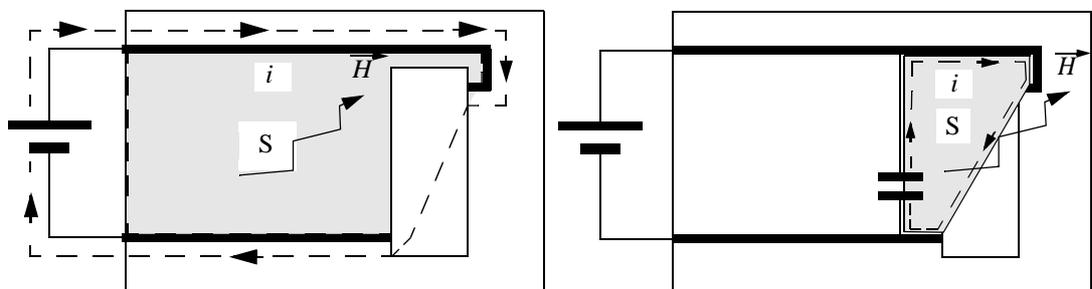

Figure 4. Decoupling capacitor reduces the magnetic field and the loop surface.

5.2. Maintain the Signal Trace close to the Ground

To maintain a low parasitic inductance of a signal trace the distance to the ground have to be maintained short. The parasitic inductance of two parallel conductors carrying uniform current in opposite direction consists of self and mutual inductances as shown in Figure 5. This figure depictes the two kinds of parallel conductors which can be found and their electrical equivalent model.
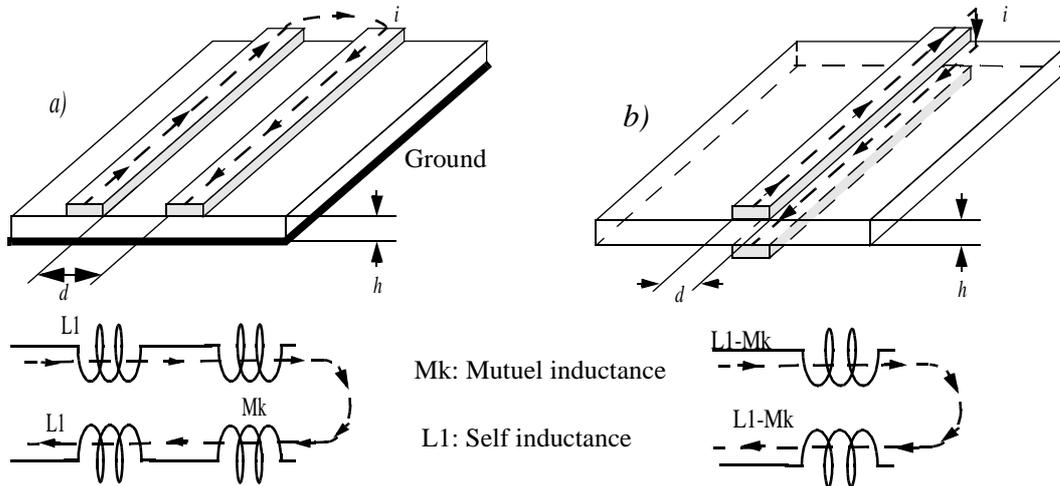

Mk: Mutuel inductance

L1: Self inductance

Figure 5. Structure of a parasitic inductance

The total inductance for such topology equal to:

$$LT = L1 + L2 - 2 \times Mk$$

$$Mk = k \times \sqrt{L1 \times L2}$$

where L1 and L2 are the self-inductance of the individual conductors and Mk is the mutual inductance between them. If the VCC and VSS are identical then LT is reduced to:

$$LT = 2 \times (L1 - Mk)$$

If the coefficient of magnetic coupling k between the two conductors is unity, the mutual inductance would be equal to the self-inductance of one conductor, since

$$Mk = L1$$

and the total inductance of the closed loop would be zero. So to minimize the total inductance of the complete current path, the mutual inductance between the conductors must be maximized. Therefore the two conductors should be placed as close as together as possible to minimize the area between them. Figure 6 and Figure 7 give the mutual inductance for different spacings.
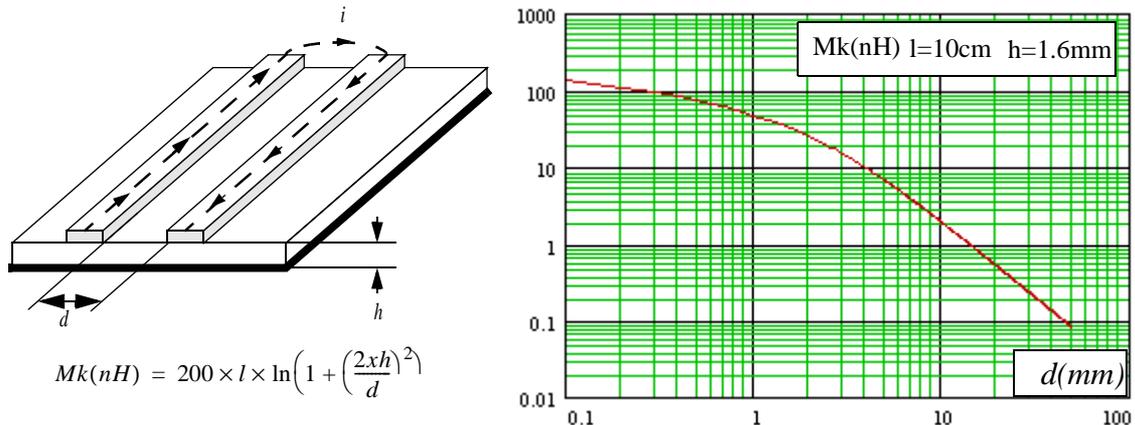
$$Mk(nH) = 200 \times l \times \ln\left(1 + \left(\frac{2xh}{d}\right)^2\right)$$

Figure 6. Mutual inductance for l=10cm and h=1.6mm

For this configuration the formula is applicable only if the direct and return currents are flowing through these two traces. Figure 7 plots different Mk values for somes PCB trace dimensions.
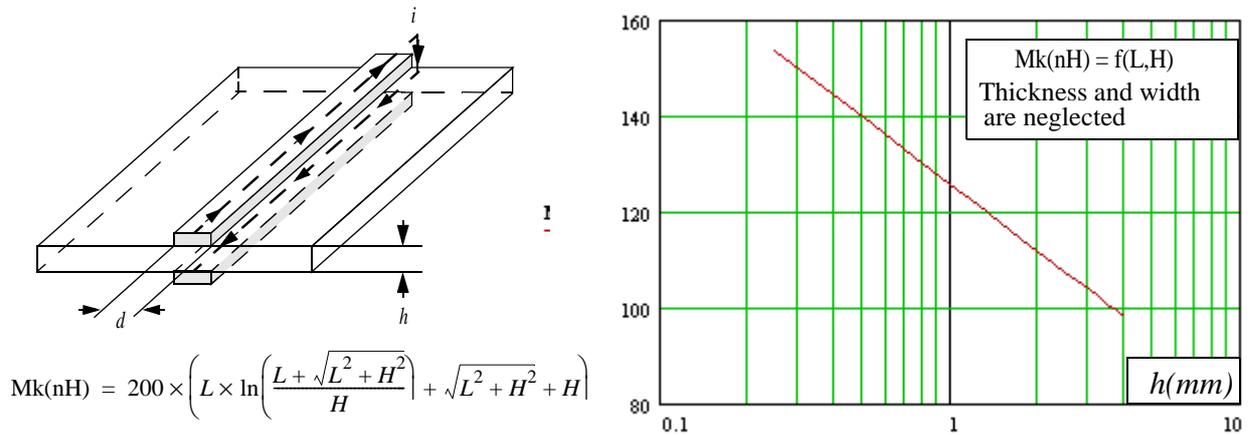

$$Mk(nH) = 200 \times \left[L \times \ln\left(\frac{L + \sqrt{L^2 + H^2}}{H}\right) + \sqrt{L^2 + H^2} + H \right]$$

Figure 7. Mutual inductance versus the length and the height of PCB traces

If there is no dedicated plane for the power it is recommended to maintained as close as possible those tracks to reduce the surface of loop and the parasitic inductance as shown in Figure 8.
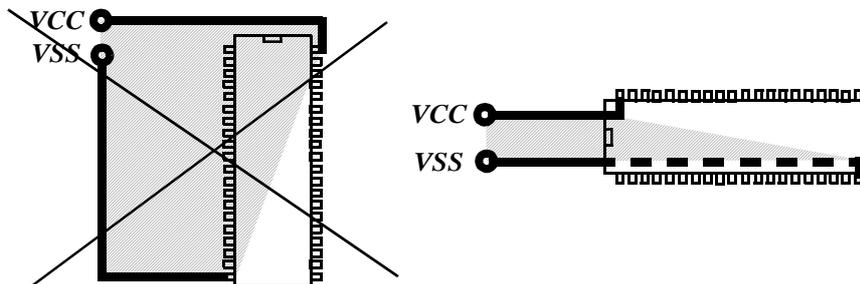

Figure 8. The surface of the VCC and VSS network has to be reduced

5.2.1. Shorten the Loops around Oscillator and Crystal

Figure 9 shows the electrical model of a common oscillator implemented in a microcontroller. At the resonance the fundamental currents i1 and i2 have the same amplitude. In the closed loop mode the oscillator is stabilized in the saturation region of the amplifier that generates some harmonics in HF. So the output loop (X2, C2, and VSS) has to be optimized first and then the input loop (X1, C1 and VSS). In both cases they have to be as small as possible.
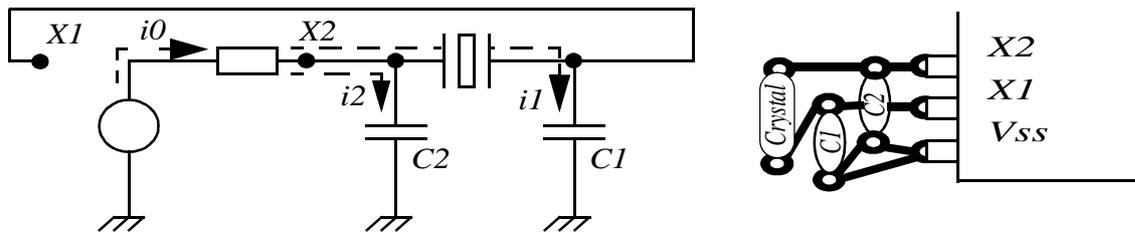

Figure 9. Oscilator lay-out

6. Cancel the H field

6.1. Opposite Magnetic Loops

Identical circuits have to be implemented like in Figure 10. In Such implementation the magnetic loop surface is the same and the H field are generated in opposite side which tends to cancel them. Other implementations can be used but this one needs only one decoupling capacitor for two chips.
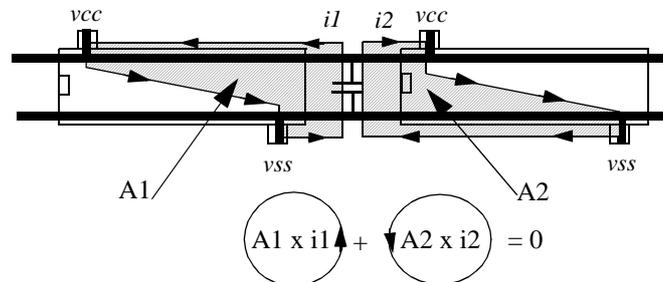

Figure 10. H field cancellation

6.2. Choose a Package with a VCC and VSS close together

When a VSS and VCC pins are close together the magnetic coupling can be closed to 0.8 and the mutuel inductance can reach the self inductance of one pin and cancel magnetic field of the total inductance of the VSS and VCC pins. This true when *ivss* and *ivcc* have the same magnitude and the same phase which is the case for the current flowing through a digital core of an I.C but not completely true for an output buffer.
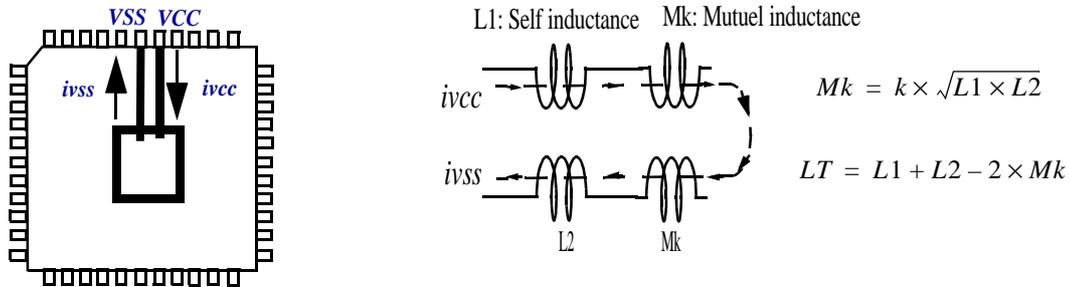

$$Mk = k \times \sqrt{L1 \times L2}$$

$$LT = L1 + L2 - 2 \times Mk$$

Figure 11. VSS and VCC pins close together can cancel the Hfield

6.3. Choose a Package with Several VSS and VCC Pins Connected in Opposite Side

Double the number of VCC and VSS pins reduce by the half the equivalent pin inductance and decrease downto 6dB the H field. If the second pin in mounted in opposite side the H field can be reduced downto 3 to 4 dB more because a part of the H filed is cancelled as shown in Figure 12 and reported in Figure 13.
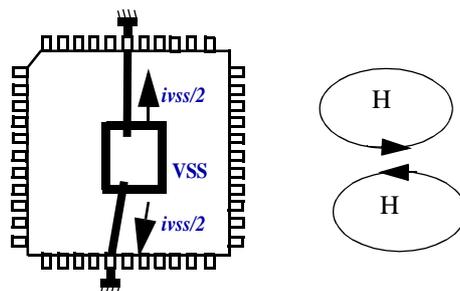

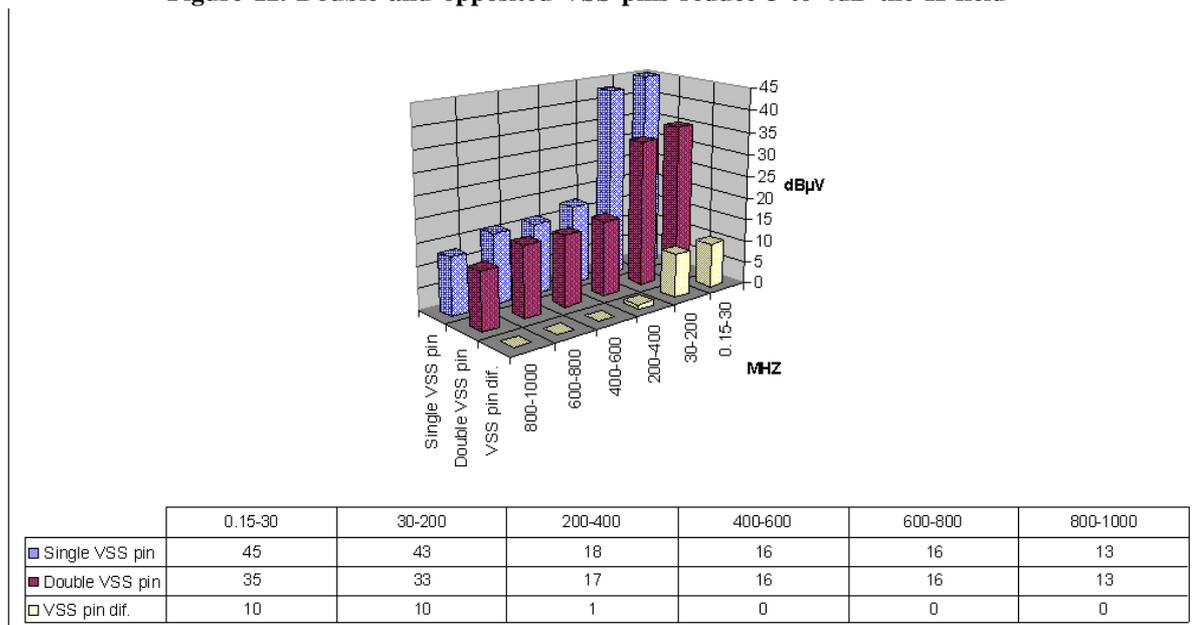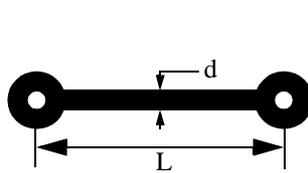**Figure 12. Double and opposited VSS pins reduce 3 to 4dB the H field**

	0.15-30	30-200	200-400	400-600	600-800	800-1000
☐ Single VSS pin	45	43	18	16	16	13
☐ Double VSS pin	35	33	17	16	16	13
☐ VSS pin dif.	10	10	1	0	0	0

Figure 13. Double and opposite VSS pins reduce downto 10dB the radiated emissions.

7. Reduce the Inductance of all Devices (PCB traces, package, capacitors, ...)

7.1. Increase the Width of the PCB Connexions

Because the real world is not ideal a power-supply connection is not a pure short-circuit but a trace with parasitic elements such as resistors and inductors.

e: PCB trace thikness in mm,

d: PCB trace width mm,

L: PCB length in m.

e=36µm for typical PCB

$$LT(\mu H) \;=\; 0,2 \times L \times \left(Ln\left(\left(\frac{2 \times L}{d+e} \right) + 0,5 + 0,22 \times \frac{d+e}{L} \right) \right)$$

$$RT(m\Omega) \;=\; 17 \times \frac{L}{d \times e}$$

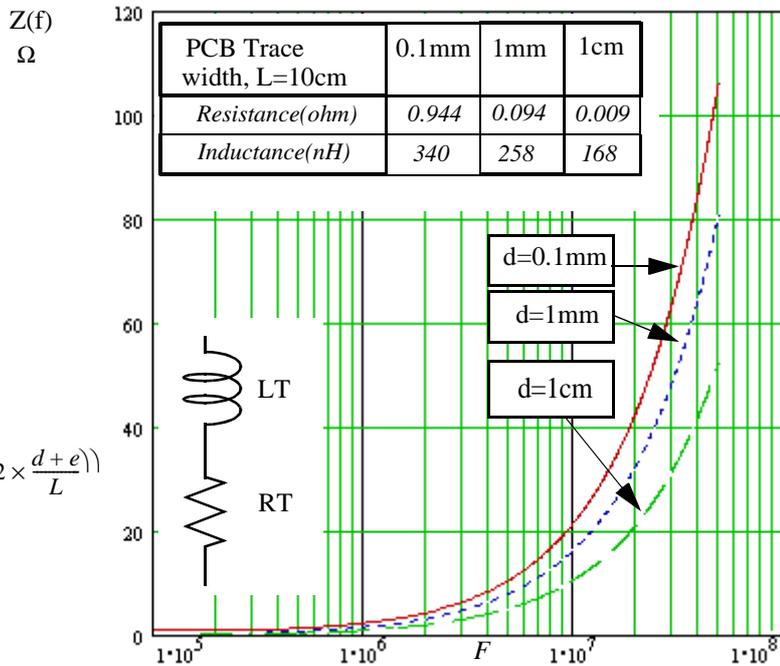| PCB Trace width, L=10cm	0.1mm	1mm	1cm
Resistance(ohm)	*0.944*	*0.094*	*0.009*
Inductance(nH)	*340*	*258*	*168*

Figure 14. PCB trace modelisation

This PCB trace is a complex impedance which varies with the frequency. Figure 14 plots the impedance versus the frequency for three different trace widths and for a length and a thickness trace assumed to be 10cm and 36µm respectively. A PCB trace introduces voltage ripples and the width of PCB traces have to be large enough not to introduce a voltage drop which could be to high. For example, when a 0.1A current at 30MHz flows a PCB trace with 10cm length and 0.1mm width, this causes a 0.62v voltage drop. If the width is 100 times the previous one the voltage drop is reduced by a factor of two.

7.2. Used Power and Ground Planes

7.2.1. Microstrip Topology

The total inductance of a loop (*LT*) is drastically reduced when using a VSS plane because the equivalent inductance of the plane (*LPlane*) is much lower than the PCB trace (*LTrace*) as it shown in Figure 15. This is mainly due to the contour taken by the H field which is much larger than the contour taken around the signal trace. These two inductances are rather independant and be evaluated separately. The ground plane inductance is not affected by the PCB trace width and can be evaluated using the following expression:

$$LPlane(\text{nH/cm}) \;=\; \frac{5 \times h}{w}$$

The PCB trace inductance can be evaluated using the following expression:

$$LTrace(\text{nH/cm}) = 10^{-9} \times \ln\left(1 + \frac{32 \times h^2}{wt^2} \times \left(1 + \sqrt{\pi \times \frac{wt}{8 \times h}}\right)\right)$$

This inductance is independant of the PCB ground width. Fors example a trace of 10cm length and 1mm width and separated from the ground plane by 1.6mm presents an inductance of 51nH. A plane with the same dimensions and 10cm width presents an inductance of 0.8nH. So the total inductance is the sum of the PCB trace and plane (51nH). The same trace without the ground plane has an inductance equal to 115nH. So thanks to the plane the trace inductance is reduced downto 2.5 factors.
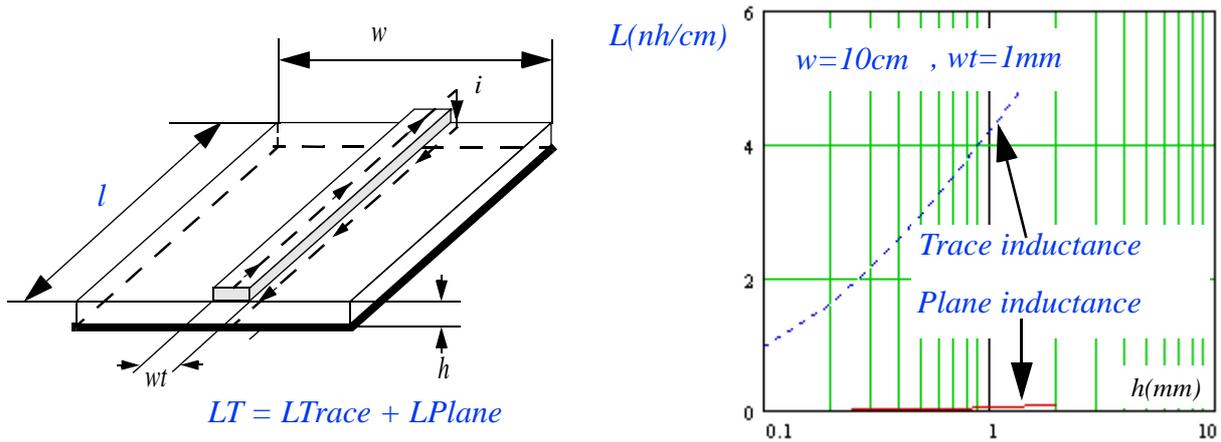

Figure 15. A VSS plane has a lower trace inductance and reduces the PCB track inductance

7.2.2. Power and Ground Planes

This is the best solution to reduce the parasitic elements because the parasitic inductance is very small due to a very large contour and a good magnetic coupling factor. It can be modelized by a LC circuit if the largest dimension between the source and the load is less than 1 tenth of the minimum wave length. Otherwise the PCB acts as a line or an antenna.
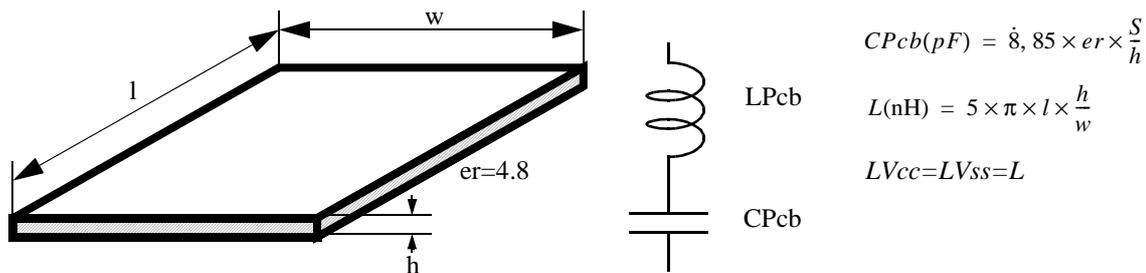

$$CPcb(pF) = 8,85 \times er \times \frac{S}{h}$$

$$L(\text{nH}) = 5 \times \pi \times l \times \frac{h}{w}$$

$$LVcc = LVss = L$$

Figure 16. A VCC and VSS planes are equivalent to a LC model

The PCB capacitor consists in two copper planes with a dielectric inserted between the two planes. The equivalent capacitor (*CPcb*) is evaluated using the formula of the Figure 16. For example a 10cm by 10cm plane with 35µm thickness and separated by 1.6mm has a total inductance of 0.05nH and a capacitor equal to 271pF. The frequency resonance of the plane is 1.4GHz. So the power-plane technics is efficient for high frequencies if the distance between the source and the load is short. These plans are not so efficient in low frequency because the equivalent capacitor is not so high and the impedance across the circuit increases and the emission levels too. In low and medium frequency ranges additionnal decoupling capacitors help to maintain this impedance low.
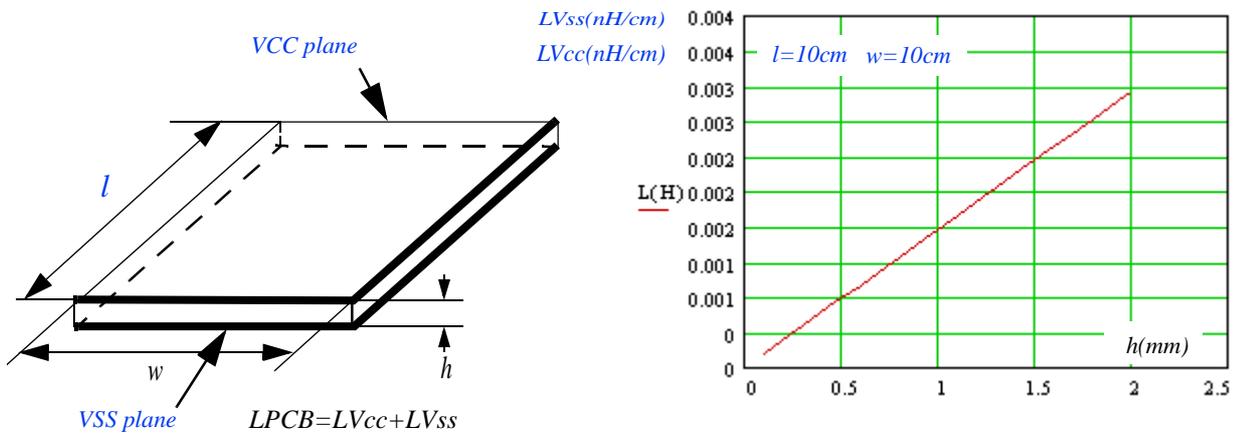
Figure 17. Power-supply planes characteristics

The next table shows the value of the PCB inductance for the three configurations sene above. The Vcc and Vss Power plane configuration is the gives the best result and a quite big decoupling capacitor

Table 1. Comparaison of the PCB inductance for w=1mm, wt=10cm,l=10cm, h=1.6mm

	Vcc PCB trace **Vss PCB trace**	**Vcc PCB trace** **Vss plane**	**Vcc Plane** **Vss Plane**
Inductance(nH)	115 + 115=230	51 + 0.8=51.8	0.025 + 0.025=0.05
Capacitance(pF)	5pF	20pF	271pF

7.3. Adapt Decoupling Capacitors to the Working Frequency

A capacitor is not a pure one and can be modelized like a RLC circuit. The surface mount devices (SMD) have the smallest internal and external inductances and have to be selected to get the best results. Figure 18 shows the equivalent electrical model and plots the frequency response for a SMD 100nF capacitor. The capacitor acts like a capacitor, a resistor or an inductor but depends on the frequency bands:

- *Medium frequency band*: 0Hz to 6MHz: the capacitor is a pure capacitor,
- *Resonance frequency*: 6-7MHz: the capacitor is a pure resistance,
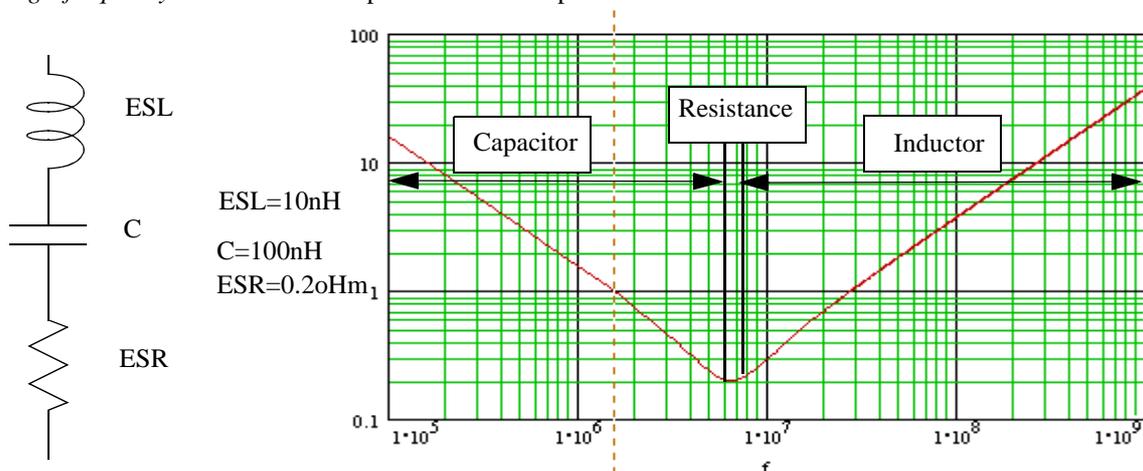- *High frequency*: > 7MHz: the capacitor acts as a pure inductance.

Figure 18. Self-Resonance frequency of true capacitor

The frequency behavior depends on the type of capacitor. Table 2 gives the electrical characteristics for different capacitors.

Table 2. Capacitor characteritics comparaison.

	1µF Tantale	100nF Ceramic	10nF Ceramic
R	0.8	0.08	0.2
L(nH)	6	3	3
Fr(MHz)	2	7.1	29

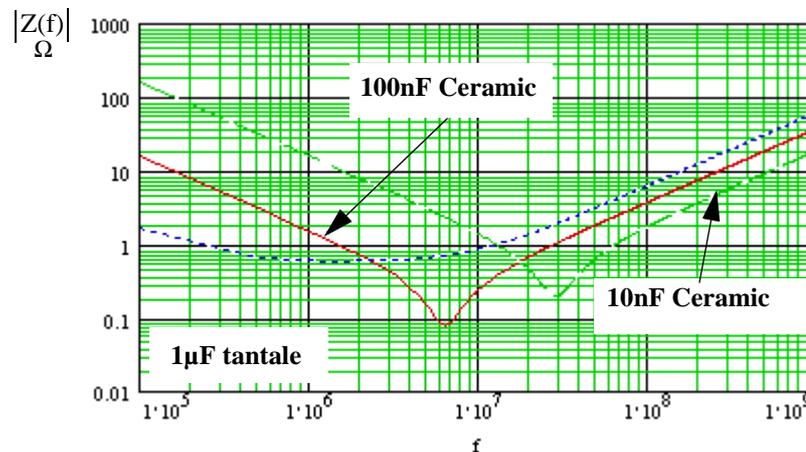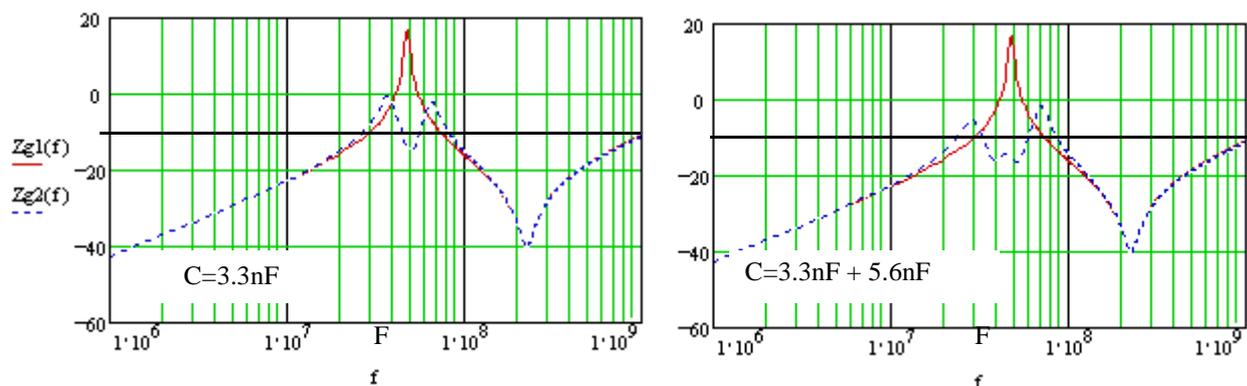Figure 19 plots the frequency response for different types of capacitor.

Figure 19. Plots versus frequency of several types of capacitor

Let's assume the frequency band of the noise is in the range 10MHz to 100MHz and to be compliant the network impedance has to be less than -10dBohms. Figure 20 plots the power network impedance versus the frequency and the impact of the decoupling capacitors on the impedance of the network. Five decoupling capacitors have to be added to be in the -10dBohms specification. Each capacitors is calculated to damp the pic of each frequency resonances.
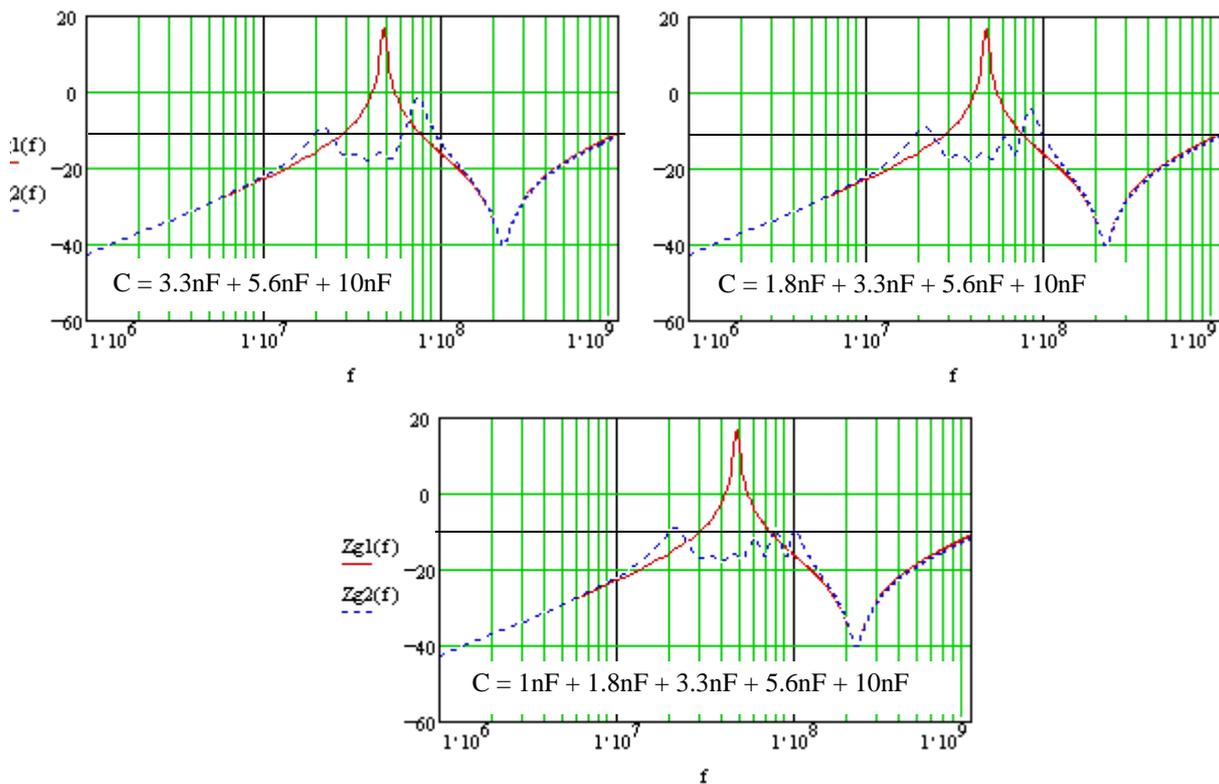
Figure 20. Decoupling effects on the network

7.4. Shorten the Capacitor Connexion Length

When the capacitor value is assumed to be constant, the resonance frequency depends on the inductance. The total inductance of the circuit consists of the intrinsinc capacitor inductance and the inductance of the connexions. Higher is the inductance, lower is the resonance frequency. It is recommended to maintain as short as possible the length of the connexions.
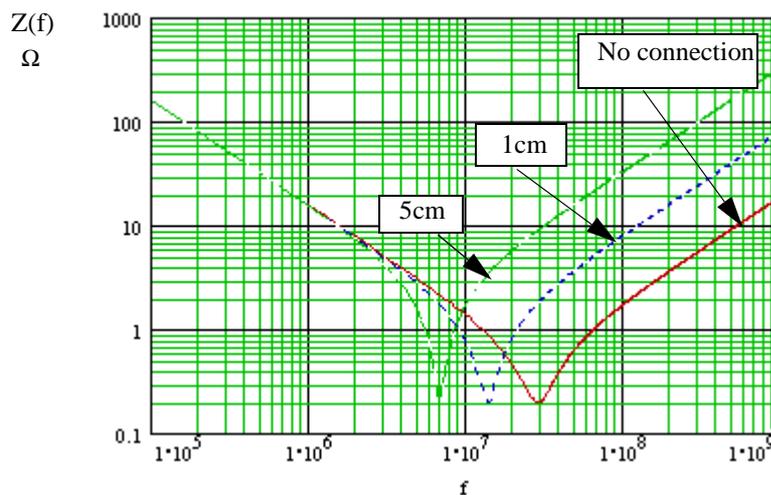

Figure 21. Connecxion increase the impedance in H.F

Figure 21 plots the capacitor impedance versus three different connection lengths. The resonance varies from 7MHz to 30MHz when the connexion length varies from 0 to 5cm.

7.5. Select the Smallest Package

The package is used to connect the die to the pins but this connexion consists of an inductance and a resistance. The die has an internal capacitance and the package in serie with the die can be modeled like a RLC circuit which has a resonance frequency. It is recommened to use the smallest package in order to reduce the Q factor. Figure 22 shows the effect on the Q factor for a DIL and PLCC package and the die without the package (COB).
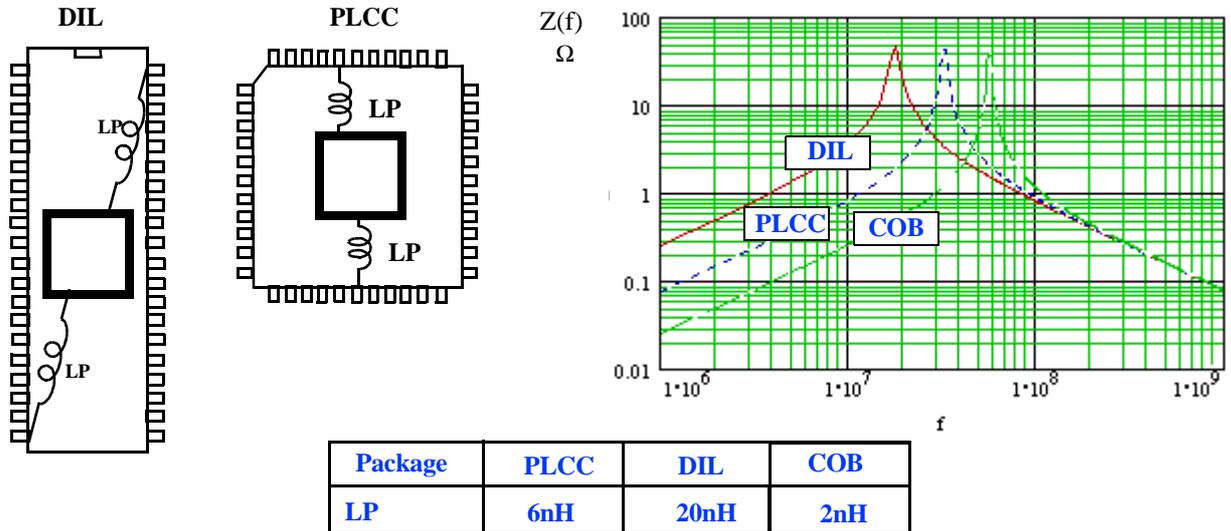

Package	PLCC	DIL	COB
LP	6nH	20nH	2nH

Figure 22. Impedance for a DIL, PLCC and a COB.

Figure 23 compares the radiated emissions between a DIL and PLCC package. Emissions can be reduced downto 7dB in the range 0.15 MHz to 400MHz using a PLCC package instead of a DIL package.
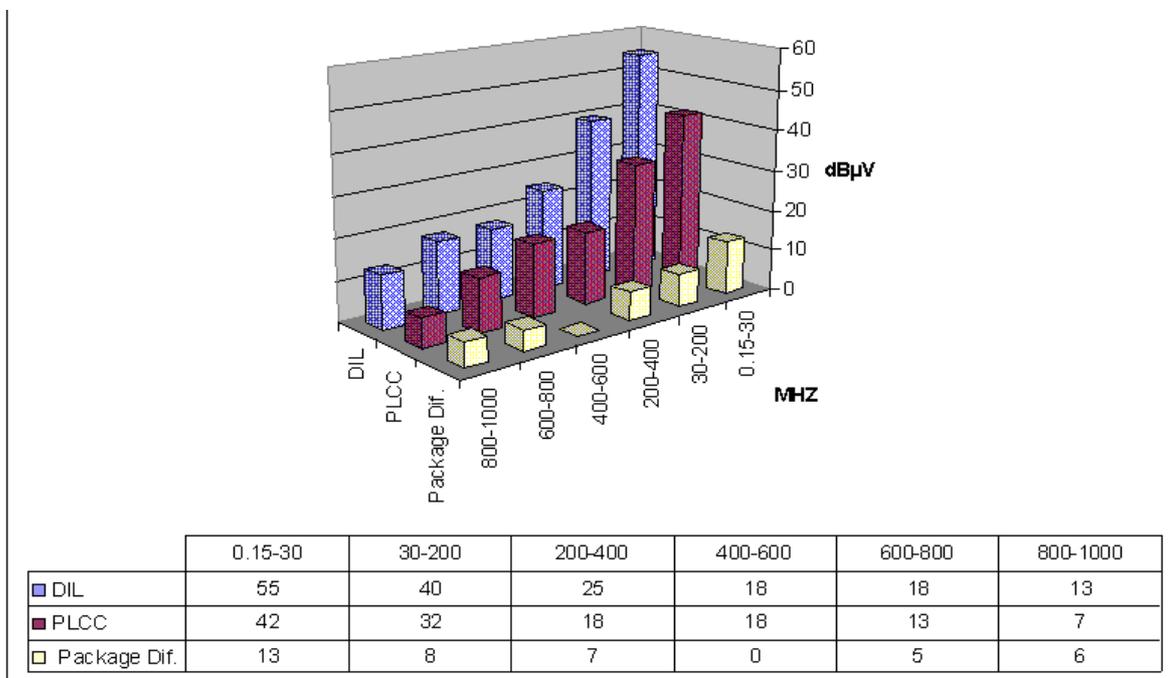

	0.15-30	30-200	200-400	400-600	600-800	800-1000
DIL	55	40	25	18	18	13
PLCC	42	32	18	18	13	7
Package Dif.	13	8	7	0	5	6

Figure 23. Package effect on the radiated emissions

8. Reduce the Equivalent Serie Resistance

8.1. Identical Capacitors in Parallel to Reduce the ESR

In the impedance of the power network is out of specification in some frequency bands, several identical capacitors can be connected in parallel to reduce the equivalent ESR. This impedance is reduced by a factor of two each time the number of capacitors is doubled (see Figure 24).
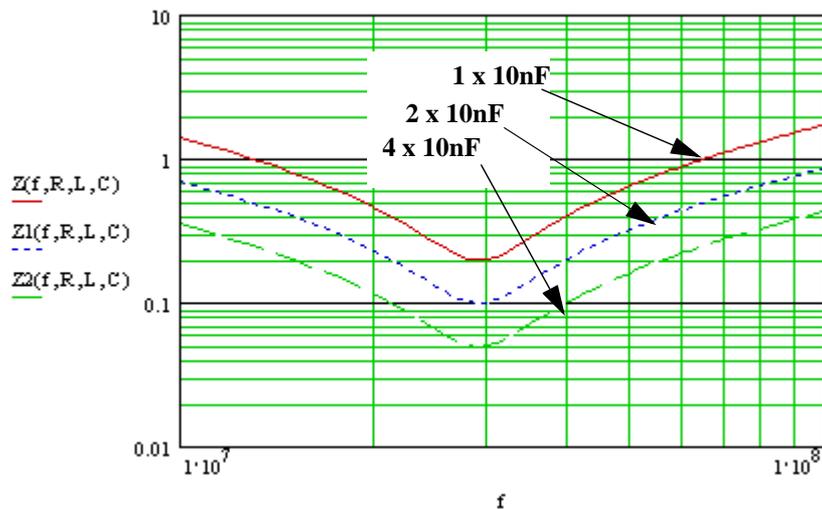
Figure 24. ESR is reduced by connected severals identicals capacitors in parallel

8.2. Choose COG, NPO and X7R dielectrique types

The capacitor taht have these dielectriques have the lowest ESR and a good stability in temperature and the value can cover from few pF to several tens of nF.

9. Conclusion

Most of the EMC improvements detailed in this application note are already known but they are not always applied. There is not the unique solution to improve the EMC of a system but most yield to a cumulative improvement. Designers must keep in mind these mechanisms to apply them early in the conception phase of a system and will be for sure the good key for EMC compliance.

10. References

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