The CEN IV Converter with Fixed Rails

XEN Audio
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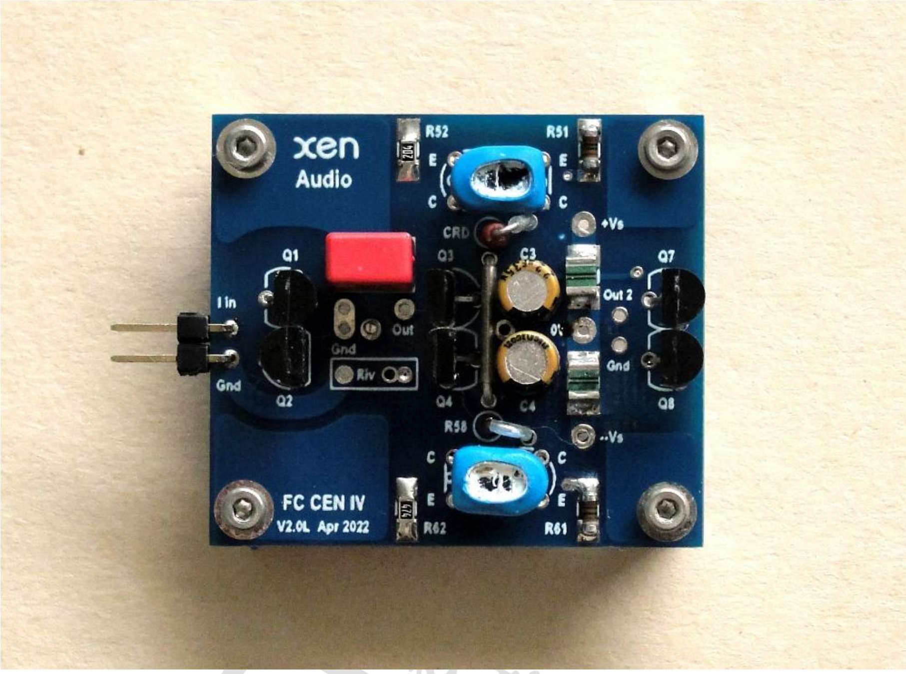


Background

A decade on, and we still have not found a better IV-Converter than our CEN / SEN IV. That is, if one can handle the issues with the floating power supply [1]. The current-mirror IV that we published lately is also a good performer when used in balanced [2], with H2 & H3 < -90dB, but with the convenience of fixed voltages. And performance is especially good in balanced mode. Many who tried both still prefer the SEN [3].

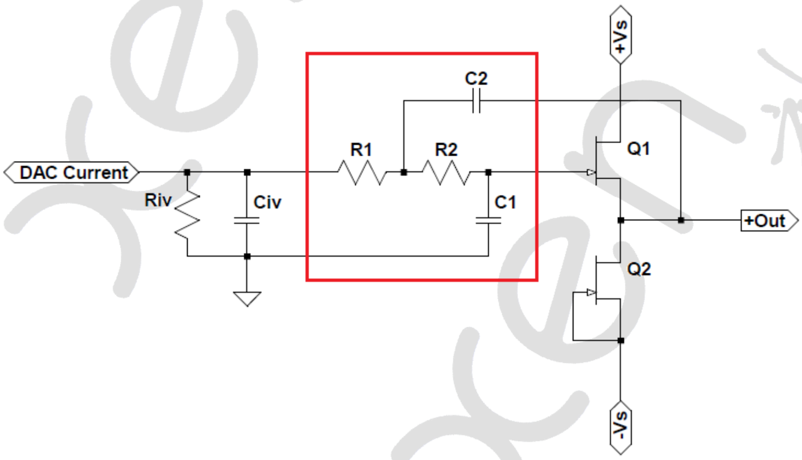
Fixed-Rail Solution

The floating power supply required for the SEN IV is sensitive to HF pickup and presents difficulties for inexperienced builders. A more practical solution with fixed rails is the folded-cascode CEN IV [4]. This differs from Nelson Pass's original ZEN IV in that it eliminates the signal coupling caps and the poor PSRR of the original circuit. It also allows a much higher gain (2.8V/mA instead of 0.5V/mA). And the folded cascode provides constant drain voltages for the input JFETs. The fixed rails also make it convenient to include an optional output buffer after the IV resistor. The key difference of this latest version, to earlier ones [5,6] published some 10 years ago, lies in the use of current sources J1,2, which is the key to low distortion as well as good PSRR. The simplified schematics has already published [4].

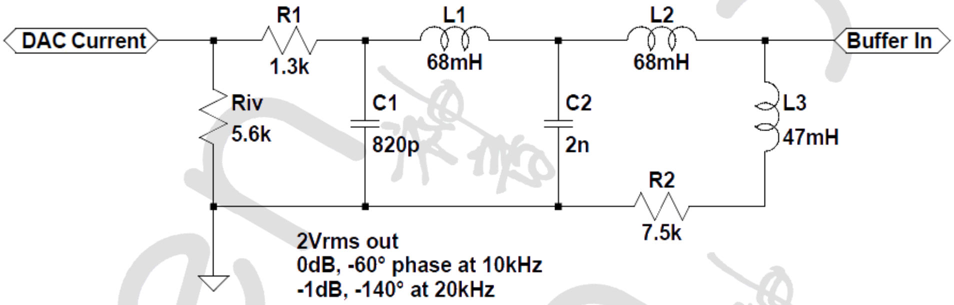
Additional Features

Third-Order Low Pass

Now that we have a JFET buffer at the output, it is only a matter of adding 4 passive components to implement an additional Sallen-Key filter, as has been done successfully with our DV20A player using the AK4495S DAC [7]. This will turn the simple first-order low-pass filter of Riv / Civ into a third order one.

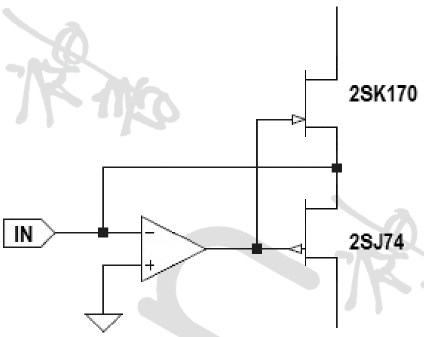


Equally, a purely passive reconstruction filter can also be placed between the Riv and the buffer input. This can be useful for NOS DACs with 44.1kHz or 48kHz sampling rates.



Input Servo

The Folded-Cascode CEN, same as the original CEN and the floating supply CEN, has an input impedance of about 15ohm, which is not perfectly linear. Some DACs work best with near-zero Zin. In such cases, one can add a FET-input opamp at the input, as proposed by Fitzfish [9]. The opamp is not in the signal-current conveying loop and this has no direct effect on the distortion of the IV circuit itself. It only acts to keep the input voltage closest to zero, i.e. it is an input servo (for both DC and AC).



Since the opamp reduces the input impedance by some 80dB at 1kHz or below, one can now consider using other JFET pairs such as 2SK246BL / 2SJ103BL with essentially the same distortion performance, but with somewhat increased noise (~2nV/√Hz at input). These JFETs, without the input servo opamp, would have way too high an input impedance (some 100 ohm) for the DAC + IV circuit to function properly.

DACs with Offset and Higher-Signal Current

Although the circuit was designed for the likes of PCM63 with up to symmetrical +/-2mA DAC current, there will certainly be desire to use this for other DACs, such as PCM1794 with +/-4mA plus 6.2mA per phase. The circuit will be able to cope the signal current with only slightly impaired performance when used with the input servo opamp. But the DC offset current needs to be sunk to the negative rail with an additional CCS. The Riv / Civ will have to be adjusted accordingly, without saying.

PCB Design

The PCB is designed as mirror-imaged left and right versions, such that the JFETs can be aligned to face each other and share a common heat spreader for thermal coupling / heat dissipation. To retain a compact signal path, only the basic circuit is included on the main PCB. Provision is made to route off the required signals to a stacker board on the rear side. This accommodates the extra components for the input servo, and either the Sallen-Key or the reconstruction filter (2 separate versions).

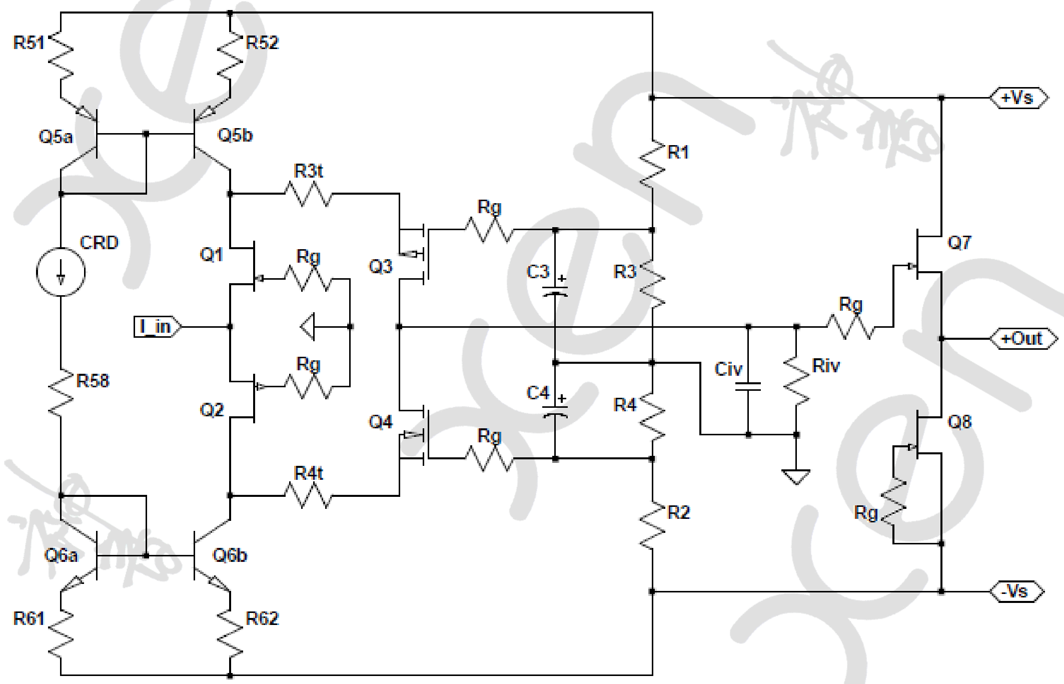
Performance

The performance in the original CEN IV (with floating supply) is guaranteed by the separate circuit loops for the bias current and the signal current, i.e. by principle. This isn't (and cannot be) the case for the folded-cascode CEN IV. The performance of the folded-cascode CEN depends solely on the current sources being as constant and identical as possible. Additional sources of distortion are the gate currents of the input- and cascode-devices. In particular, the cascode devices are more critical since the input devices are cascoded at the drain and held close to Gnd at the source. It is therefore essential to use low-capacitance FETs with reasonable Yfs for the cascode devices.

For best performance, all complementary pairs should be matched for Idss / Vgs. When perfectly matched, input DC is zero even when not using the input servo opamp. The two current sources determine the output DC offset. These are each set at ~13mA nominal; the actual value is not critical. But they have to be identical, and track each other at all times to ~ +/-1µA. This in turn results in output DC drift of ~ +/-3mV.

Same as our previous experience with the XCEN SE to BAL Converter, the main difficulty is not in the AC performance, but in keeping DC offset in check. It is anything but trivial to keep the two separate current sources stable to +/-1µA, which converts to 3mV on a 3k Riv. The only pragmatic solution is therefore to deploy the same tracking CCS circuit as in the revised XCEN 2018 [10], although the bias level now is 8x higher. With some adjustments in circuit values and good thermal coupling, this has proven to work successfully. It is possible to use the same MOSFETs in the Cascode as in the current mirrors. Using MOSFETs here has the great advantage that there is no gate current in the mirrors. But that would mean Vgs matching to well below 10mV level. So in the end, BJTs are used in the current mirrors as a pragmatic compromise.

Folded Cascode CEN IV



DIP8 Opamp Pin-Compatible

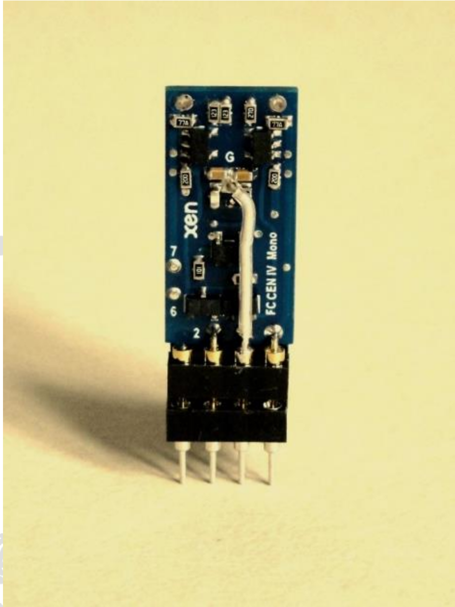
Many might already have an existing DAC using DIP8 opamps as IV converters. With the input servo option allowing the use of low-Yfs JFETs, the realisation of a DIP8-compatible version is not unimaginable using SMD components throughout. Note that it is not completely plug & play. The Riv and Civ between output and current input has to be removed.

Since this will be on a much smaller footprint than then through-hole version, dissipation will have to be reduced. Therefore, the first thing to investigate is how much reduction in bias current can be made without affecting performance.

Assuming +/-2mA DAC current as maximum, the minimum bias of the input stage would have to be at least 2.5mA to remain in rich Class A. And the current source 2x of that, i.e. 5mA. The output buffer + input servo would consume another 6mA. This would mean ~300mW dissipation per channel, which is acceptable.

This will mean using a SMD JFET input pair with Idss of ~2.5mA. The output buffer can be the likes of 2SK209GR with matched Idss to ensure low DC offset at the output. All active devices are in SOT-23 packages. Using 0603 resistors and capacitors, the entire circuit can be packages on a 11x23mm footprint for each IV circuit, including the input servo and the Sallen Key filter.

In complementary push-pull circuits, the maximum class A current is, in theory, 2x bias, or 5mA in this case. In practice, performance will suffer when it is pushed much beyond half of that. Thus, this SMD version, while very convenient, can only be used for maximum signal current of +/-2mA in practice. As long as that is the case, performance is surprisingly good, thanks to the tracking CCS's and the input servo.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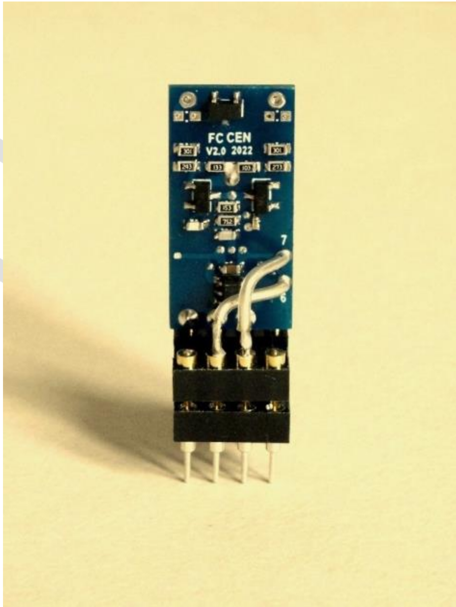
FC CEN IV Mono


FC CEN
V2.0 2022

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