Current Mirror Based IV Converter with Output Buffer

XEN Audio

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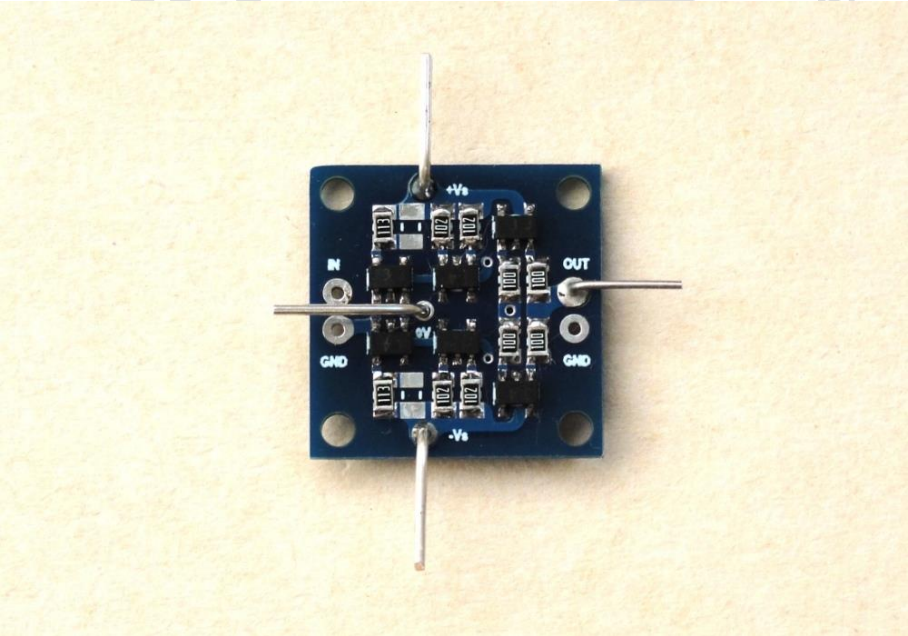


Introduction

Earlier in 2017, we discussed at the UTHAiM thread how a current conveyor amplifier can also be used as an IV converter [1].

The UTHAiM makes use of a Toshiba JFET input pair, biased at some 8mA. These JFETs are of course difficult to get. The natural question is, how can we replace the JFETs with BJTs instead. By accident, we came across the 1999 transimpedance IV circuit of Toshiyuki Beppu [2, 2a]. While this is essentially an opamp IV circuit, the input stage demonstrates a simple biasing circuit for a complementary BJT pair, utilising the principle of a current mirror. There is also a similar circuit published in 2012 by John Broskie [2b].

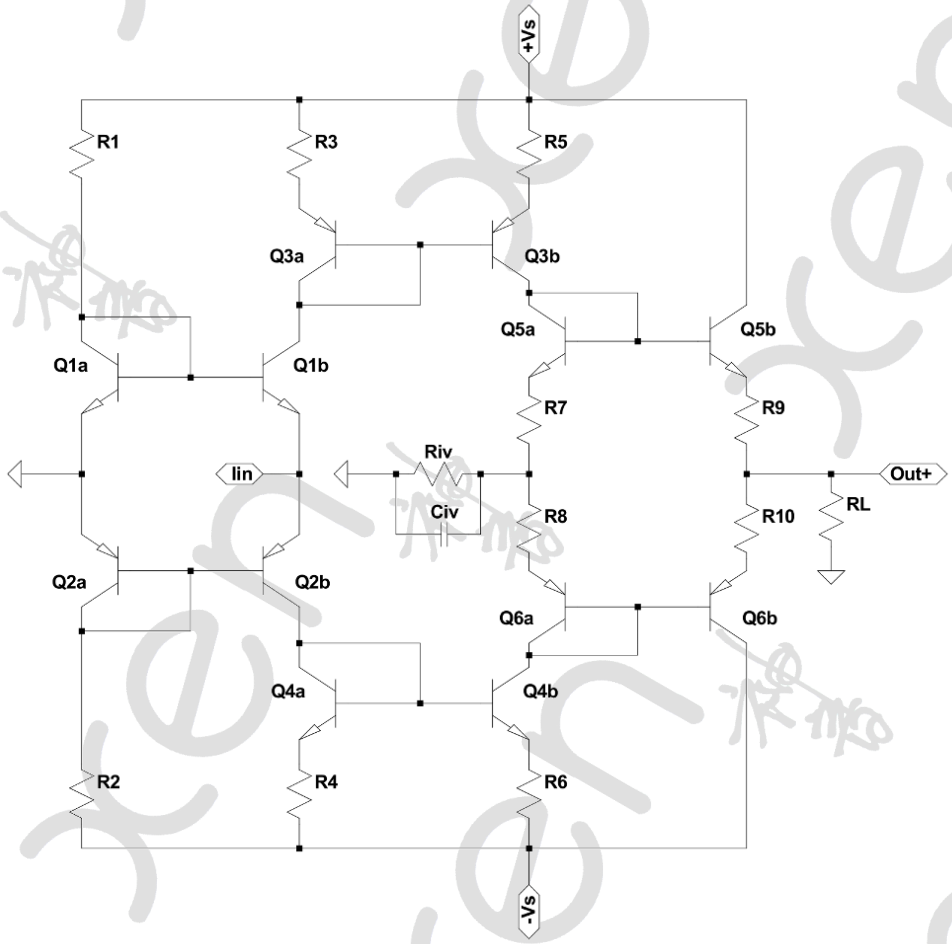
Instead of using a second current amplifying stage as per Beppu and then closing the loop with NFB, one can just use the rest of the UTHAiM for IV conversion, including the output buffer. Of course, an IV converter does not need such a powerful output buffer as in the UTHAiM. A simple Class-A BJT emitter follower is sufficient to drive a typical 10k load of the stage downstream. The entire circuit consists of no more than 3 pairs of complementary current mirrors, plus 10 resistors.

Some further search on the internet reveals very similar circuits as the above [3,4]. In fact, we also published something similar in 2011 [5]. And as Jan Didden said, you can consider it as a simplified AD844 in open loop and Class A (or 8x of them in parallel).

So why reviving it now ? At that time, JFETs were in abundance, and there were few monolithic dual BJTs with high hfe to choose from (2SC3381BL / 2SA1349BL). The situation is totally reversed today, and the idea of building a small IV module with SMD components, like the NEXEN, is rather appealing [6].

Rutgers did report relatively poor (simulated) performance, with H3 at 0.04% even at a low output level of 0.25V. Although the transistors he chose have very low capacitances, they also have very low hfe (~80). By choosing Toshiba SMD low-noise dual transistors with high hfe (~400), our simulation

returned much better performance at $2V_{rms}$ output. H2 is below 0.01%, and H3 close to 0.001%. The models used in the simulation were from Toshiba and were not well matched for hfe. In balanced mode and with well-matched devices, H2 will cancel by a factor of 5 to 10, so that the THD in differential mode should be around 0.003%. It is not quite the same performance as a SEN IV, but it does have some advantages, namely no unobtainium devices, compact size, low Zin, fixed rails, with integrated buffer, and low current consumption (~10mA per +/-1mA DAC signal current).



Circuit Description

As can be seen from the schematics, Q1, Q2 are complementary current mirrors. The bias current is set by R1, and R2, such that $I_{Q1a} = (+Vs - Vbe) / R1$

Obviously, we want to have the same bias current for Q1a and Q2a, in order that the DAC input point is at 0V. This means stable, well-regulated power supply rails that are symmetrical. And R1 / R2 can be used to fine trim the DC at input.

The (bias and signal) currents of Q1b & Q2b are mirrored by current mirrors Q3 & Q4, and the signal component is then converted to voltage with R iv. R3~R6 are essential for low distortion in the current mirrors Q3, Q4, as they have to mirror signal currents (which is not the case for Q1a & Q2a). Q5a, Q6a, R7 and R8 serve the same purpose as R21,22 in the UTHAiM circuit, namely to bias the output-stage emitter followers. In this case, by using monolithic dual devices, Q5b & Q6b will nicely track Q5a and Q6a in case of any thermal drifts. And by using identical resistor values in all of the complementary current mirrors, they all carry the same bias current determined by Q1a & Q2a. We

chose to use 2mA bias as optimum bias of the Toshiba BJTs. So total circuit consumption is about 10mA. But because of this “low” bias, one should not be passing more than +/-1mA signal current through the circuit. This works fine for all classic R2R DACs like AD1862, AD1865, PCM56, PCM1704, ….. etc. In case of higher signal current, one can simply use multiple IV modules in parallel, with the added benefit of reducing noise as well as input impedance.

The DAC input sees the effective emitter impedance of Q1b & Q2b in parallel. At 2mA bias, this works out to 6.3ohm, as verified by simulation. Output impedance is increased slightly by 0.5 x R9, which is of course not a problem when driving 10k loads.

C iv is included to suppress HF noise from the DAC. If one wish to have further LP filtering with a steeper slope, it is best to add a post filter (e.g. Sallen Key) after this IV module [7].

How about using 4-transistor Wilson current mirrors, as in the AD844 and in Ref.5 ? At least in simulation, the added complication does not bring any noticeable improvements in distortion level.

Power Supply

The simulated PSRR is not brilliant at roughly -46dB from DC to 1kHz, and starts to increase after 1kHz, reaching -33dB at 100kHz. With no DAC current output, the DAC is represented by a 1k resistor (typical R2R DAC Zout) connected to Gnd.

Q1a & Q2a are resistor biased and depends 1:1 on rail voltages, i.e. no PSRR at all. This is somewhat attenuated in Q1b & Q2b, as the rail-noise-voltage-induced current has nowhere else to go and has to be equalised between Q1b & Q2b by slight deviations in voltage at the input node. However, difference in hfe and capacitances of the NPNs and the PNPs results in slight differences in current between R3, R4 as well as R5, R6. And these differences reflect into unwanted voltage output at R iv.

If R1, R2 are replaced by perfect 2mA current sources, PSRR will improve by about 8dB at DC, but more or less unchanged at HF. The simplest solution is still a low-noise power supply up to 100kHz or higher. Here, the excellent LT3045 / LT3094 should be a good choice, and can be used to supply both IVs of a balanced output channel.

Constant Current Sink

Many modern-day audio DACs, such as the likes of ES9018 or PCM1794, use single-ended power supplies. That means that they cannot output negative current, and hence will need an offset DC current. This DC current does not carry signal, and should therefore not go through the IV converter. Instead a constant-current sink will drain this to the negative rail of the IV power supply.

For this purpose, we need to use a CCS which is stable, low noise, and has a low voltage headroom. Some people propose the MMBF4391, but this is still rather noisy at 3nV/sqrtHz. We like the 2SK209 instead for its lower noise (1.3nV/sqrtHz), and if the BL grade is used with a source resistor of 1k, you will get an Id of about 0.5mA with very low Vsat.

But 2SK209BL is difficult to get, so the dual version of 2SK2145BL is chosen, with both FETs in parallel and degenerated by a common 510R resistor. 4 of them should sink a total of 4mA constant current, but this can be increased easily by lowering the 510R resistors, if necessary. With 8 JFETs in parallel, the JFET noise contribution is reduced to 0.5nV/sqrtHz. The source resistor noise is still 1.3nV/sqrtHz. Using 2SK2145GR and reduced source resistor values will reduce this, at the expense of current stability.

PCB design

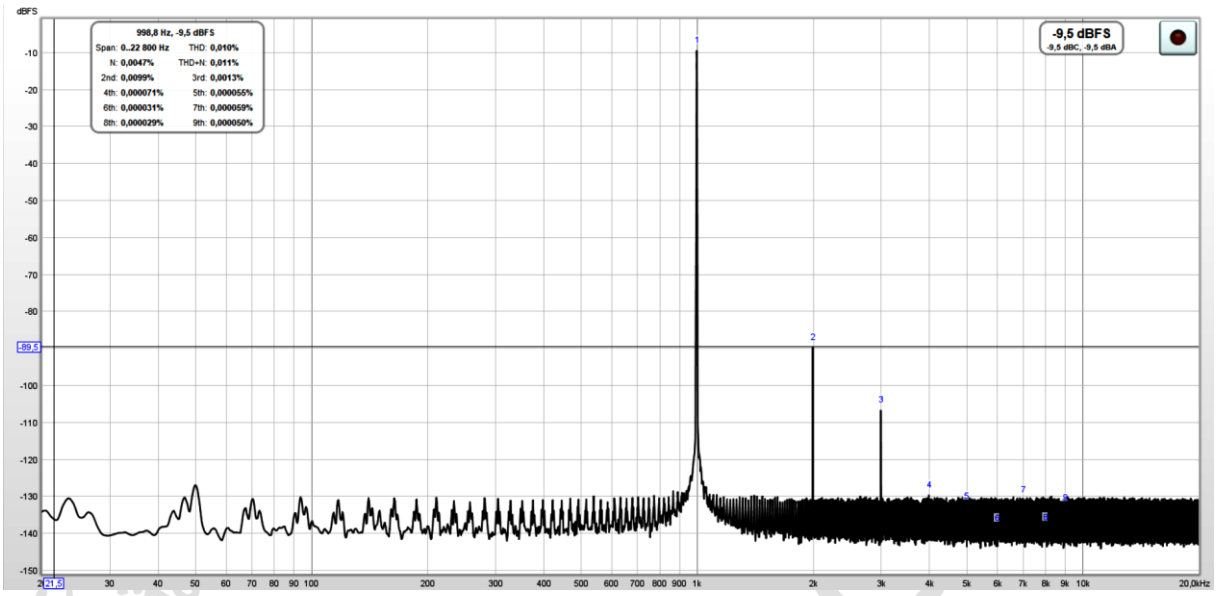
With 6x SOT23 current mirrors and 10x 0805 thin film resistors, the circuit will easily fit into a footprint of 20x20mm. In fact, mounting screws and solder pads for external wiring takes up as much space as the circuit itself. Extra trimming resistor pads are provided for R1, R2 (for trimming input DC) as well as for R5, R6 (for trimming output DC). The rail voltage needs to be known upfront before trimming can take place. With +/-12V rails, nominal value for R1, R2 is 5.6k.

Larger pads are provided for R_{iv} and C_{iv}, so that 1206 thin film resistors and PPS capacitors can be used in those positions.

Matching PCBs were also designed with same pin configurations for LT3045 / 3094 regulators, as well as for the DC constant current sink. These can then be stacked together, separated by 2mm thermal silicon pads and 1mm aluminium heat spreaders, to form an IV module for one differential channel.

Measurement

A prototype was build quickly to verify performance. The dual devices are well matched for hfe within one device. But NPN to PNP match can only be about 15% for the particular batch obtained from Mouser. Nevertheless, the performance is almost exactly as predicted by Spice. H2 is at 0.01%, H3 at 0.013%. And without Civ, bandwidth is about -1dB at 2MHz.



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