AX5689

Digital Audio Converter and Amplifier Controller

Features

- General features:
  - 4-channel BTL digital Class-D amplifier controller with digital inputs
  - 8 differential low-latency ADCs with a 115 dB dynamic range
  - 8 programmable digital loop-filter slices
  - 8 CMOS level PWM outputs, configurable as 4 BTL channels
  - Feedback loop possible after the output filter, across the loudspeaker nodes
  - Configurable interconnections between slices and ADCs for versatility and MIMO control
  - Volume control and soft mute
  - Dynamic loop control with programmable ramp enabling pop-free mode transitions
- Serial audio input / output
  - I2S / TDM Serial Audio Interface with 16 downstream and 8 upstream channels
  - Input sample rate: 32 to 768 kHz
  - 16 to 32-bit supported audio formats
- Control interface
  - SPI
  - fast mode I^2C control interface with selectable address for multi-chip systems

Applications

- Streaming audio amplifier solutions
- TV Sound-bars, audio entertainment solutions
- Active loudspeakers
- High performance DAC solutions
- High-resolution low-latency ADC solutions

General description

The AX5689 is a 4-channel BTL audio amplifier controller IC with digital inputs and CMOS level PWM outputs. It enables high order digital control loops, with feedback after Class-D output filters.

Embedded low-latency ADCs are used to close the loop behind the output filter in the digital domain. The digital control loop has a high loop gain for all audio frequencies. The AX5689 suppresses all errors caused by the power supply, power stage and output filter within the audio band (20 Hz - 20 kHz). The AX5689 reaches superb performance levels while enabling cost down options.

The low-latency ADCs, PWM outputs and programmable interconnects allow custom configurations, like analog audio inputs / analog line outputs, power supply control, current sensing, temperature sensing, etc.

The AX5689 is compatible with power stages from various vendors and can read and respond to power stage diagnostic signals. The maximum output power is dependent on the user application and is scalable with the number of channels, selected power stages, loads and supply.

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1 Block diagram

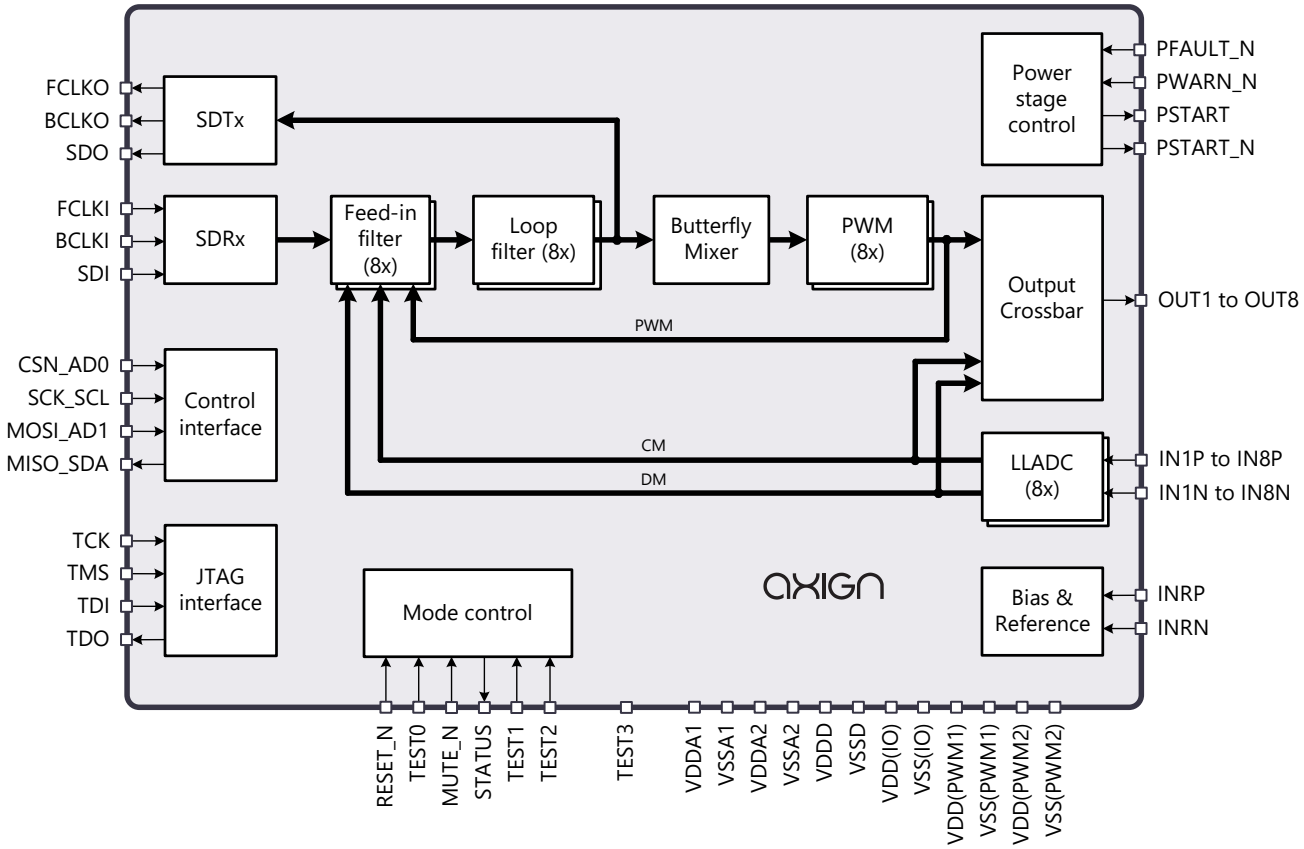


Figure 1. Block diagram AX5689

2 Pinning information

2.1 Pinning

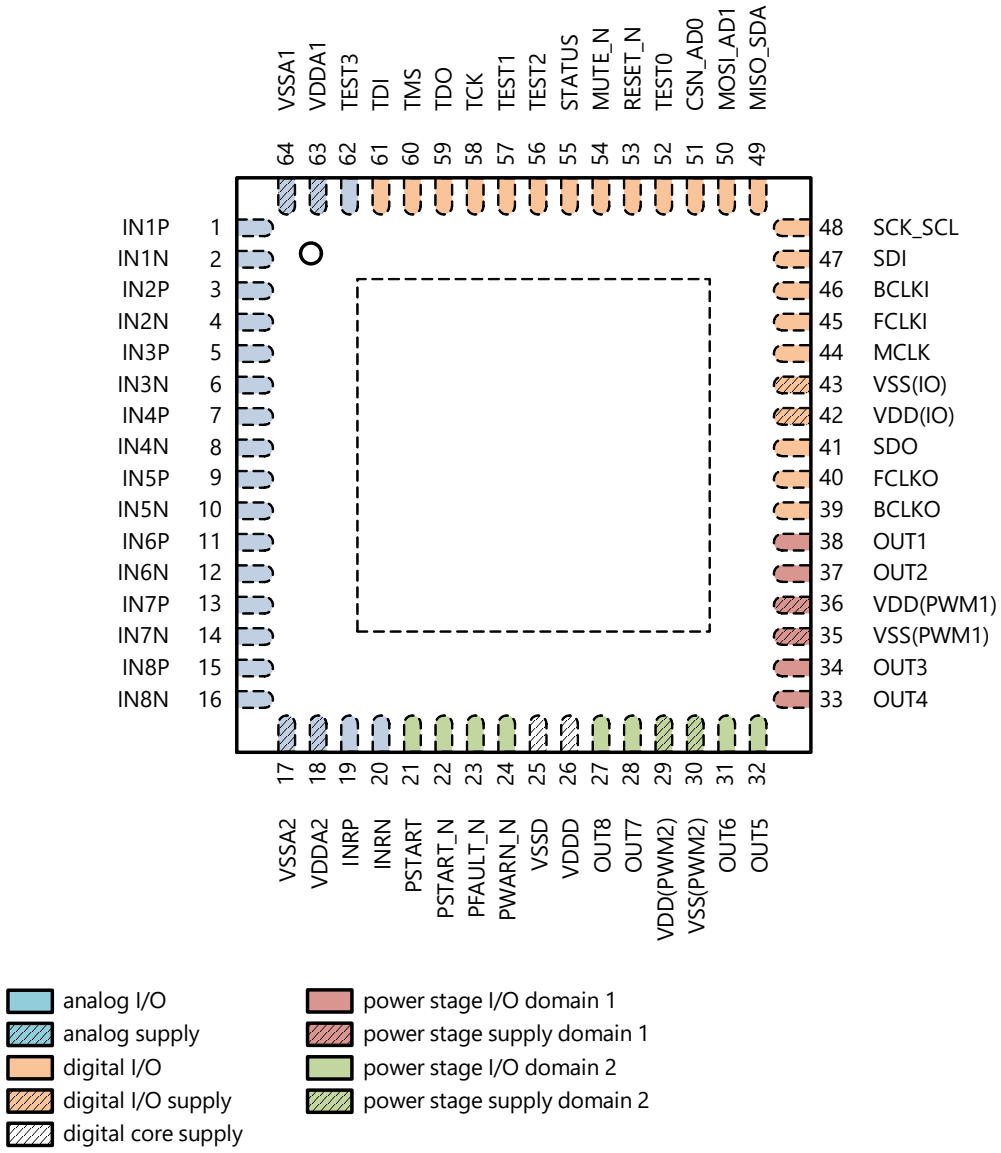


Figure 2. AX5689 top view

2.2 Pin description

Table 1. Pin description

Pin	Symbol	Type[1]	Description
1	IN1P	AI	analog input for ADC1, terminal P
2	IN1N	AI	analog input for ADC1, terminal N
3	IN2P	AI	analog input for ADC2, terminal P
4	IN2N	AI	analog input for ADC2, terminal N
5	IN3P	AI	analog input for ADC3, terminal P
6	IN3N	AI	analog input for ADC3, terminal N
7	IN4P	AI	analog input for ADC4, terminal P
8	IN4N	AI	analog input for ADC4, terminal N
9	IN5P	AI	analog input for ADC5, terminal P
10	IN5N	AI	analog input for ADC5, terminal N
11	IN6P	AI	analog input for ADC6, terminal P
12	IN6N	AI	analog input for ADC6, terminal N
13	IN7P	AI	analog input for ADC7, terminal P
14	IN7N	AI	analog input for ADC7, terminal N
15	IN8P	AI	analog input for ADC8, terminal P
16	IN8N	AI	analog input for ADC8, terminal N
17	VSSA2	P	analog ground
18	VDDA2	P	1.2 V analog supply
19	INRP	AI	input for reference ADC, terminal P
20	INRN	AI	input for reference ADC, terminal N
21	PSTART	DO	start-up power stage, active high(2)
22	PSTART_N	DIO	start-up power stage, active low(2)
23	PFAULT_N	DI	output stage fault detection, active low
24	PWARN_N	DI	output stage warning detection, active low
25	VSSD	P	digital ground
26	VDDD	P	1.2 V digital supply
27	OUT8	DO	data (PWM) for channel 8
28	OUT7	DO	data (PWM) for channel 7
29	VDD(PWM2)	P	3.3 V supply for PWM outputs
30	VSS(PWM2)	P	ground for PWM outputs
31	OUT6	DO	data (PWM) for channel 6
32	OUT5	DO	data (PWM) for channel 5
33	OUT4	DO	data (PWM) for channel 4
34	OUT3	DO	data (PWM) for channel 3
35	VSS(PWM1)	P	ground for PWM outputs
36	VDD(PWM1)	P	3.3 V supply for PWM outputs

Table 1. Pin description

Pin	Symbol	Type[1]	Description
37	OUT2	DO	data (PWM) for channel 2
38	OUT1	DO	data (PWM) for channel 1
39	BCLKO	DO	bit clock for the serial audio data output
40	FCLKO	DO	frame clock for the serial audio data output
41	SDO	DO	serial audio data output
42	VDD(IO)	P	3.3 V IO supply
43	VSS(IO)	P	IO ground
44	MCLK	DI	master clock input
45	FCLKI	DI	frame clock for the serial audio data input
46	BCLKI	DI	bit clock for the serial audio data
47	SDI	DI	serial audio data input
48	SCK_SCL	DI	control interface bit clock.
49	MISO_SDA	DO/DIO	control interface: data output in SPI mode, bidirectional data line in I^2C mode
50	MOSI_AD1	DI	control interface: data input in SPI mode, AD1 address select input in I^2C mode
51	CSN_AD0	DI	control interface: chip select in SPI mode, AD0 address select in I^2C mode
52	TEST0	DI	reserved for testing; connect to ground
53	RESET_N	DI	global reset input, active low
54	MUTE_N	DI	mute: soft mutes when low, unmutes when high
55	STATUS	DO	status output (invalid data/settings, power stage fault, etc.)
56	TEST2	DI	reserved for testing; connect to ground
57	TEST1	DI	reserved for testing; connect to ground
58	TCK	DI	JTAG interface clock
59	TDO	DO	JTAG data output
60	TMS	DI	JTAG test mode select
61	TDI	DI	JTAG data input
62	TEST3	AIO	reserved for testing; leave floating
63	VDDA1	P	1.2 V analog supply
64	VSSA1	P	analog ground
65	EPAD	P	exposed pad; connect to ground

[1] Type description: P = Power, A = Analog, D = Digital, I = Input, O = Output

3 Absolute maximum ratings

Table 2. Absolute maximum ratings[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(IO)}$	I/O supply voltage	pin VDD(IO); relative to $V_{SS(IO)}$[2]	-0.3	3.63	V
$V_{DD(PWM)}$	PWM supply voltage	pins VDD(PWM1), VDD(PWM2); relative to $V_{SS(PWM)}$[2]	-0.3	3.63	V
V_{DDD}	digital supply voltage	pin VDDD; relative to V_{SSD}[2]	-0.3	1.32	V
V_{DDA}	analog supply voltage	pins VDDA1, VDDA2 relative to V_{SSA}[2]	-0.3	1.32	V
V_{in}	input voltage	relative to V_{SSA}			
		pins IN1P to IN8P; pins IN1N to IN8N; pin INRP, pin INRN, pin VREF	-0.3	V_{DDA}+0.3	V
		relative to $V_{SS(IO)}$			
		all other pins	-0.3	$V_{DD(IO)}$+0.3	V
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model [3]	-2000	+2000	V
		charged device model [4]	-500	+500	V

[1] Absolute maximum ratings are stress ratings only. Permanent damage to the devices may be caused by continuously operating at or beyond these limits. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied.

[2] The voltage potential of the power supply grounds V_{SSA}, V_{SSD}, $V_{SS(IO)}$, $V_{SS(PWM1)}$, $V_{SS(PMW2)}$ (pins VSSA, VSSD, VSS(IO), VSS(PWM1), VSS(PWM2)) must be within ±0.3 V of each other.

[3] According to JEDEC JS-001 specification.

[4] According to JESD22-C101 specification.

4 Recommended operating conditions

Table 3. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(IO)}$	IO supply voltage	pin VDD(IO); with respect to $V_{SS(IO)}$	3.0	3.3	3.6	V
$V_{DD(PWM)}$	PWM out supply range	pins VDD(PWM1), VDD(PWM2); with respect to $V_{SS(PWM)}$	3.0	3.3	3.6	V
V_{DDD}	digital supply voltage	pin VDDD; with respect to V_{SSD}	1.1	1.2	1.3	V
V_{DDA}	analog supply voltage	pins VDDA1, VDDA2; with respect to V_{SSA}	1.1	1.2	1.3	V
f_{MCLK}	MCLK clock frequency		45.1584	-	49.152	MHz

5 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
Θ_{JA}	Junction to ambient thermal resistance	still air	23	°C/W
Θ_{JC}	Junction to case thermal resistance		1.6	°C/W

6 Characteristics

Table 5. Characteristics

Operating conditions: V_{DDD} = V_{DDA1} = V_{DDA2} = 1.2 V; $V_{DD(IO)}$ = $V_{DD(PWM1)}$ = $V_{DD(PWM1)}$ = 3.3 V; T_a = +25 ˚C; f_{sig} = 1 kHz; f_s = 48 kHz; MCLK = 49.152 MHz; 32-bits audio data; unless stated otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power						
$I_{DD(IO)}$	I/O supply current	operating; all channels enabled	-	4.4	-	mA
		power down; reset active and MCLK disabled	-	5.8	12	µA
$I_{DD(PWM)}$	PWM supply current	operating; all channels enabled	-	2.8	-	mA
		power down; reset active and MCLK disabled	-	15.8	16	µA
I_{DDD}	digital supply current	operating; all channels enabled	-	7.3	-	mA
		power down; reset active and MCLK disabled	-	8.2	9	µA
I_{DDA}	analog supply current	operating; all channels enabled	-	71	-	mA
		power down; reset active and MCLK disabled	-	38	300	µA
Low latency ADCs						
$I_{i(dm)fs}$	full-scale differential mode input current		-	4.81	-	mA
$I_{i(cm)fs}$	full-scale common mode input current		-	9.28	-	mA
$I_{os(dm)}$	differential mode input equivalent offset current		-	0.45	-	µA
$V_{i(cm)}$	common mode input voltage		-	0.52	-	V
$Z_{i(dm)}$	differential mode input impedance	ADC enabled	-	2.6	-	Ω
		ADC disabled	-	120	-	kΩ
$Z_{i(cm)}$	common mode input impedance	ADC enabled	-	1.05	-	Ω
		ADC disabled	-	120	-	kΩ
BW_{fs}	full scale bandwidth		-	60	-	kHz
DR_{dm}	differential mode dynamic range	20 Hz to 20 kHz; -60 dB input	108	111	-	dB
		A-weighted; -60 dB input	110	113	-	dB
DR_{cm}	common mode dynamic range	20 Hz to 20 kHz	80	82	-	dB
		A-weighted	82	84	-	dB
SNR	signal to noise ratio	20 Hz to 20 kHz; -1 dBFS output	105	111	-	dB

Table 5. Characteristics

Operating conditions: V_{DDD} = V_{DDA1} = V_{DDA2} = 1.2 V; $V_{DD(IO)}$ = $V_{DD(PWM1)}$ = $V_{DD(PWM1)}$ = 3.3 V; T_a = +25 °C; f_{sig} = 1 kHz; f_s = 48 kHz; MCLK = 49.152 MHz; 32-bits audio data; unless stated otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		A-weighted; -1 dBFS output	107	113	-	dB
THD+N	total harmonic distortion plus noise	20 Hz to 20 kHz; -1 dBFS output	-90	-100	-	dB
CM2DM	input equivalent common-mode to differential-mode conversion		-90	-	-	dB
PSR	power supply rejection	measured with respect to differential mode output; ADC input is open; test signal on V_{DDA} = 217 Hz, square wave and broadband noise; V_r = 66 mV_{P-P}	-100	-	-	dBFS
α_{ct}	crosstalk	between ADC channels; 20 Hz to 20 kHz	-120	-	-	dB
ΔG_{dm}	differential mode gain mismatch	between devices	-0.23	-	+0.23	dB
		between channels	-0.08	-	+0.08	dB
ΔG_{cm}	common mode gain mismatch	between devices	-0.25	-	+0.25	dB
		between channels	-0.1	-	+0.1	dB
SR	slew rate	differential mode	-	2.2	-	mA/µs
		common mode	-	14	-	mA/µs
Digital input/output						
V_{IL}	LOW-level input voltage		0	-	0.3 × $V_{DD(IO)}$	V
V_{IH}	High-level input voltage		0.7 × $V_{DD(IO)}$	-	$V_{DD(IO)}$	V
$I_{L(I)}$	input leakage current	V_I = 3.3 V or 0 V	-1	-	1	µA
$I_{L(O)}$	output leakage current	tristate output; V_O = 3.3 V or 0 V	-	-	±10	µA
C_i	input capacitance		-	-	2.5	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pins FCLKO, BCLKO, SDO, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8	13.9	-	-	mA
		V_{OL} = 0.4 V; all other digital output pins	7.0	-	-	mA
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(IO)}$ - 0.4 V; pins FCLKO, BCLKO, SDO, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8	9.8	-	-	mA

Table 5. Characteristics

Operating conditions: V_{DDD} = V_{DDA1} = V_{DDA2} = 1.2 V; $V_{DD(IO)}$ = $V_{DD(PWM1)}$ = $V_{DD(PWM1)}$ = 3.3 V; T_a = +25 ˚C; f_{sig} = 1 kHz; f_s = 48 kHz; MCLK = 49.152 MHz; 32-bits audio data; unless stated otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{OH} = $V_{DD(IO)}$ - 0.4 V; all other digital output pins	4.8	-	-	mA
$R_{pd(int)}$	internal pull-down resistor	pin TEST0, RESET_N, MUTE_N, TEST1, TEST2, TCK, TMS, TDI	36	52	85	kΩ
$R_{pu(int)}$	internal pull-up resistor	pin PFAULT_N, PWARN_N	36	54	85	kΩ

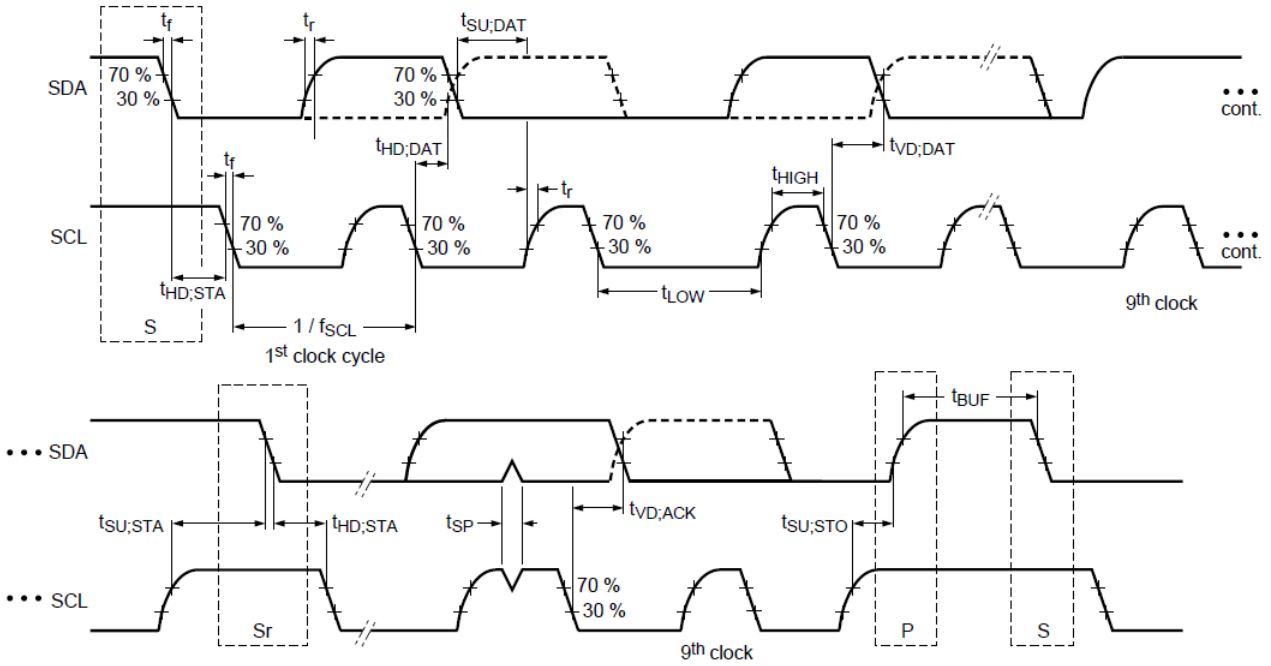
6.1 Control interface

6.1.1 I2C interface – slave

Table 6. I2C-bus characteristics

3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; T_a = -40 °C to +85 °C; simulated values

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{scl}	SCL clock frequency		0	-	400	kHz
$t_{HD(STA)}$	hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
$t_{SU(STA)}$	set-up time for a repeated START condition		0.6	-	-	µs
$t_{HD(DAT)}$	data hold time		0	-	-	µs
$t_{SU(DAT)}$	data set-up time		100	-	-	ns
t_r	rise time of both SDA and SCL signals		-	-	300	ns
t_f	fall time of both SDA and SCL signals		-	-	300	ns
$t_{SU(STO)}$	set-up time for STOP condition		0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{VD(DAT)}$	data valid time		-	-	0.9	µs
$t_{VD(ACK)}$	data valid acknowledge time		-	-	0.9	µs



The input levels of the I2C-bus receiver are with respect to $V_{DD(IO)}$ and not related to the bus voltage, as required by the I2C-bus specification. If the $V_{DD(IO)}$ supply of the device is switched off, SDA and SCL pins connected to the I2C-bus are set to a floating condition and do not disturb the I2C-bus lines.

Figure 3. I2C timing characteristics

6.1.2 SPI Interface – slave

Table 7. SPI characteristics

3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; T_a = -40 °C to +85 °C; simulated values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		-	-	10	MHz
t_{WL}	pulse width LOW	pin SCK	0.25 / f_{SCK}	-	-	ns
t_{WH}	pulse width HIGH	pin SCK	0.25 / f_{SCK}	-	-	ns
t_r	rise time	pins SCK, MOSI	-	-	0.17 / f_{SCK}	ns
t_f	fall time	pins SCK, MOSI	-	-	0.17 / f_{SCK}	ns
$t_{su(CSN)}$	CSN setup time		120	-	-	ns
$t_{h(CSN)}$	CSN hold time		120	-	-	ns
$t_{WH(CSN)}$	CSN pulse width HIGH		15	-	-	µs
$t_{su(MOSI)}$	MOSI setup time		30	-	-	ns
$t_{h(MOSI)}$	MOSI hold time		30	-	-	ns
$t_{d(o)}$	output delay time	pin MISO	-	-	100	ns
t_{PHZ}	HIGH to OFF state propagation delay	pin MISO	-	-	100	ns

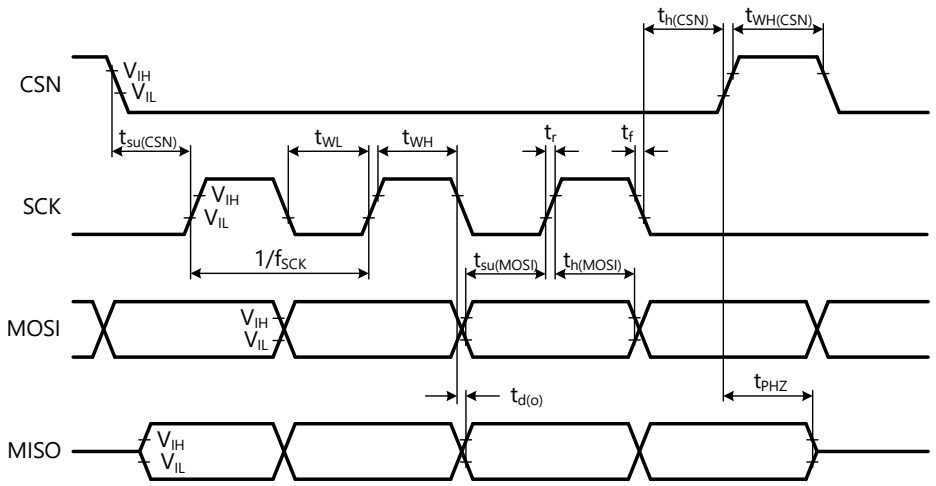


Figure 4. SPI timing characteristics

6.2 Serial data receiver

Table 8. Serial data receiver characteristics

3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; T_a = -40 °C to +85 °C; simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{FCLK}	frame clock frequency	pin FCLKI	32	-	768	kHz
f_{BCLK}	bit clock frequency	pin BCLKI	32 × f_{FCLK}	-	49.152	MHz
t_{WH}	pulse width HIGH	pin BCLKI	0.25 / f_{BCLK}	-	-	ns
t_{WL}	pulse width LOW	pin BCLKI	0.25 / f_{BCLK}	-	-	ns
t_r	rise time	pins BCLKI, FCLKI, SDI	-	-	0.17 / f_{BCLK}	ns
t_f	fall time	pins BCLKI, FCLKI, SDI	-	-	0.17 / f_{BCLK}	ns
$t_{su(FCLK)}$	frame clock input set-up time	pin FCLKI	4	-	-	ns
$t_{h(FCLK)}$	frame clock input hold time	pin FCLKI	4	-	-	ns
$t_{su(SDI)}$	serial data input set-up time	pin SDI	4	-	-	ns
$t_{h(SDI)}$	serial data input hold time	pin SDI	4	-	-	ns

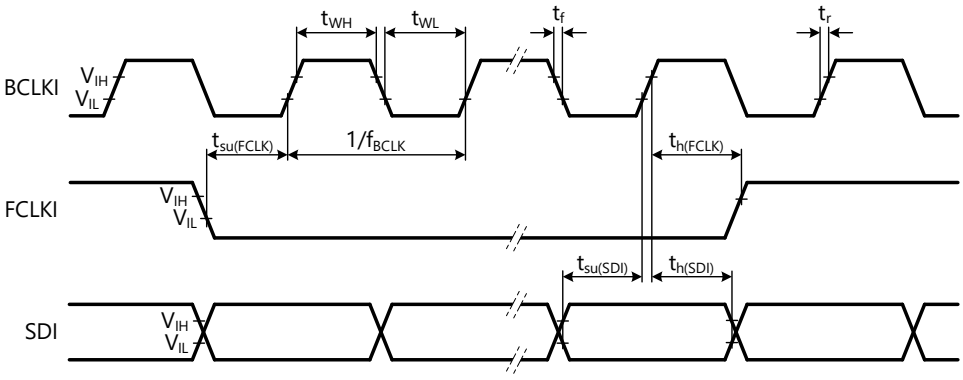


Figure 5. Serial data receiver timing characteristics

6.3 Serial data transmitter

Table 9. Serial data transmitter characteristics

3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; T_a = -40 °C to +85 °C; simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{FCLK}	frame clock frequency	pin FCLKO	32	-	768	kHz
f_{BCLK}	bit clock frequency	pin BCLKO	32 × f_{FCLK}	-	49.152	MHz
t_{WH}	pulse width HIGH	pin BCLKO; C_L = 10 pF	0.35 / f_{BCLK}	-	-	ns
t_{WL}	pulse width LOW	pin BCLKO; C_L = 10 pF	0.35 / f_{BCLK}	-	-	ns
t_r	rise time	pins BCLKO, FCLKO, SDO; C_L = 10 pF	-	-	2	ns
t_f	fall time	pins BCLKO, FCLKO, SDO; C_L = 10 pF	-	-	2	ns
t_{PF}	frame clock output propagation delay		-	-	5	ns
t_{PS}	serial data output propagation delay		-	-	5	ns

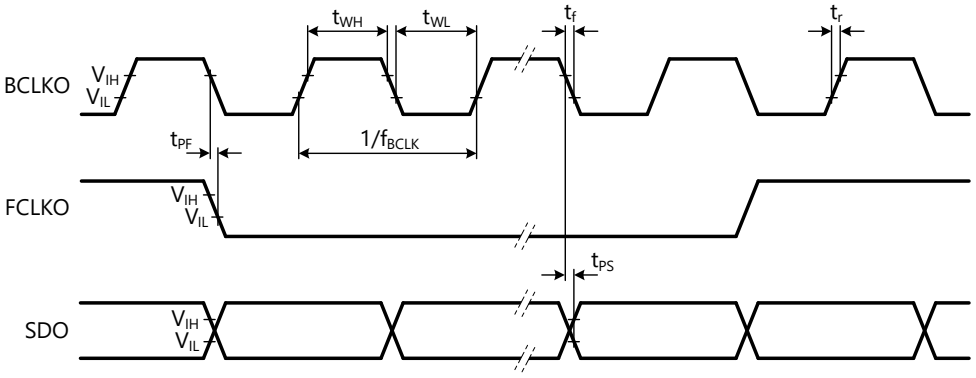


Figure 6. Serial data transmitter timing characteristics

6.4 JTAG Interface

Table 10. JTAG interface characteristics

3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; T_a = -40 °C to +85 °C; simulated values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TCK}	TCK clock frequency		-	-	10	MHz
t_{WL}	pulse width LOW	pin TCK	0.25 / f_{TCK}	-	-	ns
t_{WH}	pulse width HIGH	pin TCK	0.25 / f_{TCK}	-	-	ns
t_r	rise time	pins TCK, TMS, TDI	-	-	0.17 / f_{TCK}	ns
t_f	fall time	pins TCK, TMS, TDI	-	-	0.17 / f_{TCK}	ns
$t_{su(D)}$	data input set-up time	pins TDI, TMS	5	-	-	ns
$t_{h(D)}$	date input hold time	pins TDI, TMS	5	-	-	ns
$t_{d(o)}$	output delay time	pin TDO	15	-	-	ns
t_{PHZ}	HIGH to OFF state propagation delay	pin TDO	-	-	15	ns

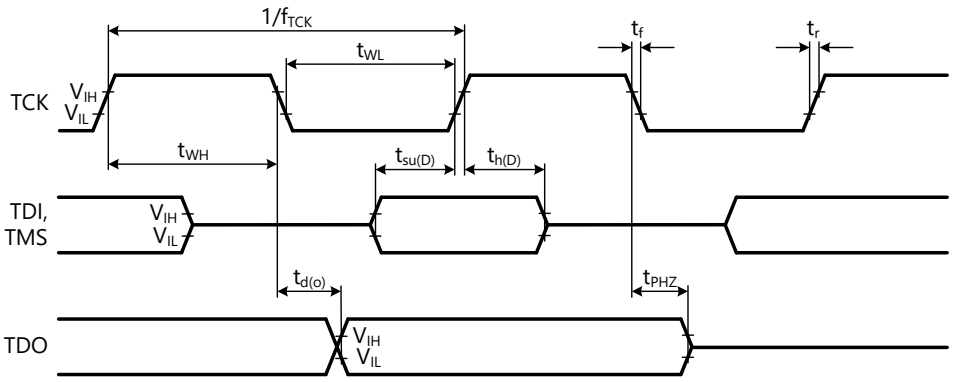


Figure 7. JTAG timing characteristics

6.5 Clock and reset requirements

Table 11. Master clock requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCLK}	MCLK clock frequency		45.1584	-	49.152	MHz
t_{WL}	pulse width LOW	pin MCLK	0.25/f_{MCLK}	-	-	ns
t_{WH}	pulse width HIGH	pin MCLK	0.25/f_{MCLK}	-	-	ns
t_r	rise time	pin MCLK	-	-	0.17/f_{MCLK}	ns
t_f	fall time	pin MCLK	-	-	0.17/f_{MCLK}	ns

[1] The wideband jitter that can be tolerated is approximately 100 ps RMS period jitter (or 600ps peak-to-peak) to keep the dynamic range above 110 dB. Baseband jitter (100 Hz to 200 kHz) must be less than 1.6 ns RMS to keep the dynamic range above 110 dB.

Table 12. Reset requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rst(L)}$	reset LOW time		20 / f_{MCLK}	-	-	ns
$t_{d(o)}$	output delay time	pins PSTART, PSTART_N	-	-	1 / f_{MCLK}	ns
t_{PHZ}	HIGH to OFF state propagation delay	pins OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8	-	-	1 / f_{MCLK}	ns

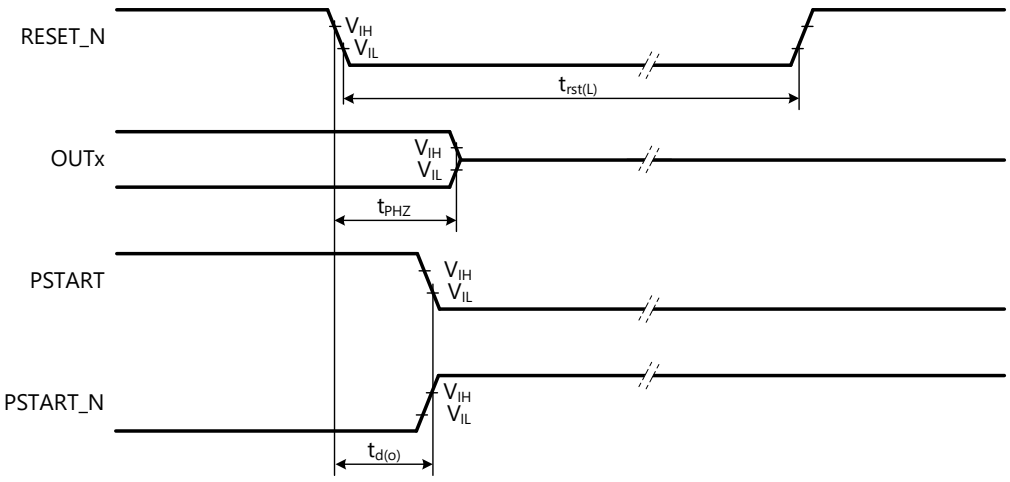


Figure 8. RESET_N Timing

7 Functional description

7.1 Overview

The AX5689 is a controller IC for digital audio reproduction consisting of 8 digital signal processing blocks and 8 analog-to-digital converters along with programmable, flexible signal routing.

The AX5689 contains 8 low-latency ADCs which are optimized for fast and therefore stable control loop operation. The typical latency from analog signal change to bitstream output change is 1 clock cycle. ADCs may also be selected for auxiliary functions such as analog inputs or power supply sensing. The outputs of the ADCs may be decimated and made available through the serial digital output interface.

The device accepts up to 16 PCM input channels through a serial audio interface and 8 balanced analog inputs through its ADCs. The serial audio interface can also deliver up to 8 channels of data from internal nodes or low-pass filtered and decimated ADC signals back to the host.

The AX5689 furthermore contains 8 sophisticated digital control loop structures, consisting of volume control, second order sections and rounding controls. Each of the channels is separately configurable and programmable. Channels may be split or cascaded to create more complex structures.

An interleaving stage is provided for combining channel outputs in a BTL or multi-phase PWM manner.

A versatile PWM controller converts the signal to 1-bit form with a wide selection of pulse frequencies and modulation methods. The CMOS level PWM outputs can be fed directly to a switching power stage that is followed by an output reconstruction filter. The filter compensation in the can correct for a wide range of external filter configurations.

The device is programmed via an SPI or I2C interface. The interface provides access to all features and is used to define the data path.

The combination of these blocks in one IC makes the AX5689 suitable as a digital amplifier with ADC feedback loop encompassing external components such as a power stage and output filter, as illustrated in Figure 9.

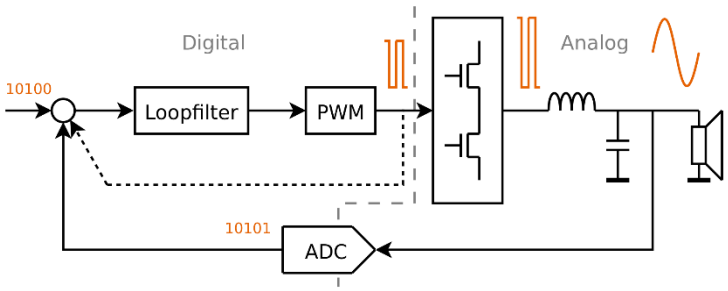


Figure 9. Digital amplifier with low-latency ADC feedback

An amplifier that uses the AX5689 can achieve high performance at low cost as all error sources within this loop are highly suppressed by the loop gain. This results in relaxed requirements for e.g. the power supply, the power stage and output filter components, thus making it easier to optimize the costs of the system.

7.2 Control interface

The control interface provides read and write access to the AX5689 control registers and consists out of four external I/O pins that may be operated in either SPI mode or I2C mode. In both modes, the AX5689 will act as slave device. Operation of this interface is asynchronous with respect to the audio sample rates.

The control interface is set to I2C mode. In I2C mode, pin CSN_AD0 and pin MISO_SDA set the desired AD0 and AD1 bit state of the I2C slave address. The control interface is put into SPI mode if a negative edge on pin CSN_AD0 is detected. Ensure that the CSN_AD0 and MISO_SDA pin are set to a fixed value using a pull-up or pull-down resistor to prevent unintentional change over from I2C mode to SPI mode.

7.2.1 Protocol

The protocol definition applies to the data words of the communication cycles via the control interface and is independent of the chosen interface mode. The number of data words transferred is unlimited and fully determined by the master device controlling the control interface. Each data word consists of 16 data bits while the bit order of all data words is MSB first.

The data word composition is shown in Table 13. For write cycles, the first data word contains the auto-increment enable bit (AINC), 5 don't care bits and the 10-bit register address pointer (RAP). Any additional data words are treated as register write data (RWD), therefore writing the second data word to the register indicated by the register address pointer. When the auto-increment bit is set, the register pointer will be incremented by one after the data word has been written to allow successive RWD words being written to consecutive register addresses. Note that when the AINC bit is cleared, successive RWD words are being written to the same currently selected register.

Table 13. Control interface data word composition

Word number	Bit number															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	AINC	don't care					RAP (9:0)									
1	RWD															
2	RWD+1															
…	…															
n	RWD+n-1															

7.2.2 I²C Mode

This operation mode of the control interface requires two interface pins for the actual communication, SCL and SDA. The remaining interface pins AD0 and AD1 are used for I2C slave address configuration.

The SDA pin is a bidirectional data pin used to transfer data into and out of the control interface synchronous to the clock signal on the SCL input pin. All communication cycles begin with a start condition (negative edge on SDA while SCL is high) and are ended by a stop condition (positive edge on SDA while SCL is high). A repeated start condition may be generated instead of a stop condition, indicating the start of the next communication cycle. Data bits on SDA are valid when SCL is high and SDA transitions will only occur while SCL is low.

Each transferred data byte is being acknowledged by the receiver of the byte. Under normal conditions the acknowledge bit will be zero, indicating correct data transfer.

The first transferred byte consists of the MSB first 7-bit slave address and R / $\overline{W}$ bit. The upper 5 bits of the I2C slave address are 01110. The two least significant bits are configurable by pins AD1 and AD0. Therefore, a maximum of four devices can operate in the same system in I2C mode.

Table 14. I2C-bus slave address table

Fixed address					Pin connectivity		7-bit hexadecimal address
A7	A6	A5	A4	A3	AD1	AD0	
0	1	1	1	0	0	0	38h
0	1	1	1	0	0	1	39h
0	1	1	1	0	1	0	3Ah
0	1	1	1	0	1	1	3Bh

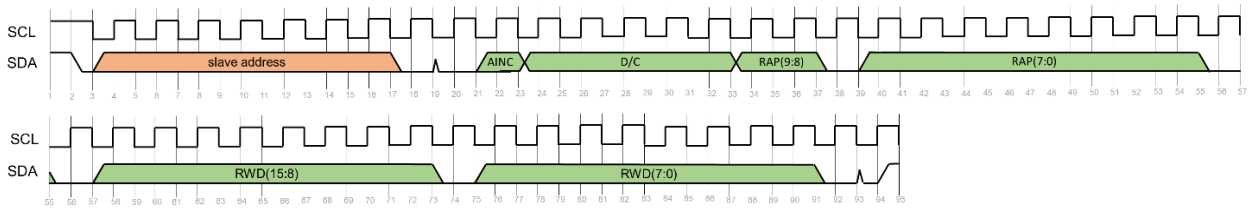


Figure 10. I²C write cycle

For read cycles, the I2C master shall indicate that it has received all data by making the last acknowledge bit one. Hereafter a stop condition or repeated start condition shall occur.

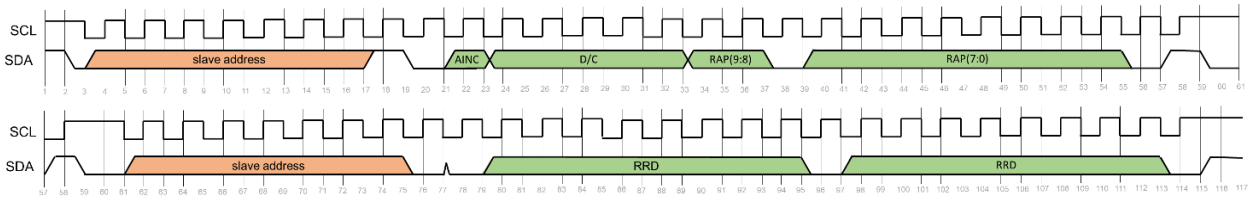


Figure 11. I²C read cycle

7.2.3 SPI Mode

In SPI mode, the chip uses the SCK, MISO, MOSI and CS_N pins. Data written to the control interface is received via the MOSI pin, while data read from the control interface will be transferred via the MISO pin. Data transfers are synchronous to the clock signal on the SCK input pin. The default state of SCK is high (also known as CPOL=1) and communication cycles are enabled by a logic low level on CS_N. The data bits are captured (MOSI) at the positive edge of the bit clock and are shifted out (MISO) at the negative edge of the bit clock (also known as CPHA=1). During data write cycles, the control interface keeps its data output in high impedance state.

The lower 2 bits of the SPI slave address are, unlike in I2C mode, not configurable and are fixed at “11”. Therefore, the default SPI slave address is 0111011.

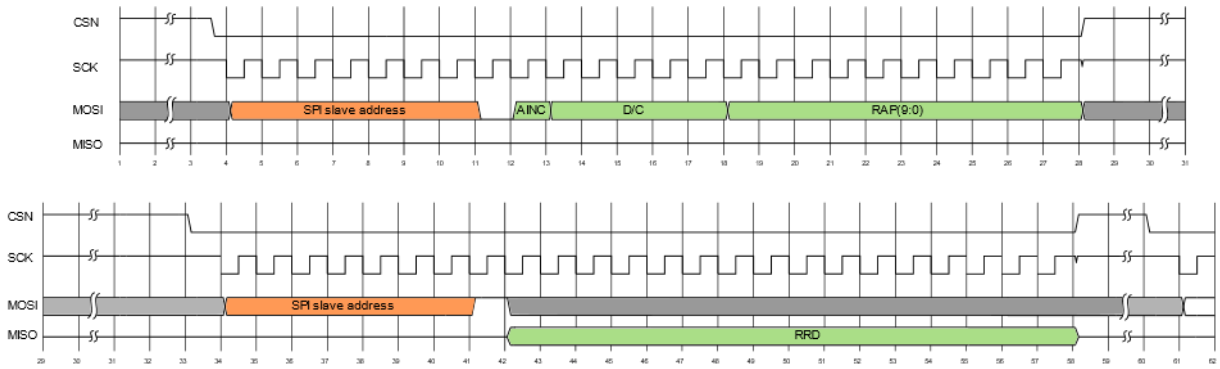


Figure 12. SPI read cycle

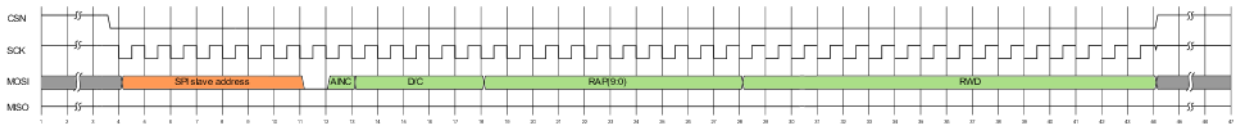


Figure 13. SPI write cycle

7.3 Serial audio Interface

The serial audio interface is used for in- and outputting data into and from the AX5689. The AX5689 is a slave on its serial audio input and a master on its serial data output. The register bits controlling audio format, word length and loop filter channel allocations are summarized in Table 18 for serial data transmitter and Table 19 for serial data receiver.

7.3.1 Audio formats

All formats can send MSB or LSB first and support frame lengths of 2, 4, 8 and 16 (receiver only) words, and word lengths of 16, 24 and 32 bits. Data may be sampled on the rising or falling edge of BCLK.

The number of BCLK clock cycles per FCLK clock cycle should be equal to the number of bits per word times the number of words per frame. A frame is synchronized to the active going flank of FCLK, or optionally one BCLK cycle after the active going flank of FCLK. There is no FCLK to BLCK word synchronization of the slots within a frame.

The data bits are all assumed to be significant. Given the requirement on BCLK with respect to FCLK there is no need for left or right justification. Should the data contain a different number of valid bits per word, zero padding is needed from the source. In case of invalid data, the last valid input data may be held.

The routing from the sub-frame data to the loop filters is programmable.

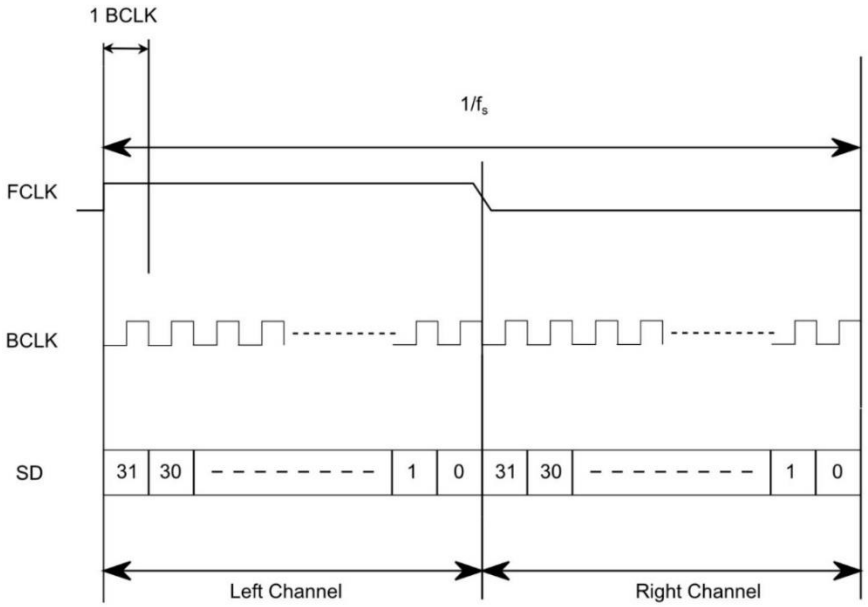


Figure 14. Serial audio interface timing with default settings

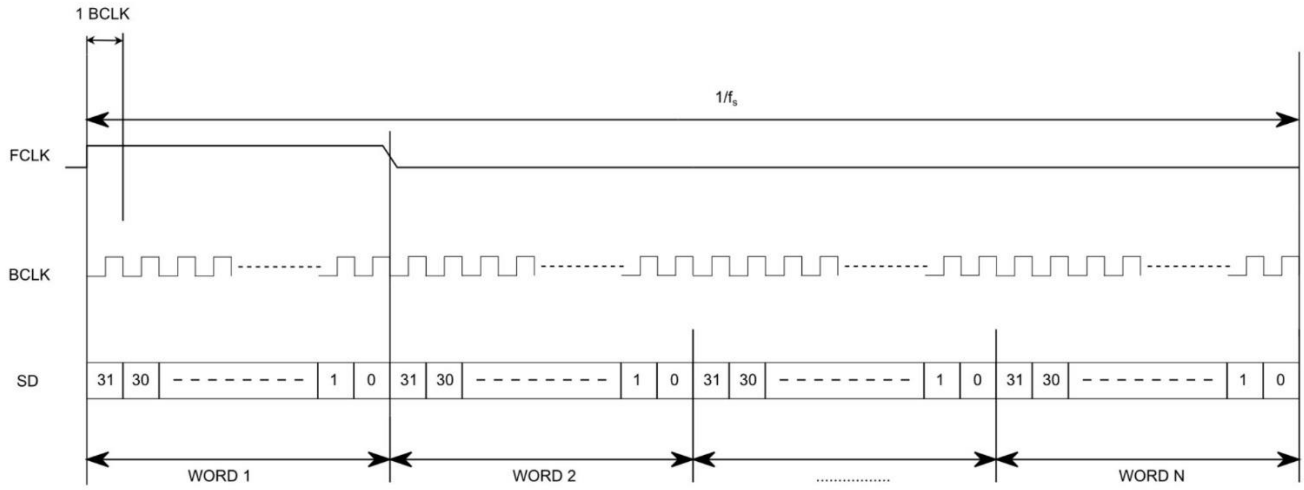


Figure 15. Generalized TDM timing diagram

7.4 Feed-in filter

The inputs of the loop filters can mix signals coming from several parts inside and outside the AX5689. Each loop filter has four inputs:

- A PCM input which receives the mapped audio data times slots from the serial data receiver.
- Two feed-in inputs which can be connected to any ADC common or differential mode output, filtered versions thereof or any PWM outputs.

- Output of the previous loop filter channel.

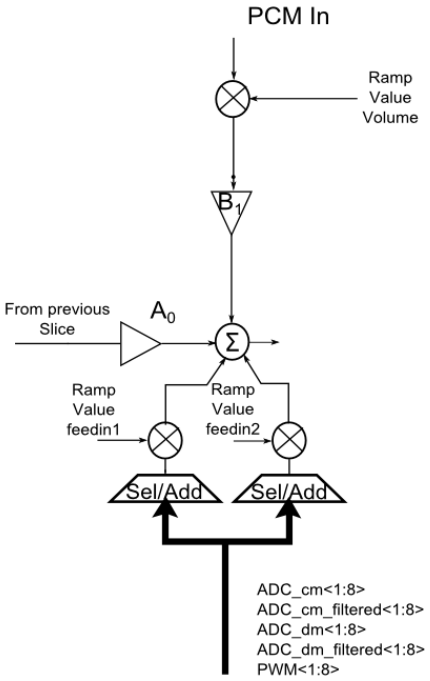


Figure 16. Feed-in filter

7.4.1 Volume/ramp generators

The inputs coming from the PCM, the feedin1 and feedin2 paths have ramp controls, these ramp controls can morph linearly between two end values called ramp value1 and ramp value2 as illustrated in Figure 17. The ramp transition time is governed by a step size value, a ramp interval time and ramp endpoint selection. The step size, ramp value1 and ramp value2 setting can be programmed for each channel, as shown in Table 26. The ramp interval is common for all channels. A separate ramp interval can be programmed for error mode, allowing for fast mute or switchover in error conditions. The ramp endpoint selection can be programmed for each channel. Table 17 shows the register description for the ramp endpoint and ramp interval setting.

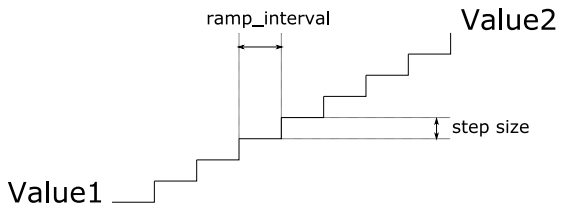


Figure 17. Ramping principle

The maximum output of the loop filters is 0 dBFS. The system will hard-limit if the combination of coefficient settings and input signals results is larger than 0 dBFS.

7.5 Loop filter

The loop filters are designed to be extremely flexible and versatile down to the configuration of the data path. This section describes the signal processing inside the control loop as shown in Figure 18. The input for the digital loop-filter is the digital input signal from the ramp and previous loop filter summation stage. The digital loop-filter consists of a programmable 7th order filter. The filter can be configured as a high-order noise shaping filter that makes sure noise and non-linearity generated inside the loop is suppressed. Each stage in the filter can be separately enabled by programming the *stage_out_enable* bit of each channel loop filter's control register, as shown in Table 27.

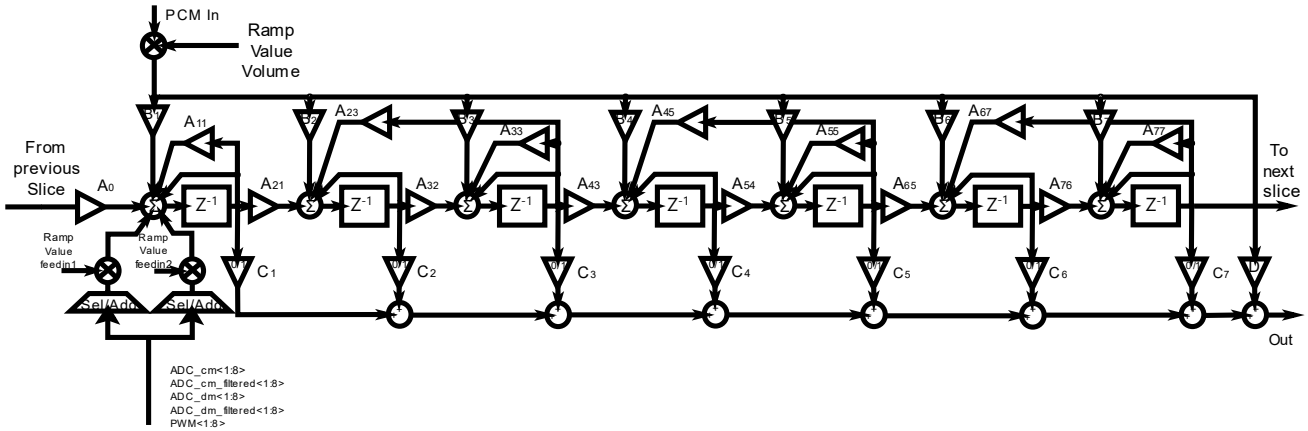


Figure 18. Loop filter slice including feed-in selection and volume/ramp generators

7.5.1 Zero detection

The states of all stages in the loop filter can be monitored for zero detection. Since LSBs can be quite noisy and thus upset the detection they can be masked off and only a certain number of MSBs used for the zero detection. This setting is possible by programming the *zerox_setting* bit of each channel loop filter's control register, as shown in Table 27.

7.5.2 Limiting and clip detection

All stages inside the loop filter may be monitored for overflow by setting the *limit_detect_enable* bit of each channel loop filter's control register to zero or one, as shown in Table 27. When overflow occurs, it can either be ignored, detected or the value may be limited to the programmed threshold. The clip value can be programmed as an integer exponent, i.e. power of 2 below 0 dBFS.

7.6 Butterfly mixer

After the loop-filter a butterfly mixer mixes the signals from the various stages to enable MIMO processing.

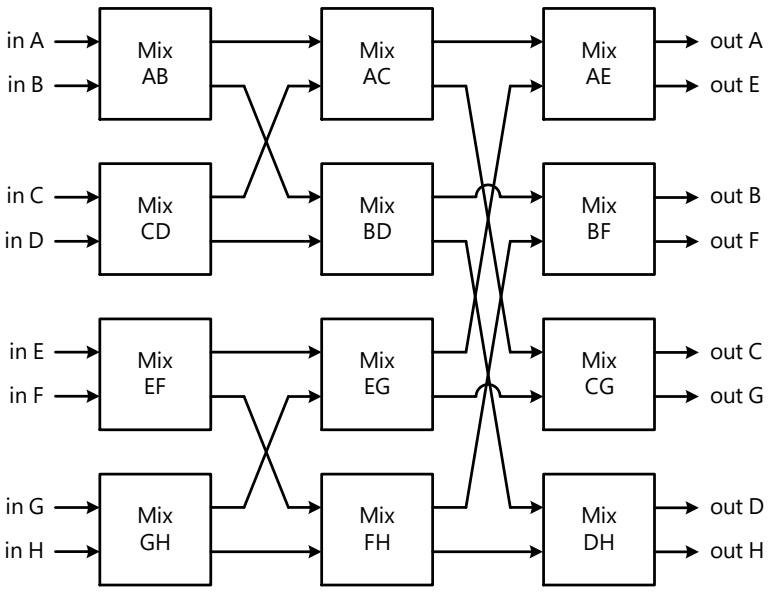


Figure 19. Butterfly mixer

The butterfly mixer as shown in Figure 19 mixes the various loop filter outputs to enable a variety of MIMO filter operations, such as differential and common-mode control filters or more complex multipath versions. The structure of the mixer resembles that of a radix-2 FFT. Each butterfly element can mix two of its inputs in a variety of ways as shown in Figure 20.

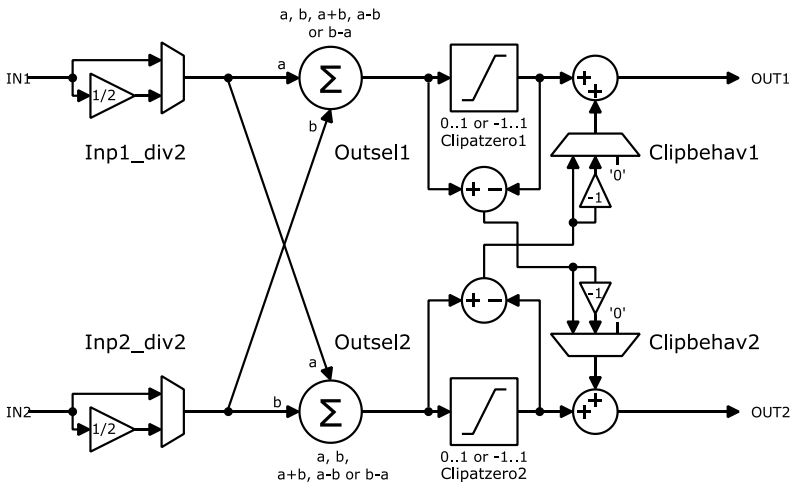


Figure 20. Butterfly mixer element

Inputs to the data paths may be halved by programming the input div2 dividers. Subsequently the 'outsel' operators can either select or combine the two input paths.

The clip control mechanism inside the butterfly mixer elements can limit the maximum and minimum signal levels. The clip compensation functionality can also prevent common-mode clipping from becoming visible in the differential mode signal.

The signal range is either between -1 and 1 (clipatzero = 0) or between 0 and 1 (clipatzero = 1). Values outside the range are clipped. When an output path clips, clipbehav determines whether either each data path clips separately (0), the remainder from clipping is added in the other path (1) or the remainder from clipping is subtracted in the other data path (2).

7.7 Pulse Width Modulator (PWM)

The pulse width modulator translates its PCM input signal into 1-bit output signals. There are two main elements to the PWM block, the carrier generator and the comparator / quantizer. The AX5689 has eight independent pulse width modulators. The block schematic is shown in Figure 21.

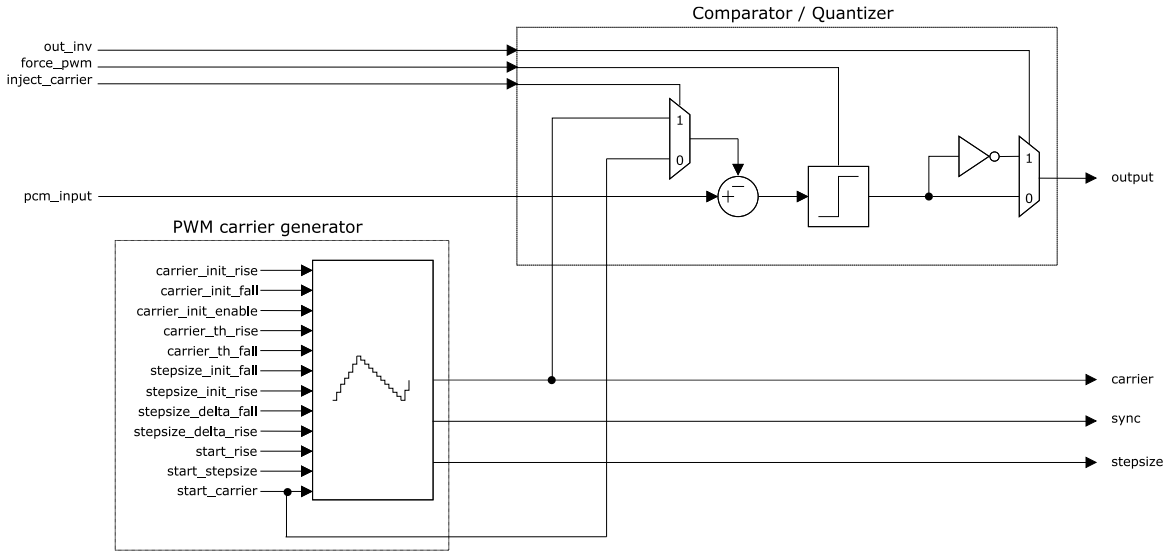


Figure 21. PWM block diagram

In normal operational mode, the PWM carrier block generates a triangle wave which is subtracted from the input signal, and the result is quantized to two levels, thus comprising the modulator function.

7.7.1 Carrier generator

The carrier generator in the pulse width modulator can be programmed for frequency and shape. The general shape of the PWM carrier is shown in Figure 22.

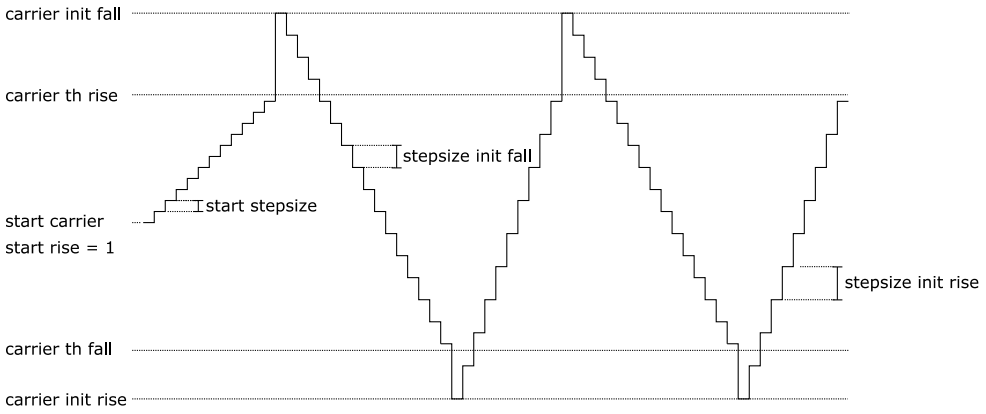


Figure 22. First order PWM carrier wave and variables governing its shape

The triangle wave is constructed as follows: the system starts at level *start_carrier* and rises or falls, depending on *start_rise*, with *start_stepsize* until it reaches the level of *carrier_th_rise*. Upon reaching this threshold the waveform jumps to *carrier_init_fall* and starts to fall by *stepsize_init_fall* until it reaches the lower threshold *carrier_th_fall*. From there it jumps to *carrier_init_rise* and rises with *stepsize_init_rise* and the cycle repeats.

Any of the variables named above may be freely chosen. From the step size combined with the distance between *init* and *threshold* levels, the PWM triangle cycle time and therefore PWM carrier frequency may be calculated. It follows that different channels can have different frequencies, but also that channels may have a phase offset with respect to each other, determined by the initial values of the carrier.

It is furthermore possible to make a second order PWM waveform by using the *stepsize_delta* parameters, such that every step has a different size.

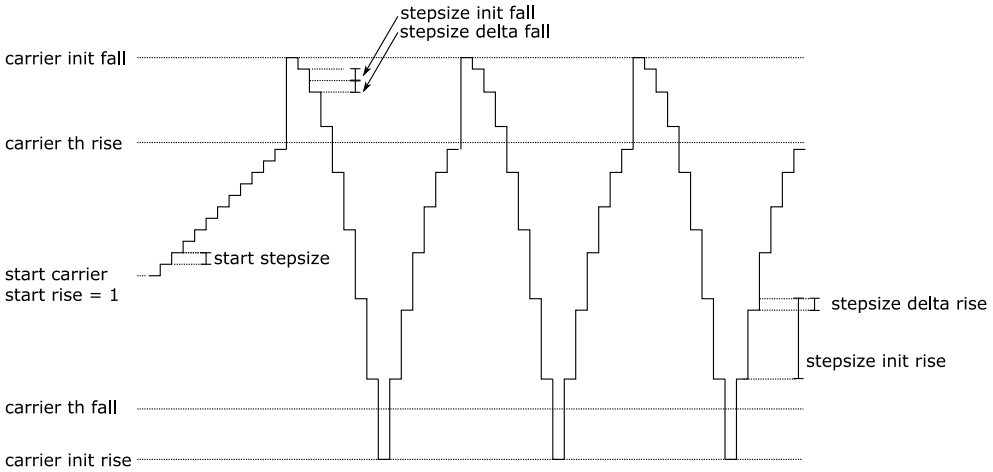


Figure 23. Second order PWM carrier wave and variables governing its shape

In Figure 23 again a waveform is constructed using the variables used in Figure 22, but this time the rising slope has a negative *stepsize_delta_rise*, causing the steps to become ever smaller, and the falling slope has a positive

stepsize_delta_fall, causing the steps to become ever larger. Thus, a non-linear second order PWM carrier is constructed. Care must be taken with negative delta values such that the step size does not become zero before the corresponding carrier threshold is reached.

7.7.2 Comparator/quantizer

The comparator block performs the modulation of the signal with the carrier and subsequently truncates the output to 1 bit.

To support both PDM and PWM outputs, control bits have been added. The *force_pwm* bit allows the quantizer to only emit one falling edge during the rising flank of the PWM carrier and one rising edge during the falling flank of the PWM carrier, even if the signal moves erratically around the carrier signal. Setting this bit thus ensures a fixed PWM frequency.

On the other hand, the *carrier_inject* bit, when set to zero, subtracts no carrier wave form in the comparator, reducing it to a 1-bit quantizer and thus turning the system into a PDM system. Instead of the carrier triangle wave, a fixed level of *start_carrier* is subtracted. When this is not desired, *start_carrier* should be set to zero. Optionally, the output may be inverted by setting *out_inv* to 1.

7.8 Output crossbar

In the crossbar, different routing options are possible. The crossbar is a multiple-input multiple-output (MIMO) block that supports flexible routing options, where every output could be programmed to pass along PWM outputs or either of the differential-mode or common-mode ADC outputs. The structure of the crossbar is shown in Figure 24.

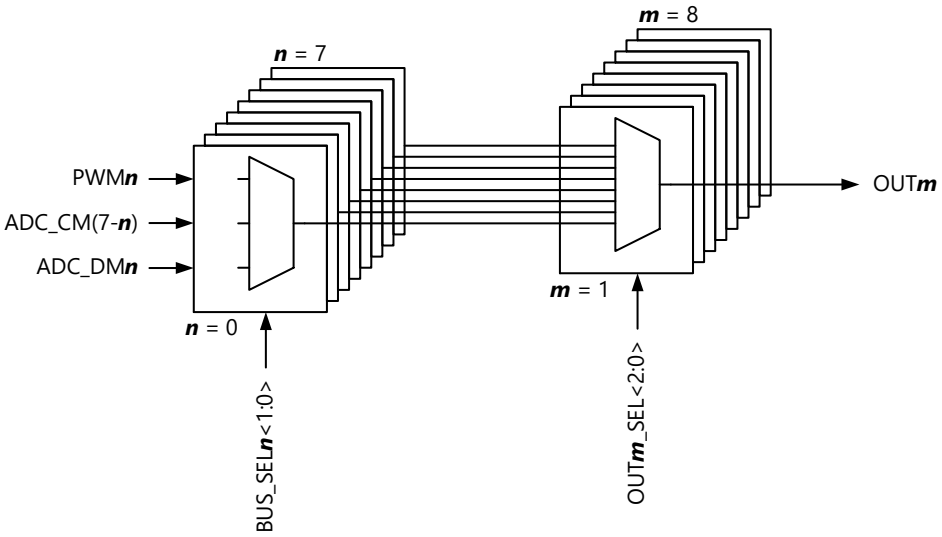


Figure 24. Output crossbar

The routing possibilities can be exploited by configuring the configuration registers that control the select lines of each multiplexer. Refer to Table 22 for the outputs crossbar configuration register description.

7.9 Low-latency ADC (LLADC)

The eight low latency ADCs on the AX5689 are of a special type of continuous-time sigma-delta ADC. Its low latency is made possible by bit stream outputs (q_dm and q_cm) which are fed back into an internal DAC with a tracking behavior as illustrated in Figure 25. Its outputs therefore track the input signal inside the signal bandwidth. The resulting system is robust towards jitter and other error sources typically associated with continuous-time 1-bit converters.

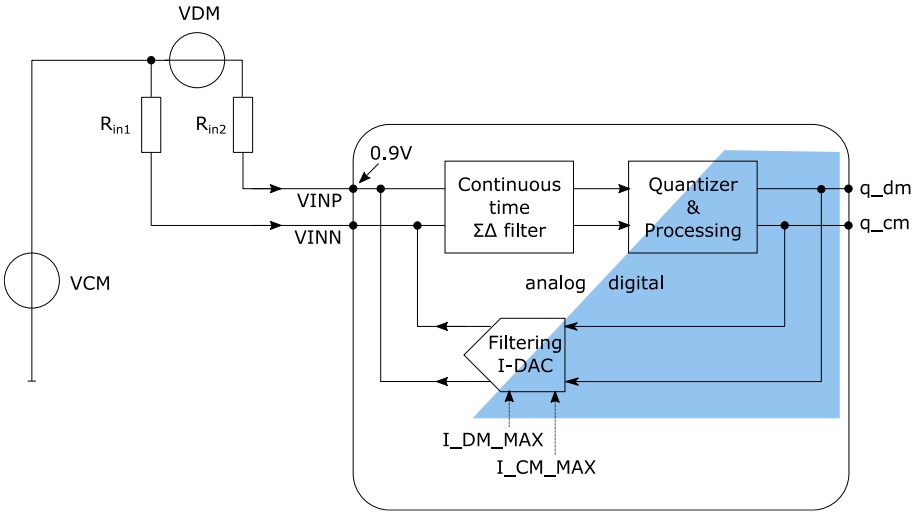


Figure 25. Low-Latency ADC principle diagram

The low latency ADC is a true differential current input ADC. It converts both single-ended and differential currents into separate bitstream outputs. By merit of a current input it can convert signals with amplitudes and biasing levels well outside its own supply level.

The ADC input terminals IN***x***P and IN***x***N (***x*** = 1 to 8) are virtual grounds which sense current and are biased at a reference voltage of 0.52 V after initialization. This voltage is derived from an integrated bandgap referenced circuit. The voltage on the outside terminals of R_{in1} and R_{in2} are thus converted into input currents.

The ADC feedback loop tracks these input currents in the DAC by recreating the common mode currents and the differential mode currents such that the currents going into the ΣΔ filter tend to zero. In doing so it has digitized the input currents and hence input voltages into bitstreams q_dm and q_cm.

An overview of possible use cases that the ADC can handle is given in Figure 26, Figure 27 and Figure 28.

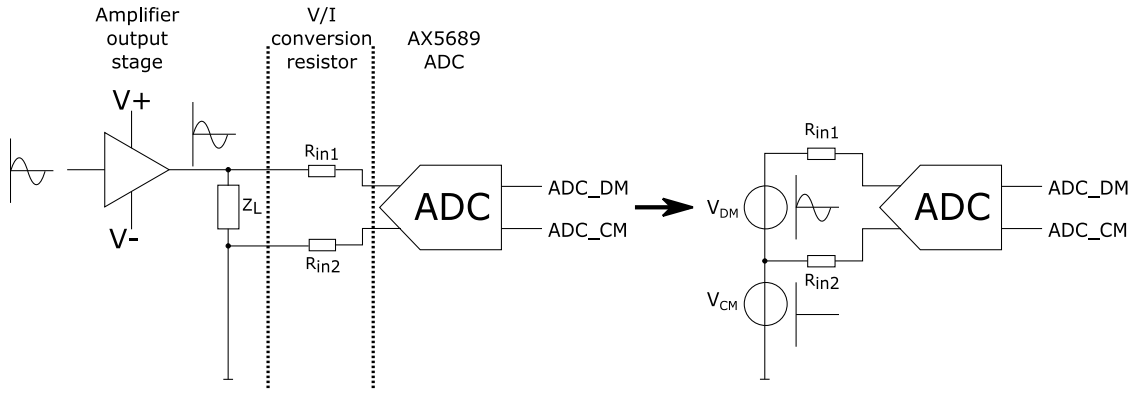


Figure 26. DC coupled Single Ended ADC use case. V_{DM} = V(Z_L); V_{CM} = V_+ + V_- = 0

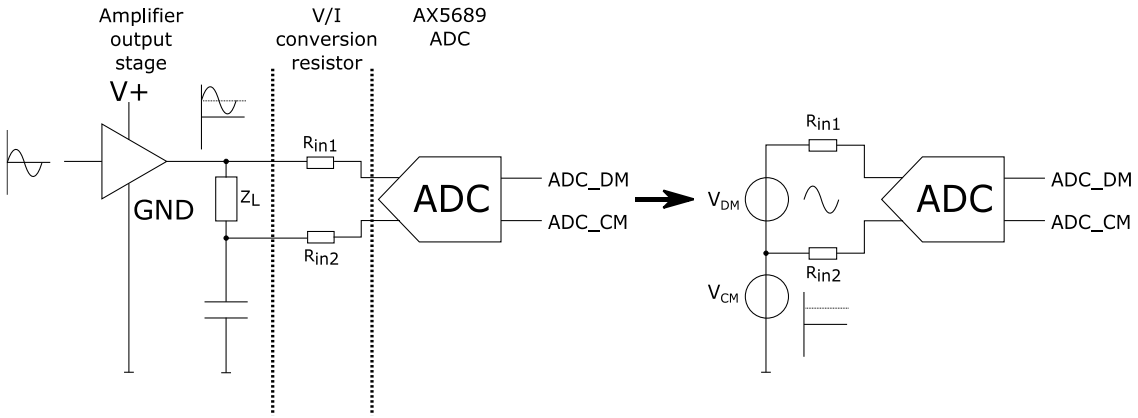


Figure 27. AC coupled Single Ended ADC use case. V_{DM} = V(Z_L); V_{CM} = V_+/2

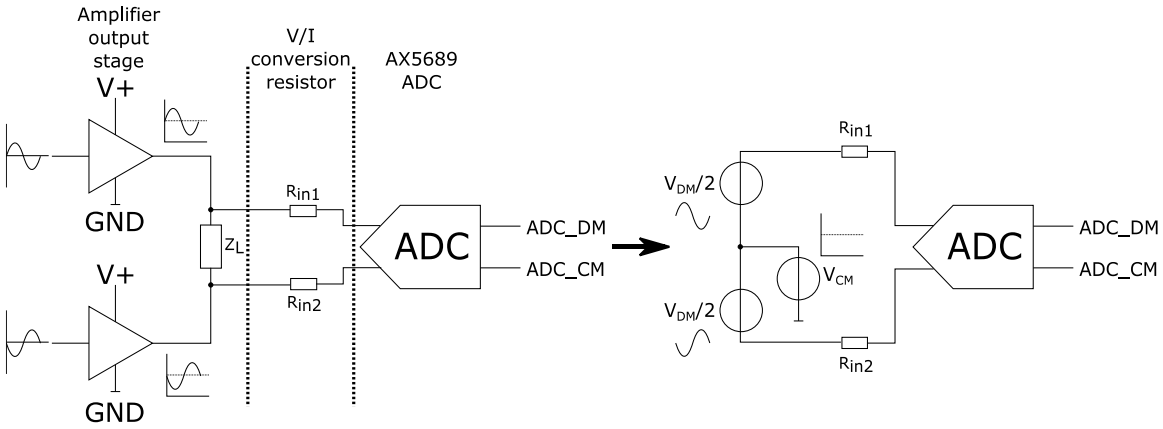


Figure 28. Differentially coupled ADC use case. V_{DM} = V(Z_L); V_{CM} = V_+/2

By selecting the correct value of voltage-to-current conversion resistors R_{in1} and R_{in2} an application can be scaled to arbitrary voltage levels. To minimize differential-mode to common-mode conversion and vice versa, the matching between R_{in1} and R_{in2} is critical, but only on a channel by channel basis.

7.9.1 Full-scale differential mode current scaling

For maximum system performance it is advised to use the full range of the LLADC. However, to save power, the current that leads to full-scale bitstream output (q_dm) may be scaled down. The differential full-scale current scaling affects all ADC channels simultaneously.

The full-scale differential mode input current is given as

$$I\_MAX\_DM = 10E\text{-}3 * REFGEN\_IREF\_FIR\_VALUE / 63$$

The default value for *REFGEN_IREF_FIR_VALUE* is 47 which leads to a maximum input differential current of 7.5 mA.

The AX5689 ADCs have a modulation depth of 64%, which means that the signal swing based on I_MAX_DM should be scaled to this:

$$I\_SIG\_DM = I\_MAX\_DM * 0.64$$

Which for the default values leads to a maximum signal current of 4.8 mA.

In case an input differential voltage of 50V is to be digitized, this means that the external resistors R_{in1} and R_{in2} should be scaled to (50V - 0.6V) / 4.8mA = 10.3 kΩ.

7.9.2 Full-scale common mode current scaling

The maximum common-mode current that leads to full-scale common-mode bitstream (q_cm) output is programmable as a fraction of the full-scale differential mode current. Contrary to the full-scale differential mode current scaling, the full-scale common-mode current scaling is programmed on a channel by channel basis.

In general, it is advised to scale the full-scale common-mode close to the expected average level rather than the worst-case occasional level for maximum stability.

The choice of common-mode current is highly dependent on the application. In case of a BTL application such as depicted in Figure 28 the voltages will always be positive; therefore, the sum of differential and common mode should always be positive, and hence the common mode should be equal to the differential mode.

In case of a single ended use case as depicted in Figure 26, the signal is symmetrical around zero and hence the common mode should equal half of the differential mode, such that the sum is symmetrical around zero.

The full-scale common-mode input current is given as:

$$I\_MAX\_CM = I\_MAX\_DM * FIR\_CUR\_RATIO / 21$$

The default value for *FIR_CUR_RATIO* is 26 which leads to roughly a ratio of 1:1 between differential and common-mode current ranges.

7.9.3 Input scaling versus frequency

The low latency ADC behaves like a tracking ADC with noise-shaping. As with other tracking ADCs the low latency ADC has a frequency-dependent maximum signal that it can convert. The maximum signal levels are given in Figure 29 (separated for differential and common-mode signals and normalized to 0 dB at low frequencies).

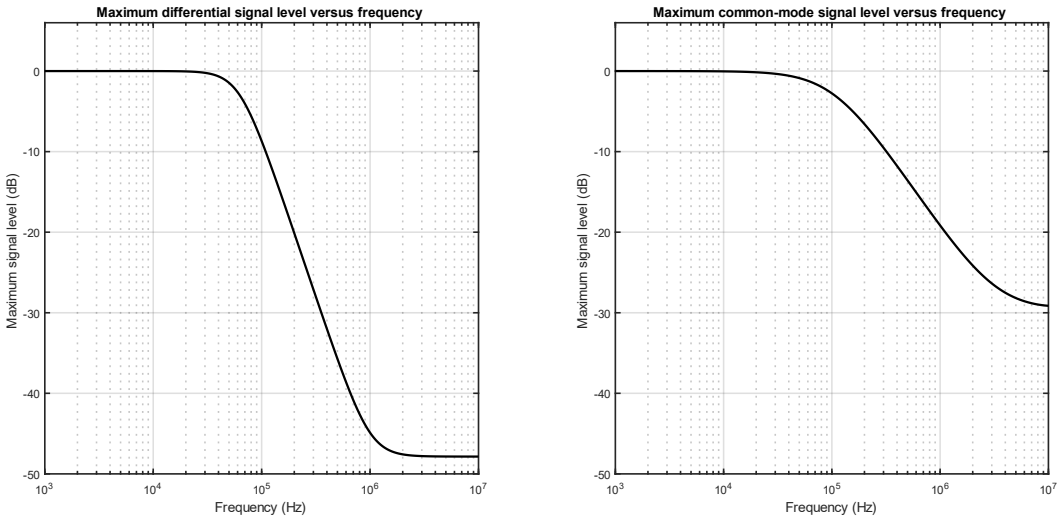


Figure 29 - ADC maximum signal levels

It is important that the input signals to the ADC do not exceed these maximum signal levels in order not to overload the ADC. It is hence important that at least some reconstruction filtering is used between the switching output and the ADC feedback.

7.10 Power stage control

The AX5689 has four pins which can be used to interact with a power stage. Pin PSTART and PSTART_N are used to enable/disable the power stage. Pin PFAULT_N and PWARN_N handle fault and warning signals from the power stage.

7.10.1 PSTART and PSTART_N

Outputs PSTART and PSTART_N operate exactly the same except for their opposite active-HIGH and active-LOW state. Both outputs are in High-Z state during a supply power-up sequence and as long as the RESET_N input is active.

7.10.2 PFAULT_N

The active-LOW PFAULT_N input is used to handle the power stage fault conditions like: overvoltage, undervoltage, short-circuit protection and over temperature protection. When pin PFAULT_N is active the AX5689 controls the PSTART and PSTART_N signals to disable the power stage. Once the power stage fault is resolved the AX5689 controls the PSTART and PSTART_N signals to enable the power stage again.

7.10.3 PWARN_N

The AX5689 has a PWARN_N input, which is active low. When this input is low, the PCM volume starts to ramp down. When the input becomes high, the PCM volume starts to ramp up. The slope of the volume ramp can be set by *pcmvol_ramp_interval* (see Table 17). The volume ramp transition time (from max volume to zero volume) can be calculated as follows:

$$t_{ramp} = \frac{ramp\_value2 - ramp\_value1}{stepsize \cdot f_{mclk}} \cdot 16 \cdot (pcmvol\_ramp\_interval + 1)$$

Where t_{ramp} is the ramp transition time, f_{mclk} is the master clock frequency of the AX5689, and *pcmvol_ramp_interval* is the value of register 0007h. The number of steps is set using the volume ramp register settings. For channel A, the volume ramp registers are *ramp_value1* (register 0040h), *ramp_value2* (register 0041h) and *stepsize* (register 0042h). See the register map for the volume ramp register base addresses of channel B to H.

7.11 Mode control

7.11.1 RESET_N pin

The AX5689 has an active low RESET_N pin. Activating the reset will set all hardware registers to their default value. After releasing the reset the device must be initialized again.

7.11.2 STATUS pin

The AX5689 can diagnose several internal and external conditions. The status of the diagnosis is stored in three registers. The registers have a dual function where a read command will output the information of the register, and a write to the same register will influence its mask setting. The following conditions can be detected for all channels:

- Channel loop filter output polarity.
- Loop filter zero; zero is detected when the number of MSB bits used for zero detection as configured in the loop filter settings are zero.
- Positive or negative clipping; separate for each channel but combined over all channel states.

In addition, the following global conditions are indicated:

- PWARN_N pin status
- Mute status
- Serial data receiver status
- PFAULT_N pin status.

The complete set of status registers is listed in Table 24.

The STATUS pin is activated if the logical OR of any of the bitwise AND operations between the status bits and mask conditions equals one, see Figure 30.

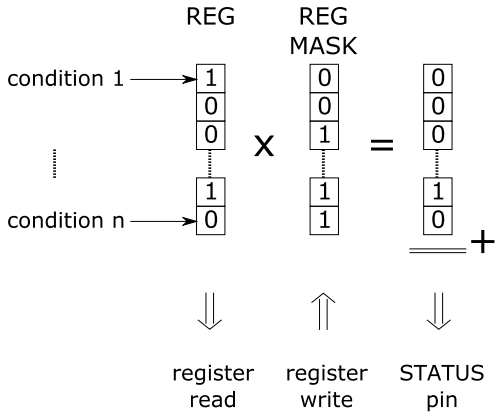


Figure 30. Overview of status register and STATUS pin

If all the mask bits are set to zero, a register read of any of the status bits will return its momentary state which will not persist in the register when the condition itself disappears. If mask bits are set to one, then the corresponding condition will activate the STATUS pin.

Upon activation of the STATUS pin the pin state and the set of register conditions that triggered it are frozen until the three status registers have been cleared. To clear the status registers, read the three registers (address 003Ch to 003Eh) in consecutive order. If a single status register is read the status information is not cleared. Registers which have their mask bit set to zero are not cleared after read.

7.11.3 MUTE_N

Activating the mute pin will ramp to Value1 for each loop filter. Setting Value1 to zero will then perform a full soft mute.

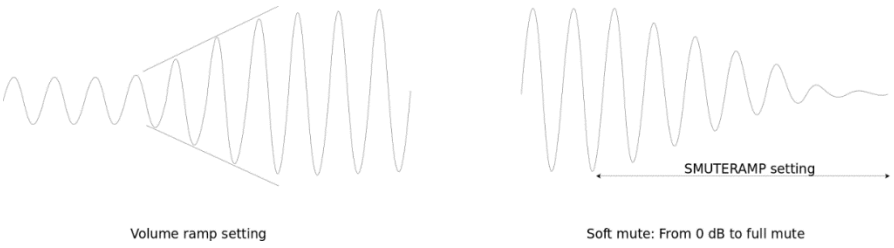


Figure 31. Volume control behavior in waveforms

7.12 Startup and shutdown

The following flow gives an high-level description of device initialization after reset and its channel startup/shutdown procedure for a typical application. Depending on the application needs, alternative flows may be better suited. Please, refer to Axign's reference designs for a detailed implementation of the startup and shutdown procedure.

7.12.1 Initialize

The following steps list the sequence to initialize the device:

1. Power-up the AX5689. Recommended order for supply power-up is VDD(IO) first, followed by VDDA and VDDD. Keep the RESET_N input logic-LOW during supply power-up to prevent unknown output conditions.
2. Power-up the supplies of the power stage (proper connections to the PSTART/PSTART_N pins ensures that it remains inactive).
3. Apply a 49.152 MHz clock to the MCLK input.
4. Provide digital I2S/TDM stream to the serial audio port.
5. Set RESET_N pin to logic-HIGH.
6. Configure data path connections, mute, signal processing coefficients and other settings via the I2C/SPI control port.
7. Enable the bandgap reference and reference ADC. Wait for the reference ADC to settle.

7.12.2 Startup

Startup the audio channels using the following sequence of steps:

1. Enable the loop filters and PWM modulators.
2. Enable external ADC feedback.
3. Enable the power stage.
4. Unmute the audio path by setting MUTE_N pin to logic-HIGH. Wait for mute sequence to complete.

7.12.3 Shutdown

To shut down the device use the following sequence of steps:

1. Mute the audio path by setting MUTE_N pin to logic-LOW. Wait for mute sequence to be completed.
2. Put the power stage in high-Z. Wait for the power stage to shutdown.
3. Disable external ADC feedback.
4. Disable the loop filters and PWM modulators.

8 Register map

The memory map consists out of 576 × 16-bit words. The registers are divided into 9 banks of 64 registers each. General configuration data is stored in bank 0 and channel specific configuration data in bank 1 to 8. The total memory size is 9.216 kbit. Figure 32 shows the register map with the 9 banks and their base addresses. The detailed register bit descriptions show the offset address with respect to the base address of the bank.

memory address = base address + offset address

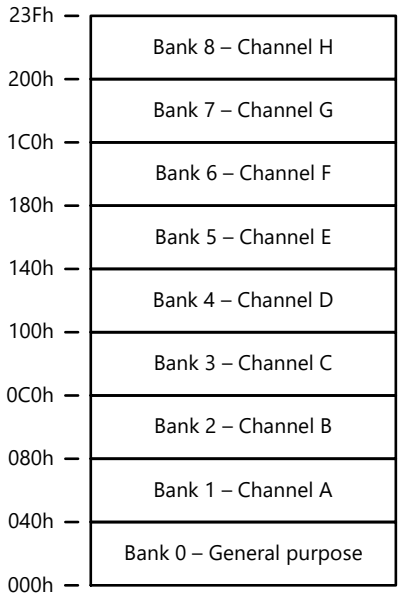


Figure 32. Register map

8.1 Bank 0 – Programming mode registers

Table 15. Bank 0 – Programming mode registers (offset address 0000h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0000h	programming mode	15:8	reserved	R/W	00h	-
		7	channel_write_select	R/W	0b	Bank 8 – Channel H write select 0: write disabled 1: write enabled
		6	channel_write_select	R/W	0b	Bank 7 – Channel G write select 0: write disabled 1: write enabled
		5	channel_write_select	R/W	0b	Bank 6 – Channel F write select 0: write disabled 1: write enabled
		4	channel_write_select	R/W	0b	Bank 5 – Channel E write select

Table 15. Bank 0 – Programming mode registers (offset address 0000h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						0: write disabled 1: write enabled
		3	channel_write_select	R/W	0b	Bank 4 – Channel D write select 0: write disabled 1: write enabled
		2	channel_write_select	R/W	0b	Bank 3 – Channel C write select 0: write disabled 1: write enabled
		1	channel_write_select	R/W	0b	Bank 2 – Channel B write select 0: write disabled 1: write enabled
		0	channel_write_select	R/W	0b	Bank 1 – Channel A write select 0: write disabled 1: write enabled

8.2 Bank 0 – Sub-system enable registers

The various sub-system enable registers are listed in Table 16.

Table 16. Bank 0 – Sub-system enable registers (offset address 0001h to 0002h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0001h	main channel enable	15	channel_pwm_enable	R/W	0b	Enable PWM channel H 0: PWM channel disabled 1: PWM channel enabled
		14	channel_pwm_enable	R/W	0b	Enable PWM channel G 0: PWM channel disabled 1: PWM channel enabled
		13	channel_pwm_enable	R/W	0b	Enable PWM channel F 0: PWM channel disabled 1: PWM channel enabled
		12	channel_pwm_enable	R/W	0b	Enable PWM channel E 0: PWM channel disabled 1: PWM channel enabled
		11	channel_pwm_enable	R/W	0b	Enable PWM channel D 0: PWM channel disabled 1: PWM channel enabled
		10	channel_pwm_enable	R/W	0b	Enable PWM channel C 0: PWM channel disabled

Table 16. Bank 0 – Sub-system enable registers (offset address 0001h to 0002h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						1: PWM channel enabled
		9	channel_pwm_enable	R/W	0b	Enable PWM channel B 0: PWM channel disabled 1: PWM channel enabled
		8	channel_pwm_enable	R/W	0b	Enable PWM channel A 0: PWM channel disabled 1: PWM channel enabled
		7	channel_filter_enable	R/W	0b	Enable loop filter H 0: loop filter disabled 1: loop filter enabled
		6	channel_filter_enable	R/W	0b	Enable loop filter G 0: loop filter disabled 1: loop filter enabled
		5	channel_filter_enable	R/W	0b	Enable loop filter F 0: loop filter disabled 1: loop filter enabled
		4	channel_filter_enable	R/W	0b	Enable loop filter E 0: loop filter disabled 1: loop filter enabled
		3	channel_filter_enable	R/W	0b	Enable loop filter D 0: loop filter disabled 1: loop filter enabled
		2	channel_filter_enable	R/W	0b	Enable loop filter C 0: loop filter disabled 1: loop filter enabled
		1	channel_filter_enable	R/W	0b	Enable loop filter B 0: loop filter disabled 1: loop filter enabled
		0	channel_filter_enable	R/W	0b	Enable loop filter A 0: loop filter disabled 1: loop filter enabled
0002h	miscellaneous enable	15:13	reserved	R/W	000b	-
		12	feedin_filter_enable	R/W	0b	Enable the feedin filters for ADC common mode, ADC differential mode and PWM 0: feedin filter disabled 1: feedin filter enabled
		11	powerstage_enable	R/W	0b	Enable the power stage

Table 16. Bank 0 – Sub-system enable registers (offset address 0001h to 0002h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						0: power stage disabled 1: power stage enabled
		10	reference_enable	R/W	0b	Enable the reference generator 0: reference generator disabled 1: reference generator enabled
		9	chargepump_enable	R/W	0b	Enable the charge pump 0: charge pump disabled 1: charge pump enabled
		8	radc_enable	R/W	0b	Enable the reference ADC 0: put analog core in power down mode 1: read enable settings from inputs
		7	adc_enable	R/W	0b	Enable ADC H 0: ADC disabled 1: ADC enabled
		6	adc_enable	R/W	0b	Enable ADC G 0: ADC disabled 1: ADC enabled
		5	adc_enable	R/W	0b	Enable ADC F 0: ADC disabled 1: ADC enabled
		4	adc_enable	R/W	0b	Enable ADC E 0: ADC disabled 1: ADC enabled
		3	adc_enable	R/W	0b	Enable ADC D 0: ADC disabled 1: ADC enabled
		2	adc_enable	R/W	0b	Enable ADC C 0: ADC disabled 1: ADC enabled
		1	adc_enable	R/W	0b	Enable ADC B 0: ADC disabled 1: ADC enabled
		0	adc_enable	R/W	0b	Enable ADC A 0: ADC disabled 1: ADC enabled

8.3 Bank 0 – Volume/ramp generator control registers

The settings listed in Table 17 set the feed-in paths to either Value1 or Value2 and govern the ramp interval.

Table 17. Bank 0 – Feedin and ramp interval control registers (offset address 0003h to 0008h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0003h	Feedin Ramp Select	15	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel H 0: Ramp value 1 selected 1: Ramp value 2 select
		14	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel G 0: Ramp value 1 selected 1: Ramp value 2 select
		13	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel F 0: Ramp value 1 selected 1: Ramp value 2 select
		12	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel E 0: Ramp value 1 selected 1: Ramp value 2 select
		11	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel D 0: Ramp value 1 selected 1: Ramp value 2 select
		10	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel C 0: Ramp value 1 selected 1: Ramp value 2 select
		9	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel B 0: Ramp value 1 selected 1: Ramp value 2 select
		8	feedin_ramp_select2	R/W	0b	Select feed-in ramp2 endpoint value for channel A 0: Ramp value 1 selected 1: Ramp value 2 select
		7	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel H 0: Ramp value 1 selected 1: Ramp value 2 select
		6	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel G 0: Ramp value 1 selected

Table 17. Bank 0 – Feedin and ramp interval control registers (offset address 0003h to 0008h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						1: Ramp value 2 select
		5	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel F 0: Ramp value 1 selected 1: Ramp value 2 select
		4	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel E 0: Ramp value 1 selected 1: Ramp value 2 select
		3	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel D 0: Ramp value 1 selected 1: Ramp value 2 select
		2	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel C 0: Ramp value 1 selected 1: Ramp value 2 select
		1	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel B 0: Ramp value 1 selected 1: Ramp value 2 select
		0	feedin_ramp_select1	R/W	0b	Select feed-in ramp1 endpoint value for channel A 0: Ramp value 1 selected 1: Ramp value 2 select
0004h	PCM Volume Ramp Select	15:8	reserved	R/W	00h	-
		7	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel H 0 = Ramp value 1 selected 1 = Ramp value 2 select
		6	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel G 0 = Ramp value 1 selected 1 = Ramp value 2 select
		5	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel F 0 = Ramp value 1 selected 1 = Ramp value 2 select

Table 17. Bank 0 – Feedin and ramp interval control registers (offset address 0003h to 0008h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		4	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel E 0 = Ramp value 1 selected 1 = Ramp value 2 select
		3	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel D 0 = Ramp value 1 selected 1 = Ramp value 2 select
		2	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel C 0 = Ramp value 1 selected 1 = Ramp value 2 select
		1	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel B 0 = Ramp value 1 selected 1 = Ramp value 2 select
		0	pcmvol_ramp_select1	R/W	0b	Select PCM volume ramp endpoint value for channel A 0 = Ramp value 1 selected 1 = Ramp value 2 select
0005h	Feedin Ramp Control	15:0	feedin_ramp_interval	R/W	0001h	Feedin ramp interval value After feedin_ramp_interval*mclk*16 cycles, the ramp values of all feedin blocks are updated with the chosen step sizes.
0006h	Feedin Ramp Control override	15:0	feedin_ramp_interval_wmode	R/W	0032h	Overrides feedin_ramp_interval when in error mode. After feedin_ramp_interval_wmode*mclk*16 cycles, the ramp values of all feedin blocks are updated with the chosen step sizes.
0007h	PCM Volume Ramp Control	15:0	pcmvol_ramp_interval	R/W	0064h	PCM ramp interval value. After pcm_ramp_interval*mclk*16 cycles, the ramp values of all PCM blocks are updated with the chosen step sizes.
0008h	PCM Volume Ramp Control override	15:0	pcmvol_ramp_interval_wmode	R/W	C350h	Overrides pcm_ramp_interval when in error mode. After pcm_ramp_interval_wmode*mclk*16 cycles, the ramp values of all PCM blocks are updated with the chosen step sizes..

8.4 Bank 0 – Serial data transmitter registers

Table 18. Bank 0 – Serial Data Transmitter registers (offset address 000Fh to 0011h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
000Fh	sdtx	15:12	reserved	R/W	0000b	-
		11	sdtx_enable	R/W	1b	Enable Serial Data Transmitter 0: Serial Data Transmitter disabled 1: Serial Data Transmitter Enabled
		10:8	sdtx_clkdiv_pow2	R/W	010b	Set the Serial Data Transmitter bit clock $bclk = \frac{mclk}{2^{sdtx\_clkdiv\_pow2}}$
		7:6	sdtx_timeslot_length	R/W	10b	Sets the number of bits per channel of the Serial Data transmitter 00: 16-bits 01: 24-bits 10: 32 bits 11: 32 bits
		5	sdtx_bclk_edge_sel	R/W	1b	Sets the clock edge on which the data is clocked out 1: Falling edge of bclk 0: Rising edge of bclk
		4	sdtx_fclk_inverted	R/W	1b	Sets frame clock polarity 0: Normal fclk 1: Inverted fclk
		3	sdtx_fclk_data_delay	R/W	1b	Sets the data delay compared to frame clock 0: No delay 1: One bit clock delay
		2:1	sdtx_set_slots	R/W	00b	Sets the number of I2S/TDM output channels 00: 2 slots 01: 4 slots 10: 8 slots 11: 8 slots
		0	sdtx_lsb_first	R/W	0b	Sets LSB/MSB first of the data in the slot 0: MSB first 1: LSB first
0010h	Serial Data Tx Channel Pointers 1	15:12	reserved	R/W	0000b	-
		11:9	sdtx_ch_pointer_3	R/W	011b	Mapping of processing channel(s)/slice(s) onto serial data channel 3 000: channel/slice A

Table 18. Bank 0 – Serial Data Transmitter registers (offset address 000Fh to 0011h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						001: channel/slice B 010: channel/slice C 011: channel/slice D 100: channel/slice E 101: channel/slice F 110: channel/slice G 111: channel/slice H
		8:6	sdtx_ch_pointer_2	R/W	001b	Mapping of processing channel(s)/slice(s) onto serial data channel 2 See sdtx_ch_pointer_3 mapping table.
		5:3	sdtx_ch_pointer_1	R/W	011b	Mapping of processing channel(s)/slice(s) onto serial data channel 1 See sdtx_ch_pointer_3 mapping table.
		2:0	sdtx_ch_pointer_0	R/W	001b	Mapping of processing channel(s)/slice(s) onto serial data channel 0 See sdtx_ch_pointer_3 mapping table.
0011h	Serial Data Tx Channel Pointers 2	15:12	reserved	R/W	0000b	-
		11:9	sdtx_ch_pointer_7	R/W	011b	Mapping of processing channel(s)/slice(s) onto serial data channel 7 000: channel/slice A 001: channel/slice B 010: channel/slice C 011: channel/slice D 100: channel/slice E 101: channel/slice F 110: channel/slice G 111: channel/slice H
		8:6	sdtx_ch_pointer_6	R/W	001b	Mapping of processing channel(s)/slice(s) onto serial data channel 6 See sdtx_ch_pointer_7 mapping table.
		5:3	sdtx_ch_pointer_5	R/W	011b	Mapping of processing channel(s)/slice(s) onto serial data channel 5 See sdtx_ch_pointer_7 mapping table.
		2:0	sdtx_ch_pointer_4	R/W	001b	Mapping of processing channel(s)/slice(s) onto serial data channel 4 See sdtx_ch_pointer_7 mapping table.

8.5 Bank 0 – Serial data receiver registers

Table 19. Bank 0 – Serial data receiver configuration registers (offset address 0012h to 0014h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0012h	Serial Data Receiver	15:10	reserved	R/W	000000b	-
		9	sdrx_enable	R/W	1b	Enable Serial Data Receiver 0: Serial Data Receiver disabled 1: Serial Data Receiver Enabled
		8:7	sdrx_timeslot_length	R/W	10b	Sets the number of bits per channel of the SD receiver 00: 16-bits 01: 24-bits 10: 32 bits 11: 32 bits
		6	sdrx_bclk_edge_sel	R/W	1b	Sets the clock edge on which the data is clocked in 1: Falling edge of bclk 0: Rising edge of bclk
		5	sdrx_fclk_inverted	R/W	1b	Sets frame clock polarity 0: Normal fclk 1: Inverted fclk
		4	sdrx_fclk_data_delay	R/W	1b	Sets the data delay compared to frame clock 0: No delay 1: One bit clock delay
		3:2	sdrx_set_slots	R/W	00b	Sets the number of I2S/TDM output channels 00: 2 slots 01: 4 slots 10: 8 slots 11: 8 slots
		1	sdrx_lsb_first	R/W	0b	Sets LSB/MSB first of the data in the slot 0: MSB first 1: LSB first
		0	sdrx_auto_hold	R/W	1b	Set data auto hold input after error 0: Do not hold input data 1: Hold input data
0013h	Serial Data Rx Channel Pointers 1	15:12	sdrx_ch_pointer_3	R/W	0001b	Mapping of serial data time slot onto processing channel/slice 3 0000: time slot 1 0001: time slot 2 0010: time slot 3

Table 19. Bank 0 – Serial data receiver configuration registers (offset address 0012h to 0014h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						0011: time slot 4 0100: time slot 5 0101: time slot 6 0110: time slot 7 0111: time slot 8 1000: time slot 9 1001: time slot 10 1010: time slot 11 1011: time slot 12 1100: time slot 13 1101: time slot 14 1110: time slot 15 1111: time slot 16
		11:8	sdrx_ch_pointer_2	R/W	0001b	Mapping of serial data time slot onto processing channel/slice 2 See sdrx_ch_pointer_3 mapping table.
		7:4	sdrx_ch_pointer_1	R/W	0000b	Mapping of serial data time slot onto processing channel/slice 1 See sdrx_ch_pointer_3 mapping table.
		3:0	sdrx_ch_pointer_0	R/W	000b	Mapping of serial data time slot onto processing channel/slice 0 See sdrx_ch_pointer_3 mapping table.
0014h	Serial Data Rx Channel Pointers 2	15:12	sdrx_ch_pointer_7	R/W	0001b	Mapping of serial data time slot onto processing channel/slice 7 0000: time slot 1 0001: time slot 2 0010: time slot 3 0011: time slot 4 0100: time slot 5 0101: time slot 6 0110: time slot 7 0111: time slot 8 1000: time slot 9 1001: time slot 10 1010: time slot 11 1011: time slot 12 1100: time slot 13 1101: time slot 14 1110: time slot 15 1111: time slot 16

Table 19. Bank 0 – Serial data receiver configuration registers (offset address 0012h to 0014h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		11:8	sdrx_ch_pointer_6	R/W	0001b	Mapping of serial data time slot onto processing channel/slice 6 See sdrx_ch_pointer_7 mapping table.
		7:4	sdrx_ch_pointer_5	R/W	0000b	Mapping of serial data time slot onto processing channel/slice 5 See sdrx_ch_pointer_7 mapping table.
		3:0	sdrx_ch_pointer_4	R/W	000b	Mapping of serial data time slot onto processing channel/slice 4 See sdrx_ch_pointer_7 mapping table.

8.6 Bank 0 – Butterfly mixer configuration registers

Table 20. Bank 0 – Butterfly mixer configuration registers (offset address 0015h to 0020h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0015h	Butterfly Mixer Element AB	15:11	reserved	R/W	00000b	-
		10:8	bfly_ab_outsel2	R/W	010b	Selects the output of the summation point in the data path B. 000: inp1 001: inp1 + inp2 010: inp1 - inp2 011: inp2 - inp1 Others: inp2
		7:5	bfly_ab_outsel1	R/W	001b	Selects the output of the summation point in the data path A. 000: inp1 001: inp1 + inp2 010: inp1 - inp2 011: inp2 - inp1 Others: inp2
		4	bfly_ab_inp2_div2	R/W	1b	Enable divide by 2 of input signal 2 0: inp2 = inp2 1: inp2 = inp2 / 2
		3	bfly_ab_inp1_div2	R/W	0b	Enable divide by 2 of input signal 1 0: inp1 = inp1 1: inp1 = inp1 / 2

Table 20. Bank 0 – Butterfly mixer configuration registers (offset address 0015h to 0020h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		2:1	bfly_ab_clipbehav	R/W	10b	Set the clip behavior of the mixer element. 00: Each data path clips separately 01: Add the remainder from clipping to the other data path 10: Subtract the remainder from clipping from the other data path 11: Each data path clips separately
		0	bfly_ab_clipatzero	R/W	1b	Set the clip behavior of the mixer element when saturated. 0: Clip the lower value at -1 1: Clip the lower value at 0
0016h	Butterfly Mixer Element CD	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
0017h	Butterfly Mixer Element EF	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
0018h	Butterfly Mixer Element GH	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
0019h	Butterfly Mixer Element AC	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB

Table 20. Bank 0 – Butterfly mixer configuration registers (offset address 0015h to 0020h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
001Ah	Butterfly Mixer Element BD	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
001Bh	Butterfly Mixer Element EG	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
001Ch	Butterfly Mixer Element FH	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
001Dh	Butterfly Mixer Element AE	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
001Eh	Butterfly Mixer Element BF	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB

Table 20. Bank 0 – Butterfly mixer configuration registers (offset address 0015h to 0020h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
001Fh	Butterfly Mixer Element CG	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB
0020h	Butterfly Mixer Element DH	15:11	reserved	R/W	00000b	See description butterfly mixer element AB
		10:8	bfly_ab_outsel2	R/W	010b	See description butterfly mixer element AB
		7:5	bfly_ab_outsel1	R/W	001b	See description butterfly mixer element AB
		4	bfly_ab_inp2_div2	R/W	1b	See description butterfly mixer element AB
		3	bfly_ab_inp1_div2	R/W	0b	See description butterfly mixer element AB
		2:1	bfly_ab_clipbehav	R/W	10b	See description butterfly mixer element AB
		0	bfly_ab_clipatzero	R/W	1b	See description butterfly mixer element AB

8.7 Bank 0 – Refgen ADC configuration register

Table 21. Bank 0 – Refgen ADC current scaling setting register (offset address 0026h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0026h	Reference Generator	15:14	reserved	R/W	00b	-
		13:8	iref_fir_value	R/W	101111b	Sets the FIRDAC current when using the bandgap reference instead of the reference loop
		7:4	reserved	R/W	1000b	-
		3:0	reserved	R/W	1000b	-

8.8 Bank 0 – Output crossbar configuration registers

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
002Fh	Crossbar bus select	15:14	bus_sel7	R/W	00b	Select signal for 8th input mux 00: PWM 01: ADC_CM 10: ADC_DM

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						11: reserved
		13:12	bus_sel6	R/W	00b	Select signal for 7th input mux See description 8th input mux
		11:10	bus_sel5	R/W	00b	Select signal for 6th input mux See description 8th input mux
		9:8	bus_sel4	R/W	00b	Select signal for 5th input mux See description 8th input mux
		7:6	bus_sel3	R/W	00b	Select signal for 4th input mux See description 8th input mux
		5:4	bus_sel2	R/W	00b	Select signal for 3rd input mux See description 8th input mux
		3:2	bus_sel1	R/W	00b	Select signal for 2nd input mux See description 8th input mux
		1:0	bus_sel0	R/W	00b	Select signal for 1st input mux See description 8th input mux
0030h	Crossbar output select 1	15	reserved	R/W	0b	-
		14:12	adc_dm1n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm1_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm1_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm1_p See adc_dm1_n_sel mapping table.
		8:6	adc_cm1_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm1_n See adc_dm1_n_sel mapping table.
		5:3	adc_cm1_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm1_p See adc_dm1_n_sel mapping table.
		2:0	out1_sel	R/W	000b	Selection of the bus index to be routed to out1

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						See adc_dm1_n_sel mapping table.
0031h	Crossbar output select 2	15	reserved	R/W	0b	-
		14:12	adc_dm2_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm2_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm2_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm2_p See adc_dm2_n_sel mapping table.
		8:6	adc_cm2_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm2_n See adc_dm2_n_sel mapping table.
		5:3	adc_cm2_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm2_p See adc_dm2_n_sel mapping table.
		2:0	out2_sel	R/W	000b	Selection of the bus index to be routed to out2 See adc_dm2_n_sel mapping table.
0032h	Crossbar output select 3	15	reserved	R/W	0b	-
		14:12	adc_dm3_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm3_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		11:9	adc_dm3_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm3_p See adc_dm3_n_sel mapping table.
		8:6	adc_cm3_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm3_n See adc_dm3_n_sel mapping table.
		5:3	adc_cm3_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm3_p See adc_dm3_n_sel mapping table.
		2:0	out3_sel	R/W	000b	Selection of the bus index to be routed to out3 See adc_dm3_n_sel mapping table.
0033h	Crossbar output select 4	15	reserved	R/W	0b	-
		14:12	adc_dm4_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm4_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm4_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm4_p See adc_dm4_n_sel mapping table.
		8:6	adc_cm4_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm4_n See adc_dm4_n_sel mapping table.
		5:3	adc_cm4_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm4_p See adc_dm4_n_sel mapping table.
		2:0	out4_sel	R/W	000b	Selection of the bus index to be routed to out4 See adc_dm4_n_sel mapping table.

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0034h	Crossbar output select 5	15	reserved	R/W	0b	-
		14:12	adc_dm5_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm5_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm5_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm5_p See adc_dm5_n_sel mapping table.
		8:6	adc_cm5_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm5_n See adc_dm5_n_sel mapping table.
		5:3	adc_cm5_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm5_p See adc_dm5_n_sel mapping table.
		2:0	out5_sel	R/W	000b	Selection of the bus index to be routed to out5 See adc_dm5_n_sel mapping table.
0035h	Crossbar output select 6	15	reserved	R/W	0b	-
		14:12	adc_dm6_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm6_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm6_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm6_p

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						See adc_dm6_n_sel mapping table.
		8:6	adc_cm6_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm6_n See adc_dm6_n_sel mapping table.
		5:3	adc_cm6_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm6_p See adc_dm6_n_sel mapping table.
		2:0	out6_sel	R/W	000b	Selection of the bus index to be routed to out6 See adc_dm6_n_sel mapping table.
0036h	Crossbar output select 7	15	reserved	R/W	0b	-
		14:12	adc_dm7_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm7_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm7_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm7_p See adc_dm7_n_sel mapping table.
		8:6	adc_cm7_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm7_n See adc_dm7_n_sel mapping table.
		5:3	adc_cm7_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm7_p See adc_dm7_n_sel mapping table.
		2:0	out7_sel	R/W	000b	Selection of the bus index to be routed to out7 See adc_dm7_n_sel mapping table.
0037h		15	reserved	R/W	0b	-

Table 22. Bank 0 - Crossbar configuration registers (offset address 002Fh to 0037h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
	Crossbar output select 8	14:12	adc_dm8_n_sel	R/W	000b	Selection of the bus index to be routed to adc_dm8_n 000: bus 0 001: bus 1 010: bus 2 011: bus 3 100: bus 4 101: bus 5 110: bus 6 111: bus 7
		11:9	adc_dm8_p_sel	R/W	000b	Selection of the bus index to be routed to adc_dm8_p See adc_dm8_n_sel mapping table.
		8:6	adc_cm8_n_sel	R/W	000b	Selection of the bus index to be routed to adc_cm8_n See adc_dm8_n_sel mapping table.
		5:3	adc_cm8_p_sel	R/W	000b	Selection of the bus index to be routed to adc_cm8_p See adc_dm8_n_sel mapping table.
		2:0	out8_sel	R/W	000b	Selection of the bus index to be routed to out8 See adc_dm8_n_sel mapping table.

8.9 Bank 0 – Power stage control registers

Table 23. Bank 0 – Expert Fault mode behavior registers (offset address 0038h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0038h	Expert Fault Mask	15:12	reserved	R/W	0000b	
		11	fault_mask	R/W	0b	Fault mask 0: Disable sticky fault mode 1: Enable sticky fault mode (stay in fault mode even if PFAULT_N goes high again)
		10	pcmvol_ramp_mask	R/W	0b	PCM ramp volume mask 1: Ramp volume down to ramp value1 (by default equal to mute) 0: Enable pcm volume ramp select according to register x bit y

Table 23. Bank 0 – Expert Fault mode behavior registers (offset address 0038h) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		9	adc_mask	R/W	0b	LLADC mask 1: Disable all ADCs 0: Enable ADCs according to register x bit y
		8	chargepump_mask	R/W	0b	Charge pump mask 1: Disable charge pump 0: Enable charge pump according to register x bit y
		7	radc_mask	R/W	0b	Reference ADC mask 1: Disable reference ADC 0: Enable reference ADC according to register x bit y
		6	reference_mask	R/W	0b	Disable the bandgap reference 1: Disable the bandgap 0: Enable the bandgap according to register x bit y
		5	feedin_ramp2_mask	R/W	0b	Feedin ramp 2 mask 1: Ramp feed-in 2 down to ramp value1 0: Enable feed-in ramp 2 select according to register x bit y
		4	feedin_ramp1_mask	R/W	0b	Feedin ramp 1 mask 1: Ramp feed-in 2 down to ramp value 1 0: Enable feed-in ramp 1 select according to register x bit y
		3	channel_pwm_mask	R/W	0b	PWM mask 1: Disable all PWM modulators 0: Enable PWM according to register x bit y
		2	chanel_filter_mask	R/W	0b	Channel filter mask 1: Disable all loop filters 0: Enable default settings according to register x bit y
		1	feedin_filter_mask	R/W	0b	Feed-in filter mask 1: Disable feed-in filter 0: Enable default settings according to register x bit y
		0	pstart_mask	R/W	0b	PSTART mask 1: Keep PSTART equal to value set in register 002h, bit 11 0: Deassert PSTART

When in Expert mode fault state, register values are propagated: When the chip was in expert mode fault state, changes to the enable registers and ramp select registers are propagated to the internal signals. This behavior makes the expert mode fault state behavior programmable (using register 038h).

8.10 Bank 0 – Status registers

Table 24. Bank 0 – Status registers (offset address 003Ch to 003Eh) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
003Ch	Status information 1	15	chflth_sign_detect	R/W	0	Sign of channel H loop filter output On read: Status On write: Set/clear IRQ
		14	chfltg_sign_detect	R/W	0	sign of channel G loop filter output On read: Status On write: Set/clear IRQ
		13	chfltf_sign_detect	R/W	0	Sign of channel F loop filter output On read: Status On write: Set/clear IRQ
		12	chflte_sign_detect	R/W	0	Sign of channel E loop filter output On read: Status On write: Set/clear IRQ
		11	chfltd_sign_detect	R/W	0	Sign of channel D loop filter output On read: Status On write: Set/clear IRQ
		10	chfltc_sign_detect	R/W	0	Sign of channel C loop filter output On read: Status On write: Set/clear IRQ
		9	chfltb_sign_detect	R/W	0	Sign of channel B loop filter output On read: Status On write: Set/clear IRQ
		8	chflta_sign_detect	R/W	0	Sign of channel A loop filter output On read: Status On write: Set/clear IRQ
		7	chflth_zero_detect	R/W	0	Zero detection of channel H loop filter On read: Status On write: Set/clear IRQ
		6	chfltg_zero_detect	R/W	0	Zero detection of channel G loop filter On read: Status On write: Set/clear IRQ
		5	chfltf_zero_detect	R/W	0	Zero detection of channel F loop filter On read: Status On write: Set/clear IRQ

Table 24. Bank 0 – Status registers (offset address 003Ch to 003Eh) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
		4	chflte_zero_detect	R/W	0	Zero detection of channel E loop filter On read: Status On write: Set/clear IRQ
		3	chfltd_zero_detect	R/W	0	Zero detection of channel D loop filter On read: Status On write: Set/clear IRQ
		2	chfltc_zero_detect	R/W	0	Zero detection of channel C loop filter On read: Status On write: Set/clear IRQ
		1	chfltb_zero_detect	R/W	0	Zero detection of channel B loop filter On read: Status On write: Set/clear IRQ
		0	chflta_zero_detect	R/W	0	Zero detection of channel A loop filter On read: Status On write: Set/clear IRQ
003Dh	Status information 2	15:14	chflth_clip_detect	R/W	00b	Pos/neg clipping detect channel H loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		13:12	chfltg_clip_detect	R/W	00b	Pos/neg clipping detect channel G loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		11:10	chfltf_clip_detect	R/W	00b	Pos/neg clipping detect channel F loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		9:8	chflte_clip_detect	R/W	00b	Pos/neg clipping detect channel E loop filter. On read: 00: No overflow

Table 24. Bank 0 – Status registers (offset address 003Ch to 003Eh) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		7:6	chfltd_clip_detect	R/W	00b	Pos/neg clipping detect channel D loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		5:4	chfltc_clip_detect	R/W	00b	Pos/neg clipping detect channel C loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		3:2	chfltb_clip_detect	R/W	00b	Pos/neg clipping detect channel B loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
		1:0	chflta_clip_detect	R/W	00b	Pos/neg clipping detect channel A loop filter. On read: 00: No overflow 01: Negative overflow 10: Positive overflow 11: Reserved On write: Set/clear IRQ
003Eh	Status information 3	15:7	reserved	R/W	00h	-
		6	pfault	R/W	0	Power stage fault. Inverse state of PFAULT_N pin On read: Status On write: Set/clear IRQ
		5	reserved	R/W	0	-
		4	pwarn	R/W	0	Power stage warning. Inverse state of PWARN_N pin

Table 24. Bank 0 – Status registers (offset address 003Ch to 003Eh) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						On read: Status On write: Set/clear IRQ
		3	reserved	R/W	0	-
		2	mute	R/W	0	Mute status. Inverse state of MUTE_N pin On read: Status On write: Set/clear IRQ
		1:0	sdrx_status	R/W	00b	Serial Data Receiver status On read: Status 00: No errors detected 01: The number of programmed bit clock cycles does not match the received amount of cycles per channel in the frame 10: The counted number of frames does not match the programmed number of frames 11: reserved On write: Set/clear IRQ

8.11 Bank 0 – Revision status registers

The AX5689 hardware and settings registers are incremented for every change. The current setting is indicated in Table 25.

Table 25. Bank 0 –Revision status register (offset address 003Fh) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
003Fh	revision information	15:8	ax5689_revision	R	C3h	revision of the AX5689
		7:0	config_revision	R	0Ah	revision of the configuration registers and its default

8.12 Bank 1 – Feed-in configuration registers

The feed-in configuration settings as listed in Table 26 are for channel A. The other channels have similar register bits, see the register map for their base addresses.

Table 26. Bank 1 – Channel A feed-in configuration registers (offset address 0000h to 000Ch) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0000h	Channel A Volume Ramp Value 1	15:0	ramp_value1	R/W	0000h	Upper limit of volume ramp 1. Unsigned fixed-point format UQ0.16
0001h	Channel A Volume Ramp Value 2	15:0	ramp_value2	R/W	0000h	Upper limit of volume ramp 2. Unsigned fixed-point format UQ0.16
0002h	Channel A Volume Ramp Step Size	15:0	stepsize	R/W	0030h	Size of ramp step. Unsigned fixed-point format UQ0.16
0003h	Channel A loop filter feed-in 1 input control	15:11	reserved	R/W	00000b	-
		10:3	offset	R/W	FAh	Offset to feed-in input. Format Q2.5
		2:0	input_select	R/W	001b	Input select between filtered/un-filtered ADC_CM, ADC_DM, PWM. 000: adc_cm un-filtered 001: adc_cm filtered 010: adc_dm un-filtered 011: adc_dm filtered 1xx: pwm
0004h	Channel A loop filter feed-in 1 Input mask 1	15:14	mask_8	R/W	10b	Set mask and invert input for feed-input 8 00: Output equals input 01: Output equals inverse of input 1x: Block input
		13:12	mask_7	R/W	00b	Set mask and invert input for feed-input 7 Please see description of input 8 above.
		11:10	mask_6	R/W	10b	Set mask and invert input for feed-input 6 Please see description of input 8 above.
		9:8	mask_5	R/W	10b	Set mask and invert input for feed-input 5 Please see description of input 8 above.
		7:6	mask_4	R/W	10b	Set mask and invert input for feed-input 4 Please see description of input 8 above.
		5:4	mask_3	R/W	10b	Set mask and invert input for feed-input 3 Please see description of input 8 above.
		3:2	mask_2	R/W	10b	Set mask and invert input for feed-input 2 Please see description of input 8 above.
		1:0	mask_1	R/W	10b	Set mask and invert input for feed-input 1 Please see description of input 8 above.

Table 26. Bank 1 – Channel A feed-in configuration registers (offset address 0000h to 000Ch) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
0005h	Channel A loop filter feed-in 1 ramp1 value 1	15:0	ramp_value1	R/W	5181h	Ramp value 1. Two's complement fixed-point format Q1.14
0006h	Channel A loop filter feed-in 1 ramp1 value 2	15:0	ramp_value2	R/W	0000h	Ramp value 2. Two's complement fixed-point format Q1.14
0007h	Channel A loop filter feed-in 1 ramp 1 step size	15:0	stepsize	R/W	0008h	Size of ramp step. Two's complement fixed-point format Q1.14
0008h	Channel A loop filter feed-in 2 input control	15:11	reserved	R/W	00000b	-
		10:3	offset	R/W	01h	Offset to feed-in input. Format Q2.5
		2:0	input_select	R/W	001b	Input select between filtered/un-filtered ADC_CM, ADC_DM, PWM. 000: adc_cm un-filtered 001: adc_cm filtered 010: adc_dm un-filtered 011: adc_dm filtered 1xx: pwm
0009h	Channel A loop filter feed-in 2 Input mask 2	15:14	mask_8	R/W	10b	Set mask and invert input for feed-input 8 00: Output equals input 01: Output equals inverse of input 1x: Block input
		13:12	mask_7	R/W	10b	Set mask and invert input for feed-input 7 Please see description of input 8 above.
		11:10	mask_6	R/W	10b	Set mask and invert input for feed-input 6 Please see description of input 8 above.
		9:8	mask_5	R/W	10b	Set mask and invert input for feed-input 5 Please see description of input 8 above.
		7:6	mask_4	R/W	10b	Set mask and invert input for feed-input 4 Please see description of input 8 above.
		5:4	mask_3	R/W	10b	Set mask and invert input for feed-input 3 Please see description of input 8 above.
		3:2	mask_2	R/W	10b	Set mask and invert input for feed-input 2 Please see description of input 8 above.
		1:0	mask_1	R/W	10b	Set mask and invert input for feed-input 1

Table 26. Bank 1 – Channel A feed-in configuration registers (offset address 0000h to 000Ch) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
						Please see description of input 8 above.
000Ah	Channel A loop filter feed-in 2 ramp 2 value 1	15:0	ramp_value1	R/W	0000h	Ramp value 1. Two's complement fixed-point format Q1.14
000Bh	Channel A loop filter feed-in 2 ramp 2 value 2	15:0	ramp_value2	R/W	0670h	Ramp value 2. Two's complement fixed-point format Q1.14
000Ch	Channel A loop filter feed-in 2 ramp 2 step size	15:0	stepsize	R/W	0001h	Size of ramp step. Two's complement fixed-point format Q1.14

8.13 Bank 1 – Loop filter configuration registers

The registers in Table 27 pertain to the programming of the coefficients in the loop filter for channel A. The other channels have similar register bits, see the register map for their base addresses.

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
000Dh	Channel A loop filter PCM coefficient Stage 1	15:0	pcm_coefficient_stage_1	R/W	0000h	Multiplying factor for input PCM to Stage 1. Two's complement fixed-point format Q1.14
000Eh	Channel A loop filter PCM coefficient Stage 2	15:0	pcm_coefficient_stage_2	R/W	0000h	Multiplying factor for input PCM to Stage 2. Two's complement fixed-point format Q1.14
000Fh	Channel A loop filter PCM coefficient Stage 3	15:0	pcm_coefficient_stage_3	R/W	0000h	Multiplying factor for input PCM to Stage 3. Two's complement fixed-point format Q1.14
0010h	Channel A loop filter PCM coefficient Stage 4	15:0	pcm_coefficient_stage_4	R/W	CA41h	Multiplying factor for input PCM to Stage 4. Two's complement fixed-point format Q1.14

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
0011h	Channel A loop filter PCM coefficient Stage 5	15:0	pcm_coefficient_stage_5	R/W	FC96h	Multiplying factor for input PCM to Stage 5. Two's complement fixed-point format Q1.14
0012h	Channel A loop filter PCM coefficient Stage 6	15:0	pcm_coefficient_stage_6	R/W	FAFFh	Multiplying factor for input PCM to Stage 6. Two's complement fixed-point format Q1.14
0013h	Channel A loop filter PCM coefficient Stage 7	15:0	pcm_coefficient_stage_7	R/W	FFC4h	Multiplying factor for input PCM to Stage 7. Two's complement fixed-point format Q1.14
0014h	Channel A loop filter feedout stage out enable	15:8	reserved	R/W	00000000b	-
		7	zoh_enable	R/W	0b	Zero order hold enable 0: disable 1: enable
		6:0	stage_out_enable	R/W	000100b	Enables for stage outputs 7 to 0.
0015h	Channel A loop filter feed-out input feed-forward coefficient	15:0	input_ff_coefficient	R/W	0000h	Feed forward coefficient. Two's complement fixed-point format Q1.14
0016h	Channel A loop filter feed-forward coefficient stage 1	15:12	reserved	R/W	0000b	-
		11:4	ff_coeff_significand	R/W	00h	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0001b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0017h	Channel A loop filter feed-back coefficient stage 1	15:12	reserved	R/W	0000b	-
		11:4	fb_coeff_significand	R/W	8Bh	Feed-back significand. Two's complement fixed-point format Q0.7

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
		3:0	fb_coeff_exponent	R/W	0101b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0018h	Channel A loop filter stage 1 MAC control	15:10	reserved	R/W	000000b	-
		9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition
0019h	Channel A loop filter feed-forward coefficient stage 2	15:12	reserved	R/W	0000b	-
		11:4	ff_coeff_significand	R/W	9Bh	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0100b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
001Ah	Channel A loop filter feed-back coefficient stage 2	15:12	reserved	R/W	0000b	-
		11:4	fb_coeff_significand	R/W	59h	Feed-back significand. Two's complement fixed-point format Q0.7
		3:0	fb_coeff_exponent	R/W	0110b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
001Bh	Channel A loop filter stage 2 MAC control	15:10	reserved	R/W	000000b	-
		9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition
001Ch	Channel A loop filter feed-forward coefficient stage 3	15:12	reserved	R/W	0000b	-
		11:4	ff_coeff_significand	R/W	A5h	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0100b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
001Dh	Channel A loop filter feed-back coefficient stage 3	15:12	reserved	R/W	0000b	-
		11:4	fb_coeff_significand	R/W	A4h	Feed-back significand. Two's complement fixed-point format Q0.7
		3:0	fb_coeff_exponent	R/W	0100b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
001Eh	Channel A loop filter stage 3 MAC control	15:10	reserved	R/W	000000b	-
		9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition
001Fh	Channel A loop filter feed-forward coefficient stage 4	15:12	reserved	R/W	0000b	-
		11:4	ff_coeff_significand	R/W	A5h	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0100b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0020h	Channel A loop filter feed-back coefficient stage 4	15:12	reserved	R/W	0000b	-
		11:4	fb_coeff_significand	R/W	A4h	Feed-back significand. Two's complement fixed-point format Q0.7
		3:0	fb_coeff_exponent	R/W	0100b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0021h	Channel A loop filter stage 4 MAC control	15:10	reserved	R/W	000000b	-
		9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition
0022h	Channel A loop filter feed-	15:12	reserved	R/W	0000b	-

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
	forward coefficient stage 5	11:4	ff_coeff_significand	R/W	A5h	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0100b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0023h	Channel A loop filter feed-back coefficient stage 5	15:12	reserved	R/W	0000b	-
		11:4	fb_coeff_significand	R/W	A4h	Feed-back significand. Two's complement fixed-point format Q0.7
		3:0	fb_coeff_exponent	R/W	0100b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0024h	Channel A loop filter stage 5 MAC control	15:10	reserved	R/W	000000b	-
		9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition
0025h	Channel A loop filter feed-forward coefficient stage 6	15:12	reserved	R/W	0000b	-
		11:4	ff_coeff_significand	R/W	A5h	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0100b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0026h		15:12	reserved	R/W	0000b	-

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
	Channel A loop filter feed-back coefficient stage 6	11:4	fb_coeff_significand	R/W	A4h	Feed-back significand. Two's complement fixed-point format Q0.7
		3:0	fb_coeff_exponent	R/W	0100b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0027h	Channel A loop filter stage 6 MAC control	15:10	reserved	R/W	000000b	-
		9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition
0028h	Channel A loop filter feed-forward coefficient stage 7	15:12	reserved	R/W	0000b	-
		11:4	ff_coeff_significand	R/W	A5h	Feed-forward significand. Two's complement fixed-point format Q0.7
		3:0	ff_coeff_exponent	R/W	0100b	Feed-forward exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
0029h	Channel A loop filter feed-back coefficient stage 7	15:12	reserved	R/W	0000b	-
		11:4	fb_coeff_significand	R/W	A4h	Feed-back significand. Two's complement fixed-point format Q0.7
		3:0	fb_coeff_exponent	R/W	0100b	Feed-back exponent UQ4.0 Exponent of radix 2. Value [0,15] maps to [1,-14]
002Ah		15:10	reserved	R/W	000000b	-

Table 27. Bank 1 – Channel A loop filter configuration registers (offset address 000Dh to 002Ah) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
	Channel A loop filter stage 7 MAC control	9	stage_enable	R/W	1b	Enable the stage. 0: Stage disabled 1: Stage enabled
		8:5	zerox_setting	R/W	0000b	Number of MSBs to be used to detect zero crossing
		4	limit_detect_enable	R/W	1b	Enable limit detection 0: ignore clip/overflow detection 1: detect overflow/clip at chosen threshold of limit setting
		3:1	limit_setting	R/W	001b	UQ3.0 representing exponent of radix 2. Register value [0,7] maps on exponent [1,-6]
		0	limit_enable	R/W	1b	0: Overflow condition 1: Clip condition

8.14 Bank 1 – PWM configuration registers

The register bits governing PWM carrier generator and comparator for Channel A are listed in Table 28. These values result in a triangular wave at 768 kHz, with amplitude ranging from 0 to 1. The other channels have similar register bits, see the register map for their base addresses.

Table 28. Bank 1 – Channel A PWM carrier configuration registers (offset address 002Bh to 0035h) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
002Bh	Channel A PWM carrier init rise	15:0	carrier_init_rise	R/W	FF80h	Start level for rising sequence of carrier signal. Two's complement fixed-point format Q1.14
002Ch	Channel A PWM carrier init fall	15:0	carrier_init_fall	R/W	4000h	Start level for falling sequence of carrier signal. Two's complement fixed-point format Q1.14
002Dh	Channel A PWM carrier threshold rise	15:0	carrier_th_rise	R/W	3F7Dh	End level for rising sequence of carrier signal. Two's complement fixed-point format Q1.14
002Eh	Channel A PWM carrier	15:0	carrier_th_fall	R/W	0003h	End level for falling sequence of carrier signal. Two's complement fixed-point format Q1.14

Table 28. Bank 1 – Channel A PWM carrier configuration registers (offset address 002Bh to 0035h) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
	threshold fall					
002Fh	Channel A PWM Step size init rise	15:0	stepsize_init_rise	R/W	020Ch	Start step size for rising sequence of carrier signal. Two's complement fixed-point format Q1.14
0030h	Channel A PWM step size delta rise	15:0	stepsize_init_fall	R/W	FDF4h	Start step size for falling sequence of carrier signal. Two's complement fixed-point format Q1.14
0031h	Channel A PWM step size delta rise	15:0	stepsize_delta_rise	R/W	0000h	Step size delta for rising sequence of carrier signal. Two's complement fixed-point format Q1.14
0032h	Channel A PWM step size delta fall	15:0	stepsize_delta_fall	R/W	0000h	Step size delta for falling sequence of carrier signal. Two's complement fixed-point format Q1.14
0033h	Channel A PWM start carrier	15:0	start_carrier	R/W	FF80h	Start value of carrier signal. Two's complement fixed-point format Q1.14
0034h	Channel A PWM start step size	15:0	start_stepsize	R/W	020Ch	Start value of carrier step size signal. Two's complement fixed-point format Q1.14
0035h	Channel A PWM control	15:5	reserved	R/W	00000000000b	-
		4	carrier_init_enable	R/W	1b	Carrier init enable 0: Only stepsize_reg is set when threshold value is passed, carrier_reg value is unchanged 1: Both carrier_reg and stepsize_reg are set to appropriate set value when threshold value is passed
		3	force_pwm	R/W	1b	Ensures each carrier rising and falling slope can only result in one PWM transition. 0: PWM output can change multiple times per carrier slope. 1: The PWM output can change only once per carrier slope.
		2	out_inv	R/W	0b	Invert output 0: PWM output not inverted 1: PWM output inverted
		1	carrier_inject	R/W	1b	0: Subtract start_pwm from input 1: Subtract carrier from input

Table 28. Bank 1 – Channel A PWM carrier configuration registers (offset address 002Bh to 0035h) bit description

Offset Address	Register	Bit	Symbol	Access	Value	Description
		0	start_rise	R/W	1b	Start direction of carrier signal 0: Start with rising sequence 1: Start with falling sequence

8.15 Bank 1 – LLADC configuration registers

The configuration register bits for LLADC A are listed in Table 29. The other channels have similar register bits, see the register map for their base addresses.

Table 29. Bank 1 – Channel A LLADC configuration register (offset address 003Bh) bit description

Offset address	Register	Bit	Symbol	Access	Value	Description
003Bh	Channel A ADC analog | ADC analog 1	15:6	reserved	R/W	0000000000b	-
		5:0	fir_cur_ratio	R/W	011010b	Set the ratio between CM and DM current

Figure 33. Application diagram

9 Ordering information

Table 30. Ordering information

Device	Package	Moisture level Sensitivity	Peak soldering Temperature
AX5689GRK	QFN-64 (9mmx9mm)	MSL3	260 ˚C

10 Package outline AX5689GRK

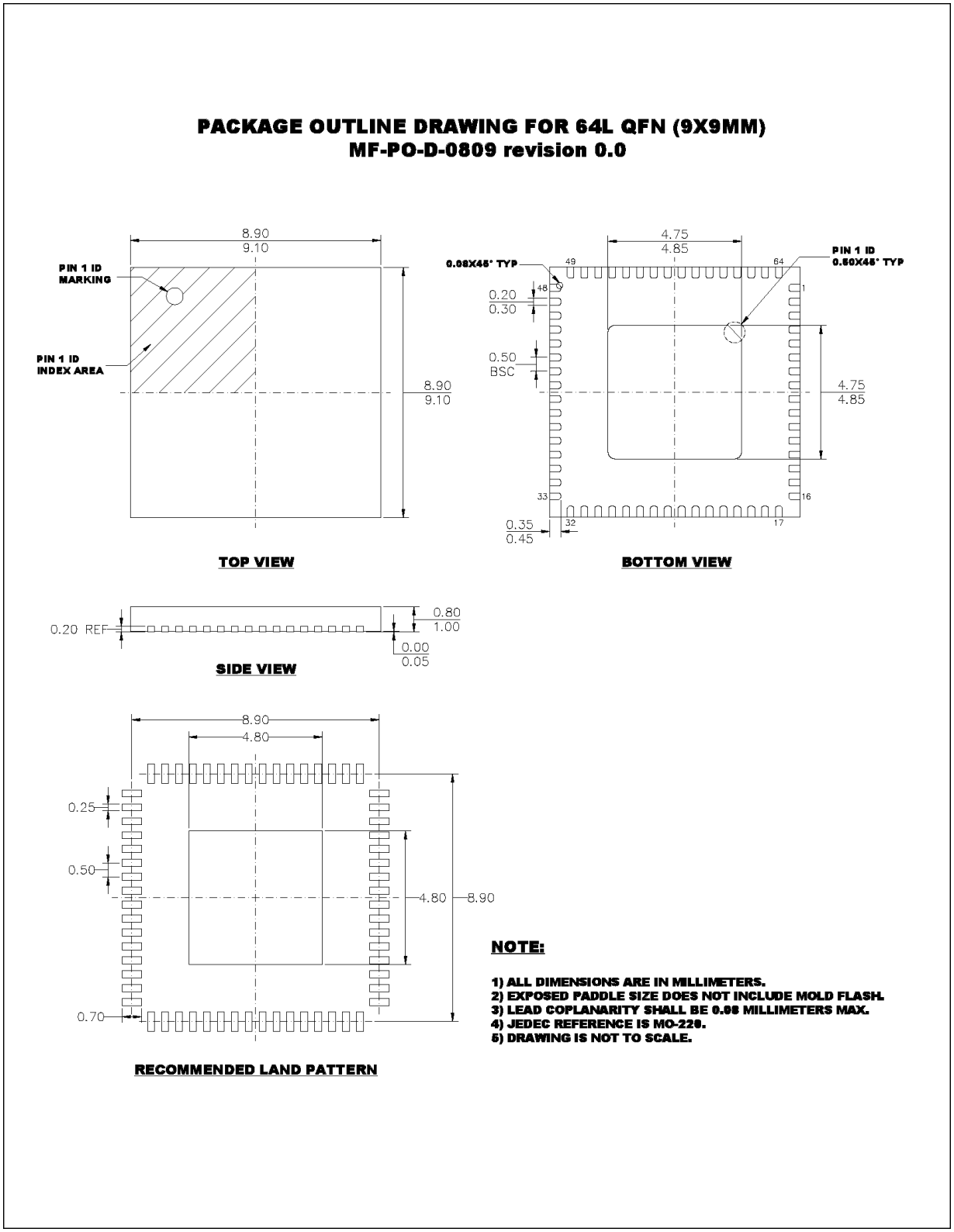


Figure 34. Package diagram AX5689GRK

11 Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
AX5689 r1.2	20240202	Product Datasheet	-	AX5689N2 v1.1
	• Updated part number, headers, and footers on all pages • Added notices on page 1 and 78 • Updated sdtx_bclk_edge_sel (1 is falling edge) in Table 18, register 000Fh, bit[5] on page 45 • Updated sdrx_bclk_edge_sel (1 is falling edge) in Table 19, register 0012h, bit[6] on page 47 • Updated Q2.14 to UQ0.16 and "two's complement" to "unsigned" in Table 26, registers 0000h, 0001h, 0002h on page 64 • Updated Q3.5 to Q2.5 in registers 0003h and 0008h (bits[10:3] for all registers) on pages 64–65 • Updated Q2.14 to Q1.14 in Table 26, registers 0005h, 0006h, 0007h, 000Ah, 000Bh, 000Ch; Table 27, registers 000Dh, 000Eh, 000Fh, 0010h, 0011h, 0012h, 0013h, 0015h; Table 28, registers 002Bh, 002Ch, 002Dh, 002Eh, 002Fh, 0030h, 0031h, 0032h, 0033h, 0034h on pages 65–67, 73–74 • Updated Q1.7 to Q0.7 in Table 27, registers 0016h, 0017h, 0019h, 001Ah, 001Ch, 001Dh, 001Fh, 0020h, 0022h, 0023h, 0025h, 0026h, 0028h, 0029h (bits[11:4] for all registers) on pages 67–72 • Updated UFIX4.0 to UQ4.0 in Table 27, registers 0016h, 0017h, 0019h, 001Ah, 001Ch, 001Dh, 001Fh, 0020h, 0022h, 0023h, 0025h, 0026h, 0028h, 0029h (bits[3:0] for all registers) on pages 67–72 • Updated UFIX3.0 to UQ3.0 in Table 27, registers 0018h, 001Bh, 001Eh, 0021h, 0024h, 0027h, 002Ah (bits[3:1] for all registers) on pages 68–73 • Updated Ordering Information and Package Outline sections on pages 76–77 • Removed Legal Notice and Contact Information sections		
AX5689N2 v1.1	20230516	Product Datasheet	-	AX5689N2 v1.1
	• Package outline drawing fix			
AX5689N2_v1.0	20221114	Product data sheet	-	AX5689N2_v0.6