CAPACITOR BASICS V – Performance Characteristics

The following Application Note defines the various characteristics that affect performance of the capacitor. Information provided here will give the reader an appreciation for how a capacitor may behave when operated within their intended operating environment. Topics covered include:

Capacitor Properties

Equivalent Circuit – Although we often talk about capacitors in simple terms which imply that their only measurable characteristic is capacitance, they are in fact much more complex components exhibiting both resistive and inductive properties. A simplified schematic that outlines the equivalent circuit for a capacitor is shown in figure I:

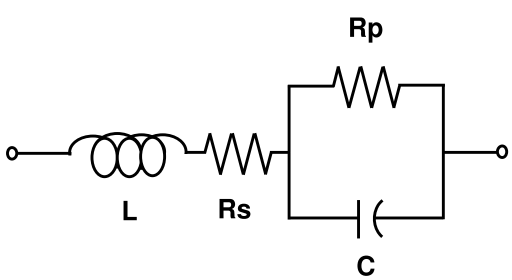

Figure I

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Equivalent Series Resistance (ESR) – ESR is a parameter that defines in simplified terms, all of the series and parallel resistive losses of a capacitor. Expressed as a basic R-C series circuit, it is the sum of the resistance of the electrodes, the termination, any leads that may be used to connect to the capacitor and losses within the dielectric itself. See figure II.

Figure II

Levels of ESR are considered to be extremely critical and often dictate the type of capacitor chosen for certain applications. Lower losses for example will provide for increased efficiency and higher power output, which might otherwise be lost as heat. Ceramic capacitors in particular exhibit extremely low levels of ESR when compared to electrolytic or tantalum capacitors. This can be especially critical for higher frequency applications and selection of a ceramic capacitor may allow the design engineer to utilize a lower capacitance value than might otherwise be required with alternative high loss systems.

Dissipation Factor (DF) - Dissipation Factor or Loss Tangent is a measurement that quantifies the efficiency of a capacitor as it relates to energy losses. For an ideal capacitor operated in an AC circuit, the voltage and current are defined as being 90ºC out of phase with each other. In actuality, a capacitor is not a perfect component where the resistivity of the dielectric material is considered infinite and as a result, there is a lag associated with polarization within the dielectric causing the actual current to be out of phase. This angle is referred to as the Loss Tangent (Tan δ) or Dissipation Factor. See figure III.

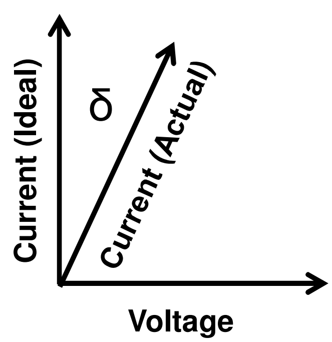

Figure III: Loss Tangent for Practical Capacitor

Polarization is a material property and in practice, higher levels of polarization are generally associated with higher dielectric constants. Consequently, highly stable, low K dielectric materials like NPO (COG) exhibit lower DF values in the range of 0.15% whereas, higher K materials like X7R may exhibit DF readings in the 2 to 2.5% range.

As ESR also contributes to losses within the capacitor, there is a proportional relationship between DF and ESR that can be expressed by the following formula:

$$\mathbf{DF} = \frac{\mathbf{ESR}}{X_C}, \text{ where } X_C \text{ (Capacitive Reactance)} = \frac{1}{2\pi f C}$$

Dissipation factor is typically expressed as a percentage and industry standard procedures specify measurements be taken at specific frequencies, with 1 kHz and 1 MHz being the most commonly used for ceramic capacitors. Generally speaking, measurement frequency is set at 1 MHz for capacitors measuring 100 pF or less and at 1 kHz for all other values.

Quality Factor (Q) – Similar to Dissipation Factor, Quality Factor or Q, is also a measurement that defines in terms of energy losses, the efficiency with which a capacitor performs. Engineers tend to use either DF or Q to define a capacitor's operating efficiency, with Q being the more common term associated with higher frequency RF applications.

To reduce high frequency losses it is important to utilize a capacitor that has a low value of ESR and DF which correlates to a higher value for Q.

In mathematical terms, the relationship between Quality factor and Dissipation Factor is quite simple. Q is the reciprocal of DF and as such measurements for an ideal capacitor would have an infinite value for Q and a null value for DF, as no energy would be lost while the device is charged.

$$Q = \frac{1}{DF}$$

Of course, capacitors are not perfect and if their inherent ESR / DF characteristics are too high to begin with, there can be a critical loss in performance, especially at higher frequencies. Consequently, it becomes of crucial importance that the design engineer select a capacitor that exhibits low ESR and DF, thereby achieving the high Quality Factor values necessary for RF applications.

Equivalent Series Inductance (ESL) – Equivalent Series Inductance is the parasitic feature of a capacitor attributed to the physical characteristics of the device. It is influenced by such things as the length and thickness of the capacitor electrode and can be of critical importance in those applications like microprocessors, where higher levels of parasitic inductance can result in unintended voltage spikes, which may compromise the devices intended response.

Impedance (Z) – The impedance of a capacitor defines the opposition or resistance to current flow that takes place within the capacitor when voltage is applied. When that potential is a DC voltage than the impedance of the circuit is purely resistive, but when an AC voltage is applied, the circuit becomes much more complex, and requires that reactance also be taken into consideration. Reactance is defined as having both magnitude and phase and as such the formula for Impedance is expressed as the square root of the sum of the ESR and the Reactance of the device.

$$Z = \sqrt{ESR^2 + X^2}$$

Reactance within a capacitor is made up of both capacitive (X_C) and inductive elements (X_L) and occurs due to the electrostatic charging mechanism between dielectric layers and the fluctuating magnetic field, which induces an oscillating current level within the capacitor's inductive components. Breaking down X into its more basic components, Impedance can be defined using the following formula.

$$Z = \sqrt{ESR^2 + (X_C - X_L)^2}$$

Taking this a step further, Capacitive and Inductive reactance are expressed by the following formulas:

$$X_C = \frac{1}{2\pi fC} \qquad X_L = 2\pi fL$$

Where f = Operating frequency

From these two formulas it can be seen that as the frequency of operation (f) increases, the magnitude of the X_C component becomes smaller and the magnitude of the X_L component becomes larger. Of important consideration is the frequency at which X_C equals X_L. At this frequency, which is referred to as the self-resonant frequency (f_r) of the capacitor, the X_C and X_L levels are at their minimums and the impedance of the circuit is essentially equal to the ESR of the device. The resonant frequency for any capacitor design can be determined using the following formula:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

It should also be pointed out that at lower frequencies, below self-resonance, that the X_C component is dominant and that the capacitor behaves like a capacitor, but that as the frequency of operation is increased above the resonant point, the X_L component dominates and the capacitor behaves more like an inductor. The relationship between Z, XC, XL and ESR is shown in Figure IV:

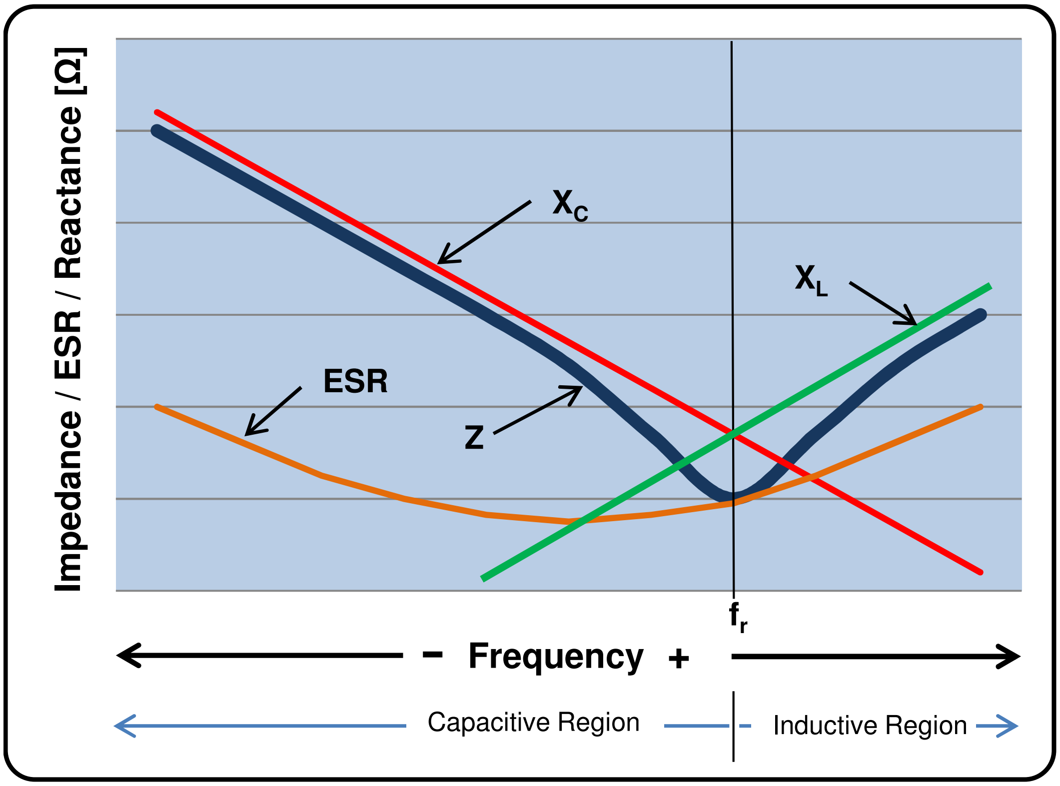

Figure IV – Impedance / ESR / Reactance

Insulation Resistance (IR) - Insulation Resistance is the electrical characteristic of a capacitor that quantifies its ability to resist the flow of DC leakage current when under bias. Represented by Rp in figure 1, this property is largely dependent on the resistivity (*p*) of both the dielectric material and the capacitor surface. The insulative properties of the dielectric are dependent on the material formulation, which in theory should be infinite, but in actuality displays a limited value due to impurities and microstructural defects within the materials atomic lattice structure. In addition, improper firing, surface conditions and test temperature can also affect the actual level of insulation resistance.

The amount of insulation resistance that can be achieved is influenced primarily by ionic imbalances in the ceramic crystal structure which create charge carriers that become mobilized in the presence of an electric field. Increased numbers of mobile charger carriers result in leakage current paths that can degrade the overall IR performance. The level of leakage current detected can be further increased with temperature, as this added thermal energy helps to overcome the energy barriers for diffusion.

From a statistical perspective, the presence of these anomalies is found to be directly proportional to the volume of the capacitor and the complexity of its design. One can conclude therefore that capacitors, which utilize larger and / or more numerous electrode layers, will exhibit a lower bulk resistivity and corresponding insulation resistance than a smaller device.

Although comprised of the same dielectric material, the surface of the capacitor may possess a different resistivity than the bulk material. The presence of moisture or surface impurities like flux and salts can adversely affect IR and care should always be taken during processing to ensure that the capacitor surface is properly cleaned to remove these contaminants.

Test methods may vary, depending on the type and rating of the capacitor, but generally speaking for ceramic capacitors, a potential equal to the voltage rating of the DUT or 500 Vdc, whichever is less, is applied across opposing terminals and a DC resistance measurement is taken after two (2) minutes of electrification. Charging times can be reduced to facilitate throughput, but the time chosen needs to be sufficient inasmuch as it allows the product to meet predefined minimums for IR.

Given the established relationship that exists between the capacitance value and the intrinsic resistivity of the dielectric material, it follows that the insulation resistance of the device is inversely proportional to the measured capacitance value. Consequently, IR limits are usually specified as the “RC product” of the capacitor and EIA standards / MIL specifications typically require that the RC product exceed 1000 MegOhm – MicroFarad (MΩ - µF) at +25ºC and 100 MegOhm – MicroFarad (MΩ - µF) at +125ºC.

Confusing as written, but simple in practice, establishing limits requires a straight forward calculation, whereby the required RC product is divided by the capacitance value for the DUT. The following calculation illustrates the means by which the minimum insulation resistance of a 0.12 µF capacitor can be determined when tested at +25ºC and +125°C for an electrification time of 2 minutes.

IR @ +25ºC = 1000 MΩ – µF

- For capacitance value of 0.10 µF the minimum IR at 2 minutes would be:

$$\text{IR (Ohms) @ +25°C} = \frac{\text{1000 Ohm} \cdot \text{Farads}}{\text{C (Farads)}} = \frac{\text{1000 Ohm} \cancel{\cdot \text{Farads}}}{0.010 \times 10^{-6} \cancel{\text{Farads}}}$$

$$= \frac{\text{1000 Ohms}}{0.010 \times 10^{-6}} = \text{100,000,000,000 Ohms}$$

IR @ +125ºC = 100 MΩ – µF

- For capacitance value of 0.10 µF the minimum +125°C IR at 2 minutes would be:

$$\text{IR (Ohms) @ +125°C} = \frac{\text{100 Ohm} \cdot \text{Farads}}{\text{C (Farads)}} = \frac{\text{100 Ohm} \cdot \cancel{\text{Farads}}}{0.010 \times 10^{-6} \cancel{\text{Farads}}}$$

$$= \frac{\text{100 Ohms}}{0.010 \times 10^{-6}} = \text{10,000,000,000 Ohms}$$

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As can be seen from the above calculation, ceramic capacitors generally exhibit extremely high levels of insulation resistance. Consequently, IR minimums are usually based on Megohm – Microfarad limits and subsequent measurements are generally reported in multiples of the Ohm:

100,000,000,000 Ohms (Ω) = 100,000 Mega Ohms (MΩ) = 100 Giga Ohms (GΩ) = 100 Kilo Mega Ohms (kMΩ)

10,000,000,000 Ohms (Ω) = 10,000 Mega Ohms (MΩ) = 10 Giga Ohms (GΩ) = 10 Kilo Mega Ohms (kMΩ)

In practical terms, the maximum value for insulation resistance is usually capped at 100 GΩ or 100 kMΩ at +25ºC and 10 GΩ or 10 kMΩ at +125ºC. Higher value measurements are certainly achievable but their precision comes into question due to the accuracy of the equipment and losses in the fixturing being utilized. Table I provides the required IR limits for typical EIA standard capacitance values at +25 and +125ºC.

Capacitance (µF)	Insulation Resistance (GΩ)		Capacitance (µF)	Insulation Resistance (GΩ)		Capacitance (µF)	Insulation Resistance (GΩ)	
	+25ºC	+125ºC		+25ºC	+125ºC		+25ºC	+125ºC
≤ 0.010	100.00	10.00	0.25	4.000	0.400	5.6	0.179	0.018
0.012	83.33	8.33	0.27	3.704	0.370	6.8	0.147	0.015
0.015	66.67	6.67	0.33	3.030	0.303	8.2	0.122	0.012
0.018	55.56	5.56	0.39	2.564	0.256	10	0.100	0.0100
0.022	45.45	4.55	0.47	2.128	0.213	12	0.083	0.0083
0.025	40.00	4.00	0.56	1.786	0.179	15	0.067	0.0067
0.027	37.04	3.70	0.67	1.493	0.149	18	0.056	0.0056
0.033	30.30	3.03	0.82	1.220	0.122	22	0.045	0.0045
0.039	25.64	2.56	1	1.000	0.100	25	0.040	0.0040
0.047	21.28	2.13	1.2	0.833	0.083	27	0.037	0.0037
0.056	17.86	1.79	1.5	0.667	0.067	33	0.030	0.0030
0.068	14.71	1.47	1.8	0.556	0.056	39	0.026	0.0026
0.082	12.20	1.22	2.2	0.455	0.045	47	0.021	0.0021
0.1	10.00	1.000	2.5	0.400	0.040	56	0.018	0.0018
0.12	8.333	0.833	2.7	0.370	0.037	68	0.015	0.0015
0.15	6.667	0.667	3.3	0.303	0.030	82	0.012	0.0012
0.18	5.556	0.556	3.9	0.256	0.026	100	0.010	0.0010
0.22	4.545	0.455	4.7	0.213	0.021	120	0.008	0.0008

Table I – Minimum IR Standards Vs Capacitance

Working Voltage - Working voltage defines the operational limit for a specific capacitor design. It quantifies the maximum voltage at which a capacitor can be safely charged.

For ceramic capacitors, working voltage limits are intended to apply across their entire operating range. Other capacitor technologies are often dual rated and generally require a de-rating from their name plate voltage as their operating temperature is increased. Polypropylene film capacitors for example, are limited to 50% of their +85°C voltage rating when operated at their maximum limit of +105°C and tantalum capacitors are limited by as much as a 67% de-rating when operated at +125°C.

Dielectric Strength – Expressed in volts per mil (volts per 0.001") or volts per cm of dielectric, Dielectric Strength defines the ability of a capacitor to withstand an increasing level of voltage without electrical breakdown. Like a balloon, the amount of pressure or energy that a capacitor can hold is not limitless. If one were to apply too much pressure to the balloon, the wall would eventually rupture and the balloon would no longer be able to maintain a functional level of air pressure. Similarly, if higher and higher voltage levels are applied to a capacitor, the resulting electric field will reach a point where the energy generated is enough to permanently breakdown the dielectric material and the device will no longer be able to store energy.

It is important to recognize that like Insulation Resistance, Dielectric Strength is also temperature dependent, with material limits decreasing as the temperature is increased. Although fluctuations in ambient operating temperature would be the most obvious reason for performance change, it should also be noted that high voltage stress itself can have an impact, as it can create heat due to losses in the dielectric material. This increase in temperature will lower the resistivity of the material and over time a localized high current leakage path and subsequent breakdown may result at the most vulnerable point in the dielectric.

Aging – Ceramic capacitors made with Class II, ferroelectric materials like X7R, exhibit a loss in capacitance with time. Known as "Aging", this condition occurs when the capacitor transitions from a point above its Curie temperature (≈ +120℃), to a point below, causing the crystal structure of the material to relax and change from a cubic to a tetragonal symmetry.

The rate at which aging occurs can be influenced by several factors including material composition, purity, grain size and structure, as well as process conditions during firing and voltage conditioning. The higher the dielectric constant of the material, the more pronounced the Aging rate with X7R for example exhibiting a more stable response than Y5V or Z5U materials. Class I dielectrics, which have very low dielectric constants, do not exhibit aging and their capacitance values remain extremely stable over time, even when subjected to changes in temperature and / or when exposed to voltage bias.

Capacitance loss due to aging is time dependent, although the degree to which the capacitance drops becomes much less pronounced the longer the part is below the Curie temperature. This relationship between capacitance loss Vs time is logarithmic in nature and is stipulated in percentage per decade hour. This means that the loss in capacitance as a percentage will be the same when measured at 10, 100, 1000 and 10,000 hours after the device has last transitioned below its Curie temperature.

When plotted on semi-log paper, the decay approximates a straight line and is therefore predictable. This Aging curve can be very valuable when manufacturing capacitors as it allows the engineer to provide a design margin for capacitance that accounts for the anticipated loss in capacitance. If for example, the engineer is using X7R dielectric with an Aging rate of 2.5% per decade hour, the part can be designed so that the minimum capacitance value measured at 1000 hours will be at least 2.5% above the specified minimum requirement. From a testing perspective, elapsed time until test is more often in the 100 hour range, so testing limits are set to allow for two decades of time, or a 5% loss in capacitance, thereby ensuring that the capacitor will still be within specification limits at 10,000 hours, or roughly one year after delivery.

Inasmuch as Aging for ferroelectric formulations is unavoidable and an inherent characteristic of these dielectric materials, it should be pointed out that the loss in capacitance can be reversed by heating the capacitor above it Curie temperature and reverting the crystalline structure back to its original cubic state. This situation may occur for example during the end users installation process and the operator needs to be aware that they may encounter inconsistent measurements during capacitance testing, especially if the part were to be tested a short time after exposure. Of course, the Aging mechanism will recommence once the part is allowed to cool, following the same predictable path for capacitance loss seen during its previous Aging sequence.

Temperature Coefficient of Capacitance (TCC) - TCC or ΔTC, defines the maximum amount by which a capacitance value measured at the reference temperature of +25°C can vary when that same capacitor is subjected to changes in operating temperature. This parameter is dependent upon specific dielectric types.

Class I Dielectrics – Referred to as Temperature Compensating dielectrics, these materials are very stable with changes in temperature. EIA-198 provides a summary of the more common Class I dielectrics by outlining the anticipated change in temperature for these materials over an established maximum and minimum operating temperature. See Table II below.

EIA-198 TC CODES FOR CLASS I CERAMIC DIELECTRICS					
Alpha Symbol	Significant Figure of Temperature Coefficient of Capacitance ppm / °C	Numerical Symbol	Multiplier Applied to Signficant Figure	Alpha Symbol	Tolerance of Temperature Coefficient ±ppm / °C
C	0.0	0	-1	G	30
B	0.3	1	-10	H	60
U	0.8	2	-100	J	120
A	0.9	3	-1000	K	250
M	1.0	4	-10000	L	500
P	1.5	5	+1	M	1000
R	2.2	6	+10	N	2500
S	3.3	7	+100		
T	4.7	8	+1000		
U	7.5	9	+10000		

Table II – EIA-198, Class I ΔTC Designations

Class I dielectrics express ΔTC as a linear curve in ppm/°C (parts per million per degrees Centigrade). Expected shifts in capacitance can be calculated by multiplying the capacitance value at the +25°C by the shift in temperature above or below this reference point and dividing that value by 1,000,000.

Example: For a COG (NPO) capacitor with a measured capacitance of 1000 pF at +25°C, what would be the maximum change in effective capacitance if the actual operating temperature were -55, -0, +85 or +125°C.

$$\Delta \text{ Capacitance @ Operating Temperature} = \frac{\text{Capacitance Value @ +25°C x TCC x }\Delta T}{1{,}000{,}000}$$

$$\Delta \text{ Capacitance @ -55°C} = \frac{1000 \text{ pF x } 30 \text{ x } 80}{1{,}000{,}000} = \pm 2.4 \text{ pF}$$

$$\Delta \text{ Capacitance @ 0°C} = \frac{1000 \text{ pF x } 30 \text{ x } 25}{1{,}000{,}000} = \pm 0.75 \text{ pF}$$

$$\Delta \text{ Capacitance @ 85°C} = \frac{1000 \text{ pF x } 30 \text{ x } 60}{1{,}000{,}000} = \pm 1.8 \text{ pF}$$

$$\Delta \text{ Capacitance @ 125°C} = \frac{1000 \text{ pF x } 30 \text{ x } 100}{1{,}000{,}000} = \pm 3.0 \text{ pF}$$

From the above calculations it has been determined that a COG (NPO) capacitor that measures 1000 pF at +25°C will measure between 997.6 pF & 1002.4 pF at -55°C, 999.25 pF & 1000.75 pF at 0°C, 998.2 pF & 1001.8 pF at +85°C and 997 pF and 1003 pF at +125°C.

Class II Dielectrics – Dielectric materials that are identified by this classification exhibit stable performance, but certainly not to the same degree as Class I dielectrics. EIA-198 also provides a table that identifies the standard designations for Class II Dielectrics. See Table III.

EIA-198 TC CODES FOR CLASS II & III CERAMIC DIELECTRICS					
Alpha Symbol	Low Temperature °C	Numeric Symbol	High Temperature °C	Alpha Symbol	Max Cap Change Over Temp Range %
Z	+10	2	+45	A	±1.0
Y	-30	4	+65	B	±1.5
X	-55	5	+85	C	±2.2
		6	+105	D	±3.3
		7	+125	E	±4.7
		8	+150	F	±7.5
		9	+200	P	±10
				R	±15
				S	±22
				T	+22 to -33
				U	+22 to -56
				V	+22 to - 82

Table III – EIA-198 Class II & III ΔTC Designations

Class II dielectrics exhibit a non-linear ΔTC response, expressed as the maximum possible percentage change that can occur in the +25°C capacitance value, when the subject capacitor is exposed to shifts from the reference temperature to some other point within the materials defined operating temperature range. An X7R dielectric for example is defined as having a maximum ΔTC of ±15% across the operating temperature range of -55 to +125°C. When compared with the 1000 pF, Class I, COG (NPO) capacitor that exhibits a worst case shift in capacitance of -2.4 pF (997.6 pF minimum) at -55°C and +3 pF (1003 pF maximum) at +125°C, a 1000 pF capacitor manufactured with Class II, X7R dielectric can exhibit a worst case shift in capacitance of ± 150 pF or somewhere between 850 and 1150 pF at any point across minimum to maximum operating temperature range.

Voltage Coefficient of Capacitance (VCC) - VCC or ΔVC is a functional characteristic that quantifies the maximum change in capacitance that one might expect to see when the capacitor is exposed to various voltage levels. Capacitance testing is typically performed at 1± 0.2 VRMS, which is extremely low in comparison to the typical working voltages encountered during actual operating conditions. At this test voltage, the effect on capacitance is negligible, but for certain dielectric types like those defined by EIA-198, Class II materials, exposure to higher DC operating voltages can result in a significant loss in effective capacitance.

In very simple terms, dielectrics manufactured with Class I formulations show little sensitivity to AC or DC voltage. Class II ferroelectric bodies on the other hand, exhibit a shift in their dielectric constant when exposed to these same AC and DC voltages and this can result in a rather significant capacitance variation from their original test value. The amount of change is dependent on the type of dielectric material being used and the level of voltage stress applied across the dielectric. Higher K dielectrics tend to exhibit the largest shift in ΔVC and in worst case situations, these capacitors can exhibit as much as a 60 to 65% loss, or more.

When exposed to AC voltage, Class II dielectrics exhibit an increase in dielectric constant (K) and a subsequent increase in capacitance. As the AC voltage is increased, the K value increases, with higher K dielectrics exhibiting the largest swing. This positive shift continues until a material specific voltage limit is reached, at which point the trend reverses and the dielectric constant / capacitance value starts to decline.

When exposed to DC bias, Class II dielectrics tend to exhibit a decrease in dielectric constant, with again, the higher K dielectrics again exhibiting the largest shift. The amount of voltage applied can also impact the amount of capacitance lost, but it is important to understand that relationship between voltage and capacitance has less to do with voltage level and much more to do with the dielectric thickness and the resulting volts per mil stress applied. Essentially, two capacitors with identical capacitance values and voltage ratings, manufactured with the same dielectric material can, depending on their internal construction, exhibit totally different capacitance values when biased at the same working voltage. One can't assume therefore that a 1 µF, 100 VDC, X7R capacitor purchased from Vendor A will behave exactly the same as a 1 µF, 100 VDC, X7R capacitor purchased from Vendor B.

Example: Two capacitor manufactures produce 1.0 µF, 100 VDC capacitors using the same X7R dielectric formulation. Vendor A designs the part with a dielectric thickness of 1.5 mils, while Vendor B designs their alternative design with a dielectric thickness of 1.0 mils. If both designs are subjected to the full maximum operating voltage of 100 VDC, what would be the resulting ΔVC for both designs?

$$\text{Voltage Stress} = \frac{\text{Operating Voltage}}{\text{Dielectric Thickness}}$$

Vendor A

Voltage Stress $= \frac{100\ \text{Vdc}}{1.5\ \text{mils}}$

= 66.67 volts / mil

Voltage Coefficient = -38%
(From Figure VI)

Actual Capacitance = 1.0 µF x (1 - 0.38)
(@ 100 Vdc)

= **0.62 µF**

Vendor B

Voltage Stress $= \frac{100\ \text{Vdc}}{1.0\ \text{mils}}$

= 100 volts / mil

Voltage Coefficient = -65%
(From Figure VI)

Actual Capacitance = 1.0 µF x (1 - 0.65)
(@ 100 Vdc)

= **0.35 µF**

Voltage – Temperature Coefficient of Capacitance (VTC) - It is important to recognize that ΔTC and ΔVC are in fact additive components and that a change in both operating temperature and working voltage or combinations thereof, will have a cumulative effect on the overall performance of the capacitor. As an example, let's re-examine the 1.0 µF,100 Vdc, X7R capacitor from the previous section that was manufactured with 1.0 mil dielectric. We know that for elevated levels in WVDC there will be a loss in capacitance and that at 100 V/mil the ΔVC for this particular capacitor will be -65%. If we now consider that the actual operating temperature is something other than +25°C and that at this temperature the ΔTC is -15%, then we need to recognize that the overall loss in capacitance or ΔVTC, can be as much as -80%.

Military specifications like MIL-PRF-49467 have evened the playing field for suppliers inasmuch as they have defined a series of dielectric subcategories that limit the amount of capacitance loss that a capacitor can exhibit due to changes in both temperature and voltage. This is most often done by utilizing an X7R formulation with a ΔTC that is well within the allowable ±15% and limiting the ΔVC through a reduction in the volts per mil stress across the dielectric. BX is one such dielectric where the maximum ΔVTC is defined as +15 / -25% across the entire operating temperature range of -55 to +125°C. Other options and their corresponding ΔVTC limits are listed in Table IV.

Military Symbol	Voltage - Temperature Coefficient
BX	+15 / -25% @ WVDC & -55 to +125°C
BR	+15 / -25% @ WVDC & -55 to +125°C
BZ	+15 / -25% @ WVDC & -55 to +125°C
BQ	+15 / -25% @ WVDC & -55 to +125°C

Table IV - Capacitance Change With Respect to +25°C

Military specifications have also established a means for testing the VTC performance of a ceramic capacitor. This is done by measuring capacitance at different temperatures, both with and without an applied working voltage and comparing those values to a baseline or reference measurement, which is established at +25℃ and 1 VRMS. See Table V.

Step	Voltage, DC	Temperature ℃
A	None	+25℃ ± 2℃
B	None	-55℃ ± 2℃
C (Ref)	None	+25℃ ± 2℃
D	None	+125℃ ± 2℃
E	Rated	+125℃ ± 2℃
F	Rated	+25℃ ± 2℃
G	Rated	-55℃ ± 2℃

Table V - Capacitance Change With Respect to +25℃ & WVDC

Dielectric Absorption – When discharged, it would seem only natural to assume that a capacitor if measured, would exhibit zero capacitance or residual charge across its terminals. This would in fact be a correct assumption if the device were an ideal capacitor, but in reality capacitors, especially those manufactured with higher K dielectric bodies, are characterized by a condition where a residual charge may persist within the capacitor for a long period of time after discharge. This condition, which is known as dielectric absorption, is expressed as the percent ratio of residual voltage to the initial charging voltage.

Certainly care needs to be taken when handling any capacitor and as a precautionary measure, higher capacitance value devices are often provided with shorting bars or bleed resistors.

Piezoelectric materials / Electro-Mechanical Coupling – Those dielectrics defined as being piezoelectric in nature are characterized by a crystal lattice structure that lacks a center of symmetry. When subjected to an electric field, the piezoelectric effect results in a realignment of ions within the crystal lattice and a subsequent physical distortion of the device, with the level of distortion directly related to amplitude of the electric field. If the applied voltage is AC, the fluctuation in field strength and resulting distortion may in fact result in an audible noise, which may become further amplified once the capacitor is mounted to a circuit board.

Ferroelectric, barium titanate dielectrics, which are commonly used in the manufacture of Class II and Class III capacitors, lack a center of symmetry at temperatures below their Curie point and as such, these capacitors are piezoelectric in nature. If heated to a temperature above the Curie point, the crystal structure of these dielectrics changes to a cubic configuration, which possesses a center of symmetry which makes them no longer susceptible to electro-mechanical distortion.

Piezoelectric dielectrics, especially those manufactured with lead zirconium titanate (PZT) are utilized in Transducer and Actuator applications, but in those instances where the piezoelectric response may adversely affect the performance of the system, the design engineer may need to consider an alternative approach. Class I dielectrics like NPO (COG), utilize non-ferroelectric formulations and consequently they do not exhibit this property. Where a low K alternative is not an option, consideration may need to be given to a special packaging approach that dampens the noise, or to an alternative capacitor technology.

For additional information on Capacitor Basics, please refer to our other Application Notes, which are available on our website, or contact CalRamic Technologies LLC with your questions. We are always here to help!

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