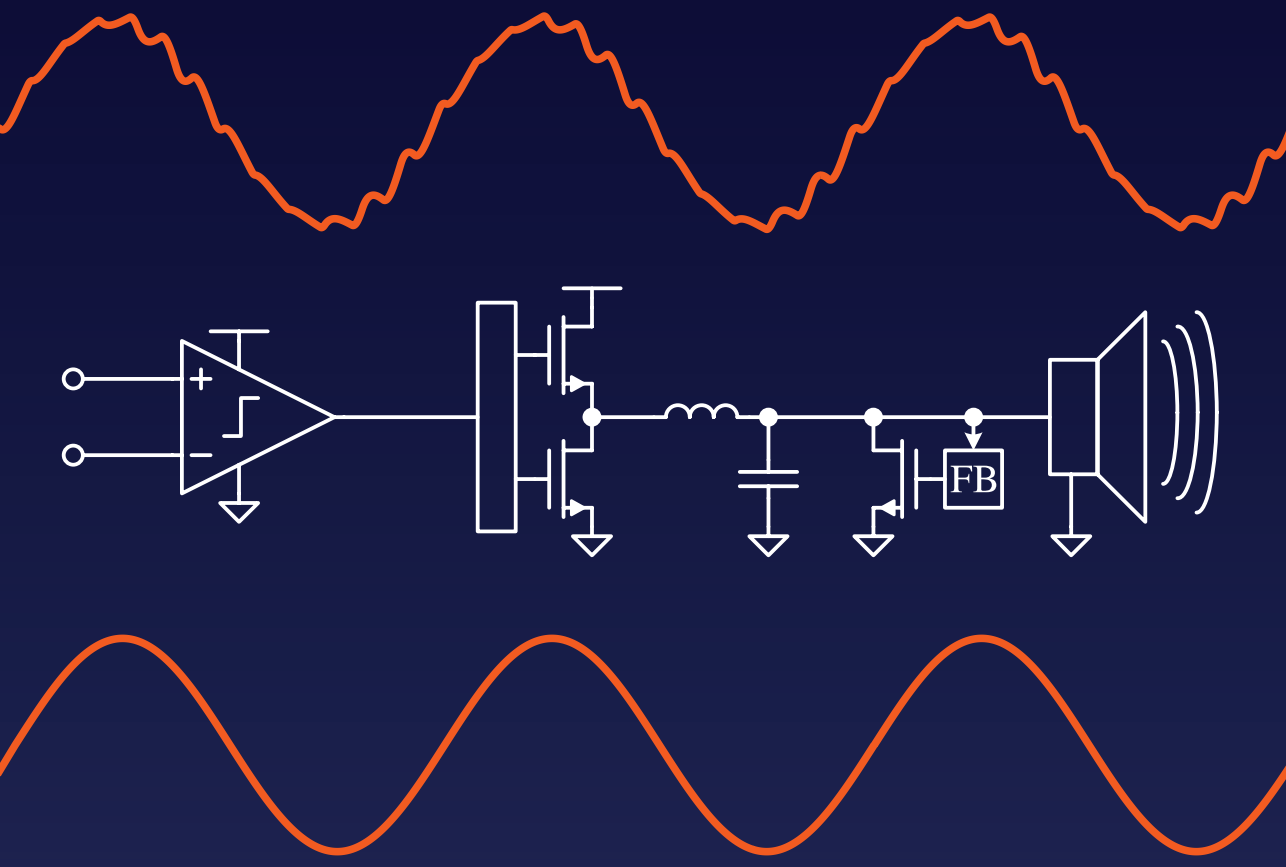
Active PWM Ripple Reduction in Class-D Amplifiers using Digital Loop Filters



Christiaan E. Lokin

Active PWM Ripple Reduction in Class-D Amplifiers using Digital Loop Filters

Christiaan Egidius Lokin

Active PWM Ripple Reduction in Class-D Amplifiers using Digital Loop Filters

Proefschrift

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de rector magnificus,
prof. dr. ir. A. Veldkamp,
volgens besluit van het College voor Promoties
in het openbaar te verdedigen
op vrijdag 24 maart 2023 om 16.45 uur

door

Christiaan Egidius Lokin

geboren op 19 januari 1992
in Hengelo, Nederland

Dit proefschrift is goedgekeurd door:

Promotor
prof. dr. ir. B. Nauta

Co-promotor
dr. ir. R.A.R. van der Zee

This research is part of the Intelligent Class-D Control project (no. 13911) and is supported by the Applied and Engineering Science division (TTW), which is part of the Netherlands Organization for Scientific Research (NWO).

UNIVERSITY OF TWENTE.

University of Twente
P.O. Box 217, 7500 AE
Enschede, Netherlands

Cover Design:	Jesse Haaksman
Printed by:	Gildeprint Drukkerijen, Enschede, The Netherlands
Lay-out:	Chris Lokin, typeset with LaTeX
ISBN (print):	978-90-365-5566-1
ISBN (digital):	978-90-365-5567-8
URL:	https://dx.doi.org/10.3990/1.9789036555678

Samenstelling promotiecommissie:

Voorzitter en secretaris:

prof. dr. J.N. Kok	Universiteit Twente

Promotor:

prof. dr. ir. B. Nauta	Universiteit Twente

Co-promotor:

dr. ir. R.A.R. van der Zee	Universiteit Twente

Leden:

prof. dr. T. Batista Soeiro	Universiteit Twente
dr. ir. A.B.J. Kokkeler	Universiteit Twente
prof. dr. K.A.A. Makinwa	TU Delft
prof. dr. ir. L.J. Breems	TU Delft

Opgedragen aan mijn ouders

"Do, or do not.
There is no try."

– Grandmaster Yoda

Abstract

The research field around sound reproduction is driven by a desire to continuously pack more powerful amplifiers in a small fan-less enclosure while providing state-of-the-art noise and distortion performance. Class-D amplifiers are a perfect candidate for these requirements, specifically because of the inherently low dissipation in their switching power stage with respect to more conventional linear amplifiers. There is, however, always a caveat: switching high currents at high frequencies causes electromagnetic emissions that could interfere with the correct operation of other electronic devices. Regulations limit the amount of electromagnetic interference (EMI) that devices are allowed to emit to maintain interoperability between the many electronic devices in the Internet of things (IoT) era.

Speakers are commonly connected to an amplifier using leads of several meters. These leads double as an antenna for high frequency signals above the audio band, such as the switching frequency and its harmonics or parasitic ringing in the output stage, thereby causing unwanted radiated emissions. This thesis is focused on reducing the EMI due to the residual power after the output filter at the pulse-width modulation (PWM) frequency, the so called ripple. Examples in literature reduce the power at the PWM frequency and its harmonics by applying spread spectrum modulation to smear power out over a larger bandwidth. However, in this way they still radiate the same amount of power, just not concentrated at distinct frequencies. To reduce the ripple current through the speaker leads, it is possible to use a higher order filter, use a multi-phase or multi-level output stage or to inject a cancellation signal after the output filter. In the research field of power electronics, cancellation schemes have been presented. First the disturbance is sensed and processed and afterwards a cancellation signal is synthesized and injected into the circuit. The processing can be done using a feedback or feed-forward topology, each having its advantages and disadvantages.

An extensive case study on multi-phase systems is done to evaluate their merits in reducing the ripple current after the output filter. In a multi-phase system, multiple half-bridges are combined in a parallel fashion to drive one or both sides of the load. Interleaving of the PWM carriers in the modulator corresponding to each half-bridge provides a reduction in the observed ripple current after combining the half bridge outputs in the output filter. The effect of adding more phases on the amount of ripple is

studied as well as the costs associated to multi-phase implementations.

In the field of power conversion, multi-level systems are often used to relax the output ripple by switching between multiple voltage levels. By reducing the voltage steps, the emissions are also lowered which is especially of importance when switching powers in excess of 1 kW. Different multi-level architectures are discussed to find whether they are applicable in audio amplifiers or not.

The feasibility of the aforementioned techniques has been considered with the main goal of having a system with fewer external components. Multi-phase and multi-level systems are hence not a suitable choice and a further case study between feed-forward and feedback ripple reduction techniques showed the latter to be the most straightforward to implement. A development board made by Axign utilizing the AX5689 digital amplifier controller IC was used as a design vehicle to realize a prototype bridge-tied-load (BTL) Class-D amplifier with ripple reduction. The built-in analog-to-digital converters (ADCs) were used to measure the output signals of both bridge halves. A selective digital band-pass loop filter was designed in the digital signal processor (DSP) core of the AX5689 to only provide high loop-gain around the PWM frequency without affecting the audio band. A ripple reduction of 28 dB for the common-mode (CM) and 18 dB for the differential mode (DM) was achieved across all signal frequencies and output powers up to 10 W. The Class-A drivers used to inject the anti-ripple have a negative impact on the total system efficiency, which drops from 84% without ripple reduction to 79% with ripple reduction enabled. The technique has virtually no impact on total harmonic distortion plus noise (THD+N) performance and could be used as an add-on to any Class-D amplifier with a fixed PWM frequency. Efficiency still has to be improved to make the solution more attractive for the industry. A monolithic realization of the system could further improve the efficiency and the ability to reduce the ripple.

Designing the digital band-pass filter of the prototype faced some challenges regarding processing delay. Compensating dynamics near the sample frequency becomes more difficult when processing delay is present. Ways to mitigate the effect of non-fractional delays on loop stability have been investigated and compared to similar techniques. In the research field of continuous-time $\Sigma\Delta$ ADCs, a technique called excess loop delay (ELD) compensation is used to stabilize the loop filter in presence of a known delay in the feedback path. When the quantizer delay is less than one clock cycle, it is possible to restore the noise transfer function (NTF) to that of the delay-less system by tuning the loop-filter coefficients and adding a direct path around the quantizer. Quantizer delays in excess of one clock cycle do not allow for full restoration of the desired NTF. This phenomenon shares similarities to our proposed delay mitigation technique. The impact of both techniques on noise-shaping performance are analyzed and the proposed method is shown to also have merits in mitigating the effect of parasitic

high-frequency poles.

In summary, this thesis has shown a technique to reduce the ripple current after the output filter. Thereby the amount of EMI that can be radiated off the speaker leads decreases. The effect of unit delays in the loop has been mitigated by applying a special filter design method to obtain a more stable system. A prototype has been made around an existing amplifier to show the effectiveness of the proposed feedback ripple reduction solution.

SAMENVATTING

Een belangrijk thema in het onderzoeksveld rond geluidsreproductie is de vraag naar krachtige versterkers in een kleine behuizing zonder ventilator terwijl ze hoogwaardige ruis- en vervormingsprestaties leveren. Klasse-D versterkers zijn een perfecte kandidaat om te voldoen aan deze eisen, met name vanwege de lagere dissipatie in hun schakelende vermogenstrap in vergelijking tot conventionele lineaire versterkers. Er zit echter een addertje onder het gras: het schakelen van hoge stromen op hoge frequenties veroorzaakt elektromagnetische interferentie (EMI) die de werking van andere elektronica kunnen verstoren. Er is regelgeving waarin is vastgesteld hoeveel elektromagnetische interferentie apparaten mogen uitzenden om samen te kunnen blijven werken met het toenemend aantal elektronische apparaten in onze wereld.

Luidsprekers worden gewoonlijk met kabels van enkele meters aangesloten aan een versterker. Deze draden werken ook als antenne voor hoogfrequente signalen boven de audio band, zoals de schakelfrequentie en de hogere harmonischen ervan of parasitaire oscillaties in de uitgangstrap, waardoor er ongewenste emissies plaatsvinden. Dit proefschrift richt zich op het verminderen van EMI veroorzaakt door het schakelresidu van de pulsbreedte modulatie (PWM) na het uitgangsfilter, de zogenoemde rimpel. In de literatuur zijn allerhande voorbeelden te vinden om het vermogen op de PWM schakelfrequentie en de harmonischen ervan te verminderen. Bijvoorbeeld, door het toepassen van 'spread spectrum' modulatie, een techniek om het vermogen uit te smeren over een grotere bandbreedte. Desalniettemin wordt er op deze manier dezelfde hoeveelheid vermogen uitgezonden, alleen is het niet geconcentreerd op specifieke frequenties. Om de rimpelstroom door de luidsprekerdraden te verminderen, kan een hogere orde filter of een multifase of multilevel uitgangstrap gebruikt worden. Een andere optie is om een signaal in tegenfase te injecteren en zo de rimpel op te heffen na het uitgangsfilter. In het onderzoeksveld van vermogenselektronica zijn zulke opheffingsmethoden al bekend. Eerst wordt de verstoring gemeten en bewerkt, waarna een opheffingssignaal gesynthetiseerd kan worden voor injectie in het circuit. De signaalbewerking kan worden gedaan door middel van terugkoppeling of feed-forward topologieën met ieder zijn voor- en nadelen.

Er is een uitvoerige case study op het gebied van multifase systemen uitgevoerd om de mogelijkheden tot het reduceren van de rimpel na het

uitgangsfilter te evalueren. In een multifase systeem worden meerdere halfbruggen op een parallelle manier gecombineerd om één of beide kanten van de belasting aan te sturen. Door de PWM draaggolven op verschillende fasen te laten lopen, kan na het combineren van de uitgangen van de halfbruggen de rimpelstroom worden gereduceerd. Het gebruik van meer fases op de hoeveelheid rimpel is bestudeerd net als de bijbehorende kosten van multifase implementaties.

In het veld van vermogensomzetting worden vaak multilevel systemen die schakelen tussen meerdere spanningen gebruikt om de rimpel aan de uitgang te verminderen. Door het verkleinen van de spanningsstappen worden de emissies ook lager wat vooral van belang is wanneer vermogens hoger dan 1 kW worden geschakeld. Verschillende multilevel architecturen zijn bestudeerd om te kijken of ze toegepast kunnen worden in audioversterkers.

De haalbaarheid van de eerdergenoemde technieken is onder de loep genomen met als hoofddoel het vinden van een systeem met zo min mogelijk externe componenten. Multifase en multilevel systemen zijn daarom niet een geschikte keuze en een daaropvolgend onderzoek naar op feedforward en terugkoppeling gebaseerde rimpelreductietechnieken wees uit dat de laatstgenoemde techniek goed te implementeren is. Een prototype Klasse-D brugversterker met rimpelreductie is gerealiseerd op een bord van Axign met daarop de AX5689 digitale versterker aansturingschip. De ingebouwde analoog-digitaal omzetters (ADCs) zijn gebruikt om de uitgang van beide halfbruggen te meten. Een selectief banddoorlaat lusfilter is ontworpen in de digitale signaal processor (DSP) van de AX5689 met als doel om alleen veel versterking te maken op de PWM frequentie zonder de inhoud van de audioband aan te tasten. Dit resulteert in een rimpelreductie van 28 dB voor common-mode (CM) en 18 dB voor differentiële-mode (DM) signalen over de gehele audioband met signalen tot 10 W. De Klasse-A versterkers van het anti-rimpel injectiecircuit hebben echter een negatief effect op de efficiëntie, die van 84% zonder naar 79% met rimpelreductie zakt. De techniek heeft praktisch geen invloed op de totale harmonische vervorming plus ruis (THD+N) prestaties en kan als toevoeging voor een willekeurige Klasse-D versterker met een vaste schakelfrequentie worden gebruikt. De efficiëntie van het systeem moet nog verbeterd worden om interessant te worden voor de industrie. Een monolithische realisatie van het systeem zou kunnen helpen om de efficiëntie en rimpelreductie verder te verbeteren.

Het ontwerp van digitale banddoorlaatfilters van het prototype bevatte een aantal uitdagingen omtrent het omgaan met signaalvertraging. Het compenseren van dynamica in de buurt van de bemonsteringsfrequentie wordt lastiger wanneer er vertraging in het signaalpad zit. Manieren om de effecten van niet-fractionele vertragingen op de stabiliteit van de lus te verminderen, zijn onderzocht en vergeleken met vergelijkbare technieken. In het onderzoeksgebied van continue-tijd Sigma-Delta analoog-digitaal-

omzetters ($\Sigma\Delta$ ADCs) wordt een techniek genaamd ELD compensatie gebruikt om de lus te stabiliseren wanneer een bekende signaalvertraging in het feedbackpad optreedt. Wanneer de quantizer vertraging minder dan één klokcyclus betreft, kan de ruisoverdracht (NTF) van het systeem zonder vertraging worden hersteld door middel van het aanpassen van de lusfiltercoëfficiënten en het toevoegen van een direct pad rondom de quantizer. Quantizer vertragingen langer dan één klokcyclus maken het onmogelijk om de ruisoverdracht volledig te herstellen. Dit fenomeen komt overeen met hoe onze techniek omgaat met vertragingen. De invloed van beide technieken op 'noise-shaping' prestaties is geanalyseerd en de voorgestelde methode laat ook zien dat er omgegaan kan worden met hoogfrequente polen.

Samengevat laat dit proefschrift een techniek zien die de rimpelstroom vermindert na het uitgangsfilter. Hierdoor wordt de hoeveelheid EMI die uitgestraald wordt van de luidsprekerdraden verlaagd. Het effect van klokcycli signaalvertraging in de lus is verholpen door het toepassen van een speciale filterontwerpmethode wat resulteert in een stabieler systeem. Een prototype is gerealiseerd rondom een bestaande versterker om aan te tonen dat de voorgestelde op terugkoppeling gebaseerde rimpelreductietechniek een effectieve oplossing is.

List of Acronyms

AC	alternating current
AM	amplitude modulation
ADC	analog-to-digital converter
BTL	bridge-tied-load
CM	common-mode
CMOS	complementary metal-oxide-semiconductor
CRFF	cascade of resonators with feed-forward summation
DAC	digital-to-analog converter
DC	direct current
DM	differential mode
DMOS	double-diffused MOS
DR	dynamic range
DSD	Direct-Stream Digital
DSP	digital signal processor
ELD	excess loop delay
EMI	electromagnetic interference
FIR	finite impulse response
FIRDAC	finite impulse response DAC
FM	frequency modulation
FPGA	field programmable gate array
HB	half-bridge
IC	integrated circuit
IIR	infinite impulse response
IoT	Internet of things
LLADC	low-latency ADC
LMS	least mean squares
LSB	least significant bit
LTI	linear time-invariant

MAE	minimum aliasing error
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
NMOS	P-type metal-oxide-semiconductor
NSPWM	natural sampling PWM
NTF	noise transfer function
PA	power amplifier
PCB	printed circuit board
PCM	pulse-code modulation
PDM	pulse-density modulation
PEDEC	pulse edge delay error correction
PMOS	N-type metal-oxide-semiconductor
PSRR	power supply rejection ratio
PWM	pulse-width modulation
RF	radio frequency
SAR	successive approximation register
SE	single-ended
SQNR	signal-to-quantization noise ratio
STF	signal transfer function
THD	total harmonic distortion
THD+N	total harmonic distortion plus noise

Contents

CHAPTER 1

INTRODUCTION

Society is making more and more use of electronic devices to fulfill work related tasks and to enjoy spare time. To provide means of interaction, transducers are used which convert for instance touch signals to the digital domain or an analog audio signal to sound pressure waves.

Class-D power amplifiers are well suited for audio amplification, and have hence become the standard for power amplifiers in electronics for consumer, mobile and automotive applications. High efficiency is realized by switching the power stage transistors on and off, eliminating the dissipation associated with Class-AB amplifiers. This allows for high power output in a small form factor, as only a modest heat sink suffices. Total harmonic distortion (THD) performance of Class-D amplifiers has become equal to, or better than, the performance of Class-AB amplifiers. Both the high efficiency and high audio performance have resulted in a growth in the use of Class-D audio amplifiers [1].

The increased efficiency of Class-D has side effects, namely electromagnetic interference (EMI) due to high frequency switching. It is common to use switching frequencies of several hundreds of kilohertz, which do produce harmonics in the AM radio band. Furthermore, the fast switching transients produce frequency content in the high megahertz range which can interfere with, for example, the FM radio band. As set-top box or car audio amplifier systems connect the speakers via long leads, these leads will function as an antenna for the common-mode (CM) switching residue.

In this chapter, the design space and common non-idealities of Class-D audio power amplifiers will be explored. First, both analog and digital pulse-width modulation (PWM) generation topologies will be discussed including ways to implement feedback. Subsequently, output stage topologies and their driver stages are discussed, including typical phenomena such as dead-time, hard-switching and soft-switching. Next, we will look

The 2nd and 3rd paragraph on this page have appeared in [CEL:3] .

at the non-ideal effects in Class-D amplifiers, mainly focusing of EMI due to high-frequency switching voltages and currents. Also, the main dissipation mechanisms in Class-D amplifiers are shortly discussed. Finally, the chapter concludes with research questions and an overview of the remainder of this thesis.

1.1 Class-D Amplifiers

A Class-D amplifier can be subdivided into three blocks, a modulator, a power stage and a filter. An example of an analog Class-D amplifier is shown in Figure 1.1. The modulator converts the input signal into a PWM signal by comparing the input to a high-frequency triangular or sawtooth reference signal. The PWM signal is amplified by a power stage, which consists of level shifting circuits to drive the high- and low side power transistors from a higher supply voltage than the modulator. After the amplification, the high-frequency switching components are filtered out using an LC low-pass filter. A power stage also includes features to ensure robust operation, such as dead-time generation, over-current protection and click/pop reduction. To achieve good THD performance, a feedback loop is often implemented to counteract the non-linearity in the power stage.

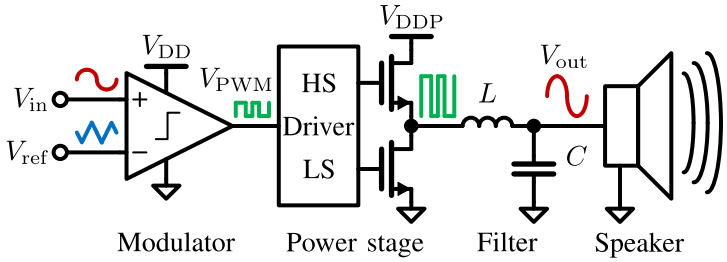


Figure 1.1: Overview of an analog Class-D amplifier with idealized internal signals.

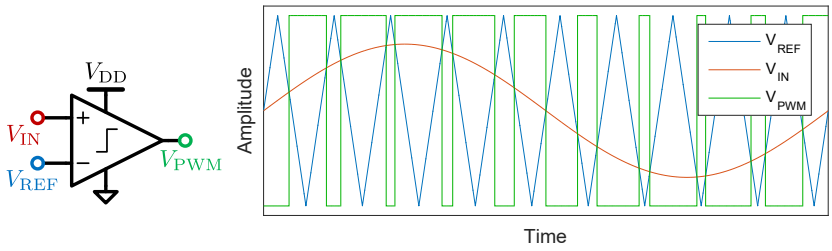
1.2 Analog PWM Generation

The first type of amplifier to be discussed is a Class-D amplifier that incorporates an analog signal processing path. A distinction between four PWM topologies can be made, namely fixed carrier systems with and without feedback and self-oscillating systems with either hysteresis or delay based feedback. These topologies are described in the following sections.

1.2.1 Fixed carrier

In a fixed carrier Class-D amplifier, the PWM signal switches at a constant frequency. The modulator consists of a comparator fed by a fixed frequency

saw-tooth or triangular reference and the input signal. The modulator output signal is high when the input signal is larger than the reference signal and the other way around. This method of modulation is called natural sampling PWM (NSPWM) and a comparator and its waveform signals are shown in Figure 1.2. Now, the PWM signal can be fed to an output stage to deliver power to the load.



(a) Comparator. (b) PWM input, reference and output waveforms.

Figure 1.2: NSPWM modulation.

A drawback of making an amplifier using this approach is that the system is feed-forward, hence there are no means of error suppression. Since the PWM signal is effectively multiplied with the supply rail, any variations on the supply voltage are directly present at the load, giving a power supply rejection ratio (PSRR) of 0 dB. Feed-forward power supply compensation has been proposed in [2] to mitigate the effect of power supply variations. Apart from disturbances in the the supply voltage, the output stage can not exactly reproduce the PWM waveform due to rise times and dead-time, which both cause distortion.

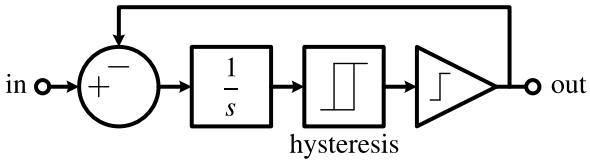
Feedback

Because the feed-forward amplifier has a bad PSRR and distortion due to the output stage, this amplifier is usually equiped with a feedback loop to compensate for these errors. Different strategies have been proposed in literature, namely, voltage feedback either from the switching output node or post filter and output current feedback. The feedback loop should provide high loop gain in the audio band to provide sufficient error suppression. [3–7]

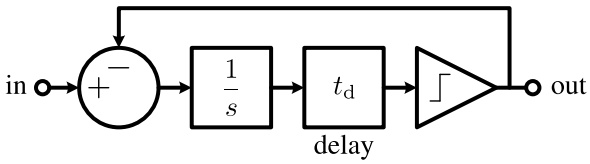
1.2.2 Self-oscillating

The other analog switched-mode amplifier is a self-oscillating amplifier, an amplifier that oscillates due to its feedback structure without requiring a reference signal. When the amplifier is idle its switching frequency is maximum. Increasing or decreasing the duty cycle by applying an input signal will reduce the switching frequency. Using near maximum modulation indices can impact the performance of the amplifier because

of low switching frequencies. Both a hysteretic and a delay based self-oscillating loop are shown in Fig. 1.3.



(a) Hysteretic self-oscillating topology.



(b) Delay based self-oscillating topology.

Figure 1.3: Self-oscillating feedback schemes.

Hysteretic

In a hysteretic switched-mode amplifier the output signal is fed back and summed with the input signal at the input of an integrator. Then, the integrator output is fed to a comparator with a hysteresis window. This approach gives a second order loop transfer in the audio band using a single integrator [8]. A hysteretic feedback loop is shown in Fig. 1.3a.

Delay based

A delay based switched-mode amplifier looks much like the hysteretic amplifier. However, instead of a hysteresis window, a time-delay is inserted after the integrator. The system provides a first order loop transfer but can be increased to a higher order by adding more integrator stages [9]. A delay based feedback loop is shown in Fig. 1.3a.

1.2.3 Distortion due to feedback

Applying feedback can cause non-linearities if not applied correctly. The ripple in a feedback system can interfere with the carrier in the PWM modulator, which can alias carrier side-bands into the audio band [4]. THD deteriorates especially when high-order loop filters are implemented. In order to circumvent this deterioration, minimum aliasing error (MAE) filters can be implemented. These filters utilize a low-pass feedback path from the output and a high-pass feedback path from before the PWM quantizer as shown in Figure 1.4. This structure can be reduced to a single linear time-invariant (LTI) filter which realizes a transfer function

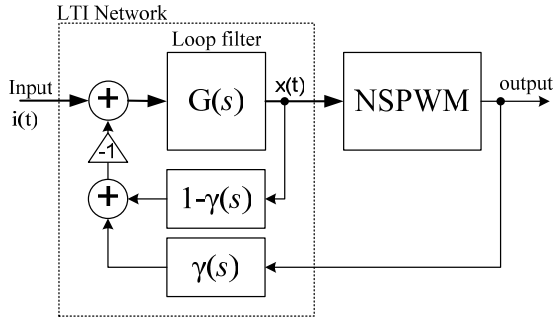


Figure 1.4: PWM implementation with 2 feedback paths [3].

with a faster decaying real part at high frequencies when compared to a generic 2nd order loop filter as shown in Figure 1.5. The total system has improved THD because of the low DC error due to carrier aliasing, which is characteristic to a 1st order modulator, and a high loop gain corresponding to a 2nd order modulator [3].

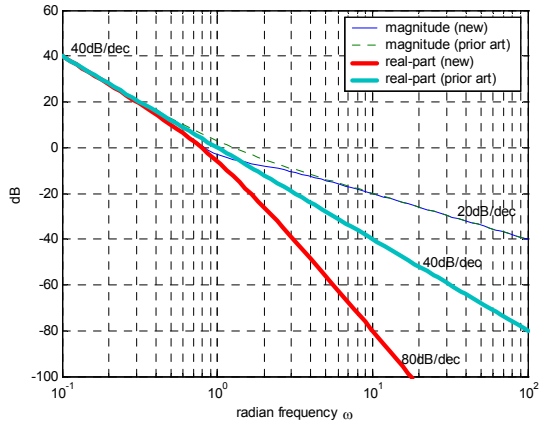


Figure 1.5: Comparison between the traditional 2nd-order loop and [3].

Another recent study has shown a feed-forward technique that injects a current to cancel the high-frequency PWM components in the feedback current before the first integrator (OP1 + C1) as shown in Figure 1.6. This

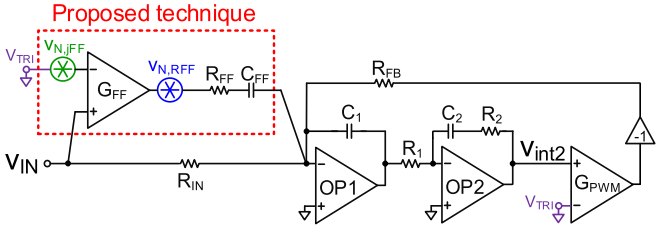


Figure 1.6: Model of the amplifier with the cancellation circuit[10].

approach improves the THD and has no influence on loop stability [10]. An improved design in [11] adds equalization to better match the phase of the cancellation current to the PWM components and linearizes the overall transfer of the amplifier.

By changing to a capacitive instead of a resistive feedback network and the application of choppers [12], it was shown that the performance limitations due to resistor noise in the the feedback network can be mitigated reaching a dynamic range in excess of 120 dB.

1.3 Digital PWM generation

Another approach is to generate PWM signals in the digital domain. In order to do this the input signal should be presented as a bitstream, hence if the input signal is analog, it has to be converted to a digital bitstream. In case of a typical pulse-code modulation (PCM) input of 16-bit samples at a 48 kHz sample rate (f_s), the input signal is up-sampled and noise-shaped afterwards to obtain a signal with fewer bits per sample, at a higher sample rate than the PCM signal. The PWM signal is obtained by comparing the up-sampled, noise-shaped signal to a digital staircase approximation of a triangular or sawtooth wave [13, 14], similar to operation of the analog PWM modulator previously discussed in this chapter. Two implementations are shown in Figure 1.7 containing the required sample-rates and bit-depths between the block [1].

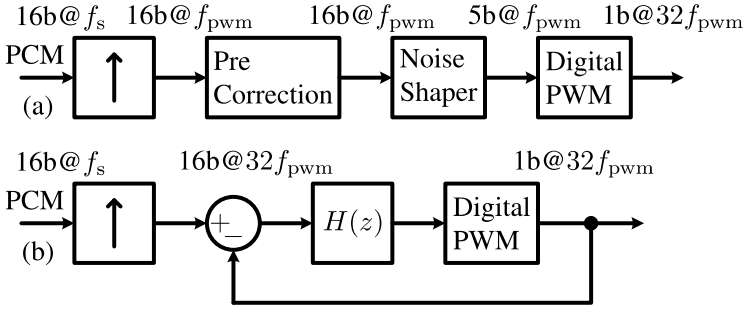


Figure 1.7: Digital PWM (a) pre-correction (b) PWM-ΣΔ (adapted from [1]).

Another method is to noise-shape the input signal to a 1-bit signal, which effectively is pulse-density modulation (PDM) instead of PWM. Coincidentally, such a noise-shaped PDM signal is also the native way of storing the Direct-Stream Digital (DSD) bitstream audio format [15]. Just like a PWM signal, this PDM signal can be amplified and filtered to reconstruct the audio signal. However, amplifying a PDM signal requires a faster switching power stage due to the majority of the switching frequency content being around $f_s/2$ compared to f_{pwm} for PWM systems [16].

1.3.1 Open-loop

A conventional topology for digital class-D amplifiers is the feed-forward or open-loop topology. Like for analog class-D amplifiers there is no feedback mechanism, hence this type of amplifier requires a stable supply because the PSRR is low. Moreover, non-linearity introduced by the modulator and the output stage is also deteriorating the THD of the system. The output stage introduces pulse-width errors due to the inserted dead-time [13, 14, 17].

To compensate for the non-linearity of the modulator and the output stage, a pre-distortion can be applied to the input signal when the modulator and output stage distortion characteristics are known. A way to reduce modulator distortion was realized by implementing a Hammerstein filter [18]. Careful design of the output stage is required, tailoring the dead-time to keep distortion at a minimum without compromising reliability [19, 20].

1.3.2 Feedback

Many ways to apply feedback to digital class-D amplifier have been published in literature [5, 6, 13, 21–30]. Hybrid types of amplifiers that generated PWM digitally have been presented where the output stage has an analog loop to mitigate supply variations [5, 13]. An approach shown in [21] is called pulse edge delay error correction (PEDEC), an algorithm that changes the position of the switching edges to eliminate distortion in the power stage due to supply variations or non-linearity.

However, digitizing the feedback loop is a technique that is becoming possible due to the reduced feature sizes of the required digital logic. A low-power analog-to-digital converter (ADC) can be inserted into the feedback path to sample the output voltage before [22–25] or after [6, 26–28] the LC-filter, providing a digital representation of the output signal. In [29], one ADC is used to digitize both the input and the feedback signal after summation. The amplifier in [30] has a signal level dependent mode control scheme that can change the modulation and pulse patterns to save power.

The advantage of applying post-filter feedback is that it allows the amplifier to correct for non-linear effects in the output filter inductor and capacitor. Further processing of the feedback signal can be done in the digital domain where the filters do not suffer from the component spread present in analog filters. A generic representation of a post-filter feedback system is shown in Figure 1.8.

1.3.3 Implementations

To highlight the differences in the implementations presented in literature, this section elaborates briefly on each topology.

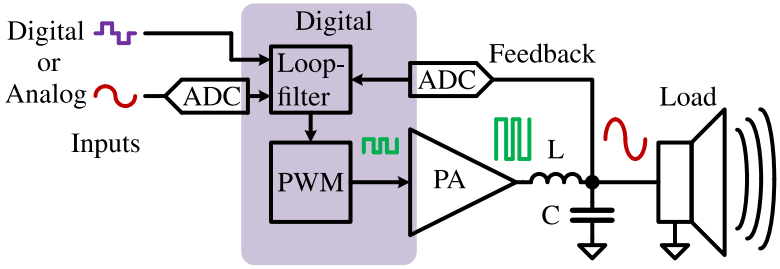


Figure 1.8: Block diagram of a class-D amplifier with digital post-filter feedback.

Before The Output-Filter

An amplifier prototype using an field programmable gate array (FPGA) board and a commercially available ΣΔ-ADC was built in [22]. The ΣΔ-ADC was carefully selected to have a direct bitstream output for minimum delay. Its input is preceded by a 1st order low-pass filter to suppress the PDM switching residue of the filter-less output. The simplified diagram of this topology is shown in Figure 1.9a.

Another paper [23] proposes a continuous-time ΣΔ-ADC tailored specifically for use in Class-D amplifiers with digital feedback. The ADC features inherent 3rd order anti-aliasing, allowing it to be connected directly to the filter-less 3-level output stage. The simplified diagram of this topology is shown in Figure 1.9b.

A more recent digital implementation [24] uses a digital-to-analog converter (DAC) to subtract a high-quality noise-shaped copy of the input signal from the output signal to relax the requirements on the feedback ADC. Now, the ADC only has to process the error signal. The simplified diagram of this topology is shown in Figure 1.9c. The amplifier also includes

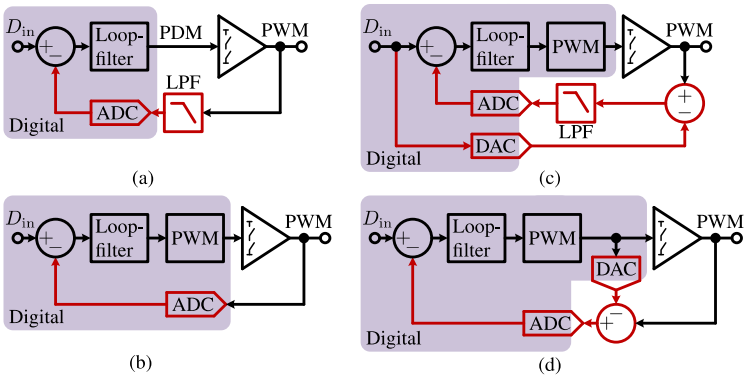


Figure 1.9: Schematics showing the topological differences of amplifiers with digital input and digital feedback directly after the power stage.

an ADC to sense the supply voltage variations and adapt the required pulse-width of the output accordingly (not shown).

Similar to the implementation in [24], the work in [25] uses a DAC to subtract the PWM signal from the filter-less output signal. Here, the error signal only contains the differences between the DAC and the output of power stage, rather than the full PWM waveform. The simplified diagram of this topology is shown in Figure 1.9d.

After The Output-Filter

The work of Mouton [6] is, to our knowledge, the first work to present a digital Class-D amplifier with global feedback. A commercially available ADC is used to digitize the voltage after the output filter before feeding it to the fully digital loop filter and modulator. The work also implements a technique to reduce the non-linearity caused by the presence of the PWM ripple residue in the feedback signal and provides a load characterization method.

Both the works in [26, 27] present a digital Class-D amplifier based on a tailor made low-latency ADC (LLADC) to provide feedback after the output filter. The amplifier in [26] is monolithically integrated on a single die, and features a multi-phase output stage. The product in [27] is a highly configurable controller chip that is to be used with an external power stage. This solution is covered in more detail in section 4.3.

Another work presents a multi-phase digital amplifier with global feedback solution based on a fixed-point core signal microcontroller with embedded successive approximation register (SAR) ADC and PWM interfaces [28]. It shows that it is possible to implement such an amplifier with just a microcontroller, significantly reducing the cost with respect to an FPGA or CMOS implementation while still achieving reasonable performance.

These implementations all resemble the architecture of the system in Figure 1.8 with the main difference being the output stage configuration. Output stages will be discussed in the next section and a more thorough analysis of multi-phase systems is presented in chapter 3.

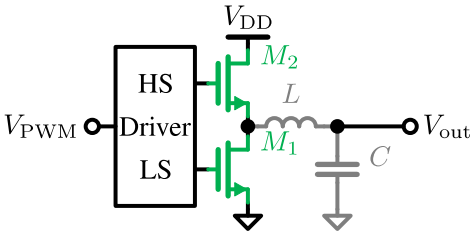
1.4 Output stage

In order to deliver power to the load, the PWM signal has to be amplified, hence, a power stage is inserted after the modulator. A basic power stage consists of two power metal-oxide-semiconductor field-effect transistors (MOSFETs) that can switch the output between the high and low supply rail. A driver circuit is required to charge and discharge the gates of the power MOSFETs. Moreover, the driver circuit inserts dead-time to prevent cross conduction preventing the power MOSFETs from breaking down.

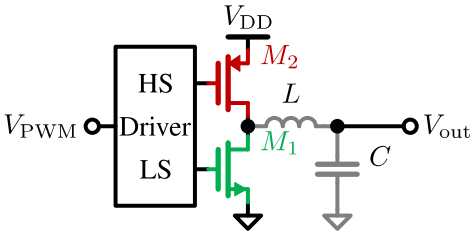
Additionally, the driver can implement clip protection. In the following sections, the design choices in a power stage will be considered.

1.4.1 Power MOSFETs

A pair of power MOSFETs forms a half-bridge that is connected to the load via an optional LC low-pass filter. These MOSFETs can either be both NMOS as in Figure 1.10a, or a complementary pair of an NMOS and a PMOS transistor as in Figure 1.10b.



(a) An output stage utilizing 2 NMOS transistors.



(b) A complementary output stage.

Figure 1.10: Commonly used output stages.

The dual NMOS transistor power stage requires a bootstrapped supply to operate the high-side driver, but can use the same driver circuit for the high- and low-side driver. In contrast, for a CMOS implementation the PMOS transistor has to be approximately three times larger to provide the same $r_{ds,on}$ as the NMOS transistor due to the lower hole mobility. Moreover, the power stage will require a different high- and low-side driver, however a bootstrapped supply is not required.

1.4.2 Gate Driver

The gate driver is a circuit that controls the power transistors of the output stage. First the PWM signal has to be level shifted to the voltage domains of the low-side (LS) and high-side (HS) gate drivers. The HS driver specifically requires a bootstrapped supply voltage for an NMOS output device or a local supply voltage with respect to V_{DD} for a PMOS output device.

A way to implement the gate drivers is by a chain of inverters with increasing drive strength. The final inverter that has to drive the power

transistors is usually designed to have a stronger pull-down than pull-up strength (in case of an NMOS) to prevent cross-conduction during switching. Drive strength can also be tuned to achieve faster or slower transients to tune for emissions. Usually, logic is added as well to ensure that one power transistor is off before the other is turned on.

For example, in [31], an adaptive gate driver is designed to avoid reverse recovery. A comparator is used to detect reverse current through the power transistor and waits before turning it off completely until the other power transistor has taken over. This way no current has to flow through the fly-back diodes.

In application where the V_{GS} is in the same order of magnitude as the V_{DD}, the losses in the output stage are dominated by charging and discharging the gates of the power transistors. In [32], a mobile class-D power amplifier is designed utilizing dynamic power stage activation. The power stage is cut into slices that can be disabled at low power output to reduce the required charge to turn the power transistors on and off, ultimately reducing the power consumption.

1.4.3 Bootstrapping

In the output stage as shown in Figure 1.10a the gate of the top NMOS has to be driven with a voltage above the supply voltage to be able to turn it on. At the same time, the driving voltage should also not exceed the maximum rated gate-source voltage. A way to do this, is to either use a charge pump or a bootstrapping circuit, the latter of which will be explained in this section. A commonly used bootstrapping circuit is shown in Figure 1.11.

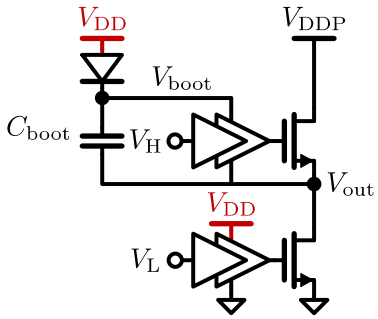


Figure 1.11: Bootstrap circuit to provide the elevated supply voltage for the high-side gate driver.

When V_{out} is low, the bootstrap capacitor C_{boot} is charged to V_{DD} minus the diode forward voltage. Then, once V_{out} is switching to V_{DDP}, it will lift V_{boot} above V_{DDP} to provide a sufficiently high voltage to drive the gate of the output transistor.

1.4.4 Levelshifting

Driving the high-side gate driver requires a levelshifting operation to propagate the low-voltage PWM signal to the bootstrapped voltage domain of the gate driver in front of the output transistor. A basic levelshifter with a latch for a dual NMOS output stage is shown in Figure 1.12.

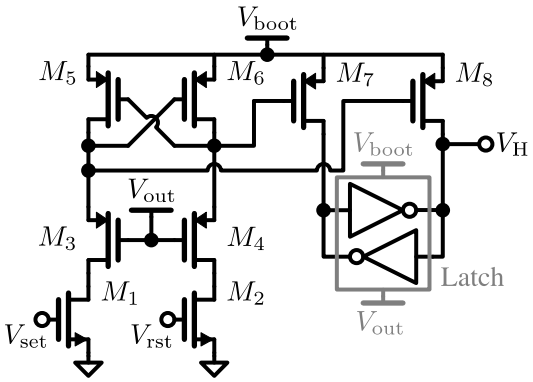


Figure 1.12: Levelshifter to drive the high-side gate driver.

When the V_{set} input is high, the gates of $M_{6,8}$ are pulled down via M_3 which pulls the drains of $M_{6,8}$ to V_{boot}. Transistors $M_{5,7}$ are turned off and the value of V_{H} is held by the latch to interface with the gate driver in Figure 1.11. Likewise, when the reset input is high, the gates of $M_{5,7}$ are pulled down which will toggle the latch. Transistors $M_{3,4}$ are used to limit the voltage swing at the input of $M_{7,8}$ to the output voltage of the power stage plus one threshold voltage. More sophisticated level shifting circuits which are optimized for speed, efficiency and supply bounce are found in literature [33–35].

1.4.5 Dead-time

Dead-time is a period in which both switching devices in the output stage are turned off as shown in Figure 1.13b. Dead-time makes the amplifier more robust by preventing the short-circuit current when the transistors are switching. However, it can deteriorate the THD because it changes the pulse widths of the PWM signal.

Control mechanisms to implement dead-time vary in complexity from a logic gate preventing both transistors to be on simultaneously to a state-machine controlled output stage driver [33]. An approach to eliminate the dead-time as much as possible to reduce distortion is shown in [36]. However, another paper [19] shows that the optimum dead-time for minimum distortion is not equal to zero.

1.4.6 Hard- and Soft-switching

Due to the dead-time, the amplifier can utilize soft-switching. Soft-switching is a phenomenon that occurs due to an interaction between the output parasitic capacitance and the filter inductor. The current that starts flowing through the filter inductor in Figure 1.13a is used to charge or discharge the parasitic output capacitance after turning the conducting transistor off in Figure 1.13b. After that, the other power transistor can be turned on while already having zero voltage over its channel as shown in Figure 1.13c, reducing switching losses.

To ensure operation in soft switching, the current through the filter inductor has to change polarity and reach sufficient magnitude during the time a switch is closed. Else it cannot (fully) charge the output capacitance to commutate the output voltage during the dead-time before the power stage switches. This can result in hard-switching or partial soft-switching, which both reduce efficiency. In [37], a tracking loop has been designed which adapts the switching frequency to keep the amplifier in soft-switching. As a result the amplifier achieves a high efficiency at any output power level.

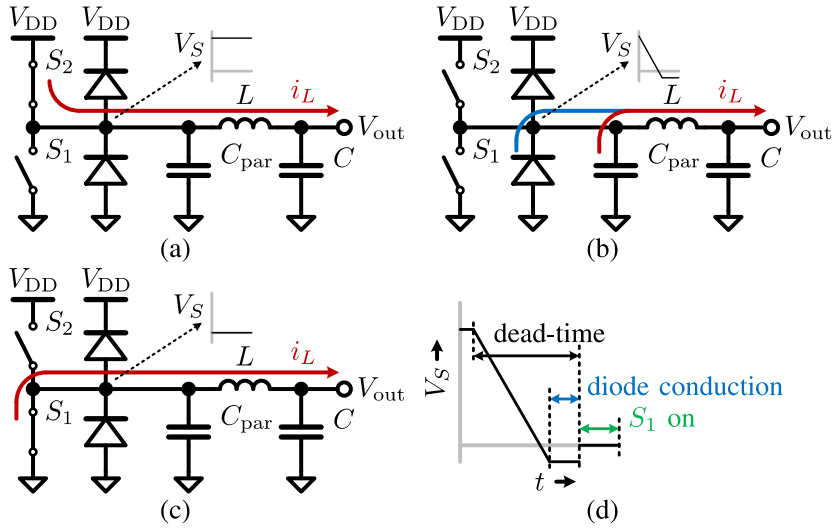


Figure 1.13: Dead-time and soft-switching visualized for a positive output current.

1.4.7 Overcurrent protection

A versatile overcurrent protection technique that acts differently for scenarios such as short circuits and load impedance variations is discussed in [38]. The implemented technique is tested to be robust against connecting the output after the LC-filter to the negative or positive supply. The current limiting in normal operation prevents audio holes that are caused by

hiccup limiting in conventional designs. Finally it is possible to use smaller double-diffused MOS (DMOS) transistors in the output stage because they do not have to be over-dimensioned for short circuit scenarios.

In mobile Class-D applications, it is often a problem that the speaker is destroyed by dissipating too much power. In the design in [39], a digital signal processor (DSP) runs a speaker protection algorithm that limits the membrane excursion and voice-coil temperature of the speaker. Furthermore, a battery safeguard that limits the current drawn from the battery when it nears discharge is implemented.

1.5 Class-D Non-idealities

The improved efficiency of Class-D amplifiers does come at a cost. The high-voltage switching transients in class-D amplifiers can radiate due to the high $\mathrm{d}V/\mathrm{d}t$ and $\mathrm{d}I/\mathrm{d}t$. The added dead-time to prevent cross-conduction degrades the linearity of the power stage, necessitating the use of a feedback loop or pre-distortion to suppress this non-linearity. Also, the theoretical 100 % efficiency is never achieved due to various loss mechanisms in the amplifier.

1.5.1 EMI

A couple of different phenomena in the Class-D amplifier cause EMI, namely, the switching frequency, its harmonics and intermodulation products, which all reside around the amplitude modulation (AM) radio band. Next, we also have the sharp transitions at the pulse edges and reverse recovery currents, which can excite resonances in parasitic LC loops, causing interference around the frequency modulation (FM) radio band. Interference with other electronic equipment has to be avoided, thus precautions should be taken to make the amplifier adhere to EMI regulations.

1.5.2 PWM Ripple

Let's focus on the EMI due to the switching frequency. The small bandwidth between the audio band and the PWM switching frequency allows for limited filtering of the switching frequency components. As a result of this the load voltage still contains a ripple component which is shown in Figure 1.14. When a load is connected through long speaker wires, these wires will act as a parasitic antenna that can radiate the switching frequency components.

The worst kind of excitation is a common-mode (CM) signal, because it excites both wires with the same signal, which is optimal for the wires to work as an antenna. On the contrary, differential mode (DM) signals excite the wires in anti-phase, which gives opposing fields around the wires that cancel most of the radiation. Due to the relatively low frequency of

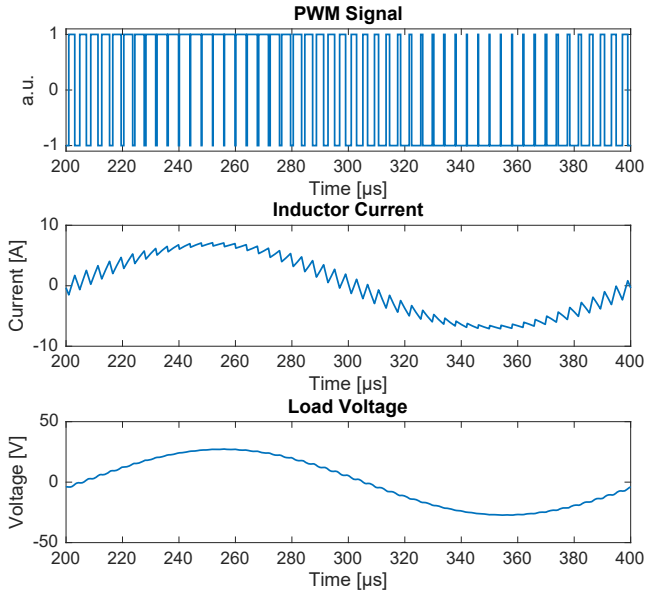


Figure 1.14: Visualization of the inductor current ripple and load voltage ripple.

this type of EMI, it could be possible to reduce it by means of additional circuitry.

1.5.3 Reverse Recovery

When dead-time is applied to the driving signal of a power stage, it is possible to get reverse recovery due to the flyback diodes that are in parallel with the switching devices. Reverse recovery is the charge dump that occurs after the flyback diode stops conducting when the opposite switch is closed. This effect is illustrated in Figure 1.15 for the hard-switching case where a current flows from ground through S_1 and the inductor.

First, the lower switch S_1 is conducting the inductor current as shown in Figure 1.15a. Then, the switch is opened and once the capacitor voltage goes below zero and reaches the forward voltage of the diode, the diode will start to conduct the current in Figure 1.15b. Finally, when S_2 is closed, the voltage difference between this state and the previous state is equalized. The diode stays in a conducting state until the stored minority carriers are fully discharged, resulting in a reverse recovery current i_{RR} to dump the space charge stored in the diode. This sharp transient can excite ringing in stray inductance from the package and PCB tracks causing EMI. [40, 41]

1.5.4 Ringing Parasitics

Both the sharp edges of the pulses and the reverse recovery current can cause ringing of parasitic LC tanks in the output stage. The capacitance

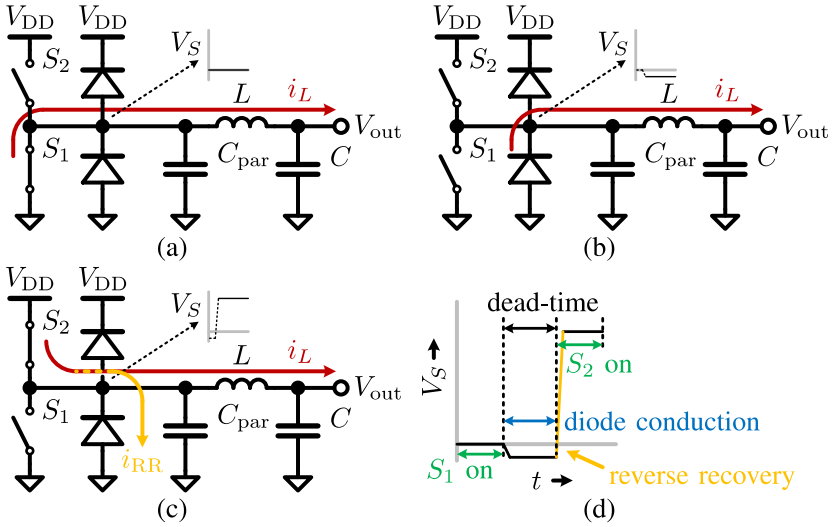


Figure 1.15: Reverse recovery visualized for a positive output current.

originates from the parasitic capacitance of the output transistors and the inductance is due to the wiring and/or lead-frame of the package. Initial research has shown that the frequency of this ringing is in the 10 MHz – 100 MHz range for a discrete output stage with off-the-shelf components. However, there are still mismatches between simulation and measurements that are yet unexplained [42, 43].

1.5.5 Dissipation sources

Class-D amplifiers owe their high efficiency to their switching output stage. The output transistor either conducts current without having a voltage drop or sustains the supply voltage without conducting current, yielding a low dissipation in the power MOSFETs.

In [37], the contributions to the power dissipation in class-D amplifiers have been investigated. The main dissipation sources have been listed in Table 1.1.

Table 1.1: List of main dissipation sources in a class-D power stage

Dissipation type	**Source**
Conduction loss P_{con}	I_{out} conduction through r_{on}
Ripple loss P_{rip}	I_{rip} conduction through r_{on} and inductor core losses
Gate driver loss P_g	(Dis)charging the gate capacitance of power transistors
Capacitive loss P_{cap}	(Dis)charging the output capacitance
Switching loss P_{sw}	Hard switching losses in the power transistors

1.6 Research Questions

As was mentioned in the previous sections, Class-D amplifiers suffer from non-ideal effects. Ideally, we would like to have a Class-D amplifier that can be used like a Class-AB amplifier, which has no EMI problems due to switching and requires less external components. A general set of research questions is presented:

- How can we reduce EMI of Class-D amplifiers due to the PWM carrier frequency?
- How to reduce the amount of external components of Class-D amplifiers?

These questions will be revisited in the next chapter

1.7 Thesis Overview

The thesis is organized as follows:

Chapter 2 focuses on potential solutions to EMI in Class-D amplifiers. Different Class-D switching schemes are discussed and how they have an impact on the EMI of the amplifier. Furthermore, an overview of the prior art in EMI reduction techniques is presented.

Chapter 3 gives an elaborate discussion on multi-phase output stage topologies as a possible solution to reduce EMI.

In chapter 4, feed-forward and feedback ripple reduction schemes are discussed to determine their feasibility and the proposed research direction is chosen. Subsequently, it explains the implementation of the Class-D amplifier based around the AX5689 chip which is used as design vehicle to test the ripple reduction technique. Finally, the design of the ripple reduction solution is presented, comprising of a digital loop filter and a Class-A driver connected after the output filter. The amplifier with ripple reduction significantly reduces the power of the fundamental PWM component after the output filter.

Chapter 5 presents the analytical filter design method used in chapter 4 to design closed loop systems with parasitic elements in the loop. This method is used to mitigate the effects of parasitic delays and high-frequency poles when they are a fixed element in the loop. The method has been applied to several different loop filter designs and manages to stabilize them. For low-pass filter design, conventional methods such as reducing the cut-off frequency or gain can also result in a stable filter, however, for band-pass filters this is less trivial. This method also manages to stabilize these band-pass loop filters.

Chapter 6 draws conclusions about the overall thesis and gives recommendations for future research in this field.

CHAPTER 2

Overview of EMI Reduction Techniques

As discussed in the previous chapter, common-mode PWM ripple is one of the major sources of EMI in class D amplifiers. Therefore, in this chapter, we will investigate techniques to reduce EMI due to the PWM ripple. First the different bridge-tied-load switching schemes of Class-D are shown. Then, the origin of both common-mode and differential-mode EMI at the output of a Class-D amplifier is discussed and an overview of EMI reduction techniques published in literature is presented. Subsequently, the topics of multi-phase and multi-level systems are briefly discussed with a more elaborate discussion on multi-phase systems in chapter 3. Finally, feed-forward and feedback ripple reduction topologies are discussed. The chapter concludes with a motivation for the chosen research questions.

2.1 Prior Art

Several studies have been done to reduce EMI in Class-D amplifiers, for instance in automotive electronics and to allow filterless operation in mobile devices. Three techniques are seen in literature, namely, switching frequency modulation [14, 44, 45], CM modulation [44, 46, 47] and Class-AB/D [48–53]. However, first we will discuss the commonly used bridge-tied-load (BTL) power stages, and their effect on EMI.

2.2 Bridge-Tied Load

Class-D amplifiers can utilize different modulation schemes [54] when their output stage is in a bridge-tied-load (BTL) configuration as shown in Fig 2.1. Advantages of using a BTL instead of a single-ended configuration are

Sections 2.1 – 2.4 and the 2nd paragraph of section 2.10 have appeared in [CEL:3] .

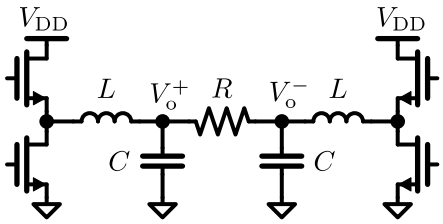


Figure 2.1: A BTL output stage.

quadruple the output power using the same supply voltage, no balanced supply requirement, no supply pumping [40], and an improved PSRR [55]. Disadvantages include having to implement the output filter twice, and requiring twice the number of output transistors, the former increasing the cost and the latter increasing system complexity.

The EMI reduction techniques that are explained in this chapter depend on the modulation scheme that is used, hence we will now first discuss these modulation schemes.

2.2.1 AD Modulation

Classical PWM is referred to as AD modulation as shown in Fig. 2.2. In an AD modulated system, the input signal V_{IN} is compared to the triangular reference V_{REF} and when the input exceeds the reference in value, a high output level is generated, otherwise a low output level is generated. This output signal is fed to the positive half bridge and an inverted version of it is fed to the negative half bridge.

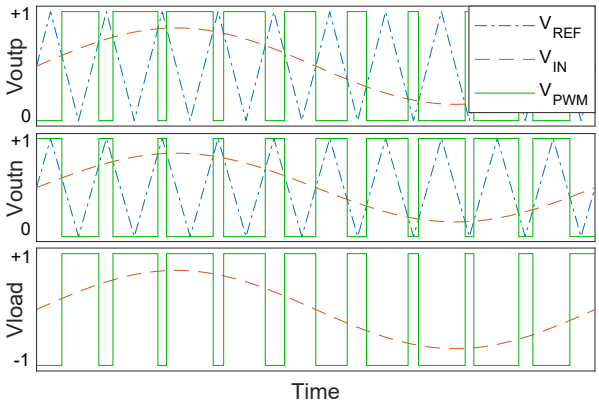


Figure 2.2: Input, reference and output waveforms as result of AD PWM for a sinusoidal input signal.

Ideally, AD modulation will not excite a CM signal over the load, because the signal is purely differential. In reality mismatch between the LC filters will cause CM to DM conversion of the ripple, because the attenuation in the stop band isn't exactly equal.

2.2.2 BD Modulation

BD modulation takes the same approach for the positive half bridge, however, to generate the negative half bridge signal, the input signal V_{IN} is inverted before it is compared to the reference V_{REF} to obtain the PWM signal as shown in Fig. 2.3. In idle this means that there is no DM voltage over the load, however the full PWM ripple is now present in the CM. Using BD modulation effectively doubles the switching frequency which is beneficial for performance.

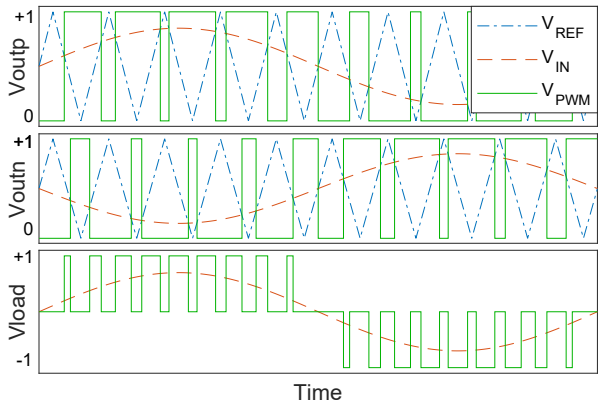


Figure 2.3: Input, reference and output waveforms as result of BD PWM for a sinusoidal input signal.

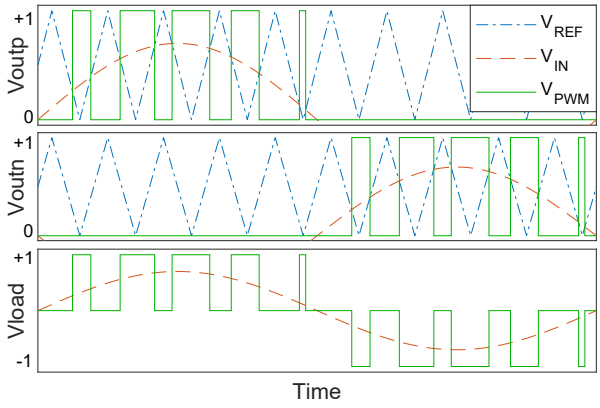


Figure 2.4: Input, reference and output waveforms as result of low-CM signaling PWM for a sinusoidal input signal.

2.2.3 Low-CM signaling

In a low-CM signaling scheme the positive half bridge is responsible for amplifying the positive part of the input signal, and the negative half bridge the other part. This is done by clipping the positive half and the

negative half of the input signal V_{IN} below and above zero, respectively, before comparing them to the reference V_{REF}, as can be seen in Fig. 2.4.

It is prevalent that this switching scheme excites the CM of the output as only one bridge half is switching at a time. The technique has merits for low-power applications, as the number of switching events is halved compared to AD or BD schemes but does suffer from lower audio performance when compared to regular BD modulation.

A hybrid implementation that combines low-CM signaling and BD can be used as a trade-off between the performance and power consumption. At lower amplitudes, the idle CM level is not put at 50% duty-cycle but between 5% and 20%. The signals for the modulators can be synthesized using the structure in Figure 2.5 and an example is shown in Figure 2.6.

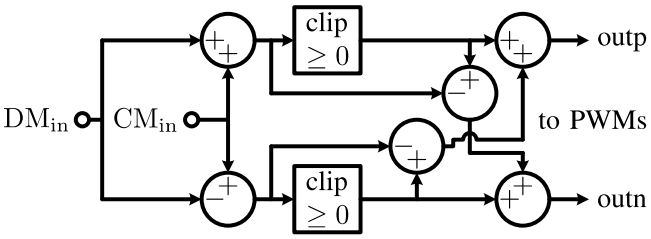


Figure 2.5: Signal processing structure to synthesize (hybrid) low-CM signaling.

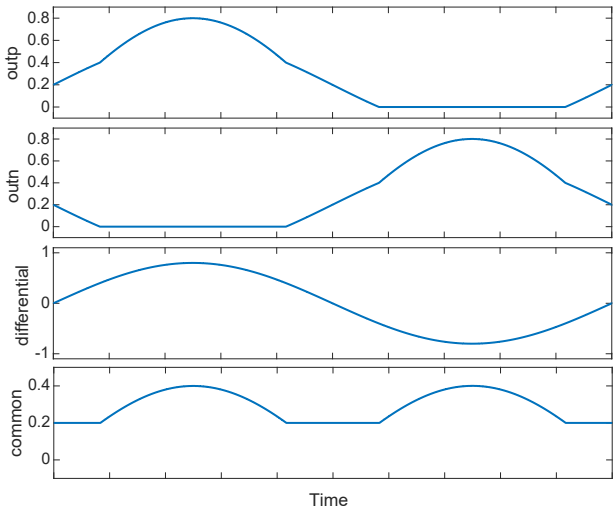


Figure 2.6: Synthesized hybrid low-CM signals and their output DM and CM components.

The DM and CM inputs provide the desired output signal and the desired idle CM level respectively. The clippers limit any signal below zero to zero, after which the excess part is added to the other output signal.

The output is fed to two equal modulators that receive carrier signals ranging from 0 to 1 ensuring that one of the bridge halves is not switching in low-CM mode. If it is also desired to have an elevated output level at that half bridge, such as in chapter 4, the carrier can be set to have a negative lower limit to raise the minimum duty cycle above 0%.

2.3 Switching Frequency Modulation

Switching frequency modulation (FM) of the PWM carrier is done by modulating the system clock or the triangle carrier wave. Modulation is done using a triangle pattern in [44], or a uniformly distributed pseudo-random spread spectrum signal in [45] and [14]. These techniques are applicable for both AD and BD modulation.

2.4 Common-mode Modulation

CM modulation is a technique that can be applied in BD modulated Class-D amplifiers. Since a zero-output level can be made by pulling both bridge halves to supply or ground, a degree of freedom exists. By randomizing the switching pattern for the zero-output level, the CM power is spread over a larger frequency range and consequently, EMI is reduced. In [44] the randomization is done using a pseudo-random sequence. A more advanced method is used in [46], where the pseudo-random sequence is noise shaped, specifically to have notches around defined AM radio frequencies. Finally the authors of [47] proposed a different BTL topology with two extra transistors to be able to shunt the load accompanied by a 3-level modulation scheme.

2.5 Multi-phase

Extending upon the BTL topology, multi-phase output stages have been made. A multi-phase output stage consists of more than two half bridges driving the load either single-ended or in a BTL configuration. Figure 2.7 shows a four-phase BTL system. The parallel inductors at each side sum the current from their respective stages at each side of the load.

The modulation for this kind of output stage is done by using four carriers that are equidistantly spaced in phase. Each carrier is used to modulate the input signal to generate four different PWM signals to drive their respective half-bridge. By using this modulation approach, the ripple voltage over the load is reduced with respect to the ripple in a conventional BTL output stage. As a result the radiated EMI will be reduced. Multi-phase systems and their ripple characteristics will be explored more thoroughly in Chapter 3.

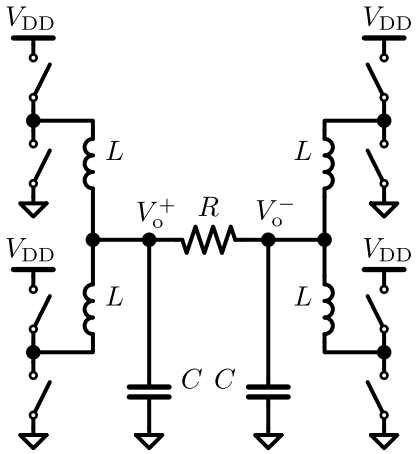
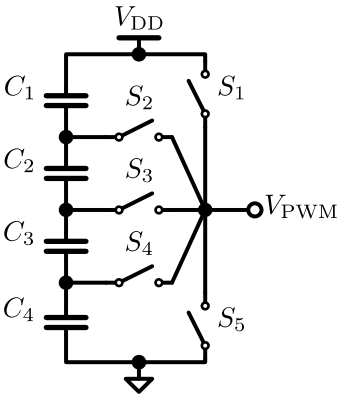


Figure 2.7: A four-phase Class-D output stage.

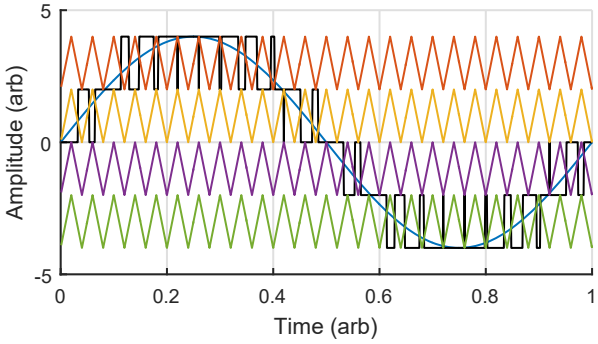
2.6 Multi-level

Multi-level converters are prevalent in the field of high-voltage alternating current (AC) generation which is used in for instance variable speed drives and uninterruptable power supplies. A DC bus voltage is subdivided into smaller voltages by a bank of capacitors. By using switches these voltages can be applied to the load at the output of the converter. Having more levels allows a better approximation of the output voltage because the voltage ripple is reduced.

Multi-level systems can be seen as the dual to multi-phase systems. Where inductors are used in multi-phase systems to sum the output currents, in multi-level systems, capacitors are used to generate different output voltage levels.



(a) An ideal multi-level output stage.



(b) Multi-level PWM modulation.

Figure 2.8: Ideal multi-level output stage with its waveform.

An ideal example of a 5-level multi-level converter is shown in Figure 2.8a. A subdivision of the supply is made using four capacitors of equal size to obtain 5 voltage levels that are spaced by a voltage of $V_{\mathrm{DD}}/4$ consecutively. By closing one switch at a time, the corresponding level can be connected to the output terminal. No more than one switch should be closed at a time to prevent short circuiting the capacitors. Hence, a non-overlapping switching scheme should be used.

The modulation for such a 5-level converter can be done by using four offset triangular carriers as shown in Figure 2.8b. The decisions are made by four comparators, resulting in a thermometer coded representation of the input signal. Logic is used to convert the thermometer code to a one-hot code to actuate the switches.

Evidently, since capacitors are used to provide the charge for the inner levels, a way to balance the charges on the capacitors should be implemented. The more voltage levels, the harder it becomes to make a controller that can achieve an acceptable charge balance during operation.

2.6.1 Possible Topologies

In literature roughly three different topologies are found to realize a multi-level converter. These three are called the diode-clamped-, stacked H-bridge- and flying capacitor converters [56–58]. In the next sections, each of these converters will be discussed in further detail.

2.6.2 Diode-clamped

The diode-clamped structure is shown in Figure 2.9. Like in the ideal converter a string of capacitors is used to make the voltage subdivision. The inner voltage levels are connected to the switches via two diodes, the clamping diodes. These diodes serve as voltage clamps to ensure that the voltage drop over the switches in their off state is equal to or lower than one level. Due to this clamping effect the maximum voltage stress per switch is reduced allowing the use switches with a lower breakdown voltage, saving component costs [59].

The switching sequence of the diode clamped converter will be discussed here. During operation of the 3-level converter in Figure 2.9 two switches are closed while the other two are open. A table showing the three possible switch states is shown in Table 2.1.

Other switch states are not allowed in order to have safe operation, for instance, when switches S_1,S_2 and S_4 are closed the voltage stress on S_3 will become V_{DD} or when switches S_1,S_2 and S_3 are closed, C_2 is connected to the supply.

The diode-clamped topology has diodes in the signal path which will cause severe degradation in THD. The diode forward voltage is also significant when compared to the supply of audio amplifiers, reducing

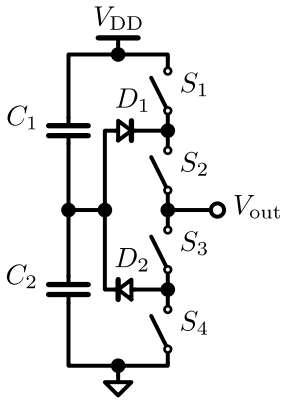


Figure 2.9: A 3-level diode-clamped converter.

Table 2.1: Switch conditions for a 3-level diode-clamped converter.

V_{out}	S_1	S_2	S_3	S_4
V_{DD}	1	1	0	0
$V_{DD}/2$	0	1	1	0
0	0	0	1	1

amplifier efficiency. Therefore, the diode-clamped topology is not suitable to make an audio amplifier with good performance.

Equivalent Schematic

The 3-level diode-clamped converter circuit can be shown in a parallel fashion instead of the totem-pole representation used in most papers. This way of drawing the circuit, shown in Figure 2.10, can more intuitive to understand.

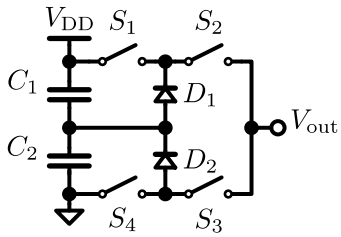


Figure 2.10: Parallel representation of the diode-clamped circuit.

More Levels

The diode-clamped converter can be extended to multiple levels by increasing the number of capacitors, switches and diodes. An extra level requires 1 capacitor, 2 switches and 2 diodes, rated appropriately for the voltage they have to sustain. The real challenge in having multiple levels lies in the control algorithm to keep the charges on the capacitors balanced.

2.6.3 Stacked H-bridge

As the name suggests, the stacked H-bridge is a cascade of separate H-bridges. A 5-level converter is shown in Figure 2.11. In order to make this topology work all the direct current (DC) sources should be decoupled from each other to allow stacking of the DC voltages. The possible switch conditions and corresponding output voltages of a single H-bridge are given in Table 2.2

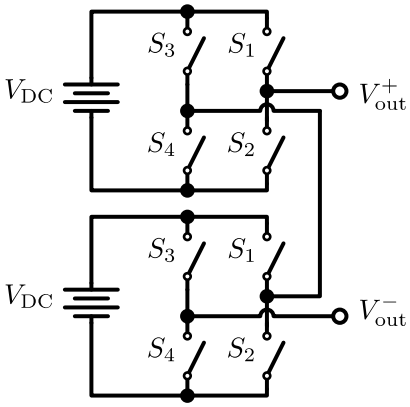


Figure 2.11: A 5-level stacked H-bridge converter.

Table 2.2: Switch conditions for an H-bridge.

V_{out}	S_1	S_2	S_3	S_4
V_{DC}	1	0	0	1
0	1	0	1	0
0	0	1	0	1
$-V_{\text{DC}}$	0	1	1	0

By connecting another H-bridge in series it is possible to add or subtract V_{DC} to the output of the first H-bridge creating two extra levels of $\pm 2V_{\text{DC}}$. While the idea of this converter looks practical because there are no capacitors required, it does require multiple independent DC-sources. When these are available, which is the case in electric cars with multiple batteries and photo-voltaic systems consisting of several cells, this is a viable converter however in the other cases the use of a stacked H-bridge converter is impractical.

In, for instance, photo-voltaic systems a DC voltage is generated and has to be converted into a 3-phase AC voltage before it can be delivered to the power grid. For this case it is possible to use the stacked H-bridge because the individual supply voltages can be made by grouping photo-voltaic cells.

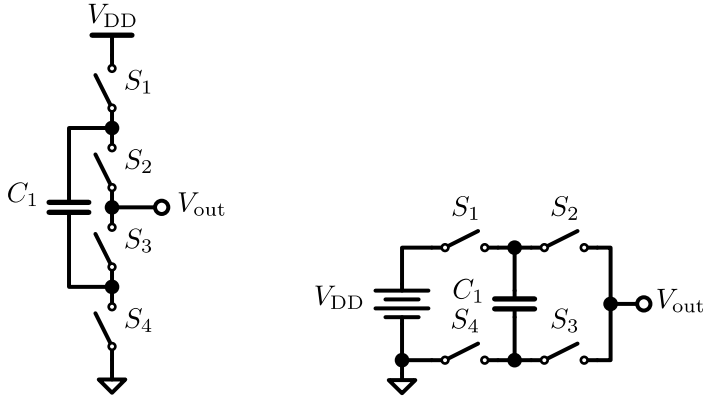
More Levels

By stacking more H-bridges in series, more levels can be generated. Each extra H-bridge adds 2 levels and requires 4 switches and a supply.

2.6.4 Flying capacitor

The third converter that is commonly used is the so called 'flying' capacitor converter. The terminology comes from the fact that neither of the terminals

of the capacitors are connected to ground or the supply rail, hence it is floating or 'flying'. A 3-level flying capacitor converter is shown in Figure 2.12. These two representation of the flying capacitor circuit are both commonly found in literature and shown here for completeness.



(a) Totem-pole. (b) Parallel.

Figure 2.12: Showing two representations of the same flying capacitor circuit.

The switching conditions for the flying capacitor converter are tabulated in Table 2.3. Here V_{C_1} is the voltage over the flying capacitor C_1. By controlling the switch states it is possible to regulate V_{C_1} to $V_{DD}/2$ yielding a voltage of $V_{DD}/2$ for both states in the middle of the table. To do this, the switch states are chosen by a feedback loop in such a way that the flying capacitor is charged or discharged in the direction of $V_{C_1} = V_{DD}/2$.

Table 2.3: Switch conditions for the 3-level flying capacitor topology.

V_{out}	S_1	S_2	S_3	S_4
V_{DD}	1	0	0	1
$V_{DD} - V_{C_1}$	1	0	1	0
V_{C_1}	0	1	0	1
0	0	1	1	0

The switch states are illustrated in Figure 2.13 showing all four possible switch states with their corresponding output voltage. The red marked wires indicate the current path to the output referred from the ground.

More Levels

As for the other topologies, it is possible to add more levels to the flying capacitor topology. This is achieved by inserting additional parallel capacitors with switches. Each extra section adds 1 level and requires 2 switches and an extra capacitor. Balancing the charges requires increasingly complex

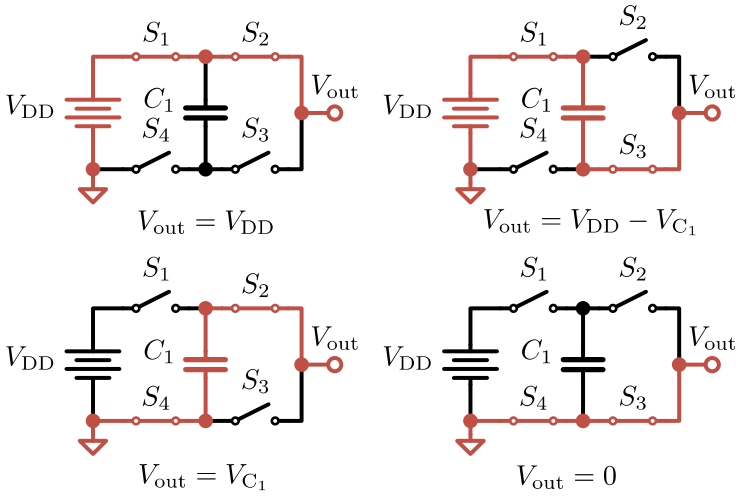


Figure 2.13: Visualized flying capacitor switch conditions.

algorithms to choose the correct combinations for every switching action when the number of capacitors is increased [57].

2.6.5 Multi-level Summary

The three most common multi-level converter stages have been discussed. To get an idea of the required components and the series resistance in each topology as function of the amount of subsections, they are conveniently listed in Table 2.4. The assumption here is that all the capacitors are equally

Table 2.4: Component requirements at increasing levels.

Topology	Levels	Switches	Caps	Diodes	DC	Series switches
Diode clamped	$n+1$	$2n$	n	$2(n-1)$ †	1	n ‡
Stacked H-bridge	$2n+1$	$4n$	0	0	n	$2n$
Flying capacitor	$n+1$	$2n$	$n-1$	0	1	n

† At higher levels, diodes with different breakdown voltages are used.
‡ Also taking series diodes into account.

charged. For the diode clamped and flying capacitors topologies $n = 1$ corresponds to an elementary half bridge, for the stacked H-bridge $n = 1$ corresponds to one H-bridge.

2.6.6 Multi-level realizations of audio amplifiers

Multi-level converter systems are commonly used to generate 3-phase outputs for interfacing with the power grid or to make variable frequency

drives for motor control. It is also possible to operate two converters in 2-phase or BTL mode to drive a loudspeaker. We will focus on applications for audio amplifiers.

The diode-clamped converter is not a good fit for audio amplifiers because of the distortion and efficiency penalty due to the diodes. A stacked H-bridge approach might be usable for an audio amplifier, however the number of required supply rails make it impractical to implement. This leaves the flying capacitor as the most suitable candidate, since it requires a single supply and no diodes.

A 5-level audio amplifier has been presented in [60]. Two 3-level flying capacitor converters were used in a filter-less BTL configuration to obtain five discrete output levels. The configuration is shown in Figure 2.14. By doubling the number of components almost twice the output levels are obtained, the exact number is $2N - 1$ with N the number of levels in a single stage. The flying-capacitor topology is proven to be suitable for implementing an audio amplifier.

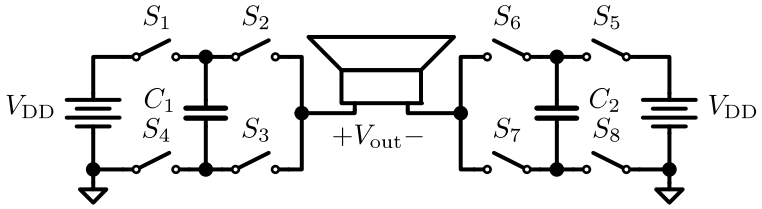


Figure 2.14: 5-level BTL flying capacitor implementation.

In both [47] and [61], a 3-level output stage is made by adding a load shunt mode to a conventional BTL output stage. CM EMI is reduced by using an AD switching scheme. Another work utilizing a 7-level output stage with AD switching was presented in [62]. Extra supply voltages are used to provide intermediate levels, which does increase the cost of this application.

2.7 Active Ripple Compensation

Class-AB/D is a technique that combines a linear amplifier with a switched-mode amplifier to improve efficiency by delivering most of the power via the switched-mode amplifier instead of the linear amplifier. A feedback loop is built around the linear amplifier to compensate the imperfections, such as distortion and the ripple current, of the switched-mode amplifier. The switched-mode can be controlled by sensing the current of the AB amplifier and using hysteretic control. However, it is difficult to make high loop gain over both the audio band and the PWM frequency range using analog filters while ensuring stability, moreover the AB amplifier will draw a quiescent bias current [49–52].

2.8 Feed-forward Cancellation

A feed-forward system that detects and injects an anti-ripple was designed in [63] giving high suppression of both the fundamental and harmonics of the switching frequency. The stationary nature of DC/DC conversion eases characterization of the ripple current, because the output voltage is regulated to be relatively constant. A least mean squares (LMS) algorithm is used to successively approximate the cancellation signal by adding residual errors to it until emission requirements are met or when the hardware limits further optimization. Variations in output voltage, load current and temperature are accounted for by having a look-up table with pre-defined coefficients for those different operation conditions. Suppression ranges from 50 dB at the fundamental to 30 dB at the 20^{th} harmonic.

Such a control scheme does not lend itself well for audio applications, as the load voltage and current changes rapidly in contrast to the steady state behavior that is present in DC/DC converters.

2.9 Research Questions

In this thesis we would like to reduce the radiated electromagnetic interference from the speaker leads originating from high-frequency switching in a Class-D power stage. A few questions have been formulated around this goal:

- Can the power at the PWM switching frequency after the output filter of the amplifier be reduced?
- Should feed-forward or feedback be used, or a combination?
- How to realize a power efficient implementation with a low component count?

Throughout the research, additional questions have surfaced:

- Is it possible to make an add-on circuit to implement this?
- Can this circuit be implemented using the existing AX5689 IC?
- How can we design loop filters with parasitics in the loop?

2.10 Conclusion

In this chapter we have discussed the mechanism behind EMI after the output filter. The EMI greatly depends on the used modulation scheme and techniques for EMI reduction from prior art have been presented.

The FM and CM modulation techniques result in spreading the power of the interference over a wider band effectively increasing the noise floor.

In Class-AB/D a lot of quiescent power is spent to eliminate the ripple in idle conditions, which is bad for efficiency.

The vast amount of components required to make a multi-level output stage compared to a conventional BTL output stage are a disadvantage for making a cost effective solution for consumer electronics. Furthermore, implementations that include diodes will have undesired distortion because of their non-linear signal transfer, making them unsuitable for audio applications. Because of these reasons it was chosen to not further pursue this direction to reduce EMI in Class-D amplifiers.

Extending the flying capacitor topology to more levels will require a sophisticated controller to maintain the charge balance between the capacitors, which could be a topic for further research.

Both the multi-phase and active ripple compensation strategies are candidates for further research and are discussed in more detail in chapters 3 and 4.

CHAPTER 3

MULTI-PHASE CLASS-D

The concept of a multi-phase Class-D amplifier was briefly discussed in the previous chapter. In the current chapter we will dive deeper into the behavior of multi-phase output stages. Note that this chapter provides information on a topic that was explored but later set aside. It is not essential for the next chapters of this thesis. First the current ripple of a single-ended output stage is discussed, followed up by a two-phase system. Subsequently a generalization for any number of phases is shown and the load ripple voltage is determined as well.

Next up, a discussion on output filters is done. The effect of adding phases on the required component values is shown and inductor non-idealities are discussed. Subsequently, by using equations it is shown how quantities such as ripple voltage, ripple current, inductance per leg, stored energy, magnetic field and series resistance are related in systems with multiple phases. Then, a trade-off is presented to show the variation in the aforementioned quantities depending on the amount of phases. Finally the practical issues of implementing multi-phase systems are discussed.

A multi-phase output stage consists of multiple half bridges driving the load either single-ended (SE) or in a BTL configuration. Figure 3.1 shows an example four-phase SE system. The parallel inductors sum the currents from their respective stages at the left side of the load.

The modulation for this kind of output stage is done by using four carriers that are equidistantly spaced in phase. Each carrier is used to modulate the input signal to generate four different PWM signals to drive their respective half-bridge. By using this modulation approach, the ripple voltage over the load is reduced with respect to the ripple in a conventional BTL output stage. The effect of a multi-phase topology on the inductor and load current ripple is investigated as a lower ripple current generates less EMI.

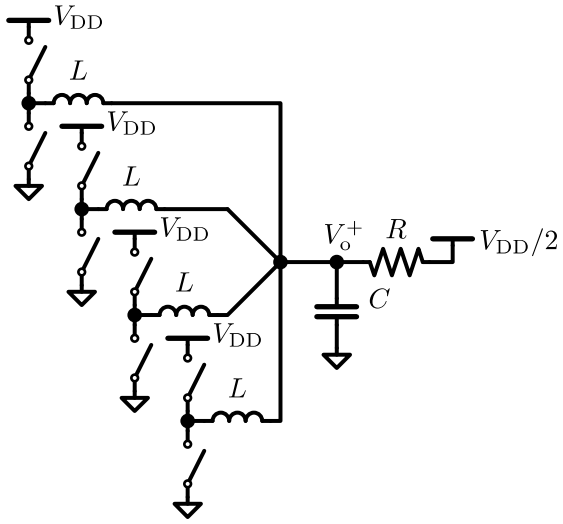


Figure 3.1: A four-phase Class-D output stage.

3.1 1-phase Ripple Current

A single-ended Class-D amplifier output stage is shown in Figure 3.2. The supply voltage is indicated with V_{DD}, D is the duty cycle of the upper switch and V_{o} is the output voltage. For the derivation of the ripple current through the inductor ΔI_{rip} it is assumed that the variations in the output voltage V_{o} due to the currents flowing in and out of the capacitor are small, hence V_{o} is assumed to be constant.

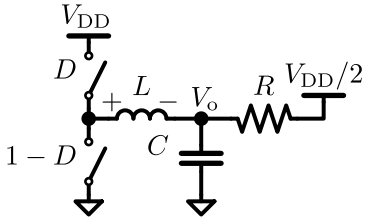


Figure 3.2: An ideal Class-D output stage.

The positive and negative ripple currents can be described as [64],

$$\Delta I_{\mathrm{rip,up}} = \frac{D \cdot T}{L} \left(V_{\mathrm{DD}} - V_{\mathrm{o}} \right) \tag{3.1}$$

$$\Delta I_{\mathrm{rip,down}} = \frac{(1-D) \cdot T}{L} \cdot -V_{\mathrm{o}}. \tag{3.2}$$

Equating these as $\Delta I_{\text{rip,up}} = \Delta I_{\text{rip,down}}$ yields,

$$\begin{aligned}\frac{D \cdot T}{L}\left(V_{\text{DD}} - V_{\text{o}}\right) &= \frac{(1-D)\cdot T}{L} \cdot -V_{\text{o}} \\ DTV_{\text{DD}} - DTV_{\text{o}} &= TV_{\text{o}} - DTV_{\text{o}} \\ DV_{\text{DD}} &= V_{\text{o}}.\end{aligned}$$

This is the expected result, the output voltage V_{o} equals the supply voltage V_{DD} times the duty cycle D. Substituting this result back into (3.1) gives,

$$\Delta I_{\text{rip,up}} = \frac{D(1-D)\cdot T}{L} V_{\text{DD}} = -\Delta I_{\text{rip,down}}. \tag{3.3}$$

The maximum ripple is found by taking the derivative with respect to D and equating it to 0,

$$\begin{aligned}\frac{\partial\left(D(1-D)\right)}{\partial D} &= 0 \\ 2D - 1 &= 0 \\ D &= \frac{1}{2}.\end{aligned}$$

Subsituting this for D in (3.3) yields,

$$\Delta I_{\text{rip,up,max}} = \frac{V_{\text{DD}} T}{4L}, \tag{3.4}$$

3.2 Ripple in Two-phase systems

In a SE system with 2 phases, the ripple current waveforms in both coils are equal in a steady state situation, however one is shifted half a period with respect to the other. The ripple current flowing through the capacitor C is the sum of both ripple currents over time. This yields a ripple current having twice the frequency with respect to the individual ripple currents.

The simulation in Figure 3.3 shows that this is the case. Observe that second half of the line representing phase 1 is identical to the first half of phase 2 and vice-versa. This implies that the addition of the two phases yields a waveform of which the first half is equal to the second half. Due to this fact it is possible to find the maximum ripple by just taking one period of the summed phases into account.

Two different conditions have to be considered, namely $D > 1/2$ and $D < 1/2$. The slopes of the increasing and decreasing part of the sum ripple current can be determined by adding the slopes of the single phase. The slopes of the single phases are determined by dividing the ripple by the period times the duty cycle,

$$\begin{aligned}\left.\frac{\partial I}{\partial t}\right|_{\text{up}} &= \frac{\Delta I_{\text{rip,up}}}{DT} \\ &= \frac{(1-D)V_{\text{DD}}}{L},\end{aligned} \tag{3.5}$$

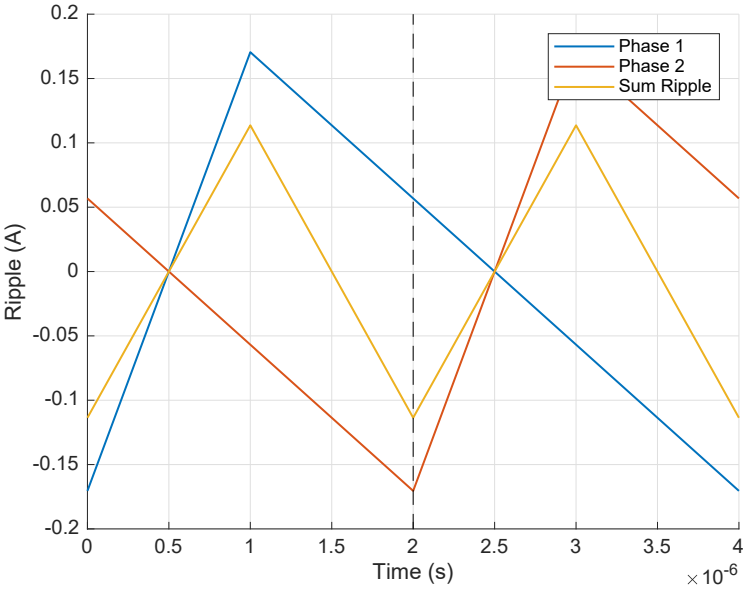


Figure 3.3: Simulated ripple currents for 2-phase operation, $L = 22\,\mu\text{H}, T = 4\,\text{ns}, V_{\text{DD}} = 10\,\text{V}, D = 1/4$.

$$\left.\frac{\partial I}{\partial t}\right|_{\text{down}} = \frac{\Delta I_{\text{rip,down}}}{DT} = \frac{-D \cdot V_{\text{DD}}}{L} . \tag{3.6}$$

Figure 3.3 shows that there are two possibilities for addition, namely the rising slope plus the falling slope or two times the falling slope. This case is specific for $D < 1/2$ and the slopes of the summed ripple signal will be,

$$\left.\frac{\partial I_{\text{sum}}}{\partial t}\right|_{\text{up}} = \left.\frac{\partial I}{\partial t}\right|_{\text{up}} + \left.\frac{\partial I}{\partial t}\right|_{\text{down}} \tag{3.7}$$

$$\left.\frac{\partial I_{\text{sum}}}{\partial t}\right|_{\text{down}} = 2 \cdot \left.\frac{\partial I}{\partial t}\right|_{\text{down}} , \tag{3.8}$$

for $D > 1/2$ a different set of equations is derived,

$$\left.\frac{\partial I_{\text{sum}}}{\partial t}\right|_{\text{up}} = 2 \cdot \left.\frac{\partial I}{\partial t}\right|_{\text{up}} \tag{3.9}$$

$$\left.\frac{\partial I_{\text{sum}}}{\partial t}\right|_{\text{down}} = \left.\frac{\partial I}{\partial t}\right|_{\text{up}} + \left.\frac{\partial I}{\partial t}\right|_{\text{down}} . \tag{3.10}$$

An expression for the ripple current within the corresponding interval of the duty cycle can be obtained by multiplying the slope with the duration of the the corresponding falling or rising part. The most convenient expression to use for the derivation is the falling slope (3.8). The duration

of this part of the waveform is obtained by calculating the duty cycle D' of the summed phases. The sum period T' is halved with respect to the single phases, $T' = T/2$. The sum duty cycle D' is double the single phase duty cycle, yielding $D' = 2D$. The falling slope of the waveform has a duty cycle of $1 - D'$, hence the ripple current can be described as,

$$\begin{aligned}\Delta I_{\text{rip,down}} &= 2 \cdot \left.\frac{\partial I}{\partial t}\right|_{\text{down}} \cdot (1 - D')T' \\ &= 2 \cdot \frac{-D \cdot V_{\text{DD}}}{L} \cdot (1 - 2D)\frac{T}{2} \\ &= \frac{-D(1 - 2D) \cdot V_{\text{DD}}T}{L}.\end{aligned} \tag{3.11}$$

The maximum ripple is found by taking the derivative with respect to D and evaluating it a 0,

$$\begin{aligned}\frac{\partial\left(-D(1 - 2D)\right)}{\partial D} &= 0 \\ 4D - 1 &= 0 \\ D &= \frac{1}{4}.\end{aligned}$$

Subsituting this for D in (3.11) yields,

$$\Delta I_{\text{rip,down,max}} = -\frac{V_{\text{DD}}T}{8L}, \tag{3.12}$$

which is half the value of the maximum for a single phase.

3.3 Ripple in Multi-phase Systems

Instead of using 2 phases, the derivation can also be carried out for n phases. For $D < 1/n$ (3.8) will become,

$$\left.\frac{\partial I_{\text{sum}}}{\partial t}\right|_{\text{down}} = n \cdot \left.\frac{\partial I}{\partial t}\right|_{\text{down}}. \tag{3.13}$$

For n phases the period is split into n parts giving $T' = T/n$ and $D' = nD$. Which yields the ripple current,

$$\begin{aligned}\Delta I_{\text{rip,down}} &= n \cdot \left.\frac{\partial I}{\partial t}\right|_{\text{down}} \cdot (1 - D')T' \\ &= n \cdot \frac{-D \cdot V_{\text{DD}}}{L} \cdot (1 - nD)\frac{T}{n} \\ &= \frac{-D(1 - nD) \cdot V_{\text{DD}}T}{L}.\end{aligned} \tag{3.14}$$

The maximum ripple is found by taking the derivative with respect to D and equating it to 0,

$$\begin{aligned}\frac{\partial\left(-D(1-nD)\right)}{\partial D} &= 0\\ 2nD-1 &= 0\\ D &= \frac{1}{2n}.\end{aligned}$$

Subsituting this for D in (3.11) yields,

$$\Delta I_{\mathrm{rip,down,max}} = -\frac{V_{\mathrm{DD}}T}{4nL}, \tag{3.15}$$

which is 1 over n times the value of the maximum for a single phase. The maximum ripple current as a function of the number of phases becomes,

$$\Delta I_{\mathrm{rip,max}}(n) = \frac{V_{\mathrm{DD}}T}{4nL}. \tag{3.16}$$

This is visualized up to 8 phases in Figure 3.4, which shows that for each extra phase a null is added and that the maximum ripple current decreases.

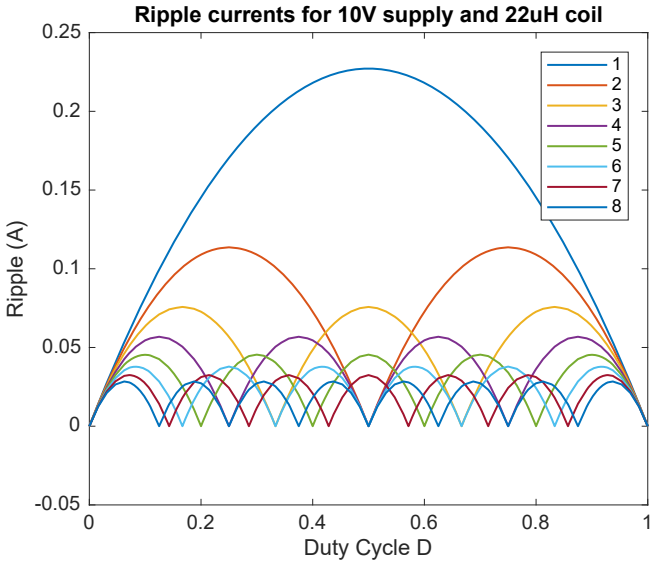


Figure 3.4: Ripple current versus duty cycle for increased phases.

3.4 Load Ripple

It was assumed that the V_o in Figure 3.2 is constant. To do a first order approximation of the voltage ripple over the load we look at the voltage over the capacitor due to the ripple current. The constitutive relation for the capacitor is,

$$v_C(t) = \frac{1}{C}\int_0^t i_C(\tau)\,\mathrm{d}\tau. \tag{3.17}$$

In a steady state situation the rising and falling parts have an identical ΔI_{rip}. The voltage ripple is determined by substituting the ripple current into the integral equation (3.17). This yields two integrals, one for the rising and one for the falling slope of the ripple current,

$$\begin{aligned}\Delta v_C =& \frac{1}{C}\int_{DT/2}^{DT} \frac{\Delta I_{\text{rip}}}{DT}(\tau - DT/2)\,\mathrm{d}\tau \\ &+ \frac{1}{C}\int_{DT}^{(D+(1-D)/2)T} \frac{-\Delta I_{\text{rip}}}{(1-D)T}(\tau - DT)\,\mathrm{d}\tau.\end{aligned} \tag{3.18}$$

Evaluating the integrals and simplification gives,

$$\Delta v_C = \frac{\Delta I_{\text{rip}} \cdot T}{8C}\left(D + (1-D)\right) = \frac{\Delta I_{\text{rip}} \cdot T}{8C} = \frac{\Delta I_{\text{rip}}}{8fC}, \tag{3.19}$$

which is the enclosed triangular area within the current ripple waveform above the x-axis (see e.g. Figure 3.3). The expression also has a close resemblance to the frequency domain transfer of a sine wave, namely,

$$v_C(f) = \frac{i_C}{j2\pi fC}. \tag{3.20}$$

Using the frequency domain transfer will overestimate the ripple by a factor $4/\pi$ with respect to (3.19).

3.4.1 Multi-phase load ripple

In multi-phase systems the frequency of the ripple current I_{rip} through the capacitor increases linearly with the number of phases as $f_{\text{rip}} = f_{\text{PWM}} \cdot n$ and thus,

$$\Delta V_{\text{rip,load}}(n) = \frac{\Delta I_{\text{rip}} \cdot T}{8nC} = \frac{\Delta I_{\text{rip}}}{8nfC}. \tag{3.21}$$

Substitution of the expression for the maximum ripple current (3.16) yields the maximum ripple voltage over the load,

$$\Delta V_{\text{rip,max,load}}(n) = \frac{V_{\text{DD}}T}{4nL}\frac{T}{8nC} = \frac{V_{\text{DD}}T^2}{32n^2LC} \tag{3.22}$$

3.4.2 Load ripple in BTL

In a BTL configuration with one phase at each side of the bridge there are two filter capacitors that each conduct the ripple current originating from the inductors at their side of the load. To obtain the ripple voltage over the load one cannot simply multiply the expression in (3.22) by two. Instead the solution is obtained by comparing a two-phase SE stage with a BTL stage with one phase per stage.

In the SE stage the two inductor currents are summed in the capacitor and then integrated to obtain the load ripple voltage $\Delta V_{\text{rip,load}}$.

$$V_{\text{rip,load}}(t) = \frac{1}{C}\int_0^t I_{\text{rip},1}(\tau) + I_{\text{rip},2}(\tau)\,\mathrm{d}\tau. \tag{3.23}$$

This differs from the BTL case in that each inductor current is integrated on the capacitor on its side respectively. The DM ripple voltage over the load is the difference between these two voltages. Also note that the ripple current on the other side of the load has changed sign.

$$V_{\mathrm{rip,load,DM}}(t) = \frac{1}{C_1}\int_0^t I_{\mathrm{rip},1}(\tau)\,\mathrm{d}\tau - \frac{1}{C_2}\int_0^t -I_{\mathrm{rip},2}(\tau)\,\mathrm{d}\tau. \tag{3.24}$$

The CM ripple voltage over the load can likewise defined,

$$V_{\mathrm{rip,load,CM}}(t) = \frac{1}{2C_1}\int_0^t I_{\mathrm{rip},1}(\tau)\,\mathrm{d}\tau + \frac{1}{2C_2}\int_0^t -I_{\mathrm{rip},2}(\tau)\,\mathrm{d}\tau. \tag{3.25}$$

Note that for $C = C_1 = C_2$ the expression in (3.24) can be reduced to the expression in (3.23). The comparison is also worked out numerically, resulting in the graphs in Figure 3.5.

The top-left and top-center plots show the inductor ripple current. In a SE design they are added and the top-right plot is obtained. The bottom 3 plots show the integral of the ripple on the left, the negative integral of the ripple in the middle. On the right the DM and CM 'BTL Ripples' are plotted together with the SE ripple. It is shown that the load ripple voltage for a SE 2-phase output stage is equal to DM ripple of a BTL stage, however there is a CM component present in the BTL stage with same $\Delta V_{\mathrm{rip,load}}$ as the two half bridges driving it. One could argue that to reduce the CM ripple, the phase could be inverted. However, for that purpose AD modulation could be used to provide the lowest CM ripple.

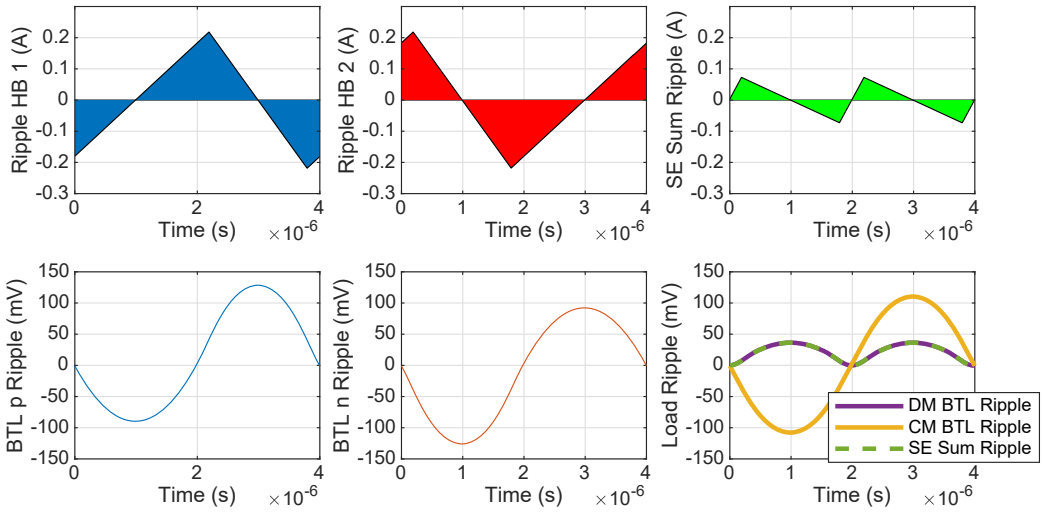


Figure 3.5: Results of the numerical evaluation of the load ripple voltage in both 2-phase SE and BTL configurations.

3.5 Output Filter

A Class-D amplifier is usually connected to the load via an output filter as was depicted in Figure 3.2. For multi-phase systems the filter needs to maintain its characteristics when adding extra switching legs to the load. A system consisting of four switching legs is shown in Figure 3.6. In order

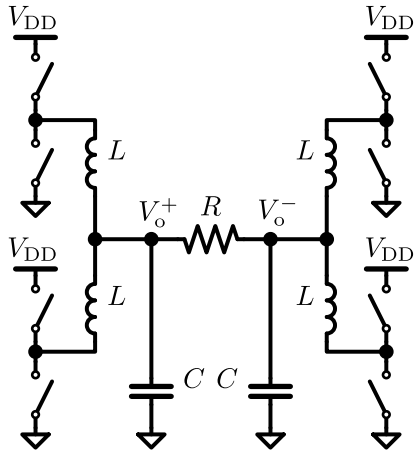


Figure 3.6: A four-phase Class-D output stage.

to visualize the effect of paralleling switching legs, an equivalent circuit is derived by replacing the switches by voltage sources, because for a given duty cycle a switching leg can be seen as a DC voltage. This substituion results in the circuit in Figure 3.7. Further simplification leads to the circuit

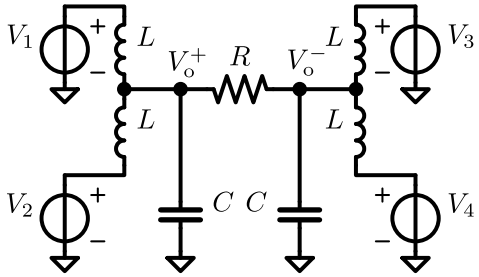


Figure 3.7: A four-phase Class-D output stage.

in Figure 3.8 where the two voltage sources and inductors on both sides of the load are replaced by their Thevenin equivalents. This shows that the inductance L in the output filter is effectively halved with respect to a regular bridge-tied-load configuration. To account for the inductance has to be doubled in this specific case. In general this means that the inductance has to be multiplied by the number of parallel switching legs with respect to the configuration with a single leg.

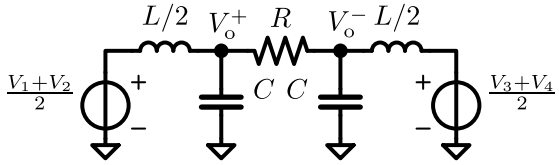


Figure 3.8: A four-phase Class-D output stage.

Summarizing, the inductance in each leg should be,

$$L_{\text{leg}} = L \cdot m, \tag{3.26}$$

with m the number of legs at one side of the load. $m = n$ for single-ended and $m = n/2$ for bride-tied-load.

3.5.1 Dimensioning the Filter

The output filter plus the load forms a parallel RLC circuit. Its transfer function is given by,

$$H_f(j\omega) = \frac{1}{1 + j\omega L/R + (j\omega)^2 LC}. \tag{3.27}$$

The standard second order filter transfer function is described as follows,

$$H_2(j\omega) = \frac{\omega_0}{(j\omega)^2 + j\omega\frac{\omega_0}{Q} + \omega_0^2}, \tag{3.28}$$

with ω_0 the natural frequency and Q the quality factor. By substitution, expressions for ω_0 and Q are obtained from (3.27) and (3.28),

$$\omega_0 = \frac{1}{\sqrt{LC}}, \tag{3.29}$$

and,

$$Q = R\sqrt{\frac{C}{L}}. \tag{3.30}$$

In an audio system the impedance of the speaker is fixed and between $4\,\Omega$ and $8\,\Omega$. Likewise the cut-off frequency is also fixed and should be around $30\,\text{kHz}$ to maintain a flat pass-band in the audio range from $20\,\text{Hz}$ through $20\,\text{kHz}$ and to provide enough suppression of the carrier. A third requirement is the quality factor, since the system should not be allowed to ring. This limits the design space for the second order LC filter as R, ω_0 and Q are fixed.

By substituting for L and C in equations (3.29) and (3.30) expressions for L and C are found,

$$L = \frac{R}{Q\omega_0}, \tag{3.31}$$

$$C = \frac{Q}{R\omega_0}. \tag{3.32}$$

Using these expressions it is possible to calculate the component values of the required inductor and capacitor in the filter. To take into account real-world values of components the calculated values will be rounded toward the nearest possible component value in the 'E6'-range. The values are 1, 1.5, 2.2, 3.3, 4.7 and 6.8 multiplied by the order of magnitude 10^x.

The required component values for output filter in a SE and BTL Class-D amplifier are tabulated in Table 3.1. Subsequently the resulting natural frequency and quality factor are recalculated from the 'E6' component values. The table uses f_0 which is $\omega_0/2\pi$.

Table 3.1: Ideal and real-world component values for $f_0 = 30\,\mathrm{kHz}, Q = 0.7$

	$R(\Omega)$	$L(\mu H)$	$C(\mu F)$	$L_{comp}(\mu H)$	$C_{comp}(\mu F)$	$f_{comp}(Hz)$	Q_{comp}
SE	4	30.3	0.928	33	1	27705	0.696
	6	45.5	0.619	47	0.68	28152	0.722
	8	60.6	0.464	68	0.47	28152	0.665
BTL	4	15.2	1.857	15	2.2	27705	0.766
	6	22.7	1.238	22	1	33932	0.640
	8	30.3	0.928	33	1	27705	0.696

It immediately becomes evident that it is not possible to realize the exact filter specification using real world component values. Changing either one of the components values will result in a relative change in Q and f_0 of approximately $\sqrt{1.5} = 1.22$, the ratio of subsequent 'E6' values. Consequently this means that if f_0 has to be kept constant, then Q can be changed by a factor of 1.5 for each subsequent step, since both L and C change Q by a factor of $\sqrt{1.5}$.

If the carrier frequency is sufficiently high, it is possible to use a higher filter cut-off frequency by reducing the inductance. When we also remove the Q constraint, even lower inductor values are possible, allowing the use of smaller, cheaper inductors.

3.5.2 Inductor Non-idealities

Power inductors utilize a ferrite core to provide high self-inductance values. This structure has a non-linear inductance depending on the current flowing trough it. Effects that influence this behavior are hysteresis and eddy currents due to the core material, furthermore the maximum current is limited by saturation of the magnetic field in the core material. Saturation occurs when an external field H is applied that will not increase the magnetization B any further. This phenomenon is illustrated in Figure 3.9 for ferromagnetic materials, showing the dependence of the flux density B and relative permeability μ_r on the magnetizing field H. In general ferrites saturate when an external field H between $0.2\,\mathrm{T}$ and $0.5\,\mathrm{T}$ is applied [65] .

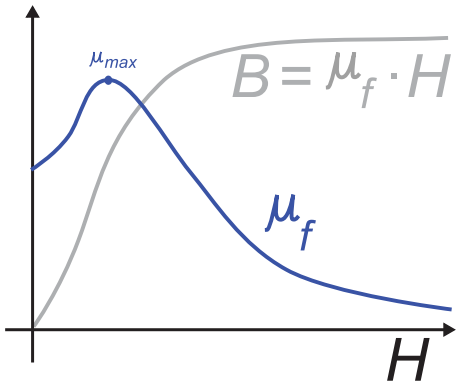


Figure 3.9: Magnetic saturation occurs when H is increased.

3.5.3 Relations for the Inductance

The general relation for the inductance L of an ideal solenoid coil as shown in Figure 3.10 is derived from the following relations,

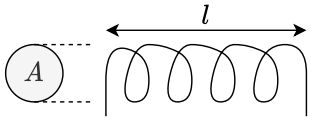


Figure 3.10: Schematical representation of a solenoid.

$$B = \frac{\mu_0 \mu_r N i}{l}, \tag{3.33}$$

describing the flux density B in the core with μ_0 the permeability of vacuum, μ_r the relative permeability of a ferromagnetic material, N the number of windings, i the current and l the length of the solenoid.

$$\Phi = BA = \frac{\mu_0 \mu_r N i A}{l}, \tag{3.34}$$

giving the magnetic flux Φ through the cross-section A. Substitution in the definition of inductance,

$$L = \frac{N\Phi}{i}, \tag{3.35}$$

gives,

$$L = \frac{\mu_0 \mu_r N^2 A}{l}, \tag{3.36}$$

with μ_0 the permeability of vacuum, μ_r the relative permeability, N the number of windings, A the cross-section and l the length of the solenoid. Take note that these equations do not hold for inductors with high permeability core materials. As a rule of thumb, the length should be μ_r times

the width of core for the formula to be valid. Hence these equations are not valid for ferrites which have a μ_r between 1500 and 3000.

In applications, the μ_r parameter is influenced by the current through the coil inducing the magnetizing field: $\mu_r(i)$. Datasheets give current ratings at which the inductance L has dropped $10\,\%$ or $20\,\%$ with respect to the nominal value. It is also seen that the same core is used with a different number of windings, this makes high inductance coils have a lower current rating as the core magnetization is proportional to the windings times the current, $N \cdot i$. This can be shown by applying the constitutive relation $H = B/\mu_0\mu_r$ to (3.33) giving,

$$H = \frac{Ni}{l}. \tag{3.37}$$

3.5.4 Energy Storage

The inductor is an energy storage element and the energy stored in the inductor is quadratically proportional to the current,

$$E = \frac{1}{2}Li^2. \tag{3.38}$$

The energy stored in the core has a given limit due to the saturation effect mentioned earlier. The amount of energy that can be stored is not affected by the amount of turns N. This can be seen from (3.36) and (3.38), when N is doubled and i is halved to maintain the same H field the inductance L will quadruple. When these values are substituted in (3.38) we get,

$$E = \frac{1}{2}(4L)(i/2)^2 = \frac{1}{2}Li^2, \tag{3.39}$$

showing that the energy stored is independent of the number of turns N and proportional to the H field meaning that the maximum stored energy is only dependent on the saturation of the core material.

3.5.5 Series Resistance

Another property of a real inductor is the series resistance from the wire that is wound around the core. The general relation for the series resistance of a wire is,

$$R = \rho \cdot \frac{\ell}{A}, \tag{3.40}$$

with ρ the specific resistance, A the cross-sectional area and ℓ the length of the wire.

Assuming that the wire thickness is the same regardless of the number of turns N, then the series resistance R is proportional to N because $\ell = \ell_{\text{turn}} \cdot N$. This differs from the inductance which is proportional as $L \propto N^2$ from (3.36).

3.6 Multi-phase Trade-off

The most common phenomena in multi-phase output stages have been discussed. To find out if it is possible to use smaller components a concise trade-off is summarized using the derived relations (3.16) (3.26) (3.21) (3.36) (3.37) (3.38) (3.40) which are relisted here for convenience,

$$\Delta I_{\mathrm{rip,max}}(n) = \frac{V_{\mathrm{DD}}T}{4nL}, \tag{3.41}$$

$$L_{\mathrm{leg}} = L \cdot m, \tag{3.42}$$

$$\Delta V_{\mathrm{rip,max,load}}(n) = \frac{V_{\mathrm{DD}}T^2}{32n^2LC}, \tag{3.43}$$

$$L = \frac{\mu_0\mu_r N^2 A}{l}, \tag{3.44}$$

$$H = \frac{Ni}{l}, \tag{3.45}$$

$$E = \frac{1}{2}Li^2, \tag{3.46}$$

$$R = \rho \cdot \frac{\ell}{A}. \tag{3.47}$$

The formulas are combined to form the expressions in Table 3.2.

- The first expression for the filter inductance is formed by taking (3.42) and substituting $m = n$ for single-ended and $m = n/2$ for bride-tied-load, because $L_{2\mathrm{phase}}$ is the inductance used in a 2-phase system.
- The maximum capacitor ripple current is found by substituting the previous expressions into (3.41).
- The ripple current per leg is n times larger than through the capacitor.
- The ripple voltage over the load is reduced by a factor n with respect to the capacitor ripple current.
- To get a certain inductance, a wire has to be wound N times around the core material. N is proportional to the root of the inductance as seen in (3.44).
- The maximum current before saturation of the core is dependent on the number of turns and the saturation magnetizing field H_{sat} as was obtained from (3.45).
- The maximum energy that can be stored in the inductor is likewise proportional to the saturating field H_{sat} and is also calculated using the formula given in (3.46).
- Finally the series resistance per leg is given using (3.47), where the length ℓ of the wire is N times the length of a single turn ℓ_{turn}.

Table 3.2: Single-ended and BTL comparison for n phases

Quantity	**Symbol**	**SE**	**BTL**
Filter inductance	$L_{\mathrm{filter}}(n)$	$L_{1\mathrm{phase}} \cdot n$	$L_{2\mathrm{phase}} \cdot n/2$
Leg ripple current	$\Delta I_{\mathrm{rip,max,leg}}(n)$	$\frac{V_{\mathrm{DD}}T}{4nL_{1\mathrm{phase}}}$	$\frac{V_{\mathrm{DD}}T}{2nL_{2\mathrm{phase}}}$
Capacitor ripple current	$\Delta I_{\mathrm{rip,max,cap}}(n)$	$\frac{V_{\mathrm{DD}}T}{4n^2L_{1\mathrm{phase}}}$	$\frac{V_{\mathrm{DD}}T}{n^2L_{2\mathrm{phase}}}$
Capacitor ripple voltage	$\Delta V_{\mathrm{rip,max,cap}}(n)$	$\frac{V_{\mathrm{DD}}T^2}{32n^3L_{1\mathrm{phase}}C}$	$\frac{V_{\mathrm{DD}}T^2}{4n^3L_{2\mathrm{phase}}C}$
Load ripple voltage (DM)	$\Delta V_{\mathrm{rip,max,ld,DM}}(n)$	$\frac{V_{\mathrm{DD}}T^2}{32n^3L_{1\mathrm{phase}}C}$	$\frac{V_{\mathrm{DD}}T^2}{16n^3L_{2\mathrm{phase}}C}$
Load ripple voltage (CM)	$\Delta V_{\mathrm{rip,max,ld,CM}}(n)$	$\frac{V_{\mathrm{DD}}T^2}{16n^3L_{1\mathrm{phase}}C}$	$\frac{V_{\mathrm{DD}}T^2}{4n^3L_{2\mathrm{phase}}C}$
Turns around core	N	$\propto \sqrt{L_{\mathrm{filter}}(n)}$	
Saturation current	i_{sat}	$\propto \frac{H_{\mathrm{sat}}}{N} \propto \frac{H_{\mathrm{sat}}}{\sqrt{L_{\mathrm{filter}}(n)}}$	
Max. energy stored	E_{max}	$= \frac{1}{2}L_{\mathrm{filter}}i_{\mathrm{sat}}^2, \quad \propto H_{\mathrm{sat}}$	
Leg series resistance	R_{ser}	$\rho \cdot \frac{N \cdot \ell_{\mathrm{turn}}}{A}$	

These quantities are also shown using a graphical representation in Figure 3.11 with the relative changes for more phases with respect to a single phase. Further conclusions on these findings are presented in the following sections.

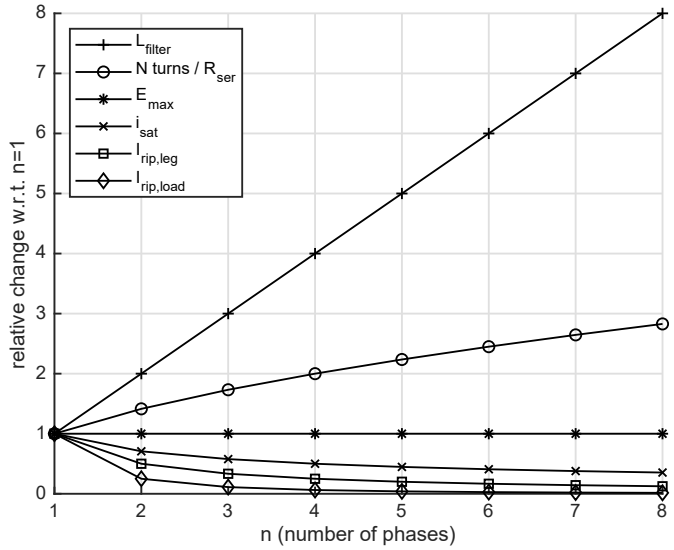


Figure 3.11: Normalized quantities for increasing number of phases.

3.6.1 Implementation Trade-offs

The implementation of multi-phase system requires more external inductors, which are costly components. This section will show a couple of trade-offs in the implementation of a multi-phase systems.

Using a single phase, the filter inductance should be $33\,\mu\mathrm{H}$ for a cut-off frequency around $30\,\mathrm{kHz}$ with a critically damped Q. Filter inductor requirements and parameters relative to a single phase system have been tabulated in Table 3.3. After looking up inductors from two manufacturers at a major retailer, their current rating, dimension, cost and series resistance have been summarized in Table 3.4.

Table 3.3: Ideal component value trade-off using a fixed filter cut-off.

	1 phase	2 phases	4 phases
Inductance	L_1	$L_2 = 2 \cdot L_1$	$L_4 = 4 \cdot L_1$
Current/leg	i	$i/2$	$i/4$
Energy/leg	$\frac{1}{2}L_1 i^2$	$\frac{1}{4}L_2 i^2$	$\frac{1}{8}L_4 i^2$
R_{ser}	1	$\sqrt{2}$	$\sqrt{4}$

Table 3.4: Real-world values using fixed cut-off.

	1 phase	2 phases	4 phases
Inductance	$33\,\mu\mathrm{H}$	$68\,\mu\mathrm{H}$	$120\,\mu\mathrm{H}$
Component (Bourns)	SRR1210	SRR1260	SRR1240
Current/leg (Irms)	4.4 A	2.1 A	1.2 A
Dimensions(lxwxh)[mm]	12x12x10	12.5x12.5x6	12.5x12.5x4
Cost/comp. (100x)	€ 0.699	€ 0.604	€ 0.6
R_{ser}	$52\,\mathrm{m\Omega}$	$110\,\mathrm{m\Omega}$	$370\,\mathrm{m\Omega}$
Component (Coilcraft)	MSS1278T-333	MSS1260T-683	MSS1038T-124
Current/leg (Irms)	3.1 A	2.3 A	1.25 A
Dimensions(lxwxh)[mm]	12.3x12.3x8.05	12.3x12.3x6.2	10.2x10.2x4
Cost/comp. (1000x)	$ 0.82	$ 0.89	$ 0.64
R_{ser}	$69\,\mathrm{m\Omega}$	$105\,\mathrm{m\Omega}$	$380\,\mathrm{m\Omega}$

The ideal scaling component values roughly agrees to the values obtained from the inductor data sheets. A doubling in inductance results in half the current rating within a product series of inductors. However, looking at the cost of the inductors, going to a 4-phase system is around 4 times as expensive as a single phase system because all inductors are priced around 70 cents. Series resistance also more than doubles from the $68\,\mu\mathrm{H}$ to $120\,\mu\mathrm{H}$ inductors. Finally, the occupied inductor area of a 4-phase system is also around 4 times as large as for a single phase, further increasing the costs of the printed circuit board (PCB). Perhaps, if they are mounted sideways, the difference in length could allow for lower area consumption.

3.6.2 Inductor Mismatch

Up to this section, ideal inductors have been considered, however in actual applications, the inductance value will spread resulting in a mismatch between the ripple current in the switching legs of a multi-phase output stage. To illustrate this, an 8-phase system is simulated using a uniform random spread of 15% on the inductance values. The ripple currents do not fully cancel any more, resulting in a residual ripple component as shown in Figure 3.12 for a duty cycle of 1/8

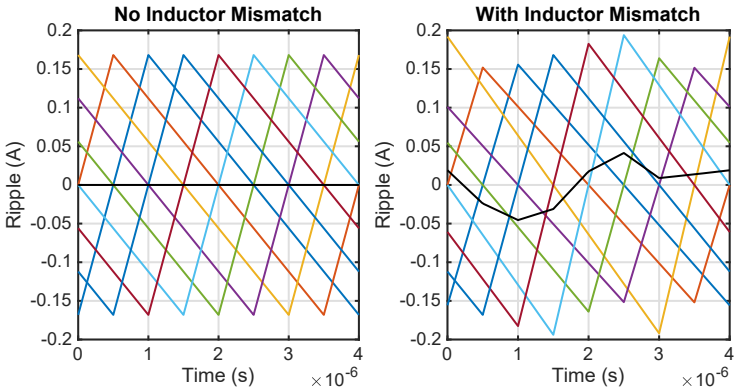


Figure 3.12: Minimum load ripple current for 8 phases with and without inductance mismatch.

In this case, the effect of mismatch results in a higher residual ripple than the maximum ripple in the ideal case. Figure 3.13 shows the load ripples for a worst-case duty cycle of 3/16.

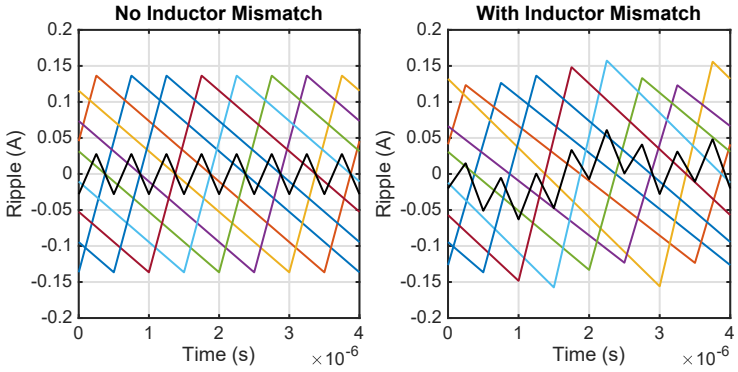


Figure 3.13: Maximum load ripple current for 8 phases with and without inductance mismatch.

3.7 Conclusion

The application of multiple phases in an amplifier design leads to an increase in component count and PCB area. Furthermore, the physical volume of the application will increase because the lower rated inductors are not proportionally smaller in their physical dimensions. Likewise, their cost is also comparable to a single larger inductor instead of proportionally smaller. At a higher number of phases, the component spread will prevent a further decrease in ripple current due to unequal ripple current amplitudes and extra phase shift. Finally, due to the high external component count multi-phase topologies do not allow for a cost effective implementation of an audio amplifier

CHAPTER 4

ACTIVE RIPPLE REDUCTION

In this chapter, a technique is proposed to reduce the CM and DM PWM ripple of a Class-D amplifier after the LC-filter by 27 dB and 18 dB respectively. This is achieved by utilizing a digital loop filter on the AX5689 integrated circuit (IC) with high gain at the PWM frequency to actively compensate the ripple. Additionally, to limit dissipation in the ripple reduction circuit, a low-CM signaling technique is used in a BTL configuration.

The chapter is organized as follows. Section 4.1 presents the ripple reduction technique, section 4.2 motivates the implementation of the chosen design, section 4.3 explains the used amplifier, section 4.4 presents the design method of the ripple feedback loop, section 4.6 provides experimental results, section 4.7 provides a discussion and conclusions are drawn in section 4.8.

4.1 Operation Principle

This section focuses on the techniques to implement a circuit that can reduce the voltage ripple on the speaker wires. First the ripple reduction principle is discussed, as well as a low-CM signaling technique to reduce dissipation. Finally, feed-forward and feedback topologies for synthesis of the ripple reduction signal are compared.

4.1.1 Active ripple reduction

To reduce the ripple, a ripple reduction signal should be synthesized. Subsequently that signal is used to draw the ripple current out of the filter inductor so it cannot go to the load and hence the ripple will not radiate from the speaker leads.

Sections 4.1 and 4.2 have been heavily edited with respect to [CEL:3] . Everything onward from section 4.4 except section 4.7 has appeared in [CEL:3] .

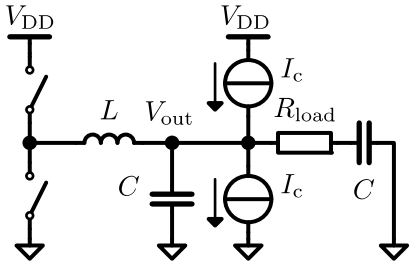


Figure 4.1: SE power stage with Class-B ripple reduction by adding current sources after the LC output filter.

Figure 4.1 shows a possible topology to apply ripple reduction to a power stage. Parallel current sources are added after the LC output filter to provide the capability to absorb the residual ripple current. A key difference of this technique with respect to other modulation techniques [14, 44–47] is that the power is removed from the spectrum, instead of being spread out over neighboring frequencies.

4.1.2 Problems with SE implementation

In a SE implementation like in Figure 4.1 it is desirable to have a symmetric supply because that eliminates the need of the bulky decoupling capacitor at the output. However, a symmetric supply requires more components and this implementation also suffers from supply pumping for low audio frequencies. To alleviate said shortcomings, BTL implementations are generally used and hence SE implementations won't be considered any further for the active ripple reduction solution.

4.1.3 Modulation scheme

A proposed BTL solution is shown in Figure 4.2. For this topology, the two

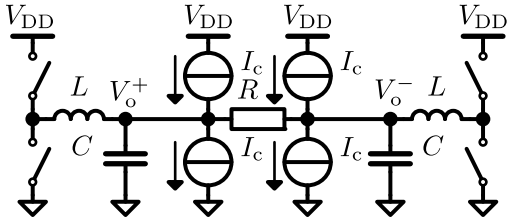


Figure 4.2: BTL power stage with Class-B ripple reduction by adding current sources after the LC output filter.

modulation schemes AD and BD explained in section 2.2 are considered. With AD modulation there is DM ripple, which is not the main problem for EMI, but still undesired. Theoretically there is no presence of CM ripple, that is until mismatch in the LC filter is considered. This mismatch will

cause CM ripple that can be reduced with active ripple reduction. With BD modulation there is CM ripple, hence active ripple reduction is required.

Both the AD and BD solutions with ripple reduction suffer from considerable dissipation in quiescence because the ripple still has to be dissipated in the ripple sinks I_c

4.1.4 How to avoid dissipation

Reducing the ripple in quiescence can be accomplished by making both bridge halves 2-phase as shown in Figure 4.3. A downside of this implementation is the requirement of extra bulky filter inductors. Another solution is to use the low-CM technique explained in 2.2.3 to reduce the ripple in idle for the BTL implementation in Figure 4.2.

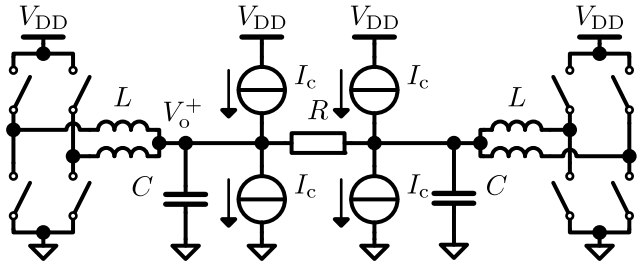


Figure 4.3: 4-phase BTL power stage with Class-B ripple reduction by adding current sources after the LC output filter.

The theoretical dissipation of both solutions should be considered to find the most efficient implementation. In the 4-phase BTL solution, it is still required to have the idle level at half the supply voltage. The dissipation in the ripple sinks caused by the ripple current for the 4-phase implementation versus the low-CM 2-phase BTL is shown on the left in

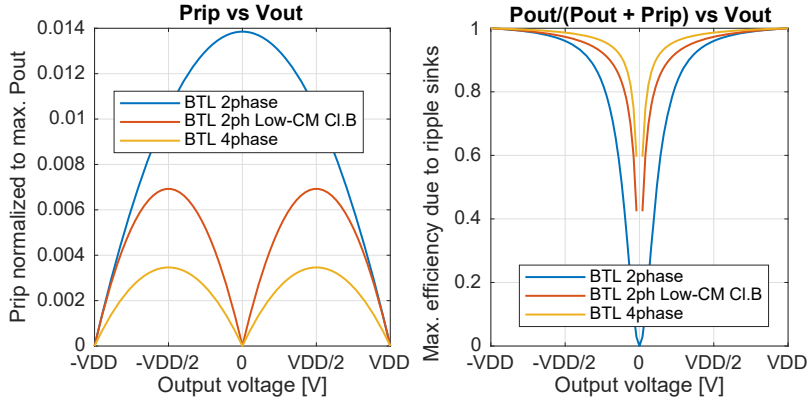


Figure 4.4: Dissipation in ripple sinks and efficiency of CM ripple reduction in BTL implementations.

Figure 4.4 with the corresponding efficiency shown on the right. The trend for a AD/BD 2-phase BTL stage using 50% CM is also shown for reference assuming you sink the full ripple and not, e.g. only the CM part.

Both the low-CM 2-phase BTL and the 4-phase BTL implementation share the same dissipation trend, however the 4-phase implementation dissipates less power due to the larger inductance values that are used to preserve the filter bandwidth. This is however at the expense of the requirement of multiple, larger filter inductors. The low-CM BTL implementation is still a favorable solution because of the lower implementation cost.

4.1.5 How to build ripple sinks

In Figure 4.2, the ripple is sinked and sourced by a Class-B implementation. The upside of this topology is that little to no quiescent current is required for operation. There are, however, many downsides to this implementation. It still has to sink the large ripple at 50% modulation to supply and ground, in low-CM operation it still sources current from the supply, giving high dissipation due to the large voltage drop over the high-side transistor, and it requires 4 power transistors.

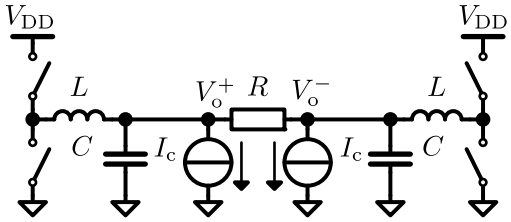


Figure 4.5: BTL power stage with Class-A ripple reduction by adding current sources after the LC output filter.

The Class-A implementation shown in Figure 4.5 sinks all the ripple current to ground and hence requires a large bias current. It is even less efficient than the Class-B implementation at 50% duty cycle. However, during low-CM operation it sinks the quiescent current with a low voltage drop to ground, making it as efficient as the Class-B implementation in idle. It also makes the dissipation proportional to the delivered output power, which is good because audio has a high crest factor. Since it requires only 2 power transistors, it is easier to control and has a lower footprint.

The comparison of power dissipation and efficiency between the Class-A and Class-B implementations is shown in Figure 4.6. Although the Class-B implementation is more efficient overall, the Class-A implementation is chosen because of its lower complexity and comparable performance at lower output powers.

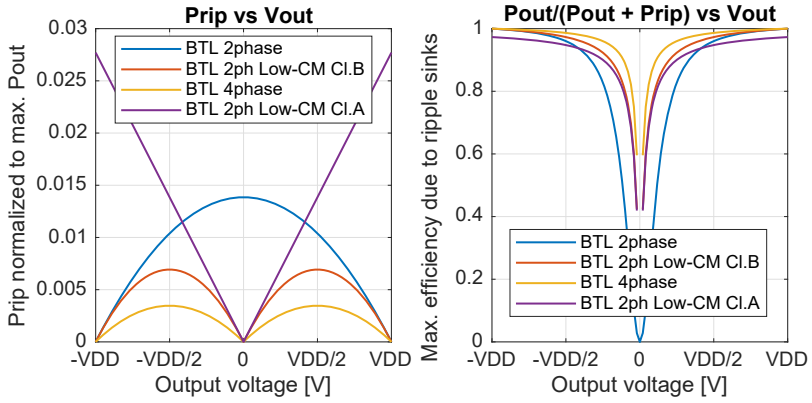


Figure 4.6: Dissipation in ripple sinks and efficiency of CM ripple reduction in BTL implementations.

4.1.6 Feed-forward or Feedback

Generally, there are two distinct architectures to implement a system that could determine a correction signal to reduce the ripple current. The first solution is to use a feed-forward method to determine the ripple signal from the known variables in the system and inject the inverted signal to cancel the ripple. The second solution is to measure the output current and or voltage, isolate the ripple signal and use negative feedback to close the loop and reduce the ripple. The following sections will provide more insight into these two architectures.

4.1.7 Feed-forward

When the physical component values and signals of the amplifier are known, it is possible to analytically calculate the ripple current and inject it as cancellation signal. An example system is shown in Figure 4.7. However, as simple as this sounds, in reality, components do have spread which has to be calibrated out before a proper cancellation signal can be synthesized. Another challenge is characterizing the non-linearity of the inductor due to magnetic saturation of the core. A servo loop could be used to let the prediction coefficients converge towards the actual component values, while also allowing the possibility to track the non-linear behavior of the inductor.

A feasibility study was done to assess the challenges of a feed-forward prediction algorithm with a servo loop based on LMS estimation. For a known inductor value, the ripple current can be determined from the PWM output voltage and the voltage after the inductor. However, with a component spread of 20% for inductors and core saturation, the exact inductance value is unknown. Additionally, a physical inductor has series resistance which also needs to be determined. The voltage to current conversion of the inductor is of importance, hence when the inductance

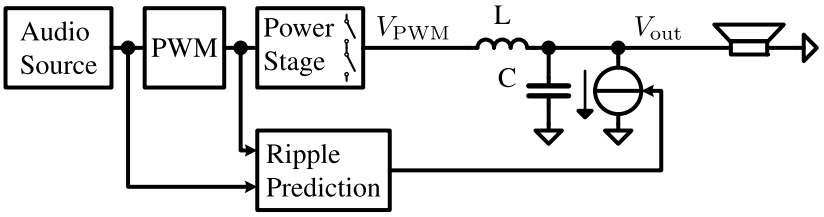


Figure 4.7: Prediction of the ripple and injection after the output filter.

value deviates by 10%, the magnitude of a generic second-order LC output filter in the stop-band changes by roughly the same percentage, limiting the reduction to 20 dB.

To overcome this limitation, the component values should estimated in real-time. This estimation will require a local servo loop of which the performance is limited by the accuracy of the ADC.

The estimation could be implemented using a replica of the LC circuit. Such a replica will not just output the ripple current, but it will also contain the audio. The audio signal has to be removed by filtering or subtraction. Filtering requires no knowledge of the audio signal, but introduces phase shift that has to be compensated for. Subtraction requires a copy of the audio signal prior to PWM that is filtered using the same L and C components, which need to be found using an estimation method. The latter option is shown in a block diagram in Figure 4.8.

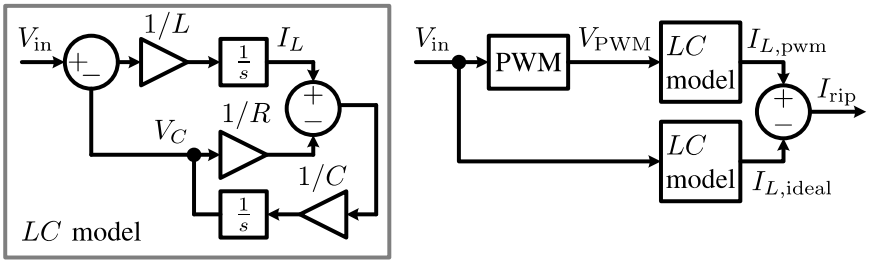


Figure 4.8: Block diagram showing how to obtain the ripple current I_{rip} using two replicas of the LC filter. Left is the model of the output filter including the load, right uses the model twice to obtain I_{rip}.

After injecting the anti-ripple current, either the load current or the load voltage can be observed to obtain the residual ripple. By correlating one of these signals, after removal of the audio signal, with the estimated ripple current, a quantity of whether the correction is too much or too little is obtained. This quantity is used in an LMS gradient descent algorithm to correct the value of the inductance in the model. The inductor value is used to calculate the theoretical ripple cancellation current to inject after the output filter. Like for any LMS algorithm there is a trade-off between accuracy and settling speed based on the step-size parameter. In order to

track the varying inductance for audio signals up to 20 kHz, the step-size parameter had to set so large that estimated inductance would deviate more than 10% from its actual value, limiting the achievable ripple reduction to less than 20 dB. Ways to also characterize the resistance and capacitance at the same time require a more complicated approach and is outside of the scope of this research.

Finally, the current DAC or amplifier that drives the output node should have a bandwidth that includes the fundamental PWM frequency and the first couple of harmonics.

4.1.8 Feedback

The most accurate way of determining the ripple, is to measure it at the output of the amplifier. Since we only want to reduce the ripple component and not alter the audio signal, the ripple signal should be isolated from the measured signal using a filter. The filtered signal can then be injected after the output filter of the Class-D amplifier to reduce the ripple. The amount of loop gain at the frequencies of the ripple components will determine the performance of this feedback topology. An example of this topology is shown in Figure 4.9.

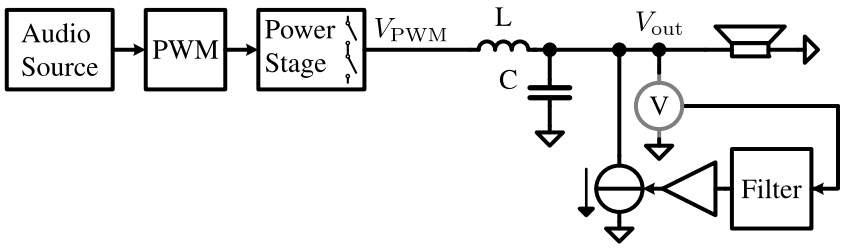


Figure 4.9: Sensing the ripple and injection after the output filter.

The undesired energy in the spectrum is concentrated around the PWM frequency, its harmonics and their intermodulation products with the input signal. A stylized plot of the spectral components of a PWM signal of a sine input is shown in Figure 4.10. Note that in reality there will be many more components which can be described using Bessel functions. Moreover, the input frequency will be much lower than the PWM frequency, putting the intermodulation tones closer to the fundamental and its harmonics. For this reason, a tailor made filter design using band pass filter with resonance at the PWM frequency and its harmonics could provide the required selectivity. The quality factor can be tuned to provide loop gain at the intermodulation frequencies next to the PWM carrier.

Finally, we choose to continue with the design of a feedback ripple reduction technique which shares some similarities with the Class-AB/D approach. The main reason for choosing feedback is that, initially, it looked more straightforward to design a loop filter with high gain, than to accu-

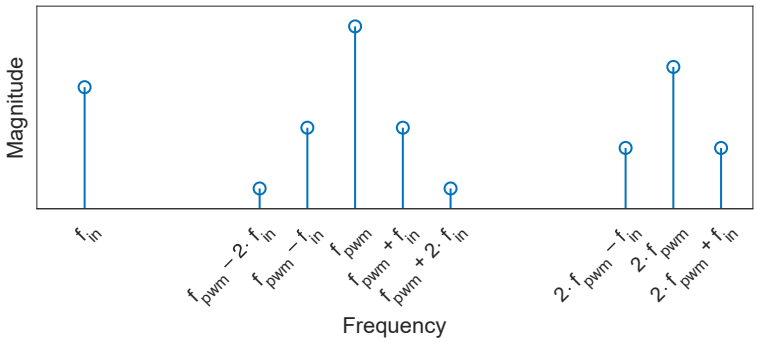


Figure 4.10: Stylized PWM spectrum with a sine as input.

rately model every aspect of a feed-forward system. The feedback system would also be more resilient to non-linearities, while in feed-forward you would have to apply proper pre-distortion.

4.2 Implementation

This section elaborates on the implementation of the Class-D amplifier with active ripple reduction. It shows the used configuration and explains the utilized hybrid low-CM switching scheme.

4.2.1 Single-ended implementation

Figure 4.11 shows the proposed topology consisting of a fixed carrier PWM Class-D amplifier and a ripple reduction circuit. An ADC digitizes the voltage over the load and feeds it to a loop filter. This loop filter has high

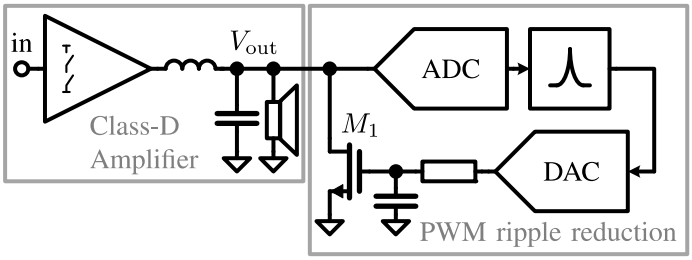


Figure 4.11: Ripple reduction using a Class-A amplifier driven by a digital loop after the output filter of a Class-D amplifier.

gain at the PWM frequency and low gain in the audio band. The output signal of the filter is converted back to an analog voltage to drive a Class-A amplifier, consisting of a MOS transistor (M_1) which serves as a current source closing the feedback loop.

4.2.2 BTL with low-CM

As was explained in section 4.1.4, dissipation can be reduced by reducing the idle output CM voltage in a BTL configuration. The implementation of this low-CM BTL topology is shown in Figure 4.12.

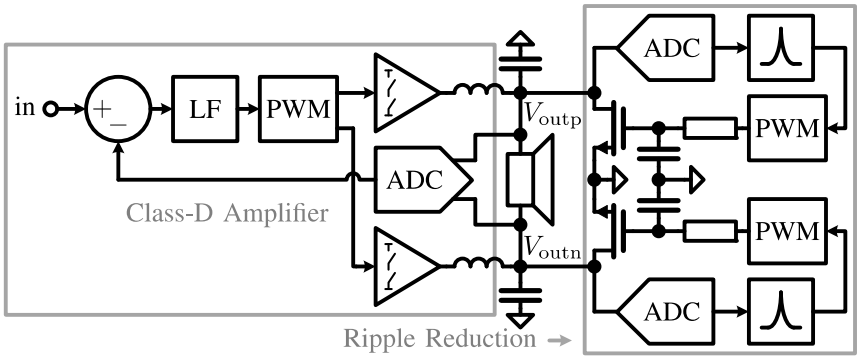


Figure 4.12: BTL implementation of the ripple reduction circuit after the output filter of a Class-D amplifier.

A hybrid implementation of low-CM BD and regular BD modulation is used for this amplifier. The operation of this hybrid scheme is explained with a sinusoidal input signal as example.

The top half of Figure 4.13 shows the half-bridge (HB) signals to obtain a low CM output level. Achieving this lower CM level is done by subtracting an offset from the positive and negative HB signals. When the HB signals

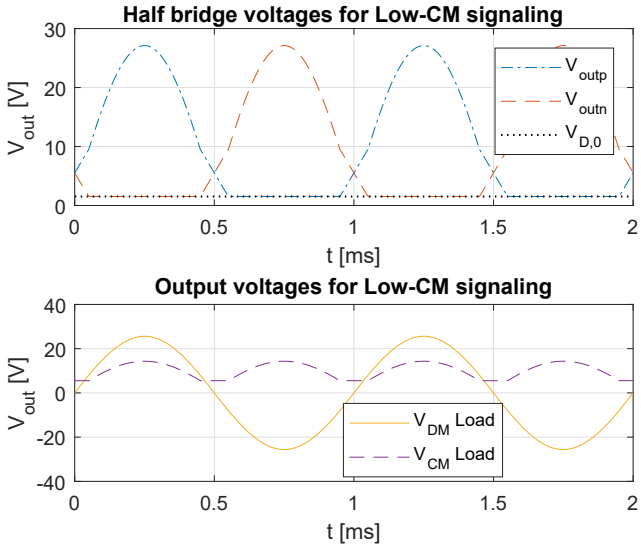


Figure 4.13: Waveform illustrating the effect of low-CM signaling on half-bridge (HB) outputs (top) and CM and DM outputs (bottom).

are high in amplitude, the subtracted offset will clip the signal at the lower bound $V_{\mathrm{D},0}$. This $V_{\mathrm{D},0}$ is defined to keep the Class-A MOS transistors saturated. To maintain linearity, the part that was clipped off below $V_{\mathrm{D},0}$ is added to the other HB signal as shown in Figure 4.13. The bottom half of Figure 4.13 shows the DM and CM output signals. Note that the V_{DM} is the reconstructed sine and V_{CM} is at 5 V except when one of the half bridge signals is clipped below $V_{\mathrm{D},0}$. The choice for V_{CM} is a trade-off between idle power dissipation and distortion. On the one hand, a low CM level reduces the idle power dissipation [66].

On the other hand, when one of the HBs is clipped to $V_{\mathrm{D},0}$, just one HB is driving the load. During this transition the loop filter has to process an instantaneous change in slope from the output of the amplifier, increasing the distortion. Therefore the V_{CM} = 5 V is a compromise between these considerations.

In the top half of Figure 4.14 the contribution of each HB for a certain output voltage is given. Around idle output, both the HBs are controlling the signal and once the output signal goes over approximately $|V_{\mathrm{DD}}|/4$ one of the HBs is clamped to $V_{\mathrm{D},0}$. The bottom half of Figure 4.14 shows the total dissipation as function of the instantaneous output voltage. The dissipation curve for Class-A active ripple reduction with conventional AD or BD modulation [54] is drawn to show the advantage in power dissipation of the low CM switching over normal AD or BD modulation. As audio has a high peak to average power ratio [67], most of the signal content resides in the valley of the graph and the ripple reduction power efficiency is up to 3 times better due to low-CM signaling.

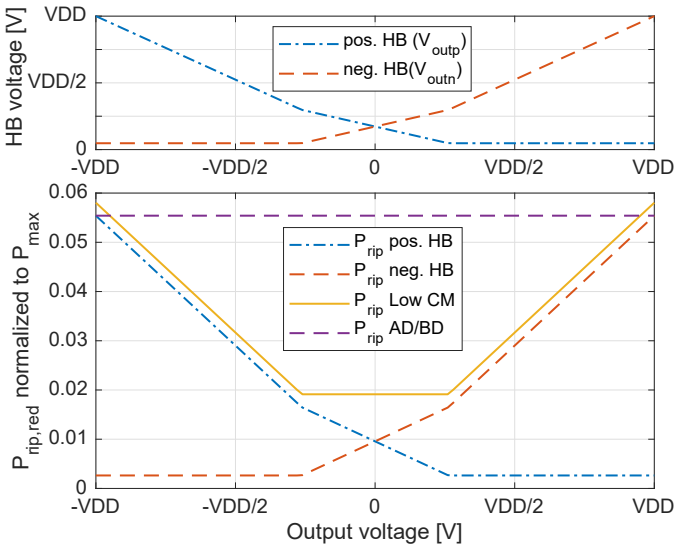


Figure 4.14: Contribution of half-bridges (HBs) to the output voltage (top) and normalized power dissipation due to the Class-A ripple reduction.

4.3 Design Vehicle: AX5689

In this work the AX5689 [68, 69] is used as a design vehicle to test the proposed ripple reduction technique. The AX5689 is a controller for fully digital Class-D amplifiers that digitally generates PWM to drive an external power stage and takes feedback after the output LC filter using a purpose built low-latency ADC (LLADC). The input is provided digitally using a S/PDIF optical or coaxial cable to connect to the audio source.

4.3.1 Architecture

The AX5689 is highly customizable, consisting of 8 configurable 7th order loop filters, 8 LLADCs, 8 PWM generators, a butterfly mixer and a crossbar at the output. This allows for various input and output configurations such as 8-channels SE, 4-channels BTL or even 2-channels with 4-phases each.

The implementation of the Class-D amplifier used in this work is shown in Figure 4.15. First, the input signal has to be upsampled to the sample

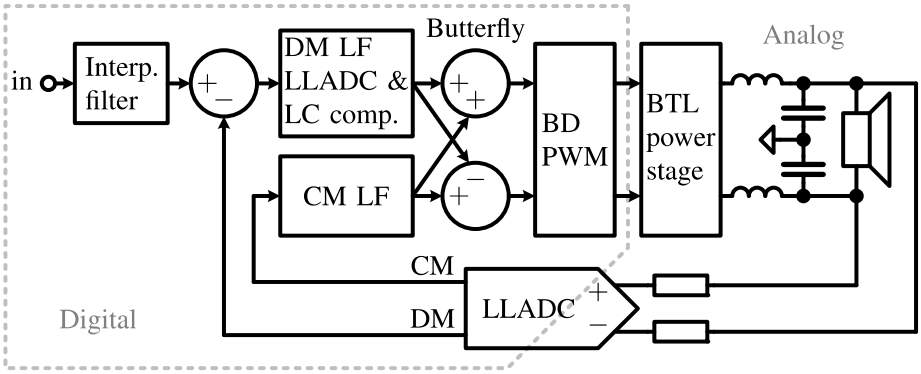


Figure 4.15: A BTL Class-D amplifier implementation powered by the AX5689.

rate of the loop filter. To prevent aliasing, an interpolation filter is used. After that, the feedback signal is subtracted from the upsampled signal and the result is fed to the loop filter. Subsequently, the output of the loop filter is fed to the two modulators to generate the PWM signals for the external power stage. Then, the amplified PWM signals are filtered by the two LC output filters to reconstruct the output signal over the load. Finally, the differential outputs are sensed and digitized by an ADC to provide a DM and CM feedback signal. For this application there are two feedback loops, one DM loop for the signal path and a CM loop to actively damp the LC response.

The LLADC will be covered in section 4.3.2 and the loop filter will be explained in detail in section 4.3.3.

4.3.2 Low-Latency ADC

For the application of amplifying sound a high accuracy ADC is required. A sigma-delta ADC is able to provide high accuracy in the audio band by applying oversampling and noise shaping. However, the increased high frequency quantization noise in combination with the compensation for the LC filter poles degrades modulator performance. At least 110 dB signal-to-quantization noise ratio (SQNR) in the audio band was set as a requirement for the ADC. This would only be possible with a low-pass reconstruction filter after the ADC, which would introduce latency into the loop. Latency or delay can be detrimental to the performance of a feedback loop, this is also further elaborated on in chapter 5. For the above mentioned reasons, the ADC within the AX5689 is a specially designed 1-bit sigma-delta ADC with an extrapolating signal transfer function (STF) with two dominant zeros placed at 60 kHz, which is shown in Figure 4.16. The resulting negative group delay in the audio band will give no net phase shift when paired with the LLADC reconstruction filter in the forward path in Figure 4.15. This reconstruction filter places two poles on the LLADC zeros which allows the placement of two zeros on the LC-filter poles to obtain a flat transfer function.

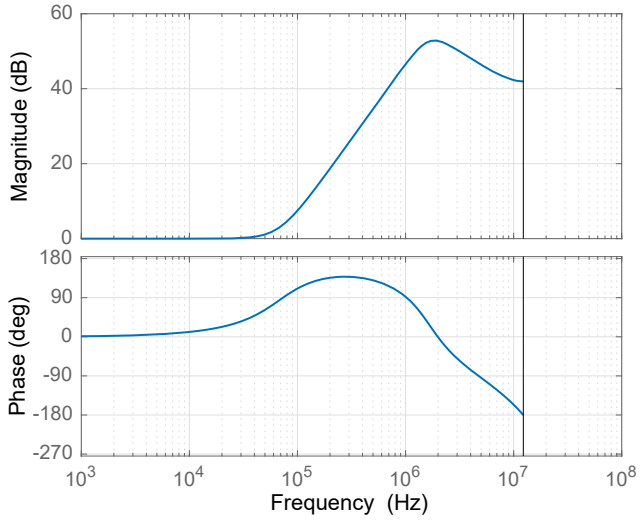


Figure 4.16: Signal transfer function of the low-latency ADC.

As result of this extrapolating STF, there is a reduction in dynamic range at frequencies above the audio band, making it less suitable for digitizing the PWM ripple. However, there is still ample dynamic range left after the 40 dB reduction at the PWM frequency of 768 kHz, allowing digitization of the ripple at sufficient resolution.

A simplified, single-ended model of the LLADC is shown in Figure 4.17. It takes an input current which is summed with the feedback current in the continuous-time integrator. The integrator output is quantized to

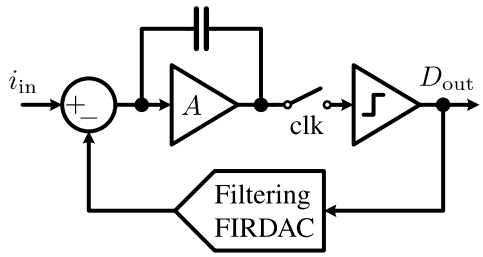


Figure 4.17: Simplified model of the low-latency ADC (LLADC).

obtain the digital bit-stream. Instead of a conventional 1-bit DAC, a finite impulse response DAC (FIRDAC) with a special filtering transfer function is implemented to provide the feedback current.

The overall LLADC is designed to have a 3rd order noise shaping characteristic of which one order originates from the integrator and the other two orders are realized in the FIRDAC. The impulse response of the ideally required infinite impulse response (IIR) prototype filter is approximated by truncating it and using these values as finite impulse response (FIR) filter coefficients [70]. The result is a 466 taps FIR filter with only minor differences with respect to the IIR prototype.

The benefits of an ADC design like this are relaxed integrator and comparator design requirements, high in-band resolution, low out-of-band noise, a unity gain transfer with reconstruction filter, no extra measures for stability and good jitter tolerance. More on the design considerations of the LLADC can be found in [26].

4.3.3 Loop Filter

Using a digital loop filter allows the use of a high order filter with high gain in the forward path without suffering from component spread which limits conventional analog filters. The used amplifier implements a 5th order loop filter with at least 75 dB gain throughout the audio band. The filter is based on a 5th order, high-pass inverse Chebyshev noise transfer function (NTF) of the closed loop, which translates to a loop filter that has a steep roll-off after 20 kHz. A 2nd order reconstruction and compensation filter compensates the LC filter and the LLADC transfer such that the combination of these three transfers has a flat transfer. This guarantees that the open loop transfer is solely dependent on the 5th order filter up to the unity-gain frequency.

The filters are implemented in a programmable cascade of resonators with feed-forward summation (CRFF) filter topology. As shown in Figure 4.18, a 1st order section is followed by three 2nd order resonator sections with an elaborate diagram shown in Figure 4.19 to allow up to 7 orders of filtering in each of the 8 on-chip filter slices. It is possible to take inputs from the PCM bitstream, PWM output or CM or DM ADC outputs with

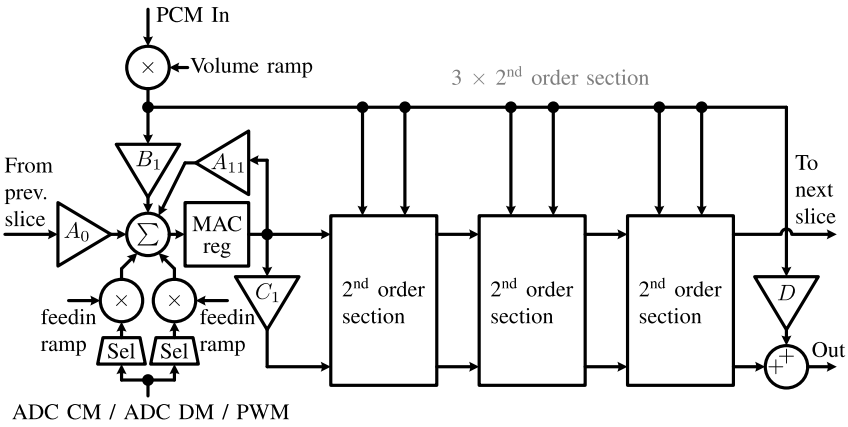


Figure 4.18: Compact model of an AX5689 loop filter slice.

the option to ramp each signal. Synthesizing filter orders greater than 7 is possible by cascading multiple filter slices.

Conveniently, the 5th order loop filter and 2nd order compensation filter can be fit into one 7th order filter slice.

Input is provided by a PCM signal which is upsampled to the loop-filter filter sampling frequency. Subsequently the upsampled signal is filtered by a 4th order elliptic interpolation filter to suppress aliases before injecting it into the previously discussed loop filter. The interpolation filter is implemented in the last two 2nd order sections of the loop filter slice (Figure 4.18). The remaining three filter orders at the beginning are used to implement the CM control loop to damp the CM LC filter response. A butterfly switching matrix (see Figure 4.15) is used to combine the CM and DM loop filter outputs as follows: CM + 0.5 DM and CM – 0.5 DM. Then these signals are fed into two PWM generators to obtain the switching signals for the positive and negative half-bridges of the output stage.

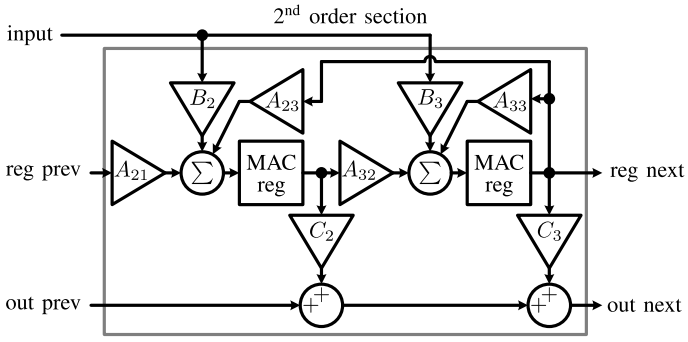


Figure 4.19: AX5689 loop filter 2nd order section internals.

4.4 Ripple Reduction Loop Design

Technology scaling has led to smart power processes which allow the integration of low-power DSP and high-power amplifiers on the same die. This allows the design of Class-D amplifiers with a digital, high-order loop filter [24] and an ADC to provide feedback at the switching node [23] or after the output filter [6, 26]. Digital filters have an advantage over analog filters, being unaffected by process and temperature variation, allowing the use of higher order filters.

First, all the blocks in the ripple reduction part of Figure 4.12 will be discussed, as they define design constraints for the digital loop filter that is to be implemented. After that, the loop design method is explained and finally compensation is added to ensure a stable system.

4.4.1 Class-A driver

In order to realize the ripple reduction feedback loop, the digital feedback signal needs to be converted to the analog domain. The AX5689 is capable of generating eight PWM outputs, of which two are used for the BTL power stage. Hence the remaining six are distributed to have 3-phase PWM for each Class-A driver to perform digital-to-analog conversion. The schematic of this circuit is shown in Figure 4.20.

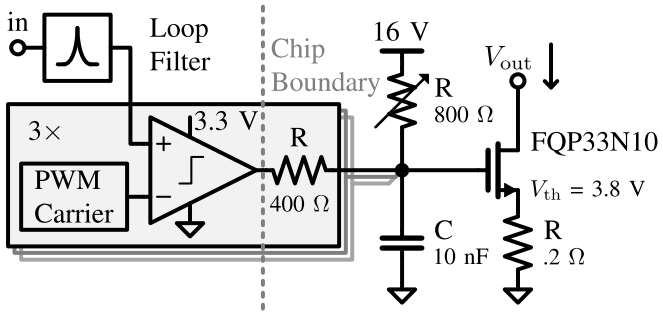


Figure 4.20: Architecture of the DAC and Class-A driver.

Analog-to-digital conversion is done using one LLADC [26] per half bridge. The ripple reduction ADC output is fed to the loop filter, of which the output is fed to three PWM modulators. The modulators run at twice the loop filter sample rate, allowing 2 conversions per sample. The three carriers are shifted 120° in phase, and to reduce quantization noise, each carrier cycles through 6 different levels as shown in Figure 4.21.

Summation of the PWM outputs is done using a resistive network that also provides level shifting and biasing to drive the MOS transistor. The drain of the MOS transistor is connected after the LC-filter as in Figure 4.12, closing the loop.

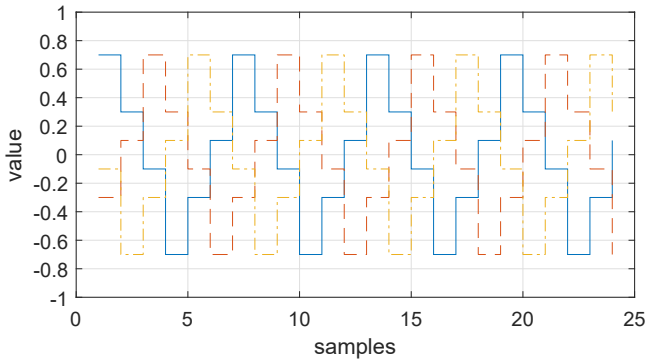


Figure 4.21: 3-phase PWM carriers for D/A conversion.

4.4.2 Loop design constraints

The ripple reduction loop consists of several blocks as can be seen in Figure 4.12. The LC-filter impedance converts the MOS transistor drain current, which is injected at the output of the LC filter, to a voltage at the output of the LC filter. This impedance has a band-pass characteristic, having 2 poles and 1 zero. Spread in C affects the ripple reduction loop stability because it changes the gain for signals above the LC corner frequency.

The used ADC is also integrated in the AX5689 chip. It has a second order rising slope of 40 dB/dec between 60 kHz and 1 MHz due to the two zeroes at 60 kHz transitioning into -20 dB/dec slope after 1 MHz due to the three poles at 1 MHz. The FIRDAC in the ADC renders the response highly insensitive to mismatch [26].

The RC filter used after the PWM DAC to reduce quantization noise provides an integrating response for signals at the PWM frequency due to the pole around 100 kHz. Spread in R and C will slightly alter the frequency of this pole and modify the integrator gain, this is however suppressed by the high overall loop gain. Finally the digital circuitry has processing delay, which gives a phase shift at frequencies in the vicinity of $f_{\mathrm{s,loop}}$.

Summarizing, these blocks contribute the following poles and zeros,

- LC-filter (2 poles @30 kHz, 1 zero @DC)
- ADC (3 poles @1 MHz, 2 zeros @60 kHz)
- RC Integrator (1 pole @100 kHz)
- 3 unit delays (3 poles in the origin of the z-plane)

4.4.3 Filter Synthesis

The next objective is to design a loop filter that can be put in the ripple reduction feedback loop in Figure 4.12. As was mentioned earlier, this filter requires high gain at f_{PWM} and low gain in the audio band. To design such

a filter, a method common in $\Sigma\Delta$ loop filter design [71] is used. With this method, a desired closed loop NTF can be chosen and used to calculate the open loop transfer function $H_{\text{loop}}(z)$. This is done by rearranging the definition of the NTF in a feedback system as follows,

$$\text{NTF}(z) = \frac{1}{H_{\text{loop}}(z) + 1}, \tag{4.1}$$

$$H_{\text{loop}}(z) = \frac{1}{\text{NTF}(z)} - 1. \tag{4.2}$$

In this case, an NTF is chosen which leaves the audio intact and suppresses the PWM ripple. A way to design this is to place a notch at the PWM frequency. To make a notch, a complex zero pair is placed on the unit circle at an angle that is corresponding to the desired frequency. A complex pole pair is then placed inside the unit circle, at the same angle, close to the complex zeros in order to set the notch bandwidth. The angle in radians is calculated as follows,

$$\alpha = 2 \cdot \pi \frac{f_{\text{pwm}}}{f_{\text{s,loop}}}. \tag{4.3}$$

Now, using the exponential function the zero locations on the unit circle can be obtained as $z_1 = \mathrm{e}^{i\alpha}$ and $z_2 = \mathrm{e}^{-i\alpha}$. The pole locations can be derived by multiplying the zeros with a factor $r < 1$, giving $p_1 = r \cdot z_1$ and $p_2 = r \cdot z_2$. The closer r is to 1, the higher the quality factor and the sharper the notch will be.

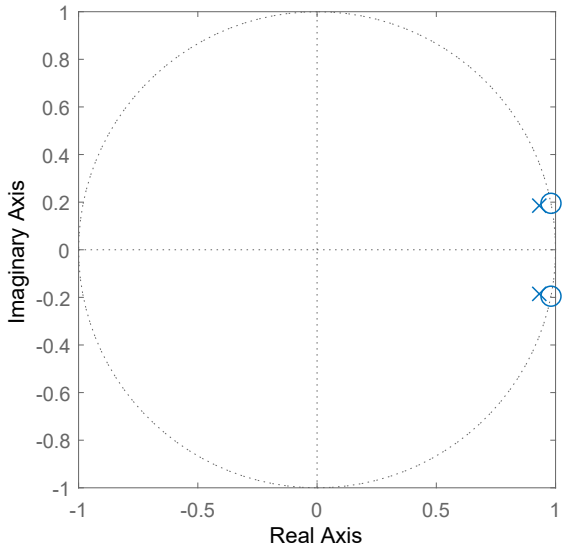


Figure 4.22: Poles and zeros of the designed NTF.

To make a visualization of the poles and zeros, values have to be substituted in (4.3). A demo board with the 'AX5689' [68] is used to implement

the filter and the audio amplifier. The default values in the controller are $f_{\text{pwm}} = 768$ kHz and $f_{\text{s,loop}} = 32 \cdot f_{\text{pwm}} \approx 25$ MHz, which is used for the loop filter and ADC. The pole-zero map is shown in Figure 4.22. In the actual system r is set to 0.996 but for visualization purposes the value for r is 0.95.

To get from this closed loop NTF description to a loop filter that can be put in the feedback loop in Figure 4.12, (4.2) is applied. The resulting loop filter has a resonator at $f_{\text{pwm}} = 768$ kHz, because of the $1/\text{NTF}$ operation in (4.2). The loop filter transfer function is shown in Figure 4.23. From the

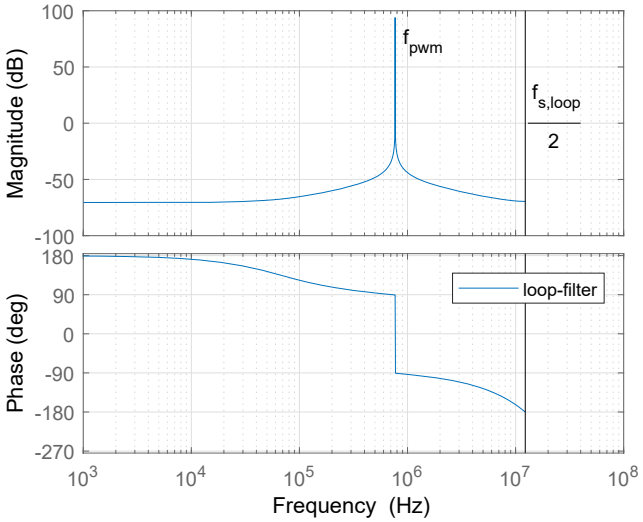


Figure 4.23: Bode plot of the designed ideal loop filter.

phase plot it can be seen that around the resonant frequency, the phase is already $\pm 90°$. Since the actual system consists of more elements than just the loop filter, maintaining stability becomes a challenge.

4.4.4 Loop compensation

Several blocks influence the stability of the ripple reduction loop. Hence, compensation has to be added to make the loop robust. All poles and zeros have been plotted in Figure 4.24

In order to compensate the ADC poles, a second order lead compensator is added 'ADC comp' in Figure 4.24. The complex pole pair of the 3 ADC poles is canceled by placing a complex zero pair on top of them. To maintain causality, two poles are added near $z = 0$. Ideally these could be unit delays.

The additional phase shift that the unit delays create is compensated by moving the zero of the resonator 'reso' more to the right, thereby reducing the phase lag near the resonator. This zero lies outside the unit circle, which is equivalent to a right half plane zero in the s-domain. The procedure to

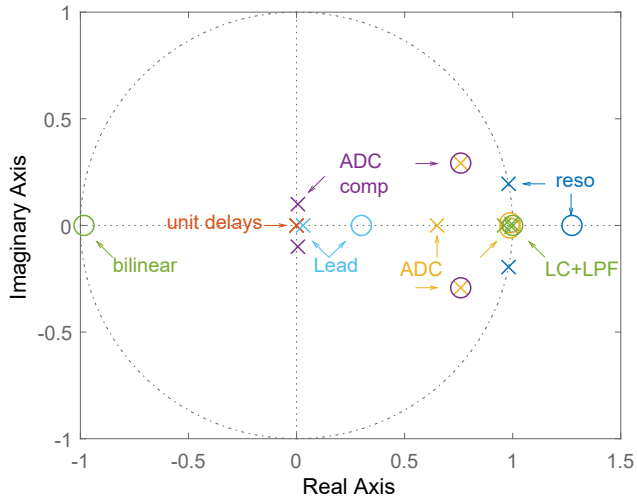


Figure 4.24: Pole-zero map of the complete open loop transfer.

determine the placement of this zero follows from the filter compensation technique that will be explained in chapter 5.

The combined continuous time transfer function of the RC-filter and the LC-filter was mapped to the z-domain using the bilinear transform resulting in the poles and zeros denoted with 'LC+LPF'. An extra zero, denoted as 'bilinear' in Figure 4.24, got added as result of the continuous to discrete time conversion.

Finally, another first order lead compensator is added providing more phase lead near 1 MHz where the magnitude crosses 0 dB for improved stability.

For comparison, the total open-loop transfer before and after adding the compensation is shown in Figure 4.25. It can be seen that the transfer is flatter around the resonant peak and the phase jump has been moved up providing a larger phase margin. The phase margins around the resonator are 47° on the left side and 44° on the right side of the resonator peak. The 44° is the most critical margin, which translates to a delay margin of 2.8 unit delays or 114 ns.

The spread in L and C has been investigated. Changes in L have hardly any effect on stability because it only influences the transfer below the LC corner frequency of the parallel LC tank seen by the loop. Changes in C do have an effect on stability and the phase margin, which nominally is 44° and remains above 40° for a 10% decrease in capacitance.

Calculations in the on-chip filter are done with limited precision, hence the filter coefficients had to be quantized to fit the on-chip registers. Manual tuning of the filter coefficients' least significant bits (LSBs) after quantization was necessary to put the resonator as close as possible to the PWM frequency.

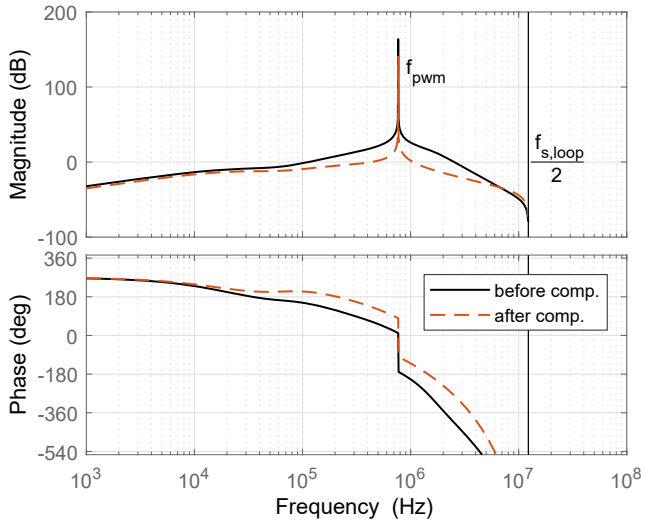


Figure 4.25: Full open-loop transfer of the ripple reduction loop before and after compensation.

4.5 Simulation results

Simulations have been performed prior to the implementation in hardware. An SE simulation setup as shown in Figure 4.11 has been used with a 90% of full scale input signal at 2 kHz. It was verified that the ripple reduction loop indeed reduces the PWM carrier component and side bands around 768 kHz as shown in Figure 4.26. The carrier component is reduced by

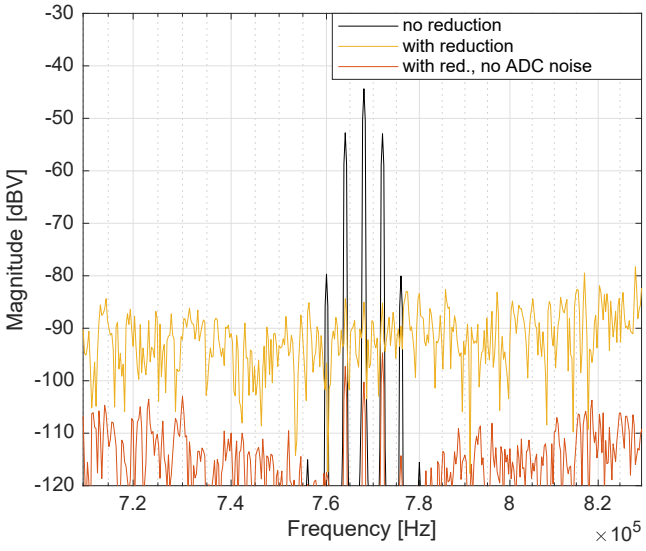


Figure 4.26: Single-ended (SE) spectrum, showing the simulated PWM spur reduction on an open loop PWM system.

40 dB, reaching the noise level that is introduced by the ripple reduction loop. Since the PWM generation for the amplifier loop is done open loop with an ideal modulator, there is no noise spectrum present when reduction is disabled. Enabling the ripple reduction loop increases the noise surrounding the carrier because of the quantization noise of the ADC, which limits the ripple reduction potential.

4.6 Experimental Results

The amplifier with ripple reduction after the output filter was built using the AX5689 demo board [68] with an additional PCB containing the ripple reduction Class-A drivers as shown Figure 4.27. The system was measured using an APX555 audio analyzer setup as in Figure 4.28. The measurement bandwidth of 1.2 MHz allows to measure the audio band as well as the PWM ripple.

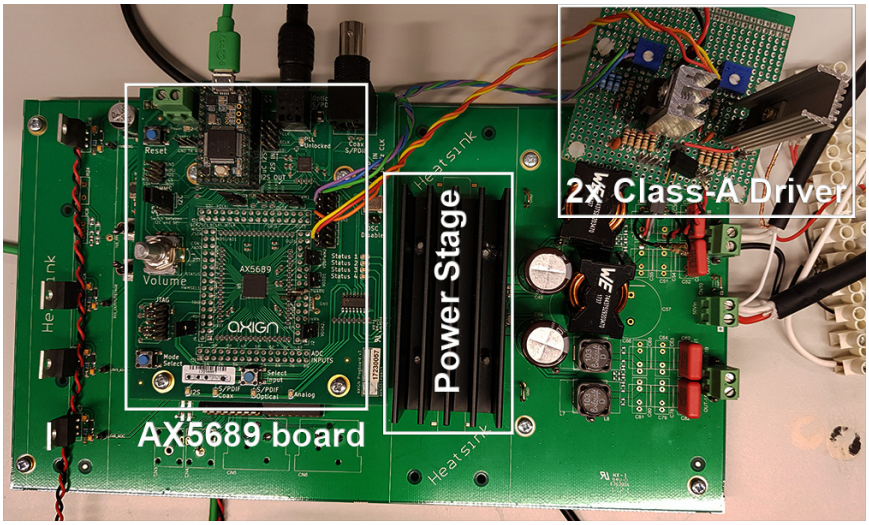


Figure 4.27: Experimental setup consisting of the AX5689 demo board and an add-on board with Class-A drivers.

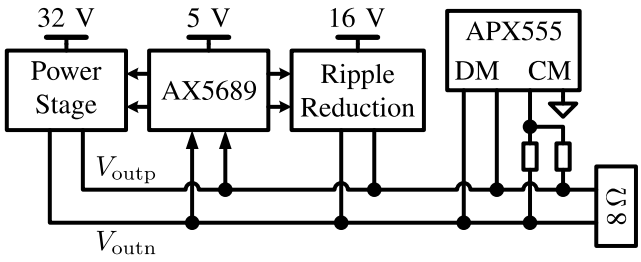


Figure 4.28: Measurement setup showing the connections between the circuits and the measurement equipment.

Spectral analysis has been done to characterize the reduction in PWM ripple after the output filter. Both the DM and CM spectra have been obtained using an f_{PWM} of 768 kHz, an 8 Ω load and a 1 kHz sine stimulus. Both measurements, with and without ripple reduction, were done using the low-CM signaling. Just the ripple reduction circuit is turned on and off. The spectra are shown in Figure 4.29 and Figure 4.30 respectively. The DM spectrum shows the 5th order noise shaping behavior, provided by the loop filter. The CM spectrum doesn't have this behavior, because it is controlled by a different filter [26].

For emissions, the CM ripple is the most important to be reduced [72]. From the spectra it can be seen that both the DM and CM ripple are reduced by 18 dB and 28 dB respectively.

The ripple reduction has been calculated as the difference in magnitude between the frequency component at f_{PWM} with ripple reduction disabled and the highest frequency component after ripple reduction is enabled. In Table 4.1 the results are shown and it can be seen that the reduction is roughly uniform over signal frequency and output power. In case of the 10 W, 10 kHz measurement, the fundamental component of the ripple is reduced to a significantly lower value than the intermodulation tones at $f_{\mathrm{PWM}} \pm f_{\mathrm{in}}$, and hence the reduction is calculated using the intermodulation tones instead of the fundamental.

Audio performance with ripple reduction enabled has been tested by doing a total harmonic distortion plus noise (THD+N) analysis for three different frequencies; 100 Hz, 1 kHz and 6 kHz. The output power was

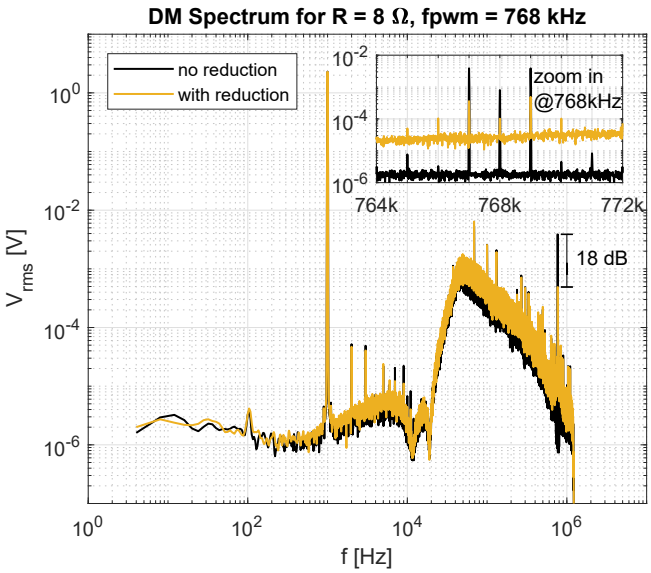


Figure 4.29: Differential mode (DM) spectrum, showing the PWM spur reduction. The zoomed inset shows the intermodulation spurs around f_{PWM}.

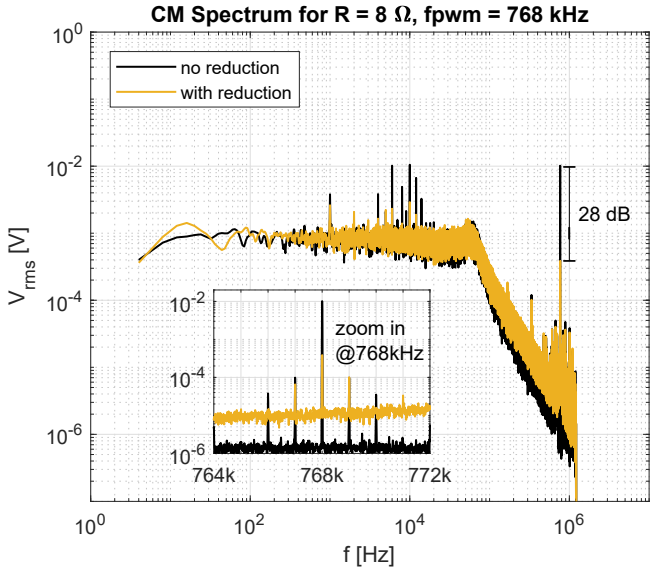


Figure 4.30: Common-mode (CM) spectrum, showing the PWM spur reduction. The zoomed inset shows the intermodulation spurs around f_{PWM}.

swept from 0.1 mW up to clipping and the result is shown in Figure 4.31. Ripple reduction had a minor penalty in THD+N, being 0.0017% without reduction and 0.0019% with reduction at 1 W 1 kHz. This is due to the slightly increased noise floor when ripple reduction is enabled. THD+N is below 0.003% at 1 W for all frequencies, the rise in THD+N above 2 W happens due to the transition from BTL to single-ended (SE) actuation where one half-bridge is clamped to $V_{\mathrm{D},0}$. This is a drawback compared to conventional AD and BD modulated systems. Maximum output power is 50 W at 10% THD+N and the idle noise of this amplifier is 50 µV (Awtd, at 32 V) resulting in a dynamic range (DR) of 110 dB.

System efficiency ($P_{\mathrm{out}}/P_{\mathrm{in}}$, where P_{in} includes power consumption of all circuits) is 84% without and 79% with ripple reduction at maximum sinusoidal output power. Both efficiencies are shown in Figure 4.32. There are three reasons that limit the efficiency, one being the dissipation in the on resistance of the power stage of 0.2 Ω, another being the dissipation in the bias circuit to provide level shifting for the Class-A driver and finally the bias current in the MOS transistor.

Table 4.1: CM Ripple reduction for different powers and frequencies

P_{out}	100 Hz	1 kHz	10 kHz
0 W	29.3 dB	29.2 dB	29.0 dB
1 W	28.2 dB	28.5 dB	28.7 dB
10 W	28.4 dB	28.4 dB	27.1 dB

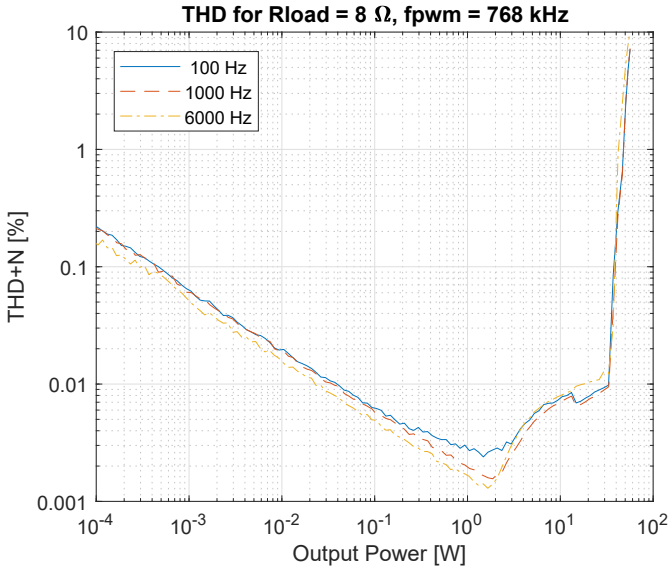


Figure 4.31: THD+N plot for three frequencies with ripple reduction enabled.

So the proposed technique does have an efficiency penalty, but in many applications were EMI is very important, this seems justifiable. An example is the use in polar radio frequency (RF) power amplifiers (PAs), where the ripple shows up directly in the spectrum and analog AB/D systems have long been used for this purpose [73]. Another advantage of the proposed

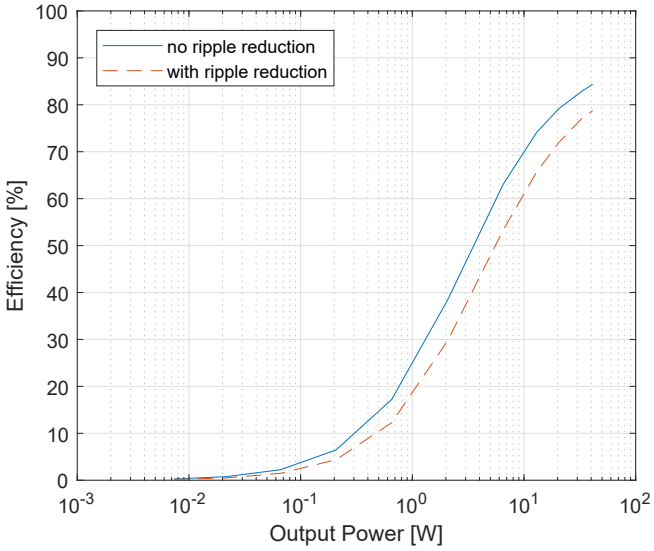


Figure 4.32: Amplifier efficiency versus output power with and without ripple reduction with $R_{\mathrm{load}} = 8\ \Omega$ and $f_{\mathrm{PWM}} = 768$ kHz.

technique is that it can be integrated on chip, providing ripple reduction without requiring extra external components.

Amplifier output voltage measurements have been taken and were sent to NXP to obtain indicative EMI simulation results using an antenna model that was internally available to them. The author has no further insight into this model and has considered it as a black box. The output of this model is shown in Figure 4.33 and has been compared to the CISPR25 emission mask to see if it would be compliant. While indeed the CM carrier is reduced below the mask. Power is increased in the 150 kHz through 280 kHz band, failing to meet compliance.

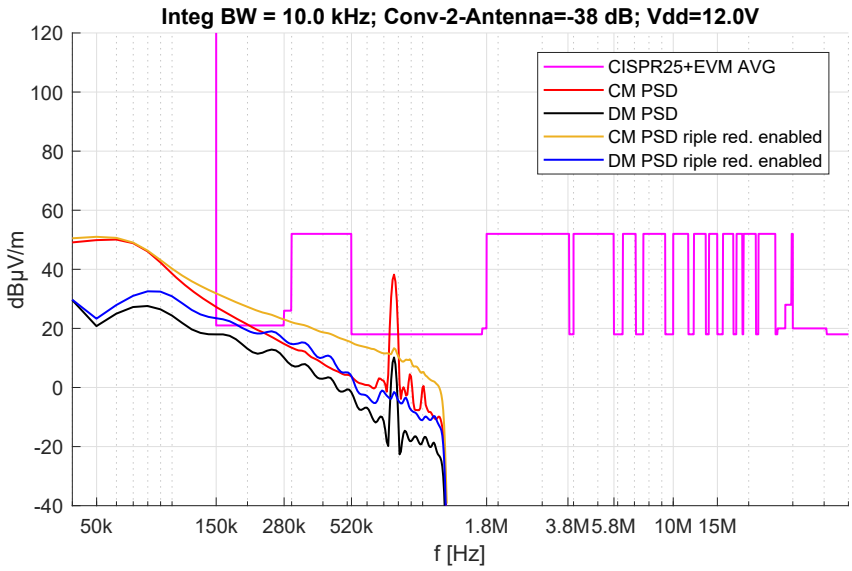


Figure 4.33: Simulated spectra of measured output voltages shown together with the CISPR25 masking curve.

A comparison to results of other works employing spread spectrum techniques is given in Table 4.2 at the end of this chapter. The listed works are amplifiers used in mobile applications which have attempted to reduce EMI. Spectra that illustrate the effect of switching frequency modulation and CM modulation and a combination of the two are presented in [44]. Apart from [46] the ripple reduction at f_{PWM} of this work is at least 10 dB better. Furthermore the presented technique does not increase the out-of-band noise as much as the spread spectrum based solutions. A downside of the proposed technique is the required extra power, whereas the other works do not consume extra power to implement the EMI reduction.

Next up, the proposed amplifier is compared to AB/D solutions listed in Table 4.3 at the end of this chapter. All these works do reduce the ripple at the output, however this cannot be compared quantitatively from the presented data. For quiescent power it is seen that this work consumes more power than [49, 52, 53] but less than [48, 50]. Efficiency could be

improved by making a monolithic integrated system. In that system, a current steering DAC tailored for this application will eliminate the biasing losses (0.5%). Furthermore, an integrated power stage will reduce on-resistance losses (2.5%). Finally this work operates from a single ended supply where all but [53] use a symmetric supply rail.

4.7 Discussion

This section provides extra details on the limitations of the feedback ripple reduction techniques.

Comparing the CM reduction of 40 dB in the SE simulation to the measured results on the BTL realization, which is effectively 2 times the SE solution, shows that the obtained CM ripple reduction is lacking performance compared to the simulation results. The open-loop gain after quantization is shown in Figure 4.34. This shows that the theoretical max-

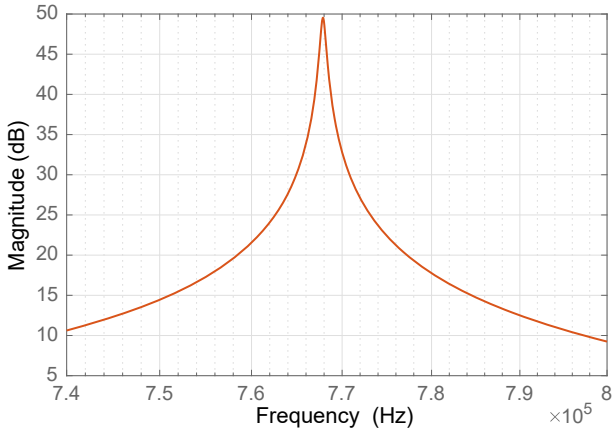


Figure 4.34: Zoomed in open-loop gain of the realized ripple reduction loop with quantized coefficients used in simulation.

imum ripple reduction is 49 dB, however it was already shown in the simulation (Figure 4.26) that noise floor due to the ADC quantization noise around the carrier is limiting ripple reduction to 40 dB. A tailor made ADC with lower noise around the carrier could improve performance. The noise floor around the carrier of the measurement does agree with the simulated result, however, the measurement only reaches 28 dB of reduction. In the measurements the frequency components at and around 768 kHz are not pushed down to the noise floor of the ADC as in the simulation.

The exact reason for this 12 dB degradation with respect to the simulation results has not been found. A possible cause are the parasitics in the PCB layout, the ripple reduction circuit could be placed closer to the LC filter in a re-design of the board or a monolithic solution. This will reduce the inductance of the trace from the ripple sink to the LC filter. Additionally, the actual ADC has a different response around the carrier

than its linear simulation model as it is based on an FIRDAC feedback loop to approximate the desired ideal behavior.

The used 3-phase PWM solution is not optimal as DAC, but was the only option in the available hardware. It could be improved by noise shaping the multi-bit digital signal to a single-bit PDM signal. Another option is to design a current-steering DAC.

The feedback technique as presented in this chapter could perform better were it not hampered by limitations of the current design. The used controller runs at a clock frequency of approximately 25 MHz and has 3 pipeline delay elements causing excess loop delay. The presented implementation already requires an excess loop delay compensation technique together with a lead compensator. A higher clock-frequency controller, or one with less pipeline delay could allow the loop to also have loop gain at the multiples of the PWM carrier frequency, increasing the effectiveness of the feedback.

The core idea behind the ripple-reduction loop filter is to place zeros on the unit circle in the NTF. This results in resonators in the open-loop transfer function, giving narrow-band suppression. However, due to the modulation of the carrier, it is required to have loop gain around the PWM carrier rather than only at the fundamental, so the nulls in the NTF have to be made more wide-band. This requirement necessitates that the compensation has to be done over a wider bandwidth, which is more difficult.

The implemented ripple reduction is a post-filter operation, hence post filter global feedback is required alongside the proposed technique to provide good audio performance. Besides this constraint it can work with any analog or digital Class-D implementation that uses an LC filter.

4.8 Conclusion

A ripple reduction technique for Class-D amplifiers has been presented. The proposed technique uses an ADC to measure and digitize the ripple at the load, because in the digital domain loop-filters with high gain at precisely the PWM frequency are easily created and do not suffer from component variability. High loop gain was provided by using a resonant digital loop filter. The CM ripple at 768 kHz is reduced by 27 dB for output power levels up to 10 W, which is in line with the simulated results. The power penalty of this technique has been reduced by implementation of a low-CM switching scheme.

State-of-the-art audio performance was provided by the AX5689, using feedback after the output filter, powered by the LLADC and a digital fifth-order loop filter.

Compared to the EMI reduction techniques that were evaluated, the disadvantage of this technique is that it consumes additional power, whereas the spread spectrum techniques use digital blocks consuming hardly any

additional power. These digital techniques however, do only spread the power over frequency, while the proposed technique reduces the PWM carrier with a minor increase in out-of-band noise.

Compared to the hybrid Class-AB/D amplifiers this solution has better control over the feedback because it is implemented in the digital domain. The efficiency of the presented approach could be improved by making an integrated system.

The final result is an audio amplifier with 28 dB ripple reduction requiring little extra power with 79% peak efficiency. Ripple power is removed instead of spread out over a wider band.

Acknowledgment

The authors would like to thank Tim van Doesum at Axign for his assistance on building the measurement setup.

Table 4.2: Comparison to Spread Spectrum Amplifiers

	Auer[44]	Guanziroli[14]	Ming[45]	Siniscalchi[47]	Balmelli[46]	This work
Architecture	Spread spectrum CM modulation	Spread spectrum	Spread spectrum	3-level	CM modulation	Active ripple reduction
Supply	5V	3.6-5V	2.5-5V	12V	2.7-6.6V	32V
f_{PWM}	390kHz	1296kHz	300kHz	250kHz	960kHz	768kHz
Ripple red. (CM)	17.8dB @390kHz / 7.3dB @10MHz	12dB @1296kHz	12dB @300kHz	HF EMI 20dB (not at f_{pwm})	25dB of AM channel	28dB @768kHz
OOB noise incr.	30+ dB @390kHz	18 dB @1296kHz	20 dB	n/a	up to 30 dB	3-6dB
Extra power	n/a	n/a	n/a	n/a	n/a	1.5W
Efficiency	n/a	81% @5V,8Ω,1W	90% @3.6V 8Ω .4W	90% @12V 8Ω 10W	85% @6.6V 3Ω 3.5W	79% @41W 8Ω
THD+N	0.018% @1W 1kHz	0.006% @4mW 3kHz, 0.2% @0.5W 3kHz	0.03% @.1W 1kHz	0.19% @5W 1kHz	0.05% @1W 1kHz	0.0016% @2W 1kHz

Table 4.3: Comparison to AB/D Amplifiers

	Nakagaki [48]	van der Zee [49]	Jung [50]	Walker [52]	Choi [53]	This work
Architecture	BTL AB w/ variable switched supply	SE AB w/ fb hyst. self osc. D	SE AB w/ fb hyst. self osc. D	SE AB w/ fb 2x self osc. Buck	BTL AB w/ fb hyst. self osc. D	BTL D w/ fb A w/ ripple fb
Supply	±10V	±18V	±22V	±20V	12V	32V
P_o max	2 × 100W	30W	60W	20W	10W	40W
f_{PWM}	200kHz	550kHz	300kHz	160kHz	180kHz	768kHz
Ripple red. (CM)	n/a	77dB w.r.t. filterless	n/a	n/a	n/a	28dB w.r.t. LC
Quiescent power	10W*	1.8W	10W*	around 1W*	0.5W*	4.3W
Dissipation	75W @P_o=75W	3.5W @P_o=10W	5.5W @P_o=50W	4W @P_o=24W	0.7W @P_o=10W	10W @P_o=40W
Efficiency	53% @100W 4Ω	85% @30W 4Ω	90% @50W 4Ω	85% @24W 7.5Ω	92% @10W 8Ω	79% @ 41W 8Ω
THD+N	0.008% @20W 1kHz	0.007% @1W 1kHz	0.005% @50W	0.003% @1W 0.05% @20W	0.1% @1W 1% @6W	0.0016% @2W 1kHz

* Estimated from graphs in the papers.

CHAPTER 5

FILTER DESIGN

In the previous chapter, a technique to reduce the effect of unit delays on stability was briefly mentioned. This chapter dives into the analytical loop filter design method that was used in the previous chapter to compensate parasitic poles in noise-shaping loop filters. This method has as benefit not having to increase the filter order and not having to change the original poles and zeros of the noise transfer function. The method has been applied to a low-pass loop filter with a parasitic unit delay and to a band-pass loop filter with either three unit delays or a high-frequency pole, obtaining stable loop filters in all three cases.

5.1 Introduction

Excess delay in a feedback loop can cause instability when it is not taken into account. Hence, solutions have been sought to mitigate or overcome the effects of excess delay on loop stability and system performance.

In the design of a noise-shaping loop, it is desirable to maximize the in-band performance for a given loop filter order and oversampling ratio (OSR). Maximizing performance also means that the stability margins are becoming small and that any parasitic element in the loop, such as a delay, could potentially make the system unstable.

In the research field of continuous-time $\Sigma\Delta$-modulators, techniques have been developed to compensate for excess loop delay (ELD). To restore the desired noise shaping characteristics of the delay-less system, a new set of coefficients for the loop filter has to be determined. Also, depending on the digital-to-analog converter (DAC) pulse shape and the length of the delay, a direct path around the quantizer may be required to restore the original noise transfer function (NTF).

The text after the section 5.1 has appeared in [CEL:4]

A shortcoming is, that when the delay in the digital path exceeds one clock cycle, it is not possible to apply classical ELD compensation. In that case, the NTF cannot be restored to its desired shape. The addition of local feedback as proposed in [74] as shown in Figure 5.1 can further improve the stability, but at the cost of requiring analog building blocks.

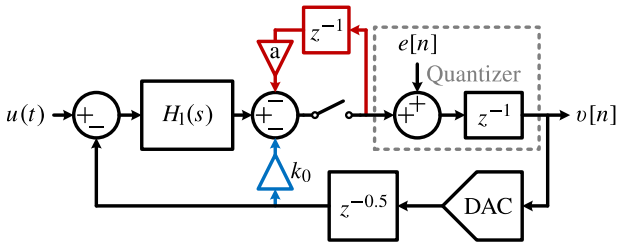


Figure 5.1: ΣΔ modulator with excess delay in the loop compensated using the method in [74] using a local loop (red) and a direct path (blue).

We aim to make a ΣΔ noise shaper in an existing piece of existing digital hardware with tunable coefficients, with no option to realize a direct path around the quantizer. Given this constraint, the objective is to still realize a stable noise shaper that can cope with excess delay and/or poles, at the expense of little performance.

The novelty of the presented technique is that it does not require additional analog building blocks to mitigate excess poles and can still gives a stability improvement. This does however result in lower performance than applying classical ELD compensation with a local feedback path. The application area where such a technique can have merits are, e.g., ΣΔ ADCs with a successive approximation register (SAR) quantizer, high-speed ΣΔ ADCs where the quantizers have to be pipelined, advanced dynamic element matching (DEM) algorithms [75], and mixed-signal systems with ADCs in the loop and digital processing delay.

An example of an implementation in existing hardware is the pulse-width modulation (PWM) ripple reduction technique presented in [CEL:3] . There, a noise shaping loop was designed using programmable digital filters in the hardware of the AX5689 [68]. The programmable loop filter in that system was originally designed to be used for signals in the audio band, however, for the application of PWM ripple reduction, higher frequency signals needed to be processed. The processing delay in the system caused a frequency-dependent phase shift which initially made the desired filter unstable after closing the loop.

In this chapter, a technique is proposed that accommodates integer cycles of excess delay and excess high-frequency poles in a digital loop filter by appending pole-zero pairs to the desired NTF. The system is stabilized without requiring additional hardware, such as direct paths or extra filter orders.

5.2 Prior Art

A common design procedure for ΣΔ analog-to-digital converters (ADCs) involves choosing the desired NTF and calculating the open-loop transfer function from the NTF [71, 76]. For this design method to work, it is assumed that the system is free of excess delay. However, in an actual continuous-time ΣΔ ADC as shown in Figure 5.1, the quantizer and the feedback DAC cannot give an instantaneous output. Consequently, the integrator(s) will integrate a delayed version of the desired feedback signal, which changes the desired closed-loop transfer and furthermore compromises the stability of the loop.

5.2.1 ELD Compensation

The open-loop transfer function of a system with ELD has to be modified so that the desired, delay-less closed-loop transfer and NTF are restored. To do this, the combination of non-idealities, such as the settling, slewing and quantizer delay can all be modeled together as a single delay term to make compensation straightforward [77, 78].

In a first order modulator this can be achieved by using, for instance, return-to-zero (RZ) coding in the DAC, making the system resilient to delays up to $\frac{1}{2}T_s$ [79]. For larger delays or when non-return-to-zero (NRZ) coding is used, part of the DAC pulse will exceed the sampling window and give an incorrect result after sampling the integrated signal. To restore the NTF in that case, it is required to add a direct feedback path around the quantizer with a gain dependent on the delay in the loop. In addition to that, the loop filter coefficients have to be tuned. Together, these measures compensate for the apparent error made by integrating the delayed DAC pulse [77, 79–83].

A different implementation uses a predictive comparator which estimates the delay of the output from the DAC pulse to change the comparison threshold [83] to obtain the same functional result as a direct path around the quantizer. Besides the analog solutions, it is also possible to compensate for the delay in the digital domain by adding a local digital feedback loop after the quantizer [82, 84]. However, this implementation does require a multi-bit DAC and sufficient precision in the digital registers to implement the coefficient that is conventionally used in the analog direct path.

A shortcoming of these classical ELD compensation solutions that has to be addressed is the compensation of delays in excess of one clock cycle.

5.2.2 Difficulties for ELD Compensation

The ELD compensation technique cannot be applied to any system, e.g. when the quantizer delay exceeds one or more clock cycles it is not possible to fully restore the desired NTF. In that case, the quantizer can be bypassed by adding a local loop (Figure 5.1) using a sample and hold circuit with

the feedback coefficient of the conventional direct path to achieve a similar stabilizing effect[74, 85, 86]. Focusing on the method in [74], the result of the compensation is essentially a lead-lag filter in front of the quantizer (Figure 5.1). Other examples of techniques in ADCs that complicate the implementation of ELD are DEM algorithms in the DAC or pipeline delay in high-speed noise-shaping algorithms. However, a direct path can be taken before the DEM algorithm to provide at least a less precise, fast feedback path [85]. In another more recent work, a time-interleaved quantizer based on a dual-slope ADC is utilized to have quantized data available before the conversion finishes, removing the conventional requirement of an extra delay after the quantizer and compensating for 2 cycles of unit delay [75].

The 'delsig' MATLAB toolbox by R. Schreier [87] provides a vast amount of functions to design loop filters for $\Sigma\Delta$ ADCs. It will be used here to implement the method in [74] to determine the compensated loop filter coefficients to compare the solution to the presented work.

In this paper, we want to present an alternative delay mitigation technique and highlight the differences and similarities between it and the ELD compensation technique from [74] in noise-shaping loops. The proposed method will allow the synthesis of a digital loop filter of equal order as the delay-free loop filter and can mitigate the effect of multiple unit delays and/or high-frequency poles without adding extra hardware. Furthermore, the original poles and zeros of the NTF do not change with respect to the system without parasitic poles or delay. The practical value of our approach is the usage in digital loop filters with tunable coefficients that have processing delay without changing the loop topology itself. Therefore the same hardware can be used.

The paper is organized as follows. Section 5.3 presents the filter design procedure, section 5.4 explains the mitigation method for a single parasitic pole, section 5.5 presents simulated results, conclusions are drawn in section 5.6 and Appendix 5.A provides mitigation methods for multiple parasitic poles.

5.3 Filter Design and Delay

In this section, the calculation of a loop filter from the NTF will be explained. Then, the effect of an added unit delay and a pole to a loop and the resulting NTF is shown.

5.3.1 Loop Filter From NTF

The loop filter with transfer $H(z)$ can be determined starting from the NTF of a closed loop system,

$$H(z) = \frac{1}{\mathrm{NTF}(z)} - 1. \tag{5.1}$$

To obtain a strictly causal loop filter, there are two constraints to the NTF, namely, equal order of numerator and denominator, as well as a unity factorized gain (the first sample of the impulse response is 1). The reason for these constraints is further explained in [71] section 4.4.1.

5.3.2 Parasitic element in a Loop

When a loop filter is derived from the NTF without taking parasitic effects, such as delay, in the feedback path into account, the actual system does not behave like the ideal design and might become unstable.

Let us look at the system by examining the resulting NTF of the system when a unit delay is added into the loop. By cascading z^{-1} with $H(z)$ and calculating the NTF using the inverse of (5.1) to obtain the actually realized $\mathrm{NTF_r}$,

$$\mathrm{NTF_r}(z) = \frac{1}{H(z) \cdot z^{-1} + 1}. \tag{5.2}$$

Since a unit delay is a pole at the origin, this equation can be written in a more general form to also take any known parasitic pole p_{par} into account,

$$\mathrm{NTF_r}(z) = \frac{1}{H(z) \cdot \frac{K}{z - p_{\mathrm{par}}} + 1}, \tag{5.3}$$

where $K = 1 - p_{\mathrm{par}}$ to preserve unity gain at DC. Since the poles of the open-loop transfer function are the zeros of the NTF, it is apparent that the parasitic pole p_{par} will appear as an extra zero in the NTF. The poles of the NTF will move with respect to their original locations in the desired NTF, which could push them close to, or out of the unit circle, indicating a marginally stable or unstable system. In the next section, we will address this further with a technique to mitigate this effect.

5.4 Mitigation Technique

The goal is to design loop filters that are stable with parasitic elements in the loop without increasing the loop-filter order as this would require changing the hardware. This work proposes a method that includes the parasitic(s) in the NTF design and keeps the original poles and zeros of the NTF at their original location. With this method, a new open-loop gain can be designed that consists of a cascade of a new loop filter and the parasitic(s) we are trying to compensate for, moreover, the filter can be stable in a closed loop. Since the parasitics are already present in the system, just realizing the new loop filter results in a stable system. The following sections explain this in more detail.

5.4.1 Design goal

In section 5.3 we described the procedure to obtain a loop filter from an NTF and have shown the effect of a parasitic unit delay on the NTF which

potentially makes the system unstable. This procedure is also shown schematically in Figure 5.2. Starting from the original NTF the loop filter H_{org} is obtained, subsequently a parasitic pole, p_{par}, is added. By transforming this open-loop transfer with parasitic back to the resulting NTF, $\mathrm{NTF_r}$ is obtained. $\mathrm{NTF_r}$ will contain an extra zero and an extra pole with respect to $\mathrm{NTF_{org}}$. This zero is at the same location as p_{par} because the zeros of the NTF are equal to the poles of the open-loop transfer function.

With this in mind we take the original NTF as a starting point and add p_{par} as a zero (z_{par}) to it as well as a pole p_{c} of which the value will be determined later. By doing this we aim to obtain a compensated NTF ($\mathrm{NTF_c}$) that after applying (5.1), yields a filter H_{new} of the same order as H_{org}.

5.4.2 Fewer Open Loop Zeros

We previously described how to obtain a strictly causal loop filter by setting constraints for the NTF. For the proposed mitigation technique it is required to have even fewer open-loop zeros. This is required to be able to separate the parasitic pole p_{par} from the loop filter H_{new} in the final step of Figure 5.2 after transforming the NTF. In this way, the filter H_{new} that has to be implemented is obtained.

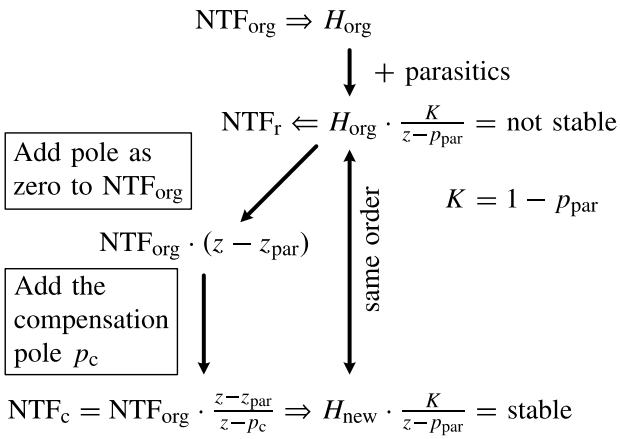


Figure 5.2: Flowchart describing the compensation method.

To reduce the order of the numerator from $N-1$ to $N-2$, where N is the order of the filter, the second-highest numerator polynomial coefficient a_{N-1} of the loop filter should also be nullified. This coefficient is a summation of all poles and zeros, which becomes apparent when the numerator term of the open-loop filter $H(z)$ is simplified to a polynomial,

$$H(z) = \frac{P_{\mathrm{NTF}}(z) - Z_{\mathrm{NTF}}(z)}{Z_{\mathrm{NTF}}(z)}, \tag{5.4}$$

with,

$$Z_{\mathrm{NTF}}(z) = (z - z_N)(z - z_{N-1})...(z - z_1), \tag{5.5}$$
$$P_{\mathrm{NTF}}(z) = (z - p_N)(z - p_{N-1})...(z - p_1). \tag{5.6}$$

The a_{N-1} coefficient is then calculated as follows,

$$\begin{aligned} a_{N-1} &= -p_1 - p_2 - ... - p_N + z_1 + z_2 + ... + z_N, \\ &= \sum_{n=1}^{N} z_n - \sum_{n=1}^{N} p_n. \end{aligned} \tag{5.7}$$

However, a degree of freedom is required to be able to nullify a_{N-1}. This degree of freedom can be found in the value of the pole p_{c}.

5.4.3 Modifying the NTF

To compensate for the parasitic pole p_{par} in the open-loop transfer, it was added as zero z_{par} to $\mathrm{NTF}_{\mathrm{org}}$. Consequently, a pole p_{c} was added to the NTF to satisfy the strict causality requirement. Since this pole location can be chosen freely, we would like to choose it such that we obtain a loop filter with a lower numerator order. This is accomplished by adding z_{par} and p_{c} to the zeros and poles in (5.7) respectively. Equating the result to zero and solving for p_{c} gives,

$$p_{\mathrm{c}} = z_{\mathrm{par}} + \sum_{n=1}^{N} z_n - \sum_{n=1}^{N} p_n. \tag{5.8}$$

The compensated NTF is now defined as,

$$\mathrm{NTF}_{\mathrm{c}}(z) = \mathrm{NTF}_{\mathrm{org}}(z) \cdot \frac{z - z_{\mathrm{par}}}{z - p_{\mathrm{c}}}. \tag{5.9}$$

From this equation, we also see that the compensated NTF contains all the poles and zeros of the original NTF, which is a key feature of this method.

5.4.4 Calculating the Required Loop Filter

To calculate the open loop transfer the modified NTF (5.9) is substituted in (5.1),

$$H_{\mathrm{c}}(z) = \frac{1}{\mathrm{NTF}_{\mathrm{c}}(z)} - 1. \tag{5.10}$$

This $H_{\mathrm{c}}(z)$ contains 2 fewer zeros than poles and because the parasitic pole was introduced as a zero in the NTF it will show as a pole in H_{c}, so H_{c} can be written as the combination of a strictly causal filter $H_{\mathrm{new}}(z)$ and the parasitic pole,

$$H_{\mathrm{c}}(z) = H_{\mathrm{new}}(z) \cdot \frac{K}{z - p_{\mathrm{par}}}. \tag{5.11}$$

Since the pole was already present in the system, the filter H_{new} has to be implemented to get the noise shaping as described by NTF_c. The filter $H_{\text{new}}(z)$ is defined as,

$$H_{\text{new}}(z) = H_{\text{c}}(z) \cdot \frac{z - p_{\text{par}}}{K}, \tag{5.12}$$

and is of the same order as the original loop filter.

This method can be extended to compensate any number of poles, which is shown in Appendix 5.A, although most practical parasitic problems are solvable with the single-pole method described in this section or possibly the 2-pole method.

5.5 Results

In this section, the mitigation method will be applied to a filter prototype to show what effect it has on the resulting loop filter and NTF. First, a low-pass loop filter with delay in the loop is designed to illustrate the approach on a familiar filter. It is compared with the result from compensating the loop filter like in [74] by using the toolbox [87], because it has in common that the NTF is modified as a result of the ELD compensation. It is also shown that a similar result can be achieved by manually relaxing the cut-off frequency or stopband attenuation.

After that, the method is used to design a band-pass loop filter with three unit delays in the loop, which is not straightforward to do manually. Finally, the method is applied to compensate for a low-pass pole to show the generality of the method.

5.5.1 Simulation Setup

First, the systems that are used to perform the simulations are discussed. The system to show the effect of the proposed method in this work is shown in Figure 5.3, and implements a loop that consists of a loop filter $H_{\text{new}}(z)$ and a quantizer modeled as an additive noise source and a unit delay element.

We examine the limiting case where exactly one unit delay is present in the quantizer, for which in a continuous-time sigma-delta ADC, compensation with a local loop around the quantizer is no longer possible. Hence,

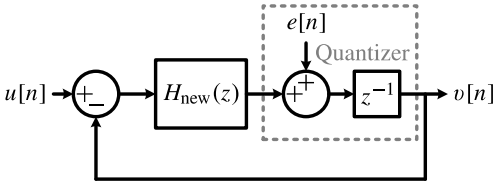


Figure 5.3: ΣΔ modulator with delay in the loop and a loop filter generated using this work.

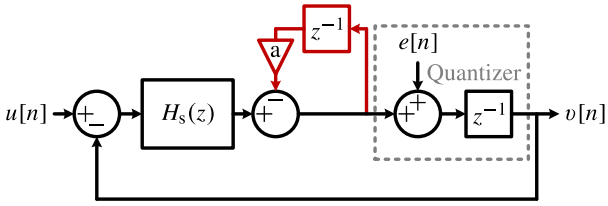


Figure 5.4: $\Sigma\Delta$ modulator with delay in the loop and a loop filter compensated using the local loop from [74].

a local loop before the quantizer is used for comparison to our proposed technique.

A comparison will be done to the system in Figure 5.4, which implements a similar system using the loop filter $H_s(z)$ and an extra local feedback loop as in [74]. The digital $H_s(z)$ filter coefficients are obtained as follows using the toolbox [87] to implement the method from Singh [74]:

- Realize a CT loop filter from the NTF with 1 cycle of delay:
  `realizeNTF_ct(NTF_org,'FF',[1 2])`
- Obtain the coefficient for the direct path from the state-space D matrix: $a = -D(3)$.
- Calculate the actual NTF for the implementation in Figure 5.4:
  $\mathrm{NTF_s} = \mathrm{NTF_{org}} \cdot (1 - az^{-1})$.
- Obtain the open loop transfer from the NTF and remove the unit delay and the local feedback, $1/(1 + az^{-1})$, from the obtained result to obtain the tuned filter $H_s(z)$:
  $H_s = (1/\mathrm{NTF_s} - 1) \cdot z \cdot (1 + az^{-1})$.

5.5.2 Unit Delay in a Low-pass Loop Filter

To design a low-pass loop filter, we start with a high-pass NTF because we want to shape the noise away from the passband of our system. A 4$^{\text{th}}$ order filter is designed from a Butterworth high-pass NTF with a corner at $f_s/20$. This NTF is quite aggressive with an out-of-band gain of 3.5 dB. All responses are normalized with f_s = 1 Hz. The original NTF ($\mathrm{NTF_{org}}$) is shown in Figure 5.5 together with the resultant NTF ($\mathrm{NTF_r}$) after adding a unit delay to the loop and the compensated NTFs: $\mathrm{NTF_c}$ and $\mathrm{NTF_s}$. Adding a delay to the aggressive loop filter makes the resulting system unstable which is illustrated by the strong peaking in $\mathrm{NTF_r}$. The compensated NTFs do not have this strong peaking, however, they do have an increased gain in the stopband up to the cut-off frequency and a roll-off in the passband. Comparing the proposed solution to the one provided by the method in [74], a weaker stopband attenuation is achieved, as well as a

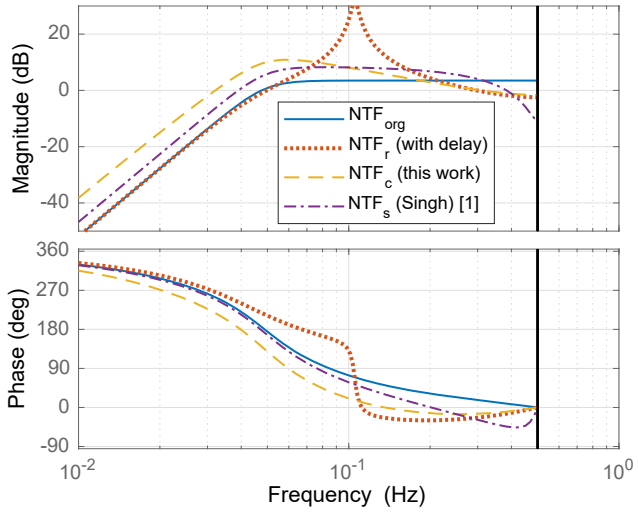


Figure 5.5: High-pass noise transfer with and without an added unit delay and with compensation.

flatter response in the passband at the expense of an extra first-order filter section.

The resultant open-loop transfers are shown in Figure 5.6. Observe that the phase margin of the compensated filter has increased with respect to the loop filter with delay. Looking at the compensated transfer, we notice that both the loop gain and cut-off frequency have decreased.

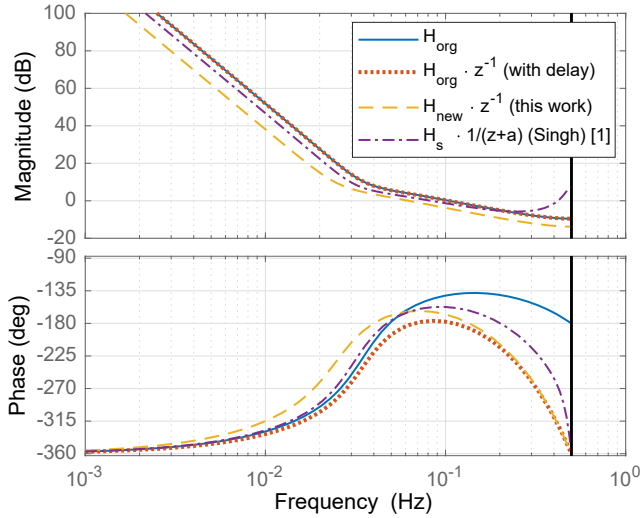


Figure 5.6: Low-pass open loop transfer with and without an added unit delay and with compensation.

5.5.3 Less Aggressive Filter

After the conclusion of the previous section, the reader might think that when the cut-off frequency and loop gain decrease by applying the proposed method, this could also be done upfront by choosing a less aggressive filter. Indeed, tuning the loop gain or cut-off frequency down by hand can also result in a more stable filter. To show this, a Butterworth filter prototype $\mathrm{NTF_m}$ that has an equal low-frequency stopband characteristic as the compensated NTF ($\mathrm{NTF_c}$) is taken to perform a comparison. The result of this comparison is shown in Figure 5.7.

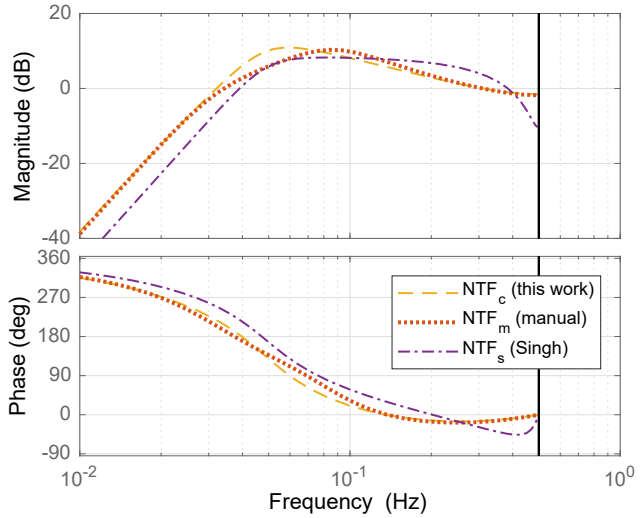


Figure 5.7: High-pass noise transfer with an added unit delay with compensation by the method versus manual tuning and the method in [74].

The difference in the plot is minimal, however, there is a difference, which can be shown by comparing the poles and zeros of both systems. Figure 5.8 shows the poles and zeros of the original and both compensated NTFs. The compensated NTF is a combination of the original NTF ($\mathrm{NTF_{org}}$) with the pole (p_c) added by the compensation method and the zero z_{par} that originates from the unit delay pole p_{par} in the loop filter. The same holds for the pole-zero pair introduced by the method adapted from [74]. The other set of poles and zeros is the resultant NTF ($\mathrm{NTF_m}$) of adding a unit delay to the loop filter that was derived from the manually tuned NTF.

5.5.4 Simulated Results

Discrete-time simulations are performed for the proposed solution, the solution based on [74] and the manually tuned solution, all three with a unit delay in the loop and a 2-bit quantizer. The original system without delay is also simulated for reference. The results for the in-band noise (IBN), maximum stable amplitude (MSA), and maximum signal-to-noise

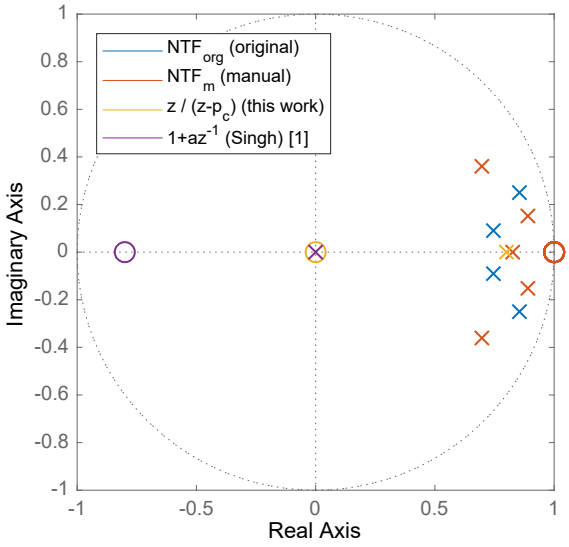


Figure 5.8: Pole zero plot of the prototype NTF, the added pole-zero pairs from the presented method and the method in [74] and the resultant NTF from the manually tuned filter.

ratio (SNR) are tabulated in Table 5.1. A bandwidth of 0 Hz – 0.02 Hz was used with a stimulus at 0.01 Hz.

Table 5.1: Simulated in-band performance: low-pass.

	IBN (dBFS)	MSA	Max SNR (dB)
Original (no delay)	–80.6	0.95	64.3
Singh [1]	–61.4	0.74	54.1
This work	–62.8	0.72	47.1
Manual tuning	–62.8	0.82	47.8

The proposed method, the Singh method, and the manually tuned filter perform comparably, except for the MSA, which is higher for the manually tuned filter, and the maximum SNR, which is 7 dB higher for the Singh method. Compared to the original filter without delay, all three see a large reduction in IBN and maximum SNR while allowing a unit delay in the loop.

5.5.5 Similarities with Prior Art

An interesting observation from Figure 5.8, is that the distance between the added pole and zero is the same for both the presented work and the method in [74]. The poles and zeros for both solutions adhere to nullifying (5.7) with the result that the open loop transfer function has 2 fewer zeros than poles. The solutions are dual in how this requirement is met: in the

method in [74] the extra NTF pole gets placed at $z = 0$ and the location of the extra zero is derived from (5.7). In this work, the extra NTF zero is placed at $z = 0$, and the extra pole follows from (5.8) instead. In equation form both NTFs are related to $\mathrm{NTF}_{\mathrm{org}}$ as follows,

$$\begin{aligned} \mathrm{NTF}_{\mathrm{c}} &= \mathrm{NTF}_{\mathrm{org}} \cdot \frac{z}{z - p_{\mathrm{c}}}, \\ \mathrm{NTF}_{\mathrm{s}} &= \mathrm{NTF}_{\mathrm{org}} \cdot \left(1 + az^{-1}\right), \\ \text{with: } p_{\mathrm{c}} &= a = 0.8 \end{aligned} \tag{5.13}$$

The modifications required on the open-loop transfers are quite different between the two solutions: In [74], an additional compensation filter (the local feedback before the quantizer) was added to compensate the unit delay (pole at $z = 0$) with a zero at $z = 0$ which effectively moves the open-loop pole to a new location at $z = -a$. In this work, only the coefficients of the noise-shaping filter have to be updated, as the additional NTF zero at $z = 0$ represents the unit-delay that is already in the loop and no additional compensation filter has to be added.

The poles and zeros of both the compensated NTFs still have the Butterworth alignment and are at the same location as in the original NTF apart from the extra compensation pole and zero, while the poles and zeros resulting from the manually tuned NTF do not. This is a key feature of both the proposed method and the method in [74].

5.5.6 Limits of the Compensation Method

The presented method to obtain the NTF that results in a stable loop filter will not work for filters with a too high order or too high cut-off frequency. Recall that the compensation pole p_{c} was calculated using (5.8) by subtracting the positions of all zeros by the positions of all poles in the filter. If we increase the cut-off frequency, the original poles will move further into the unit circle. As a result of this, the compensation pole p_{c} moves towards the unit circle and eventually escapes it, resulting in an unstable NTF. This limit does not occur for the method in [74], because the NTF will not become unstable when the zero at $z = -a$ moves out of the unit circle, however, the system does become non-minimum phase in that case.

Similarly, with a higher-order filter, more poles will be placed on the half-circle of the Butterworth formation which increases the sum of the pole locations. This also eventually pushes the compensation pole out of the unit circle.

When compensating for multiple poles, it is less intuitive to see what happens to the compensation poles as the filter becomes more aggressive. The resulting compensation poles are calculated by solving a system of equations as is explained in Appendix 5.A. The roots of these equations can yield complex compensation pole pairs. To obtain a stable compensation, all poles should satisfy the condition $\mathrm{abs}(p_{\mathrm{c}}) \leq 1$, stating that they reside inside the unit circle.

5.5.7 Delay in a Band-pass Loop Filter

A band-pass loop filter is designed by taking a 3rd order (6-pole) inverse Chebyshev band-reject NTF with a stopband attenuation of 55 dB in a bandwidth of .015 Hz centered around 1/8 Hz at a normalized sample rate of 1 Hz. Three unit delays are added into the loop, like in the system in Figure 5.3 with z^{-3} substituted for z^{-1}, and their effect is mitigated using the presented method. The realization of the compensation obtained from the method in [74] is shown in Figure 5.9, which now contains extra local feedback paths before the quantizer with coefficients corresponding to the direct path coefficients.

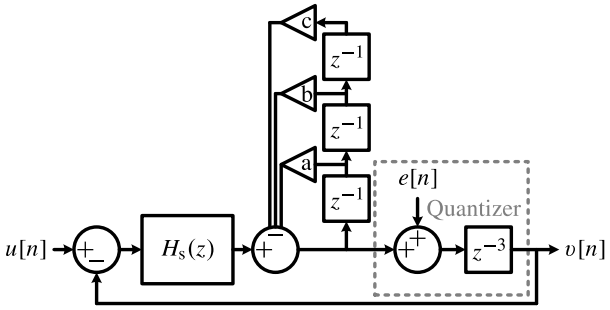


Figure 5.9: Noise shaper with delay in the loop and a loop filter compensated using the toolbox [87] and the method in [74].

The desired NTF is shown in Figure 5.10, together with the resulting NTFs after adding three unit delays in the loop. The corresponding open-loop transfers are shown in Figure 5.11. H_d is used to denote the three

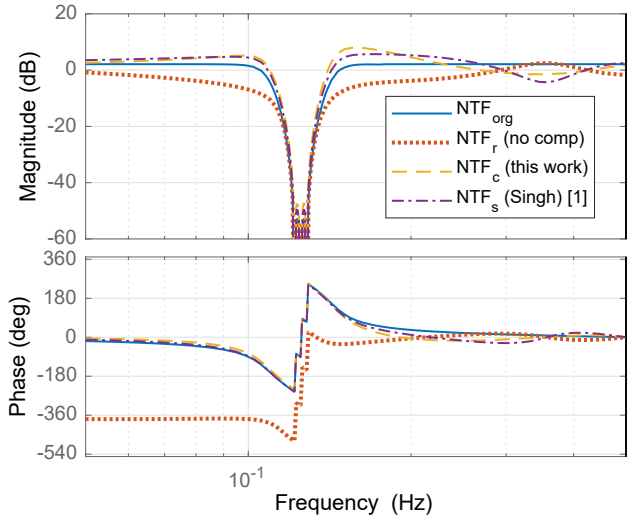


Figure 5.10: Band-reject noise transfer with and without three added unit delays and with compensation.

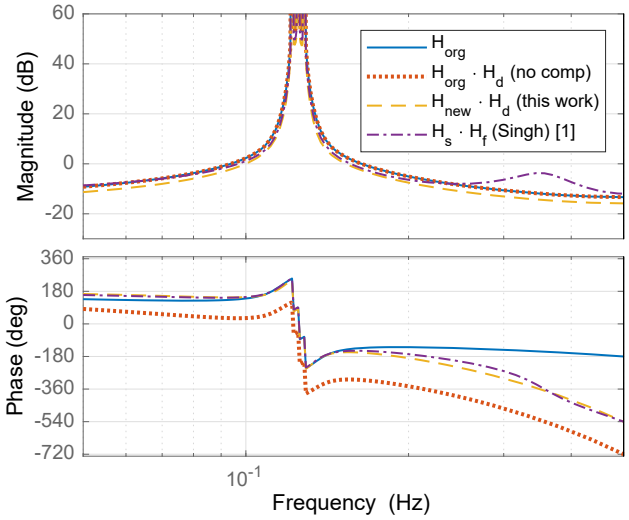


Figure 5.11: Band-pass open loop transfer with and without three added unit delays and with compensation.

unit delays and H_f is the transfer of the local feedback combined with the delays: $1/\left(z^3 + az^2 + bz + c\right)$. Adding delay to the loop filter renders the closed-loop system unstable. However, both compensation methods realize a stable system by matching the phase of the compensated loop gains to the phase of the original filter.

From Figure 5.12 it can be observed that the compensated NTFs have the desired poles at the exact same location as the prototype NTF, with

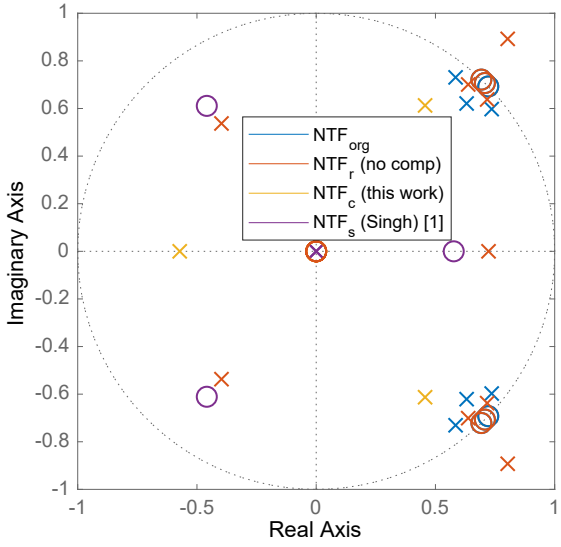


Figure 5.12: Pole zero plot of the prototype NTF, the added compensation poles and zeros and the resultant NTF from adding three unit delays.

the addition of the three compensation poles and zeros for the three unit delays. It is worth mentioning that both methods produce an NTF that satisfies the conditions that the second (5.7), third (5.17) and fourth (5.25) numerator coefficient of the open-loop transfer are nullified. This shows that both solutions share a common solution space where the proposed solution has a minimal realization and the prior art gives better noise shaping performance. Intermediate solutions where both the extra poles and zeros in the NTF are not in the origin have been investigated but did not yield better results than the two presented methods.

The filters have been simulated using a discrete-time Matlab Simulink model resembling Figure 5.9 with a single bit quantizer to show the effect of the added non-ideality on the performance of the modulator. Table 5.2 lists the IBN without any input, the MSA with a stimulus at 1/8 Hz, and the maximum SNR. Both the presented work and the method in [74] see a more than 10 dB drop in IBN compared to the ideal modulator, with the presented work performing only 2.6 dB worse than the prior art. The SNR shows a similar trend with a 5.4 dB drop compared to the prior art and the MSA is .06 lower than the prior art.

Table 5.2: Simulated in-band performance: band pass.

	IBN (dBFS)	MSA	Max SNR (dB)
Original (no delay)	–91.1	0.99	81.6
Singh method [74]	–80.7	0.91	73.8
This work	–78.1	0.85	68.4

Just like in the low-pass example from the previous section, manual tuning of the gain of the original NTF can be tried to design a stable closed-loop filter. For this case, the manually tuned NTF was designed by using a lower stopband attenuation factor which is equal to the attenuation in the compensated NTF. However, this manual tuning method does not yield stable results for band-pass filters.

The reason for this can be observed in the pole-zero plot in Figure 5.12, which shows the pole and zero locations of the resulting NTFs when a delay is added to the loop. In the uncompensated filter, one complex pole pair is still outside the unit circle, showing that it is unstable. The manually tuned filter will also have a complex pole pair outside of the unit circle.

5.5.8 Low-pass Pole in a Band-pass Loop Filter

A more generic case is to compensate a pole rather than a unit delay. In this section, an example is given to compensate a parasitic pole in the loop. Such a pole could originate from analog bandwidth limitations. The characterization of this pole in a system is outside of the scope of this theoretical analysis, hence this section will solely focus on the compensation of the pole.

A band-pass loop filter is designed by taking a 3rd order inverse Chebyshev band-reject NTF with a stopband attenuation of 55 dB in a bandwidth of 0.005 Hz centered around 1/16 Hz at a sample rate of 1 Hz. The added parasitic low-pass pole in the feedback path is located at 0.11 Hz. The original, uncompensated, and compensated NTFs are shown in Fig 5.13.

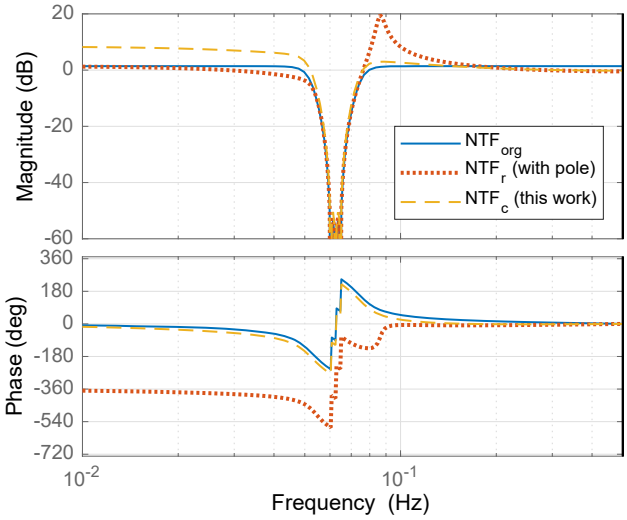


Figure 5.13: Band-reject noise transfer with and without an added pole and with compensation.

The NTF resulting from the parasitic pole ($\mathrm{NTF_r}$) shows peaking, while the NTF with the mitigation technique applied has a 7 dB increased passband gain at frequencies below the stopband. Looking at the pole-zero plot in Figure 5.14, it is seen that $\mathrm{NTF_r}$ with the parasitic pole is unstable, just like the filter with the three delays from the previous section. It is also apparent that the NTF zero (z_{par}) originating from the pole (p_{par}) in the loop is not in the center of the unit circle as was the case for the delay. Hence, compensation of a pole becomes increasingly difficult as the NTF pole location p_{c} calculated by (5.8) will be offset towards 1. This amount is set by the NTF zero that originates from the parasitic pole in the loop. The lower the parasitic pole frequency, the further the compensation NTF pole is pushed towards 1, eventually making compensation impossible.

5.5.9 Spread of the Low-pass Pole

In an actual system, the parasitic pole can be in the analog domain. This means that the component that causes this pole can be affected by process spread. In this section, we investigate if the compensation method is robust against the resulting spread in the parasitic pole location.

The NTF prototype of the previous section is taken again and the same pole is compensated for. However, for the actual implementation we keep the designed filter H_{new}, but take a different pole in the feedback path that

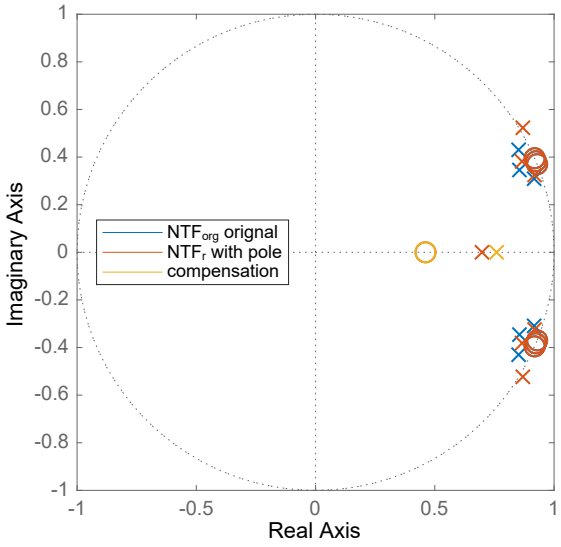


Figure 5.14: Pole zero plot of the prototype NTF, the added compensation poles and zeros and the resultant NTF with the parasitic.

has a $\pm 20\%$ deviation with respect to the original pole p_{par}. From that open-loop transfer function, the resulting NTF is calculated. The resulting pole-zero plot is shown in Figure 5.15. Observe that the Chebyshev poles have shifted from their original location, but that the NTFs have not become unstable. Furthermore, it can be seen that when the zero (z_{par}) at the location of the parasitic pole moves towards 1, then p_{c} also moves towards

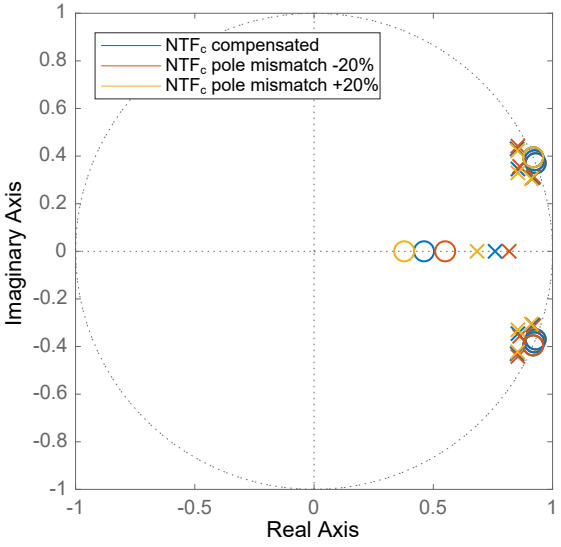


Figure 5.15: Pole zero plot of the compensated NTF and the resultant NTFs from having a deviation of the actual parasitic.

1. The closer the frequency of the parasitic pole is to the desired filter, the smaller the headroom for spread becomes before the filter becomes unstable.

The effect of the spread in the parasitic pole on modulator performance has been evaluated through simulation of the schematic in Figure 5.16 with a 2-bit quantizer and K as $1 - p_{\mathrm{par}}$ to have a unity-gain at DC for the feedback pole p_{par}. A sinusoidal stimulus at the center of the band was used like in the previous simulation to obtain the results shown in Table 5.3. Stable operation is obtained in the nominal case and the $\pm 20\%$ cases with very minor differences in the IBN, MSA, and maximum SNR. Compared to the original filter, the maximum SNR is reduced by at least 4 dB, the MSA drops by 9%, and the IBN increases by 15 dB.

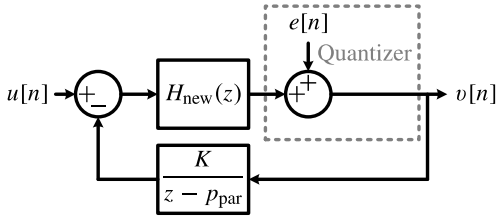


Figure 5.16: $\Sigma\Delta$ modulator with delay in the loop and a loop filter generated using this work.

Table 5.3: Simulated in-band performance of the band-pass modulator with mismatch between the actual and compensated parasitic low-pass filter.

	IBN (dBFS)	MSA	Max SNR (dB)
Original (no parasitic)	–106.3	1.00	93.7
This work (nominal)	–91.1	0.91	87.8
This work (f_{pole} +20%)	–92.2	0.86	89.0
This work (f_{pole} –20%)	–95.0	0.90	86.6

5.6 Conclusion

In this paper, an analytical technique to design stable loop filters with parasitic poles in their feedback paths was presented. A step-by-step method has been given to get from the desired NTF and a parasitic pole to an implementable stable loop filter. The method does not require any additional feedback paths or additional filter orders. Instead, it adapts the open-loop filter dynamics such that the closed-loop poles and zeros remain at their original location in the presence of the parasitic. Next to the original closed-loop poles and zeros, the parasitic does introduce an additional pole-zero pair in the NTF, which results in a performance penalty compared to the desired NTF. Moreover, the closed-loop filter can

still become unstable if the parasitic is too dominant for the desired NTF. The method has been applied to both low-pass and band-pass loop filter design methods to show its versatility.

The presented method has been compared to a modified ELD compensation method based on the work in [74], referred to as the 'Singh method'. It was presented which conditions the NTF has to adhere to such that the loop-filter derived from it contains $N+1$ fewer zeros than poles, where N is the number of unit delays. For a single unit delay, the constraint is that the sum of the poles of the NTF should equal the sum of the zeros. This implies that the distance between the pole and zero that are added to the original NTF is constrained and irrespective of the chosen compensation method. And indeed this distance was found to be the same for both methods, and that it equals the coefficient for the direct path in classical ELD compensation. In summary, both solutions share the same solution space, where the presented method favors a minimal realization using the existing hardware with no required extra hardware and the prior art favors performance at the expense of extra filter orders or direct paths.

Appendix 5.A Mitigation of Multiple Poles

Section 5.3 has shown the mitigation technique for a single parasitic pole. The extension to mitigate two, three, and four poles is shown in this appendix.

5.A.1 Method for Two Poles

When two poles $(p_{\mathrm{par1}}, p_{\mathrm{par2}})$ are in the loop, two zeros $(z_{\mathrm{par1}}, z_{\mathrm{par2}})$ are added to the NTF, resulting in the requirement of two extra poles $(p_{\mathrm{c1}}, p_{\mathrm{c2}})$ as well. These two poles can be calculated as such that $H_{\mathrm{c}}(z)$ contains 3 fewer zeros than poles. In order to do this the a_{N-2} coefficient in the numerator polynomial of $H_{\mathrm{c}}(z)$ needs to be nullified in addition to the a_{N-1} and a_N coefficients. The coefficient a_{N-2} consists of a summation of unique products of pole pairs and zero pairs,

$$\begin{aligned} a_{N-2} &= p_1p_2 + ... + p_{N-1}p_N - (z_1z_2 + ... + z_{N-1}z_N), \\ &= \sum_{n=1}^{N-1} p_n \left(\sum_{m=n+1}^{N} p_m \right) - \sum_{n=1}^{N-1} z_n \left(\sum_{m=n+1}^{M} z_m \right), \end{aligned} \tag{5.14}$$

which will be simplified to (5.15) for conciseness,

$$a_{N-2} = \sum P_{\mathrm{pairs}} - \sum Z_{\mathrm{pairs}}. \tag{5.15}$$

By equating the condition for one pole in (5.7) to 0 we can derive the first condition that has to be satisfied,

$$p_{\mathrm{c1}} + p_{\mathrm{c2}} + \sum_{n=1}^{N} p_n = z_{\mathrm{par1}} + z_{\mathrm{par2}} + \sum_{n=1}^{N} z_n. \tag{5.16}$$

The second condition is derived from (5.15),

$$p_{c1} \cdot p_{c2} + (p_{c1} + p_{c2}) \sum_{n=1}^{N} p_n + \sum P_{\text{pairs}} = \sum Z_{\text{pairs}}. \tag{5.17}$$

The constraints in (5.16) and (5.17) have to be solved first for $p_{c1} + p_{c2}$ and then for $p_{c1} \cdot p_{c2}$. By taking $p_{c1} + p_{c2} = a$ and $p_{c1} \cdot p_{c2} = b$ we can solve for p_{c1},

$$p_{c1} = a - p_{c2} = a - b/p_{c1}, \tag{5.18}$$

$$p_{c1}^2 = a p_{c1} - b, \tag{5.19}$$

$$p_{c1}^2 - a p_{c1} + b = 0. \tag{5.20}$$

Now, a and b can be derived from (5.16) and (5.17),

$$a = \sum_{n=1}^{N} z_n + z_{\text{par1}} + z_{\text{par2}} - \sum_{n=1}^{N} p_n, \tag{5.21}$$

$$b = \sum Z_{\text{pairs}} - a \sum_{n=1}^{N} p_n - \sum P_{\text{pairs}}. \tag{5.22}$$

Solving (5.20) will yield two solutions for p_{c1}, with the second solution automatically being p_{c2}. Now we can write compensated NTF as follows,

$$\text{NTF}_c(z) = \text{NTF}(z) \cdot \frac{(z - z_{\text{par1}})(z - z_{\text{par2}})}{(z - p_{c1})(z - p_{c2})}. \tag{5.23}$$

After transforming NTF_c to $H_c(z)$ using (5.1), the filter that has to be implemented can be calculated,

$$H_{\text{new}}(z) = H_c(z) \cdot \frac{K_1}{z - p_{\text{par1}}} \cdot \frac{K_2}{z - p_{\text{par2}}}, \tag{5.24}$$

where $K_1 = 1 - p_{\text{par1}}$ and $K_2 = 1 - p_{\text{par2}}$.

5.A.2 Method for More Poles

Instead of showing the full derivation, we show the equations that have to be solved. In the case of a system with three parasitic poles, the following open loop numerator coefficient should be nullified as well,

$$a_{N-3} = \sum Z_{\text{triplets}} - \sum P_{\text{triplets}}. \tag{5.25}$$

By adding this constraint to the prior constraints for two poles, mitigating the effect of three open loop poles can be achieved by using the solutions of (5.26) as extra poles in the NTF,

$$p_c^3 - a \cdot p_c^2 + b \cdot p_c - c = 0, \tag{5.26}$$

with,

$$a = \sum_{n=1}^{N} z_n + \sum_{m=1}^{M} z_{\mathrm{par},m} - \sum_{n=1}^{N} p_n, \tag{5.27}$$

$$b = \sum Z_{\mathrm{pairs}} - a \sum_{n=1}^{N} p_n - \sum P_{\mathrm{pairs}}, \tag{5.28}$$

$$c = \sum Z_{\mathrm{triplets}} - b \sum_{n=1}^{N} p_n - a \sum P_{\mathrm{pairs}} - \sum P_{\mathrm{triplets}}. \tag{5.29}$$

Where M in (5.27) is the number of added zeros, which is three in this case. The 'triplets' summation is the sum of products of unique pole/zero triplets.

Likewise for four poles the equation that has to be solved is,

$$p_{\mathrm{c}}^4 - a \cdot p_{\mathrm{c}}^3 + b \cdot p_{\mathrm{c}}^2 - c \cdot p_{\mathrm{c}} + d = 0, \tag{5.30}$$

with a, b and c as in (5.27), (5.28) and (5.29) respectively and,

$$\begin{aligned} d = \sum Z_{\mathrm{quads}} - c \sum_{n=1}^{N} p_n - b \sum P_{\mathrm{pairs}} \\ - a \sum P_{\mathrm{triplets}} - \sum P_{\mathrm{quads}}. \end{aligned} \tag{5.31}$$

The 'quads' summation is the sum of products of unique pole/zero quadruplets.

An extension to even more parasitic poles is possible by extending the equations with quintuplets, sextuplets, etc.

CHAPTER 6

Conclusions and Recommendations

In this chapter, the results of the work in this thesis are summarized and the overall conclusions are drawn. Finally, recommendations for future work are given

6.1 Summary and Conclusion

In this thesis, an overview of commonly used techniques in Class-D amplifiers was presented. Then, the prior art of EMI reduction techniques were discussed. A deeper dive into the subjects of multi-phase and multi-level converters was done to find a direction for further research. However, both these techniques require a lot of undesired external components and were hence not pursued further. Instead, the focus was shifted towards an active ripple reduction technique. Considerations on whether to make a feed-forward or feedback solution were given. The feed-forward solution requires full knowledge of the used components and requires a servo loop to estimate the component values in real-time. The feedback solution can compensate for all non-linearities given that it can be made stable with ample loop gain. The feedback solution was deemed to be the most feasible and chosen for implementation.

The prototype presented in chapter 4 has shown that ripple voltage after the output filter was reduced, resulting in a CM ripple reduction of 28 dB. The AX5689 IC was used to implement the designed loop filter, while the IC also provides the ADCs to digitize the ripple and has PWM outputs to drive the current source to sink the ripple current. It has been shown that peak system efficiency with ripple reduction enabled is 79% and ripple power is removed from the spectrum instead of spread out over a wider band.

The challenge of designing a loop filter with parasitics in mind has been addressed and a method which extends on the NTF loop filter design routine was developed in chapter 5. This method was used to obtain a stable loop filter by taking one or more parasitic poles, such as unit delays, into account by putting them into the desired NTF as zeros. This method has successfully been applied to mitigate the effect of processing delay on stability in the control system of the implemented ripple reduction loop.

The final combined result is a Class-D amplifier with 28 dB of CM ripple reduction governed by the proposed active circuit and digital loop-filter.

6.2 Discussion and Recommendations

The choice of implementing the system inside the AX5689 controller has limited the design space of the ripple loop filter. A custom implementation would allow for compensation of multiple PWM harmonics in addition to the fundamental tone. Local feedback around the 1-bit DAC that controls the current source would shape its quantization noise, possibly allowing a single phase PWM DAC instead of three phases. A 2-tap moving average filter could be used inside the ripple reduction loop to reject the component at $f_s/2$ and filter the frequencies below that frequency.

The implementation of the current source could also be improved by implementing a current steering DAC. This would enable the fabrication of a monolithic solution which contains the controller, ripple feedback as well as a power stage. The current source could also be implemented as a low-power Class-D amplifier, however, this would require switching at a higher frequency than the main amplifier which could shift the EMI problem to higher frequencies. One could argue that in that case, it might be better to design just one amplifier using a PWM frequency in the megahertz range.

Ripple reduction is more efficient when the ripple current is small. In 3.1 it was shown that the ripple current scales inversely proportional to the switching frequency and the output filter inductance. This gives a trade-off between inductor size and dissipation of the ripple current. It further suggests that high frequency switching could be a good alternative.

The power efficiency of the total amplifier solution does suffer from the additional power dissipation in the ripple sinks, hence when efficiency is of paramount importance, a ripple reduction solution as was presented is not a viable option.

Lowering the component count of the amplifier solution was not achieved in this work, while the ripple reduction circuity has added components to the existing solution. A monolithic solution would allow component reduction of the ripple reduction circuitry as it can be fully integrated in the silicon.

Another phenomenon that was not looked at in further detail is the high-frequency ringing when the output stage is switched. This also causes EMI and is not yet fully understood. Future work could provide insight into

the fundamental mechanisms of this ringing and give directions towards minimizing or compensating the emissions from it.

6.3 Original Contributions

- A digital feedback system was used to reduce the ripple in Class-D amplifiers, which can be applied to any fixed carrier PWM system.
- Digital feedback was developed, which allows for selective filtering, providing high gain at the PWM frequency component without suffering from analog component spread.
- To limit the power dissipation, a low-CM signaling modulation scheme was implemented. For small signals the load will be actuated from both half bridges, however when the signal becomes large, one half bridge is clamped to a minimum level while the other half bridge handles the signal.
- An NTF-based loop filter design method was proposed where parasitic poles, such as delays, can be taken into account by putting zeros into the NTF at those pole locations to stabilize the loop.

REFERENCES

[1] M. Berkhout, L. Breems, and E. van Tuijl, "Audio at Low and High Power," in *Proc. ESSCIRC*, Sep. 2008, pp. 40–49.

[2] A. I. Colli-Menchi, J. Torres, and E. Sanchez-Sinencio, "A Feed-Forward Power-Supply Noise Cancellation Technique for Single-Ended Class-D Audio Amplifiers," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 718–728, Mar. 2014.

[3] C. Neesgaard and L. Risbo, "PWM Amplifier Control Loops with Minimum Aliasing Distortion," in *120th Audio Eng. Soc. Conv.*, Paris, May 2006, pp. 1–15.

[4] Wei Shu and J. Chang, "THD of Closed-Loop Analog PWM Class-D Amplifiers," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 55, no. 6, pp. 1769–1777, Jul. 2008.

[5] K. Philips, J. van den Homberg, and C. Dijkmans, "PowerDAC: a single-chip audio DAC with a 70\%-efficient power stage in 0.5 μm CMOS," in *IEEE ISSCC Dig. Tech. Pap.* IEEE, 1999, pp. 154–155.

[6] T. Mouton and B. Putzeys, "Digital Control of a PWM Switching Amplifier with Global Feedback," in *Proc. AES 37th Int. Conf.*, Hillerod, Aug. 2009, pp. 1–10.

[7] H. Zhang, M. Berkhout, K. A. Makinwa, and Q. Fan, "A - 121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1153–1161, Apr. 2022.

[8] E. Gaalaas, B. Liu, N. Nishimura, R. Adams, and K. Sweetland, "Integrated stereo $\Delta\Sigma$ class D amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2388–2397, Dec. 2005.

[9] B. Putzeys, "Simple Self-Oscillating Class D Amplifier with Full Output Filter Control," in *118th Audio Eng. Soc. Conv.*, Barcelona, May 2005.

[10] S. H. Chien, Y. W. Chen, and T. H. Kuo, "A low quiescent current, low THD+N Class-D audio amplifier with area-efficient PWM-residual-aliasing reduction," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3377–3385, 2018.

[11] S.-h. Chien, T.-h. Kuo, H.-y. Huang, H.-b. Wang, and Y.-z. Qiu, "A 0.41mA Quiescent Current, 0.00091% THD+N Class-D Audio Amplifier with Frequency Equalization for PWM-Residual-Aliasing Reduction," in *IEEE ISSCC Dig. Tech. Pap.*, vol. 51, no. 6. IEEE, 2020, pp. 352–354.

[12] H. Zhang, M. Berkhout, K. A. Makinwa, and Q. Fan, "A 121.4-dB DR Capacitively Coupled Chopper Class-D Audio Amplifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3736–3745, Dec. 2022.

[13] M. Berkhout and L. Dooper, "Class-D Audio Amplifiers in Mobile Applications," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 57, no. 5, pp. 992–1002, 2010.

[14] F. Guanziroli, R. Bassoli, C. Crippa, D. Devecchi, and G. Nicollini, "A 1 W 104 dB SNR Filter-Less Fully-Digital Open-Loop Class D Audio Amplifier With EMI Reduction," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 686–698, Mar. 2012.

[15] D. Reefman and P. Nuijten, "Why Direct Stream Digital is the best choice as a digital audio format," in *110th Audio Eng. Soc. Conv.*, 2001, pp. 1–8.

[16] B. Putzeys and R. de Saint Moulin, "A True One-Bit Power D/A Converter," in *112th Audio Eng. Soc. Conv.*, Munich, 2002.

[17] K. Nielsen, "A Review and Comparison of Pulse Width Modulation (PWM) methods for analog and digital input switching power amplifiers," in *102nd Audio Eng. Soc. Conv.*, Munich, Mar. 1997.

[18] L. Risbo and H. K. Andersen, "Conversion of a PCM signal into a UPWM signal," U.S. Patent 6 657 566, Dec. 2, 2003.

[19] F. Nyboe, C. Kaya, L. Risbo, and P. Andreani, "A 240W Monolithic Class-D Audio Amplifier Output Stage," in *IEEE ISSCC Dig. Tech. Pap.* IEEE, 2006, pp. 1346–1355.

[20] C. Neesgaard, T. Efland, C. Kaya, K. Mochizuki, F. Nyboe, L. Risbo, D. Skelton, and A. Zhao, "Class D Digital Power Amp (PurePath Digital) High Q Musical Content," *16th Int. Symp. Power Semicond. Devices ICs, 2004. Proceedings. ISPSD '04.*, pp. 97–100, 2004.

[21] K. Nielsen, "PEDEC - A Novel Pulse Referenced Control Method for High Quality Digital PWM Switching Power Amplification," in *29th Annu. IEEE Power Electron. Spec. Conf.*, vol. 1, no. 1. IEEE,

1998, pp. 200–207.

[22] H. Ihs and C. Dufaza, "Digital-Input Class-D Audio Amplifier," in *128th Audio Eng. Soc. Conv.*, 2010.

[23] A. Donida, R. Cellier, A. Nagari, P. Malcovati, and A. Baschirotto, "A 40-nm CMOS, 1.1-V, 101-dB dynamic-range, 1.7-mW continuous-time ΣΔ ADC for a digital closed-loop class-D amplifier," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 3, pp. 645–653, Mar. 2015.

[24] E. Cope, J. Aschieri, T. Lai, F. Zhao, W. Grandfield, M. Clifford, P. Rathfelder, Q. Liu, S. Kavilipati, A. Vandergriff, and G. Miaille, "A 2×20W 0.0013% THD+N Class-D audio amplifier with consistent performance up to maximum power level," in *IEEE ISSCC Dig. Tech. Pap.*, vol. 61. IEEE, Feb. 2018, pp. 56–58.

[25] M. Auer and T. Karaca, "A Class-D Amplifier with Digital PWM and Digital Loop-Filter using a Mixed-Signal Feedback Loop," in *Proc. ESSCIRC*, 2019, pp. 153–156.

[26] D. Schinkel, W. Groothedde, F. Mostert, M.-J. Koerts, E. van Iersel, D. Groeneveld, and L. Breems, "A Multiphase Class-D Automotive Audio Amplifier With Integrated Low-Latency ADCs for Digitized Feedback After the Output Filter," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3181–3193, Dec. 2017.

[27] "Digital audio converter and amplifier controller," Axign B.V., Enschede, The Netherlands, Product brief, 2015. [Online]. Available: http://axign.nl/wp-content/uploads/AX5689_amplifier_controller_product_brief_D2g.pdf (Accessed 15-11-2016).

[28] M. Sobaszek, "Self-Tuned Class-D Audio Amplifier with Post-Filter Digital Feedback Implemented on Digital Signal Controller," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 67, no. 3, pp. 797–805, 2020.

[29] M. Kinyua, R. Wang, and E. Soenen, "Integrated 105 dB SNR, 0.0031% THD+N Class-D Audio Amplifier With Global Feedback and Digital Control in 55 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1764–1771, Aug. 2015.

[30] A. Matamura, N. Nishimura, P. Birdsong, A. Bandyopadhyay, A. Spirer, M. Markova, and S. Liu, "An 82mW ΔΣ-Based Filter-Less Class-D Headphone Amplifier with -93dB THD+N, 113dB SNR and 93% Efficiency," in *IEEE ISSCC Dig. Tech. Pap.* IEEE, Feb. 2021, pp. 432–434.

[31] M. Berkhout, "A 460W Class-D Output Stage with Adaptive Gate Drive," in *IEEE ISSCC Dig. Tech. Pap.*, Feb. 2009, pp. 452–453,453a.

[32] L. Dooper and M. Berkhout, "A 3.4 W Digital-In Class-D Audio Amplifier in 0.14 µm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1524–1534, Jul. 2012.

[33] M. Berkhout, "An Integrated 200-W Class-D Audio Amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1198–1206, Jul. 2003.

[34] H. Ma, R. van der Zee, and B. Nauta, "An integrated 80-V class-D power output stage with 94% efficiency in a 0.14µm SOI BCD process," in *Proc. ESSCIRC*, Sep. 2013, pp. 89–92.

[35] Z. Liu, L. Cong, and H. Lee, "Design of On-Chip Gate Drivers With Power-Efficient High-Speed Level Shifting and Dynamic Timing Control for High-Voltage Synchronous Switching Power Converters," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1463–1477, 2015.

[36] M. Berkhout, "A Class D Output Stage With Zero Dead Time," in *IEEE ISSCC Dig. Tech. Pap.*, Feb. 2003, pp. 134–135.

[37] H. Ma, R. van der Zee, and B. Nauta, "A High-Voltage Class-D Power Amplifier With Switching Frequency Regulation for Improved High-Efficiency Output Power Range," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1451–1462, Jun. 2015.

[38] M. Berkhout, "Integrated Overcurrent Protection System for Class-D Audio Power Amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2237–2245, Nov. 2005.

[39] M. Berkhout, L. Dooper, and B. Krabbenborg, "A 4Ω 2.65W Class-D Audio Amplifier With Embedded DC-DC Boost Converter, Current Sensing ADC and DSP for Adaptive Speaker Protection," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2952–2961, Dec. 2013.

[40] J. Honda and J. Adams, "Class D Audio Amplifier Basics," International Rectifier, Application Note, 2005. [Online]. Available: https://www.infineon.com/dgdl/an-1071.pdf?fileId=5546d462533600a40153559538eb0ff1 (Accessed 12-04-2022).

[41] J. Cerezo, "Class D Audio Amplifier Performance Relationship to MOSFET Parameters," International Rectifier, Application Note, 2004.

[42] R. Haddad, "Electromagnetic Interference Analysis in Class D Amplifiers," BSc Thesis, University of Twente, 2017.

[43] H. Reurslag, "Electromagnetic Interference Analysis in Class D Amplifiers," BSc Thesis, University of Twente, 2018.

[44] M. Auer and T. Karaca, "Digitally Assisted EMI-Reduction Techniques for Class-D Amplifiers with Digital Control," in *Proc. 2017 11th Int. Work. Electromagn. Compat. Integr. Circuits, EMCCompo 2017*, Jul. 2017, pp. 33–38.

[45] X. Ming, Z. Chen, Z.-k. Zhou, and B. Zhang, "An Advanced Spread Spectrum Architecture Using Pseudorandom Modulation to Improve EMI in Class D Amplifier," *IEEE Trans. Power Electron.*, vol. 26,

no. 2, pp. 638–646, Feb. 2011.

[46] P. Balmelli, J. M. Khoury, E. Viegas, P. Santos, V. Pereira, J. Alderson, and R. Beale, "A low-EMI 3-W audio class-D amplifier compatible with AM/FM radio," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1771–1782, Aug. 2013.

[47] P. Siniscalchi and R. K. Hester, "A 20 W/Channel Class-D Amplifier With Near-Zero Common-Mode Radiated Emissions," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3264–3271, Dec. 2009.

[48] H. Nakagaki, N. Amada, and S. Inoue, "A High-Efficiency Audio Power Amplifier," *J. Audio Eng. Soc*, vol. 31, no. 6, pp. 430–436, Oct. 1983.

[49] R. A. R. van der Zee and E. A. J. M. van Tuijl, "A power-efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, Jul. 1999.

[50] N. S. Jung, J. H. Jeong, and G. H. Cho, "High efficiency and high fidelity analogue/digital switching mixed mode amplifier," *Electron. Lett.*, vol. 34, no. 9, p. 828, Apr. 1998.

[51] L. R. Dalton Vidor, N. Rigo, and J. R. Pinheiro, "DC-DC and DC-AC Series or Parallel Hybrid Converters," in *2018 13th IEEE Int. Conf. Ind. Appl.* IEEE, Nov. 2018, pp. 789–794.

[52] G. R. Walker, "A Class B Switch-Mode Assisted Linear Amplifier," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1278–1285, Nov. 2003.

[53] S. C. Choi, J. W. Lee, W. K. Jin, J. H. So, and S. Kim, "A design of A 10-W single-chip class D audio amplifier with very high efficiency using CMOS technology," *IEEE Trans. Consum. Electron.*, vol. 45, no. 3, pp. 465–473, Jun. 1999.

[54] T. Karaca and B. Deutschmann, "Electromagnetic evaluation of Class-D switching schemes," in *2015 11th Conf. Ph.D. Res. Microelectron. Electron.*, vol. 2, no. 1. IEEE, Jun. 2015, pp. 113–116.

[55] Tong Ge, J. S. Chang, and Wei Shu, "PSRR of Bridge-Tied Load PWM Class D Amps - ISCAS2008," in *IEEE Int. Symp. Circuits Syst.* IEEE, May 2008, pp. 284–287.

[56] M. H. Rashid, *Power Electronics Handbook, Third Edition*. Elsevier, 2011.

[57] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May 1996.

[58] J. Lechevallier, "A Multilevel RF Power Amplifier," Masters Thesis, University of Twente, Nov. 2014.

[59] Xiaoming Yuan and I. Barbi, "Fundamentals of a New Diode Clamping Multilevel Inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 711–718, Jul. 2000.

[60] M. Høyerby, J. K. Jakobsen, J. Midtgaard, T. H. Hansen, N. Nielsen, and H. Hasselby-andersen, "A 2x70W Monolithic Five-Level Class-D Audio Power Amplifier," in *IEEE ISSCC Dig. Tech. Pap.*, Feb. 2016, pp. 1–23.

[61] H. Zhang, S. Karmakar, L. Breems, Q. Sandifort, M. Berkhout, K. Makinwa, and Q. Fan, "A -107 . 8 dB THD + N Low-EMI Multi-Level Class- D Audio Amplifier," in *Proc. VLSI*, 2020, pp. 8–9.

[62] J. H. Lee, J. S. Bang, K. D. Kim, H. D. Gwon, S. H. Park, Y. Huh, K. S. Yoon, J. B. Baek, Y. M. Ju, G. Lee, H. Park, H. M. Bae, and G. H. Cho, "An 8Ω 10W 91%-power-efficiency 0.0023%-THD+N multi-level Class-D audio amplifier with folded PWM," in *IEEE ISSCC Dig. Tech. Pap.*, vol. 60. IEEE, 2017, pp. 88–89.

[63] A. Bendicks and S. Frei, "Broadband Noise Suppression of Stationary Clocked DC/DC Converters by Injecting Synthesized and Synchronized Cancellation Signals," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 1–1, 2019.

[64] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Boston, MA: Springer US, 2001.

[65] S. Chikazumi, *Physics of Ferromagnetism*, 2nd ed., C. D. Graham Jr., Ed. Oxford, NY: Oxford University Press, 2009.

[66] M. D. Score, P. M. Dagli, R. C. Jones, and W. T. Chen, "Modulation scheme for filterless switching amplifiers with reduced EMI," U.S. Patent 6 614 297, Jan. 9, 2003.

[67] R. A. R. van der Zee, "High Efficiency Audio Power Amplifiers," PhD Thesis, University of Twente, 1999.

[68] "Digital audio converter and amplifier controller," Axign B.V., Datasheet, 2016. [Online]. Available: http://www.axign.nl/ (Accessed 18-03-2019).

[69] D. Schinkel, "Digital Audio Converter and Amplifier Controller," U.S. Patent 0 081 621, Mar. 14, 2019.

[70] D. Schinkel and W. Groothedde, "Sigma-Delta Analog-to-Digital Converter," U.S. Patent 0 341 046, Nov. 26, 2015.

[71] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. Piscataway, NJ, USA: IEEE Press, 1997.

[72] C. R. Paul, *Introduction to Electromagnetic Compatibility*. Wiley, 2006.

[73] F. Wang, D. F. Kimball, J. D. Popp, A. H. Yang, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for

802.11g WLAN Applications," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4086–4099, Dec. 2006.

[74] V. Singh, N. Krishnapura, and S. Pavan, "Compensating for quantizer delay in excess of one clock cycle in continuous-time $\Delta\Sigma$ modulators," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 57, no. 9, pp. 676–680, 2010.

[75] Y. Hu, H. Venkatram, N. Maghari, and U. K. Moon, "A Continuous-Time $\Delta\Sigma$ ADC Utilizing Time Information for Two Cycles of Excess Loop Delay Compensation," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 62, no. 11, pp. 1063–1067, 2015.

[76] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 2nd ed., R. J. Baker, Ed. Piscataway, NJ, USA: IEEE Press, 2017.

[77] P. Benabes, M. Keramat, and R. Kielbasa, "A Methodology for designing Continuous-time Sigma-Delta Modulators," in *Proc. Eur. Des. Test Conf. ED TC 97*. IEEE Comput. Soc. Press, 1997, pp. 46–50.

[78] S. Loeda, H. M. Reekie, and B. Mulgrew, "On the Design of High-Performance Wide-band Continuous-Time Sigma-Delta Converters Using Numerical Optimization," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 53, no. 4, pp. 802–810, 2006.

[79] S. Pavan, "Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 55, no. 11, pp. 1119–1123, Nov. 2008.

[80] J. Cherry and W. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 46, no. 4, pp. 376–389, Apr. 1999.

[81] J. Guo and M. E. Magaña, "Compensation method of the excess loop delay in continuous-time delta-sigma analog-to-digital converters based on model matching approach," *IET Circuits, Devices Syst.*, vol. 10, no. 1, pp. 29–36, Jan. 2016.

[82] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli, "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma-Delta Modulators," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 55, no. 11, pp. 3480–3487, 2008.

[83] K. El-Sankary, H. Alamdari, and E. El-Masry, "An Adaptive ELD Compensation Technique Using a Predictive Comparator," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 56, no. 8, pp. 619–623, Aug. 2009.

[84] P. Fontaine, A. Mohieldin, and A. Bellaouar, "A Low-Noise Low-Voltage CT $\Delta\Sigma$ Modulator with Digital Compensation of Excess Loop Delay," in *IEEE ISSCC Dig. Tech. Pap.* IEEE, 2005, pp. 498–500.

[85] A. Yahia, P. Benabes, and R. Kielbasa, "Bandpass Delta-Sigma Modulators Dynthesis with High Loop Delay," in *IEEE Int. Symp. Circuits Syst.*, vol. 1, 2001, pp. 344–347.

[86] F. Jiang, C. Chen, Y. Xiao, J. Xu, and J. Ren, "Beyond-one-cycle loop delay CT $\Delta\Sigma$ modulators with proper rational NTF synthesis and time-interleaved quantizers," in *Midwest Symp. Circuits Syst.*, vol. 1. IEEE, 2013, pp. 558–561.

[87] R. Schreier, "Delta Sigma Toolbox," MATLAB, 2020. [Online]. Available: https://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox (Accessed 10-09-2020).

List of publications

Peer-reviewed

[CEL:1] H. S. Bindra, C. E. Lokin, A. J. Annema, and B. Nauta, "A 30fJ/comparison Dynamic Bias Comparator," in *Proc. ESSCIRC*, 2017, pp. 71–74.

[CEL:2] H. S. Bindra, C. E. Lokin, D. Schinkel, A. J. Annema, and B. Nauta, "A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1902–1912, 2018.

[CEL:3] C. E. Lokin, R. A. R. van der Zee, D. Schinkel, and B. Nauta, "EMI Reduction in Class-D Amplifiers by Actively Reducing PWM Ripple," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 67, no. 3, pp. 765–773, Mar. 2020.

[CEL:4] C. E. Lokin, D. Schinkel, R. A. R. Van Der Zee, and B. Nauta, "Compensating Processing Delay in Excess of One Clock Cycle in Noise Shaping Loops Without Altering the Filter Topology," *IEEE Access*, vol. 9, pp. 108 101–108 111, 2021.

Other

[CEL:5] C. Arocho, "UT and Axign put the brakes on radio interference," *Bits&Chips*, May 2020. [Online]. Available: https://bits-chips.nl/artikel/ut-and-axign-put-the-brakes-on-radio-interference/ (Accessed 12-04-2022).

[CEL:6] C. E. Lokin, R. A. R. van der Zee, D. Schinkel, and B. Nauta, "EMI Reduction in Class-D Amplifiers by Actively Reducing PWM Ripple," in *ProRISC*, Eindhoven, Netherlands, 2021.

Acknowledgements

I would like to use this space to express my gratitude and thanks to everyone who has helped me in one way or another during this seven-year journey towards the defense of my thesis. I've got to know so many people during my time at the University of Twente that it is nigh impossible to mention everyone.

First, I would like to thank Ronan, Bram and Daniël for their supervision during my time at the integrated circuit design group. Ronan, I always felt welcome to have a discussion whenever I got stuck or needed your opinion on something. No matter the occasion, your positive mindset and practical approach during our meeting was really motivating for me. Thanks for reviewing the numerous versions of my manuscripts and providing helpful advice and playing 'devil's advocate' to keep me sharp. Bram, thanks for the interesting discussions, out-of-the-box ideas and your critical comments on my manuscripts. I could always have a good laugh over your 'Bramatic' jokes, as we called them in our office. They were so bad, that they were good! Daniël, while formally not being my supervisor, you have contributed a lot during my research and hence appeared on the author list of my papers. Your help with the implementation on the Axign controller has been invaluable. I am happy that we will continue to cooperate on Class-D amplifiers at Axign.

My thanks also go out to our scientific staff Anne-Johan, Eric, Mark, Sander and Frank for the insightful discussions around the coffee machine and their thought provoking questions during my chiptalks.

Next, thanks to our supporting staff members Henk, Gerard, Arnoud and Gerdien. Henk, thanks for helping me to acquire the APX555 audio analyzer for doing my measurements. It has been of great use! After your retirement, your tasks were taken over by Arnoud. I would like to thank him for his assistance on doing a measurement for me during the coronavirus lockdown while I wasn't allowed on the premises. Gerard, we have had a fair share of conversations about computer hardware, gaming and stuff happening around the office. Thanks for assisting me with ICT stuff whenever required and for providing me with the CAD tools. I'm saddened that he is no longer with us, but he will always be in our hearts. Thanks Gerdien for scheduling my meetings with Bram in his ever so full calendar and for organizing the many social events for the ICD group.

Alexander and Theo, thanks for being my paranymphs. It is nice to

have two close friends by my side to support me. Theo, we shared a lot of time training at Euros, the rowing club, resulting in a lot of victories at regattas and other valuable memories. It was good to have your company during the lockdown when social events were reduced to a minimum. Alexander, we've laughed a lot about the many controversial jokes during our time in the office. I fondly remember the various board game evenings and bike rides of which there are many still to come.

During my PhD term I have shared the CR2728 room with several people. Thanks Dirk-Jan, Hugo, Johan, Yuan-Ching, Ines, Ali, Bart, Labrinus, Alexander, Thomas, Erwin, Anoop, Andreas and Nimit for the good times in our room. Also thanks to my other ICD PhD colleagues, Joeri, Maikel, Harijot, Joep, Vishal, Vijay, Dawei, Sajad, Zhiliang, Claudia, Anton, Roel and Maryam. I've enjoyed the conversations in the coffee corner, the occasional lunch walks and movie nights. I'd like to thank some of you in special. Harijot, for giving me the opportunity to assist in the tape-out and measurement of the dynamic bias comparator which resulted in 2 papers. Joep, for occasionally cycling together after work and our numerous cycling holidays.

Every nine months I would meet with the user committee, a group of experts in the fields of circuit design and audio amplification. I would like to thank them for their valuable comments and advice on the direction of my research. One of the members, Ed van Tuijl has sadly passed away during my term at the University. I will always remember him as a brilliant researcher with the capability to think out-of-the-box and am happy to have worked with him, both during my PhD and my internship at Teledyne Dalsa.

I had the privilege to supervise several BSc and MSc projects, thanks Harm, Eva, Jeroen, Lucas, Pepijn, Ragheed, Olaf, Rick and Fabian for the interesting discussions and outcomes. I'm happy that the latter three are also colleagues at Axign and look forward to keep working with you.

Rowing at Euros has had a big influence during my PhD. It helped me a lot to free my mind with a training session in the boat after work and I have made friends for life at this amazing club. I would like to thank all my coaches and crew members for the many training hours and victories we shared. It would be impossible to name everyone here, thanks to all the crews Licht'12, MGL'13, MGL'14, Ojee'16, MGL'17, OJL'18 and 'de Blikkentaxi'. Special thanks to Johan for making our training programs throughout all these years.

I've also participated in some committees of which I would like to specially mention the DJCie. Together we've hosted many parties spinning the records behind the decks.

Thanks to Klein Verzet, the cycling association, for providing a nice atmosphere to get hooked on cycling after my retirement from rowing. I've enjoyed the many training sessions, competitions and holidays both on the road and off-road. Furthermore, I'd like to thank 'nochill' for the

numerous intense rides with a special mention to Bryan, Seth and Fausto for our weekly 100k+ rides, usually including the Holterberg.

I've had the pleasure to have a lot of supporting friends around me. Thanks to Theo, Bryan, Lara and Melanie for our occasional board game nights. Elise, I've enjoyed our many movie nights and lunch walks and am happy to also have you as a colleague at Axign. Judith, thanks for all your motivational words whilst finishing my paper, helping me to think more critical and for great times together. Thanks Jasmina for the conversations and workout plans during the first lockdown. Seth, thanks for your down-to-earth reasoning and helping me to see matters from different perspectives and providing a listening ear.

I would like to thank Axign to allow me to finish some of the thesis work on company time and not having to do all of it in my vacations and spare time. Also thanks to my colleagues for their encouragement during the last year of writing the thesis.

Finally I would like to thank my parents, Janny and Jan Willem, and my sisters, Maud and Lieke for their support throughout this journey in academia.

About the Author

Chris E. Lokin was born in Hengelo, Overijssel, the Netherlands in 1992. He received the B.Sc. and M.Sc. *(cum laude)* in electrical engineering from the University of Twente, Enschede, the Netherlands in 2013 and 2015, respectively.

From 2015 to 2022, he was a research assistant at the Integrated Circuit Design group resulting in this dissertation. In 2020, he joined Axign, Enschede, the Netherlands, where he is a system architect working on Class-D audio amplifiers.

Chris has authored two technical journal papers and is a co-author of one other journal paper. His current research interests include mixed-signal systems, control systems for applications in Class-D power amplifiers and low-level DSP algorithms.