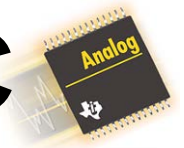
State of Art Techniques in Digital to Analog Converter Design

Dr. Rahmi Hezar
Senior Member of Technical Staff
Kilby Labs, Texas Instruments

What to Expect from a DAC



Short answer: Everything ☺

Reality: Depends on the application with different weighting

- Audio Applications:
  a. Linearity is the king: Improves dynamic range, reduces distortion, reduces requirements on the amplifier, just better listening experience.
  b. Power Consumption is somewhat critical: On phones and tablets DAC is not the main source of power consumption
  c. Out of band noise: Some what Important needs large capacitors to remove
- RF Applications:
  - Absolute linearity is relaxed compared to audio but high clock speeds make it challenging.
  - Power now is the king: RF circuits drain the battery very quickly and heat the chip, create reliability problems.
  - Out of band noise is more critical compared to audio, requires expensive, very large, high-Q band-pass filters to meet tight RF masks requirements.
- **Other:** DACs are the bottleneck in ADC design. A Sigma Delta ADC is as good as its feedback DAC

What to Expect from this Presentation

Short answer: Everything about DACs ☺

Reality: Smart Architectures and Signal Processing Methods for DACs

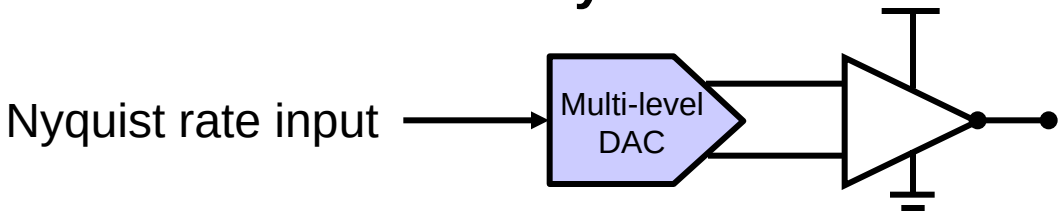
- Analog design side of DACs is very simple and well developed
  a. Current steering DACs: Summing current sources via switches
  b. Voltage DACs: Summing voltages via switching capacitors
- We want them to be
  a. Infinitely fast
  b. Absolutely perfect (no change from the original value, no variation)
  c. Add no distortion, no noise
- **Fact:** they are imperfect and never fast enough ☺
- **Question:** how do we use them so that their weaknesses are not exposed and strength are shown?
- **Answer:** lies in the rest of this presentation

Smart Architecture Design:

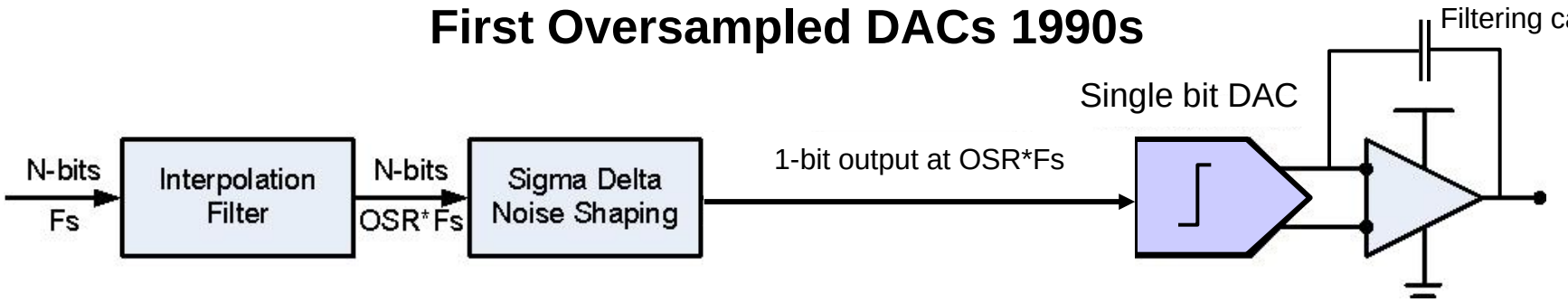
Cascaded Modulator For Oversampled Digital-to-Analog Converters

A Brief Look at the Audio DAC's Past

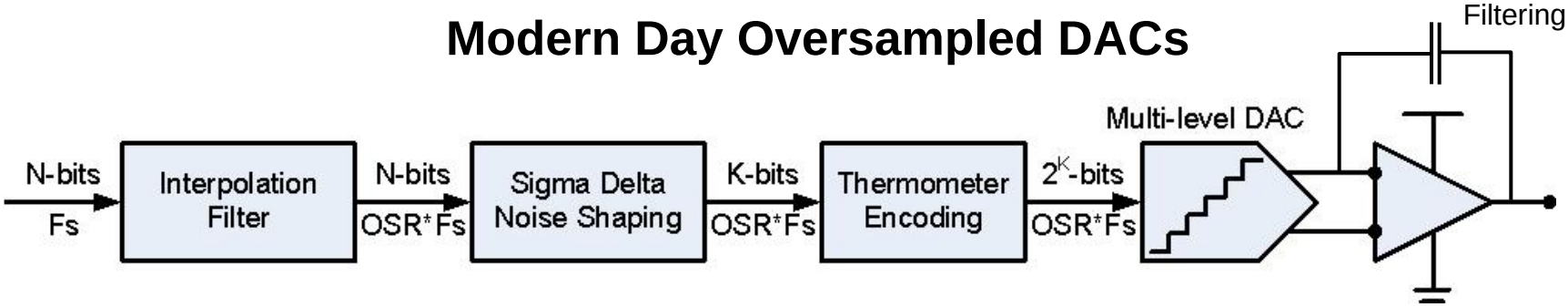
From CD Childhood days 1980s



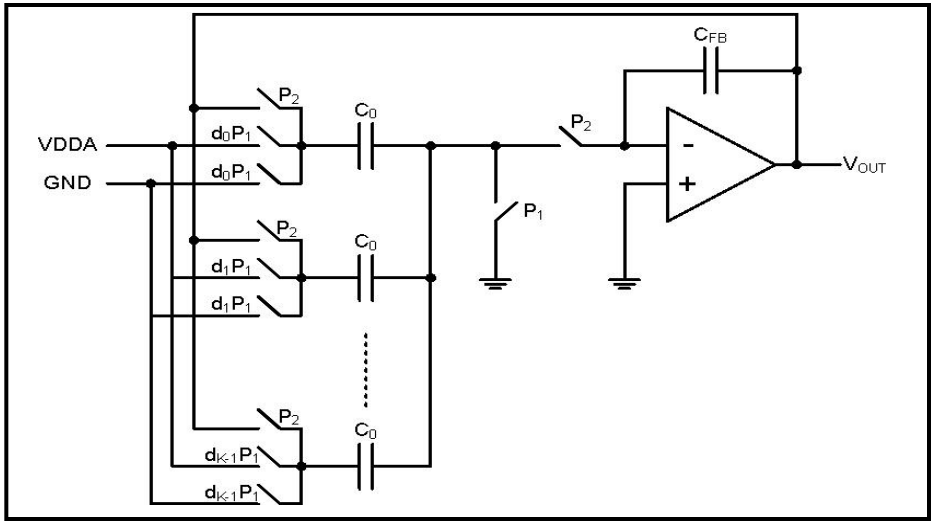
First Oversampled DACs 1990s



Modern Day Oversampled DACs



Switch-Cap & Current Steering

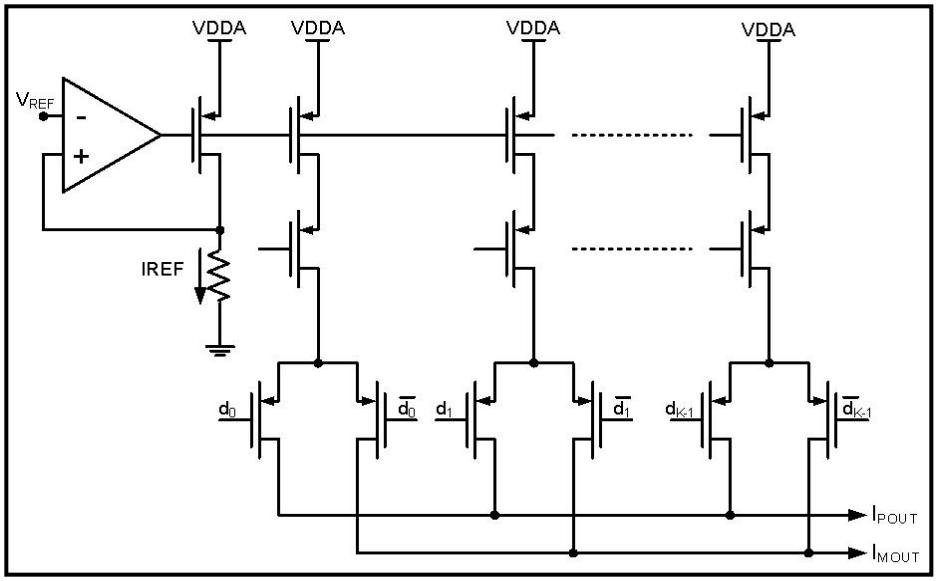


Pros-

- ✓ Less sensitive to Phase-noise
- ✓Less sensitive to ISI if settling is fast
- ✓ Allows for a simple single ended voltage output circuit

Cons-

- × Sensitive to static element mismatch
- × Very power/area hungry so no of DAC levels is limited
- × Out of band noise is high needs very good filtering
- × Does not scale with the process
- × very sensitive to high frequency noise



Pros-

- ✓ Allows for very small area implementation especially in CMOS processes.
- ✓ Can be clocked at much faster rates
- ✓ Less prone to aliasing due to CT nature
- ✓ Scales very well with the process
- ✓ Overall very low power circuit, total current is about I_{REF}

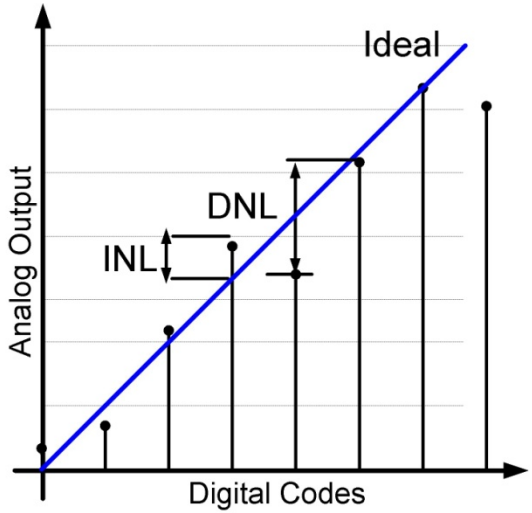
Cons-

- × Sensitive to static element mismatch
- × More sensitive to jitter if OBN is high
- × Sensitive to ISI

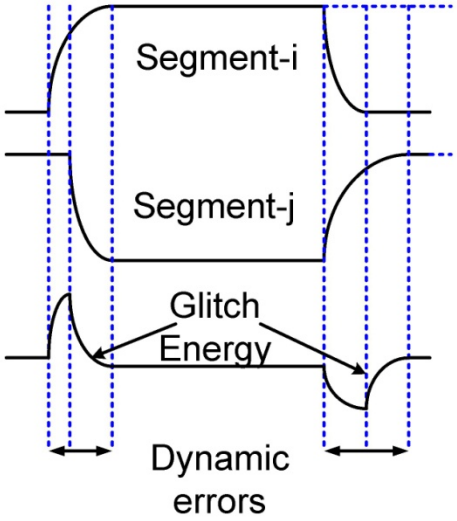
Dominant Error Sources in DACs

- DAC Element Mismatch
- DAC Asymmetrical Switching (ISI)
- Clock Jitter & Amplifier Nonlinearity

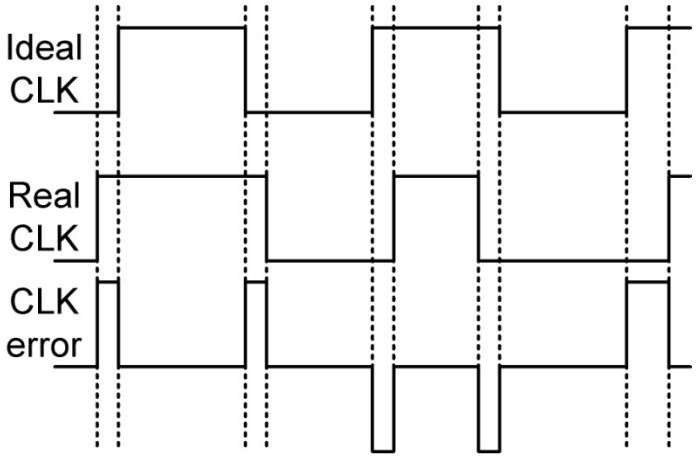
$$DACe_{[n]} = \underbrace{\sum_{i=1}^{N} \varepsilon_i S_{i[n]}}_{\text{Static Element Mismatch Errors}} \underbrace{- \sum_{i=1}^{N} \delta_{r,i} \left[S_{i[n]} \cdot \left(1 - S_{i[n-1]}\right) \right]}_{\text{Dynamic Rise Time Errors}} + \underbrace{\sum_{i=1}^{N} \delta_{f,i} \left[\left(1 - S_{i[n]}\right) \cdot S_{i[n-1]} \right]}_{\text{Dynamic Fall Time Errors}}$$



Element Mismatch

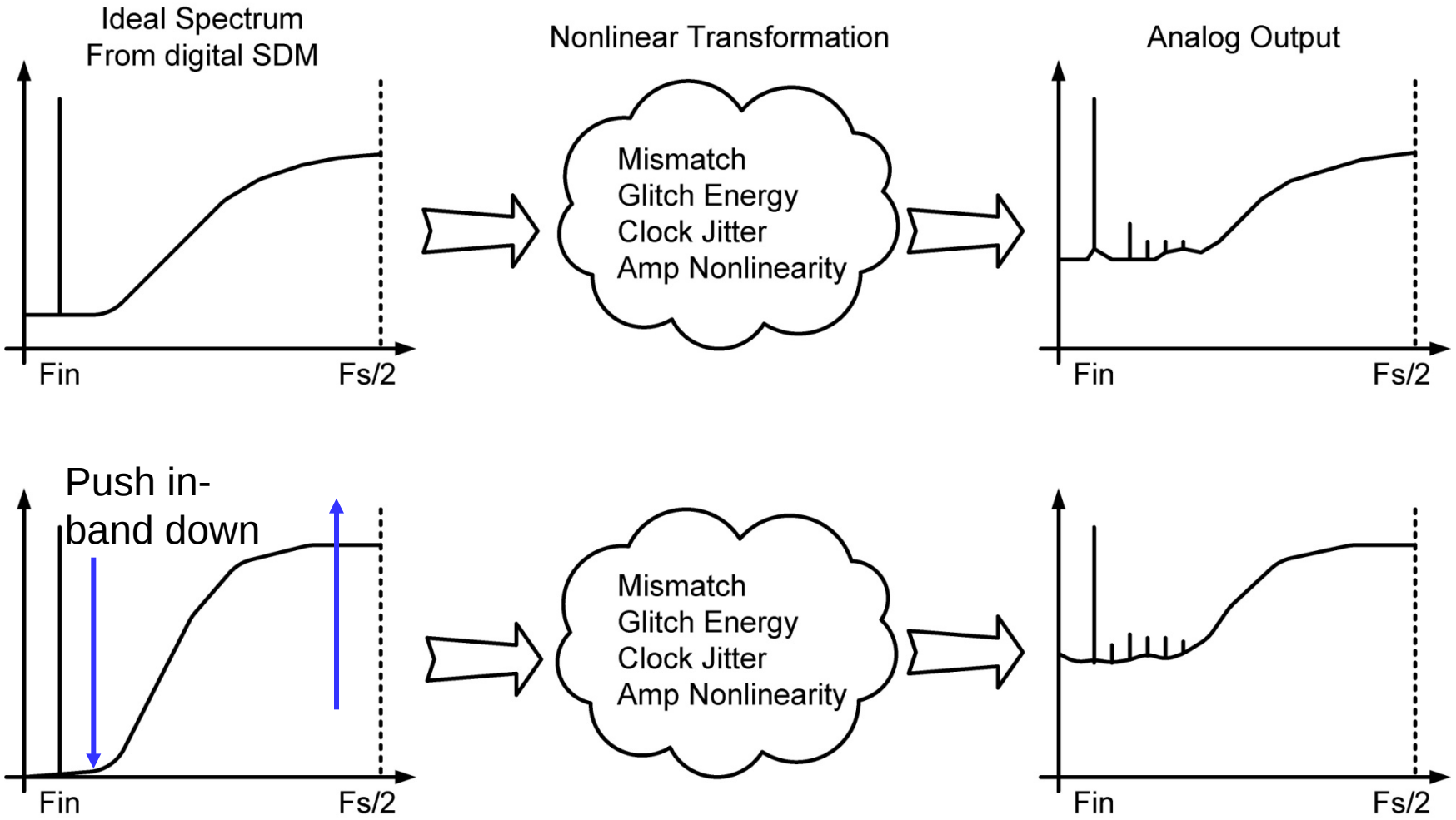


Asymmetrical Switching



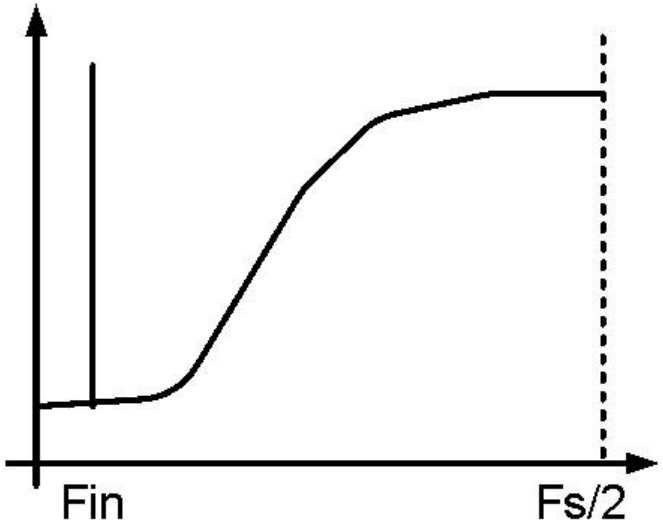
Clock Jitter

Impact of DAC Non-linearity



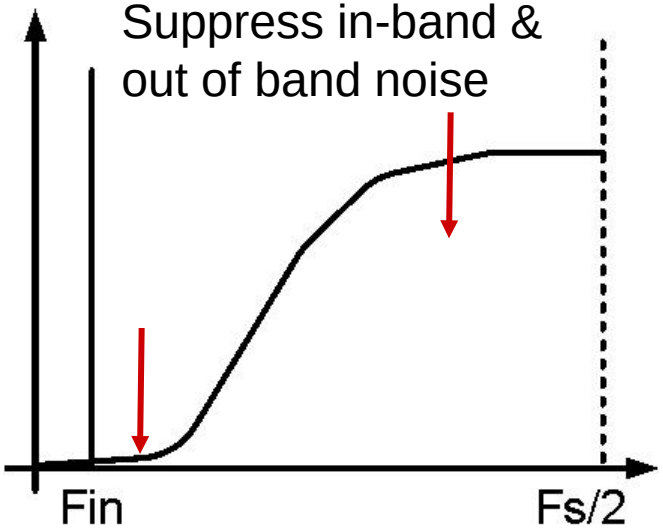
➢ We need to reduce out of band noise

Single-Bit and Multi-bit Trade-off



Single Bit DAC:

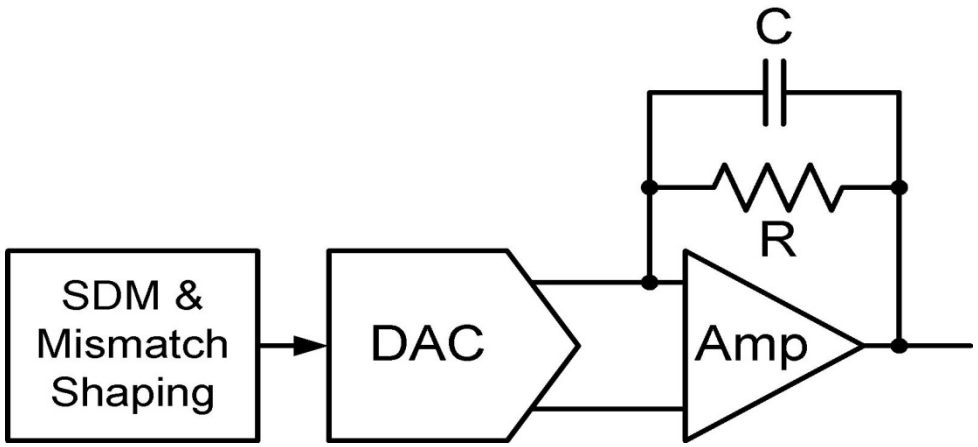
- More out of band noise
- Faster clocking to get the in-band low
- Element mismatch does not matter
- BUT, worst case scenario for ISI, there is no way to correct for it



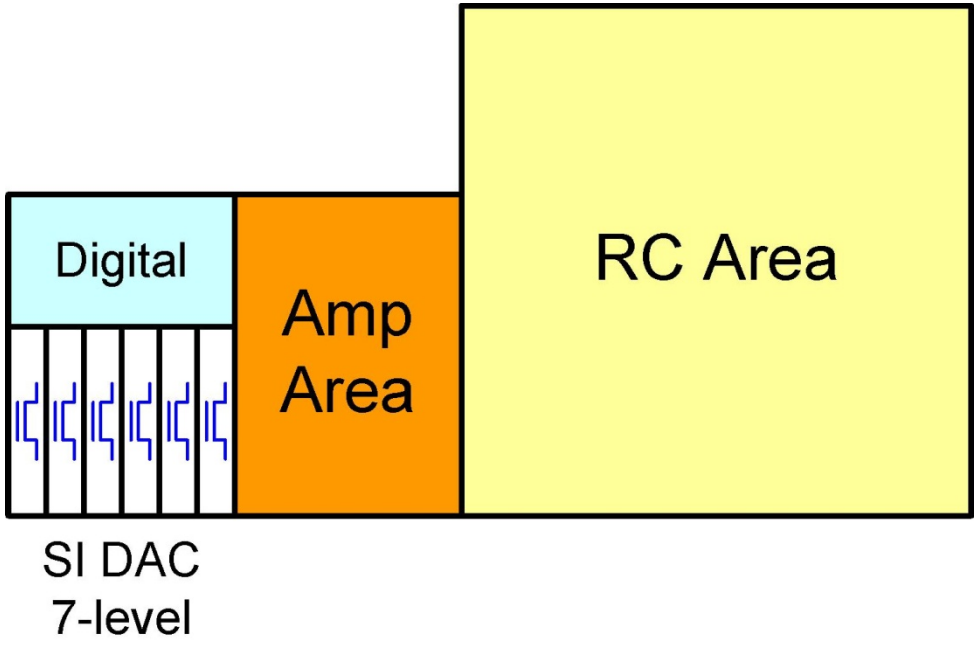
Multi Bit DAC:

- Reduce both Out of Band Noise and Inband
- Slower clock rates relax the ISI errors
- Multi-level glitch errors have less impact
- BUT, worst case scenario for mismatch
- **Good news:** There are algorithms to shape element mismatch

Cost of Filtering OBN

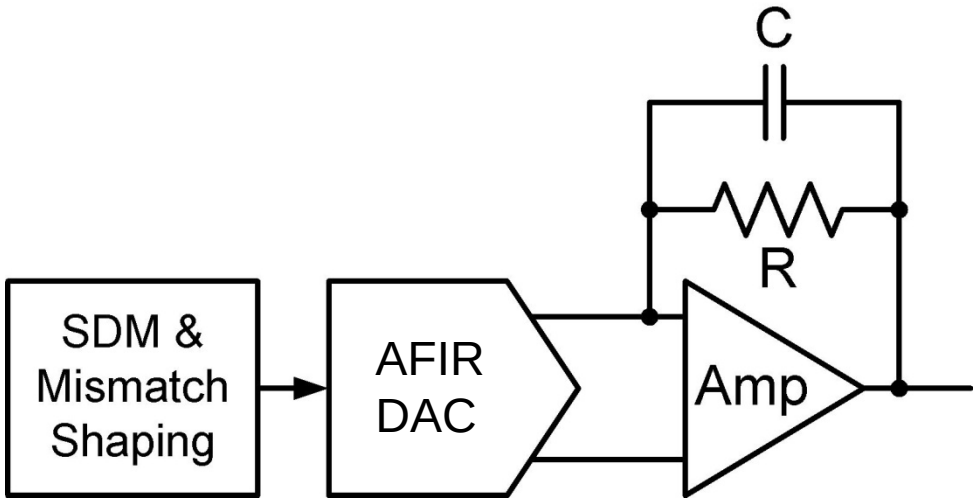


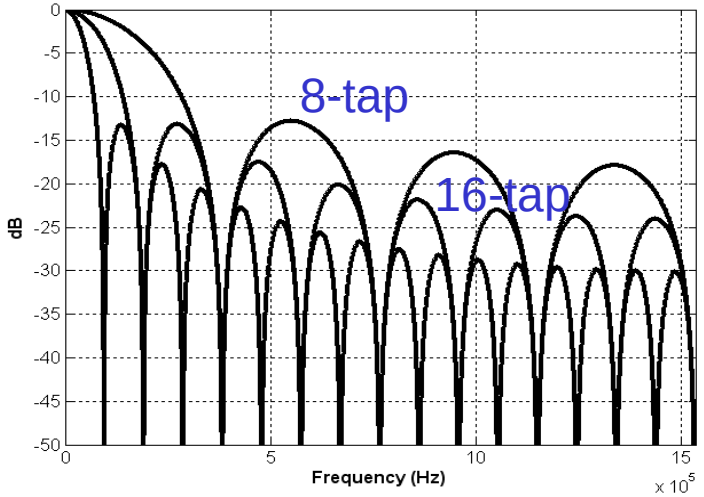
Classical RC Filtering of out of band noise

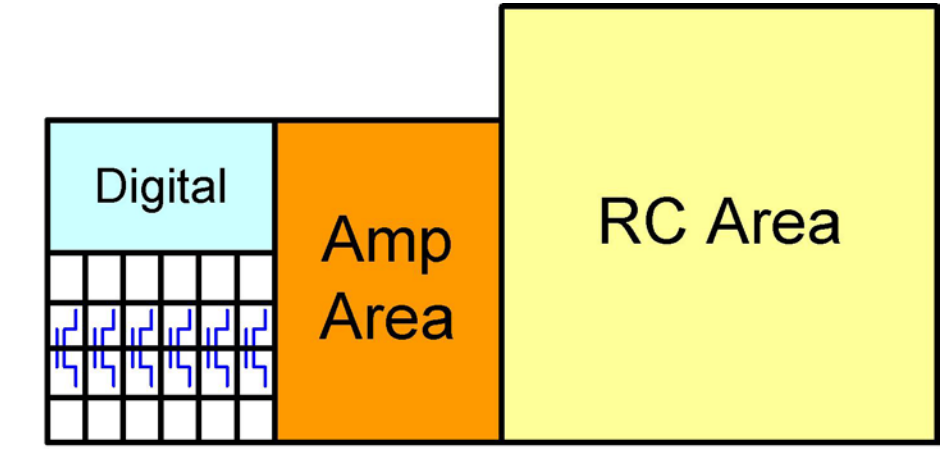


Area usage is dominated by RC filtering

Try Analog-FIR Filtering







SI DAC 7-level
+ 4-tap AFIR

Unity FIR does not provide enough suppression.

Does AFIR Really Reduce OBN

M : DAC elements

N : Number of AFIR Filter taps

AFIR DAC has $\left(\frac{M}{N}+1\right)$ q - levels

$$AFIR(f)=\frac{Sin(\pi\cdot f\cdot N/F_s)}{Sin(\pi\cdot f/F_s)}$$

Assume 2nd order NTF for ΣΔM

Lets formulize the OBN energy for DAC with AFIR Configuration

$$OBN_A=\int_{F_{BW}}^{F_s/2} AFIR^2(f)\cdot\left|2\cdot Sin\left(\frac{\pi\cdot f}{F_s\cdot N}\right)\right|^2\cdot\frac{1}{12F_s}\cdot\left(\frac{N}{M+N}\right)^2\cdot df$$

$$OBN_A=\frac{1}{3F_s}\cdot\left(\frac{N}{M+N}\right)^2\cdot\int_{F_{BW}}^{F_s/2}\left|Sin\left(\frac{\pi\cdot f}{F_s\cdot N}\right)\right|^2 df$$

Now lets look at the 2 extreme cases: Remember we have only L>>1 DAC segments to use

1. Spend all the segments on FIR filtering and use only 1-bit DAC

$M=1$, $N=L$

$$OBN_A=\frac{1}{3F_s}\cdot\left(\frac{L}{L+1}\right)^2\cdot\int_{F_{BW}}^{F_s/2}\left|Sin\left(\frac{\pi\cdot f}{F_s\cdot L}\right)\right|^2 df\approx\frac{1}{3F_s}\cdot\left(\frac{1}{L}\right)^2\cdot\left(\frac{\pi\cdot f}{F_s}\right)^2\cdot\left(\frac{F_s}{2}-F_{BW}\right)^2$$

2. Spend all the segments on the DAC and don't do AFIR

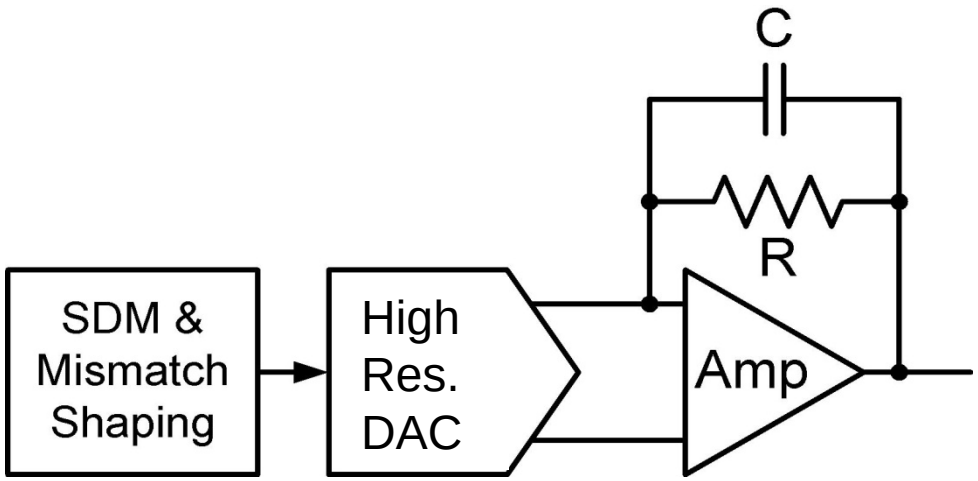
$M=L$, $N=1$

$$OBN_A=\frac{1}{3F_s}\cdot\left(\frac{1}{L+1}\right)^2\cdot\int_{F_{BW}}^{F_s/2}\left|Sin\left(\frac{\pi\cdot f}{F_s\cdot 1}\right)\right|^2 df\approx\frac{1}{3F_s}\cdot\left(\frac{1}{L}\right)^2\cdot\left(\frac{\pi\cdot f}{F_s}\right)^2\cdot\left(\frac{F_s}{2}-F_{BW}\right)^2$$

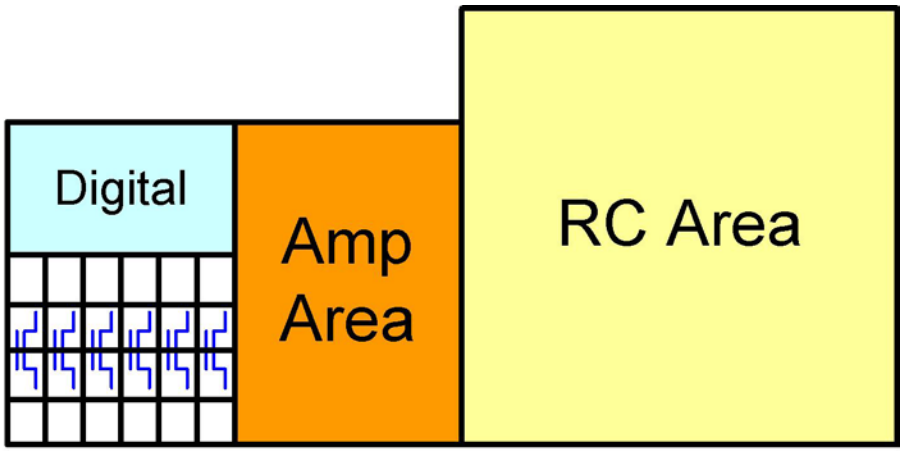
Same OBN !!!

Clearly, with 1st order approximation, **there is no change in OBN in either cases.**

Try Adding More Quantizer Levels



Increase quantizer resolution in the modulator



Similar type of reduction to AFIR plus the digital complexity

25-Level DAC ⟶ Element Matching is more difficult

Segmented DAC in ISSCC 2008

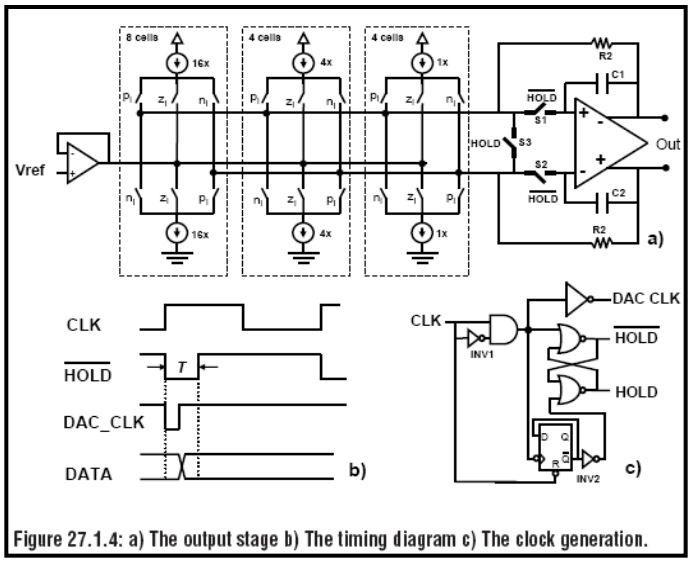
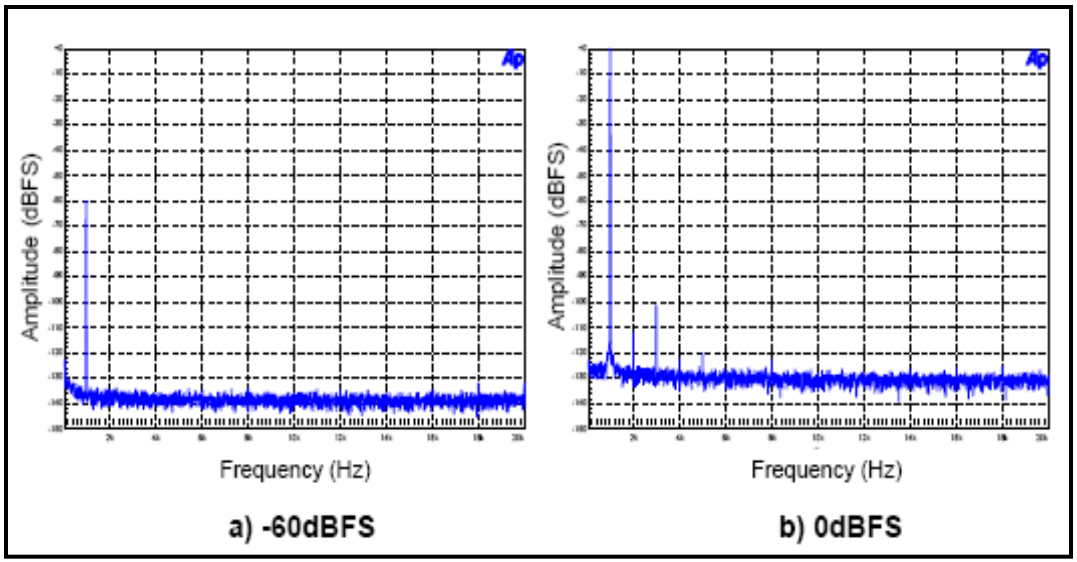


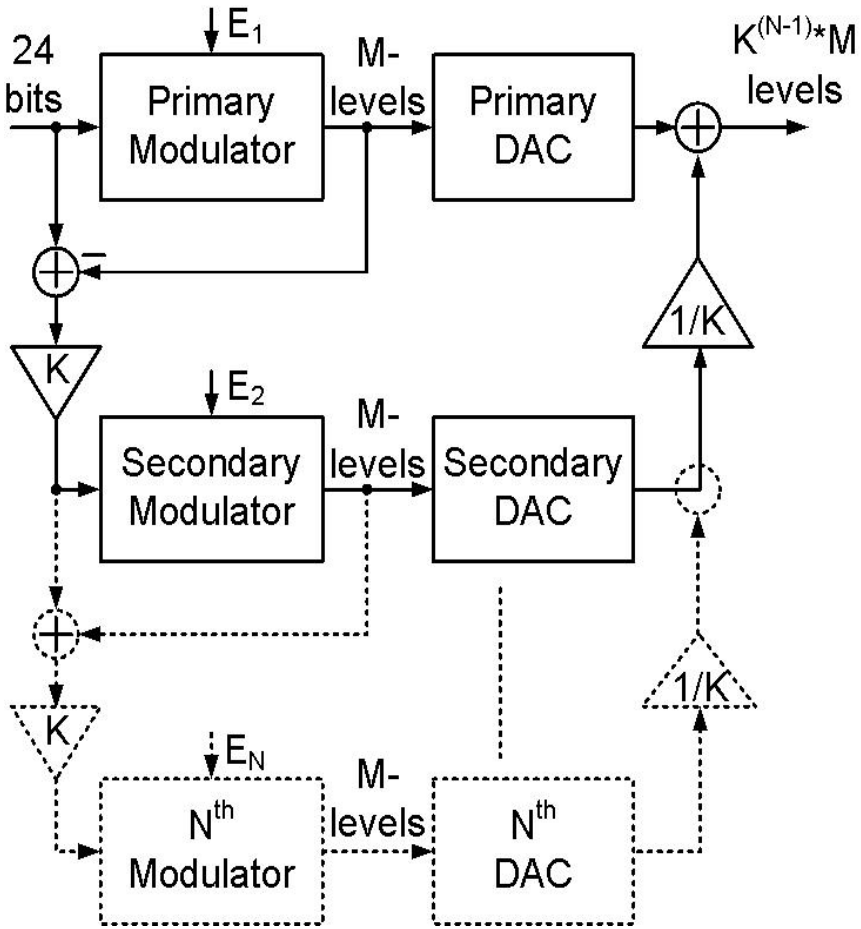
Figure 27.1.4: a) The output stage b) The timing diagram c) The clock generation.



Implemented in 0.18CMOS, 0.4mW digital power and 0.7mW analog power:

- ✓ **Out of band noise:** Segmentation (non-uniform, 16:1 weighted) results in high no of quantization levels and smooth signal. Effective no of levels is 256 using only 16 cells.
- ✓ **Static mismatch:** Shuffling algorithm better than direct first order shaping and cheap in 0.18u CMOS
- ✓ **Dynamic mismatch:** ISI free switching at the I/V converter. This is the bottleneck of this design
  - ❖ It requires I/V converter and headphone driver separately
  - ❖ HOLD clock mechanism makes increases sensitivity to phase noise again
- ✓ **1/f noise:** Segment 1/f is reduced by shuffling algorithm. Does not mention reference 1/f
- ✓ **Thermal noise:** Shuffling algorithm creates 3-level logic and DAC segments have 3-switches unused segments dump noise to the ground, therefore thermal noise scales with the signal

Cascaded Modulator Architecture Presented in ISSCC 2010



For a 2-level cascade

$$Y(z) = X(z) + \frac{1}{K} \cdot NTF(z) \cdot E_2(z)$$

Resolution is boosted by K.

For N-level cascades

$$Y(z) = X(z) + \frac{1}{K^{N-1}} \cdot NTF(z) \cdot E_N(z)$$

Impact of Mismatch on Resolution

- Ideal output for a 2-level cascade

$$Y(z) = X(z) + \frac{1}{K} \cdot NTF(z) \cdot E_2(z)$$

- If digital Kd and analog Ka do not match

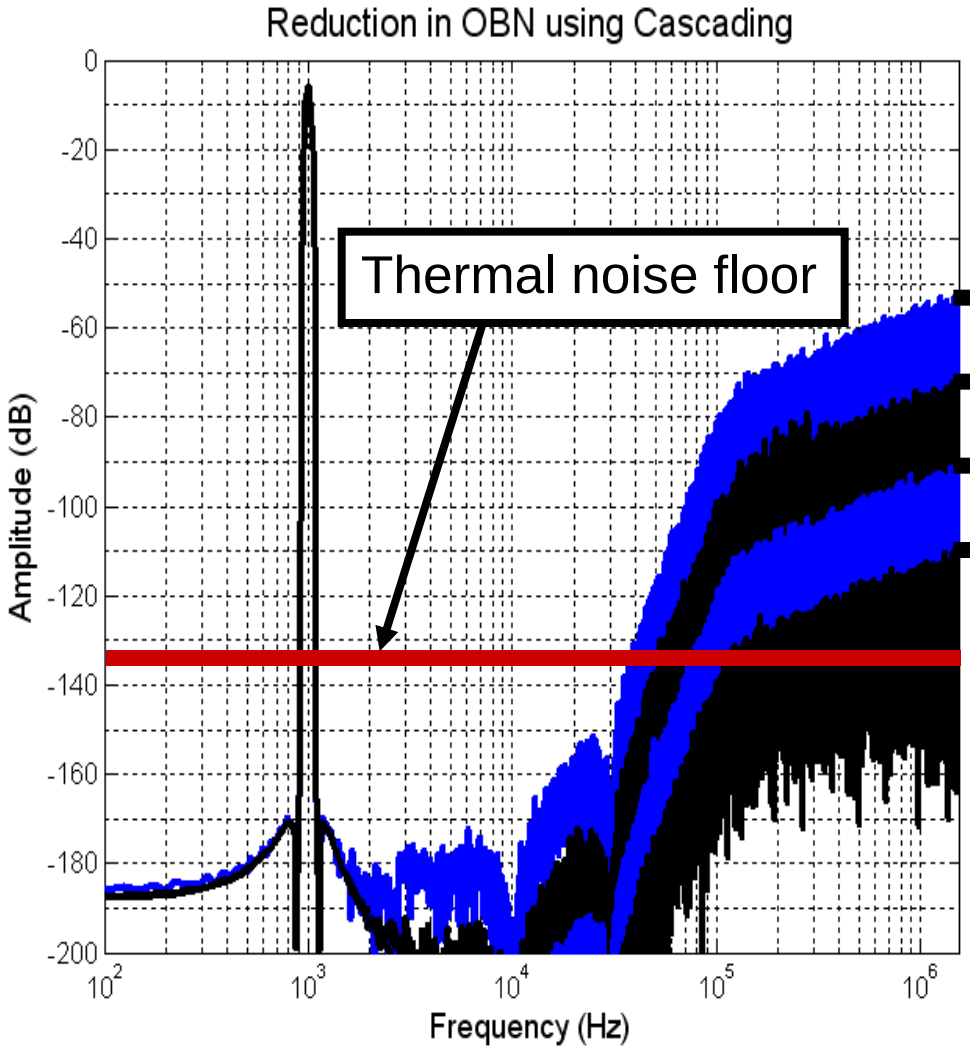
$$Y(z) = X(z) + \left(1 - \frac{K_d}{K_a}\right) \cdot NTF(z) \cdot E_1(z) + \frac{1}{K_a} \cdot NTF(z) \cdot E_2(z)$$

- Mismatch between Kd and Ka is shaped inherently
- Mismatches between the DACs are shaped similarly

This is not MASH

- **Purpose of MASH is to get higher order from simple 2nd and 1st order modulators.**
  - Same can be achieved with higher order single loop
  - The purpose of Cascade is to get finer quantization from coarse quantized modulators.
- **MASH sub-modulators are summed in digital domain always**
  - Cascaded modulators are summed in analog domain.
- **MASH is very sensitive to analog/digital mismatch**
  - Cascaded architecture has built in shaping

Reducing OBN Cost Effectively

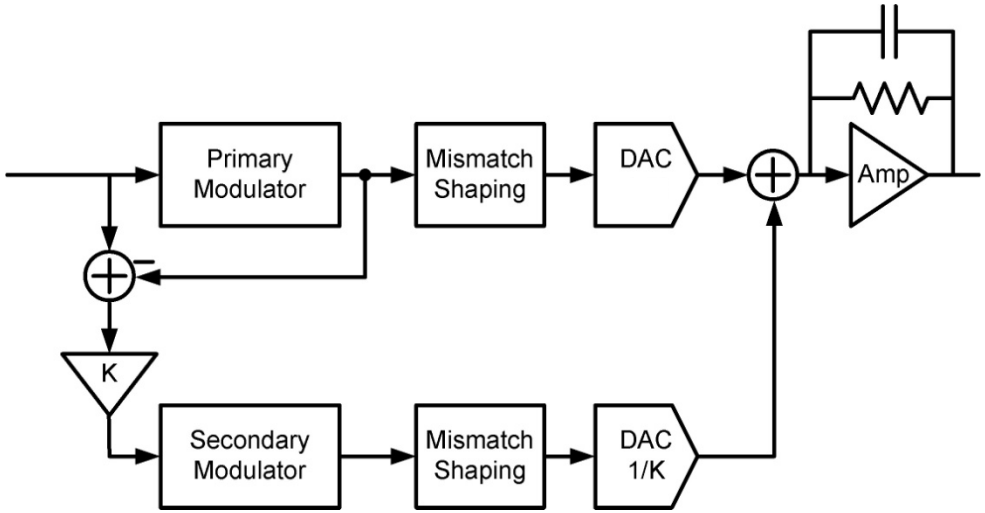


- Primary Modulator Only
- 2-level Cascading
- 3-level Cascading
- 4-level Cascading

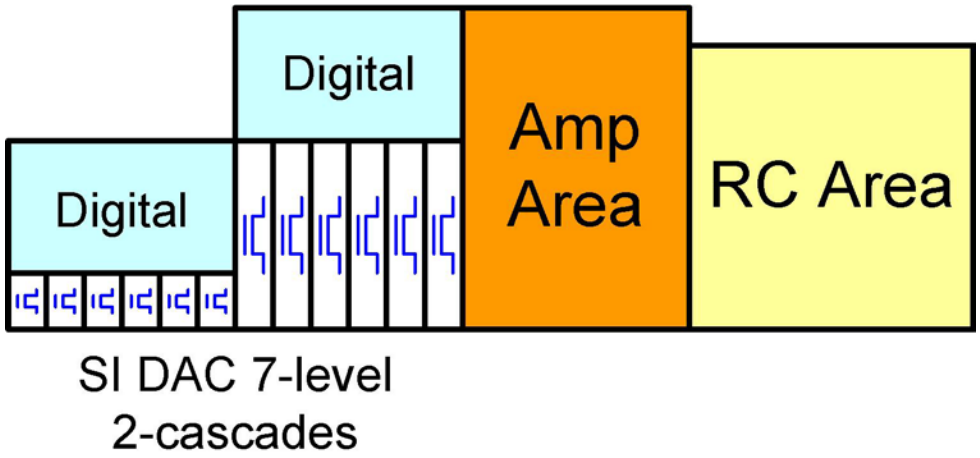
Impact on OBN is huge:

By cascading smaller and smaller DACs, out of band noise can be pushed down to the thermal floor.

Impact of Cascading on Area



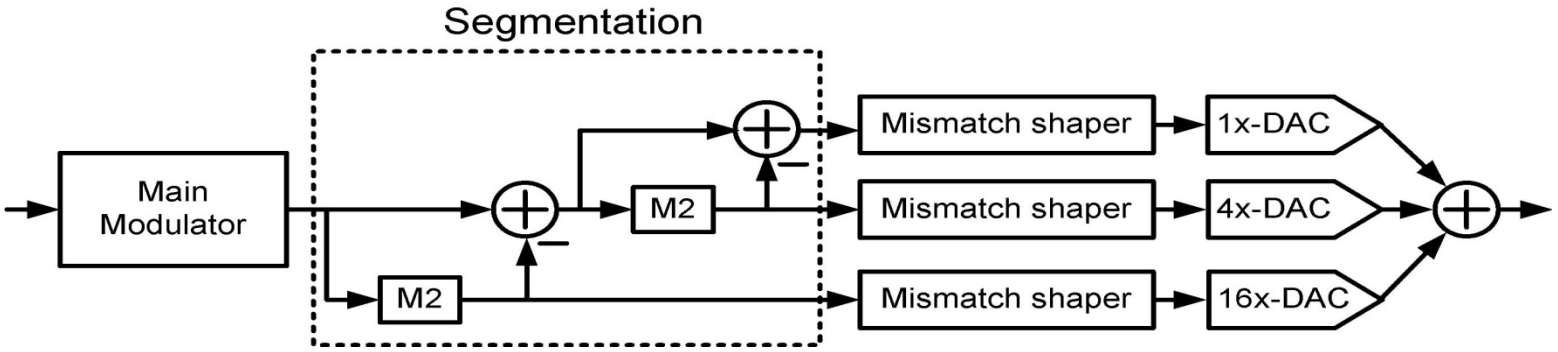
Cascaded architecture with secondary DAC



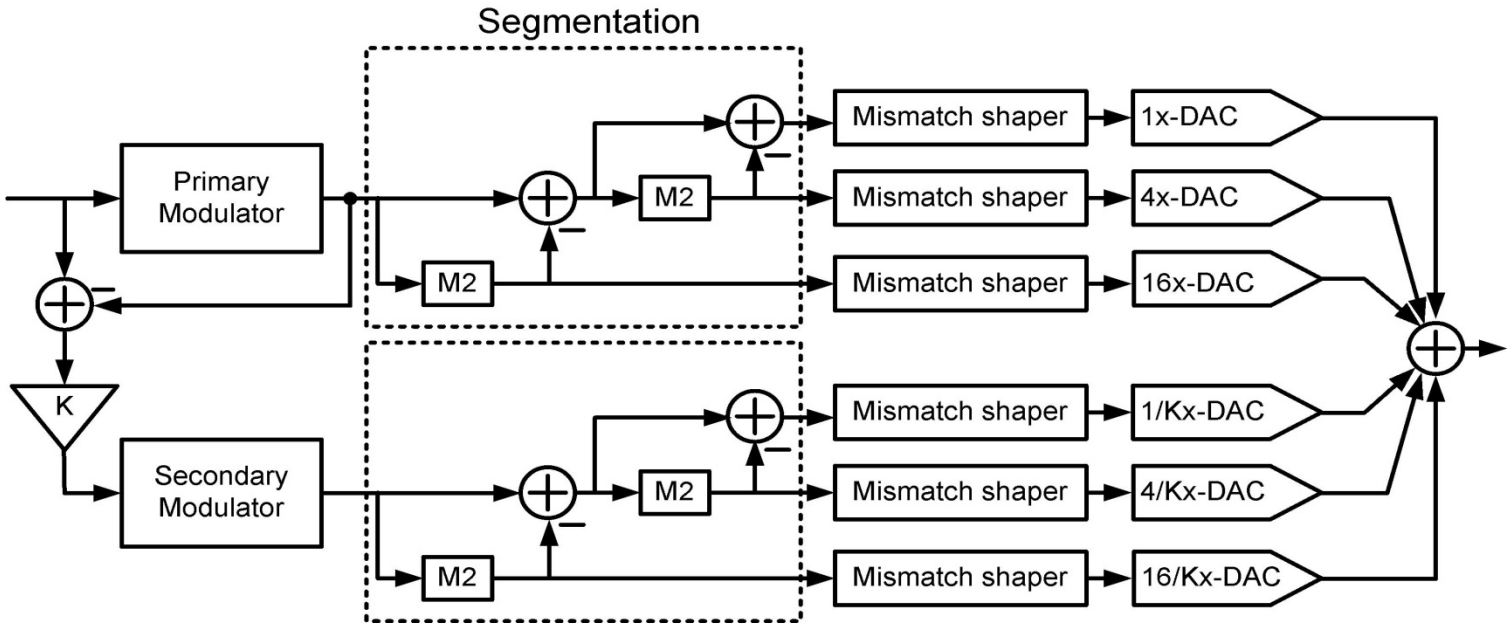
SI DAC 7-level
2-cascades

Resolution is increased significantly with a small DAC

Comparing to Segmented DACs



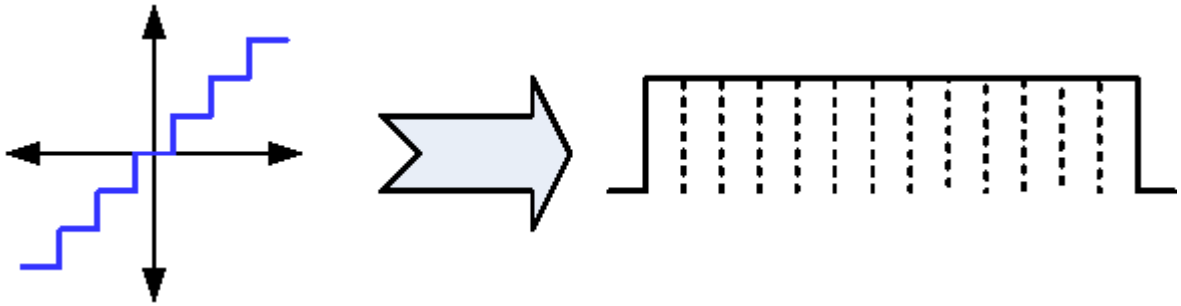
Segmentation is used for high resolution modulators



Segmentation and Cascading are not exclusive

What is Pulse Width Modulation?

PWM: Convert amplitude quantized signals to time representation by changing the pulse width of a carrier signal.

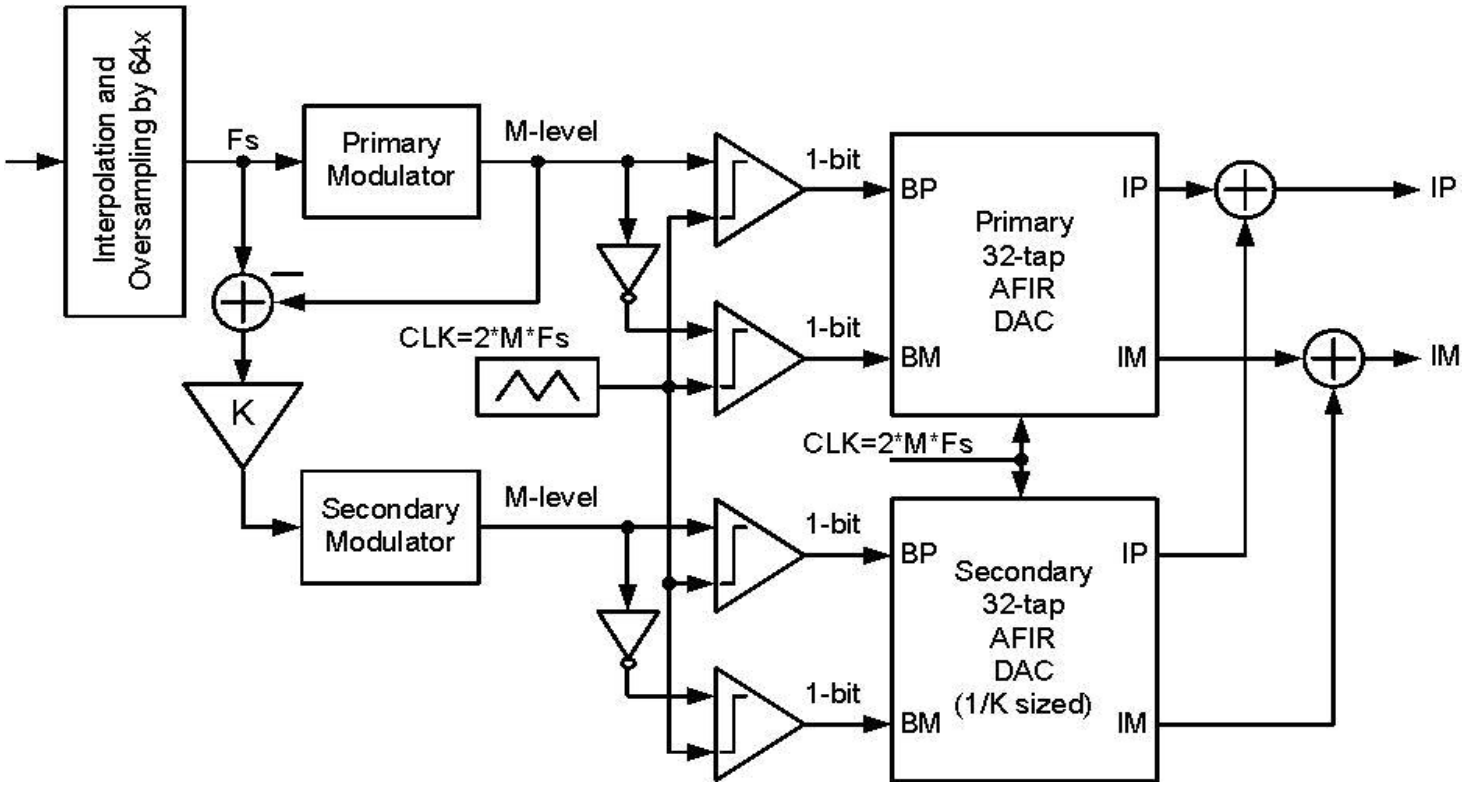


What is driving this?

I. DACs and ADCs are now all integrated with the massive digital cores in CMOS
II. Shrinking CMOS technology is leaving no head room to implement reliable multi level amplitude quantization
III. However, CMOS speeds are always going up
IV. So Time Quantization is getting cheaper and Amp Quantization is getting expensive

Adapt or die ☹

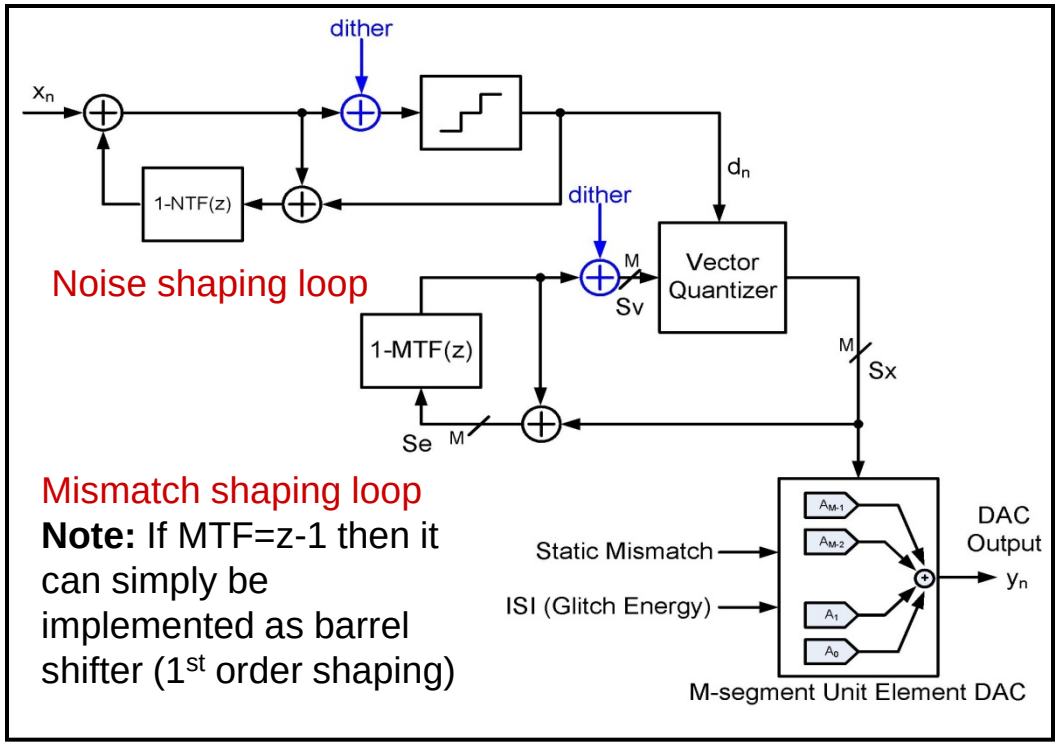
Using PWM and AFIR in DAC

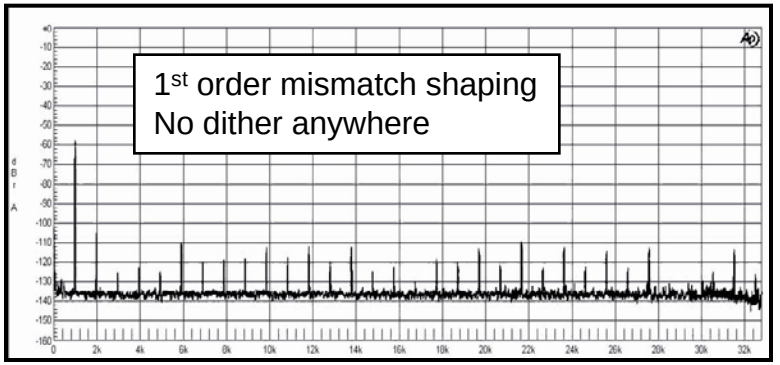


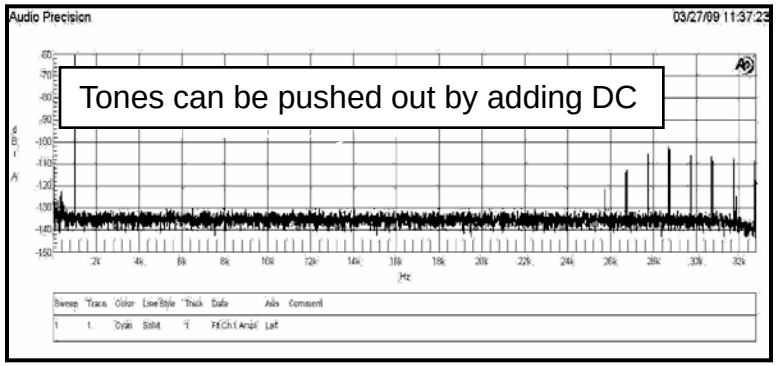
PWM: M-level data @ Fs → 2-level data @ 2*M*Fs

- 1-bit data is inherently insensitive to mismatch
- Reduced sensitivity to asymmetrical switching

Why Not stay at PCM and use DWA?







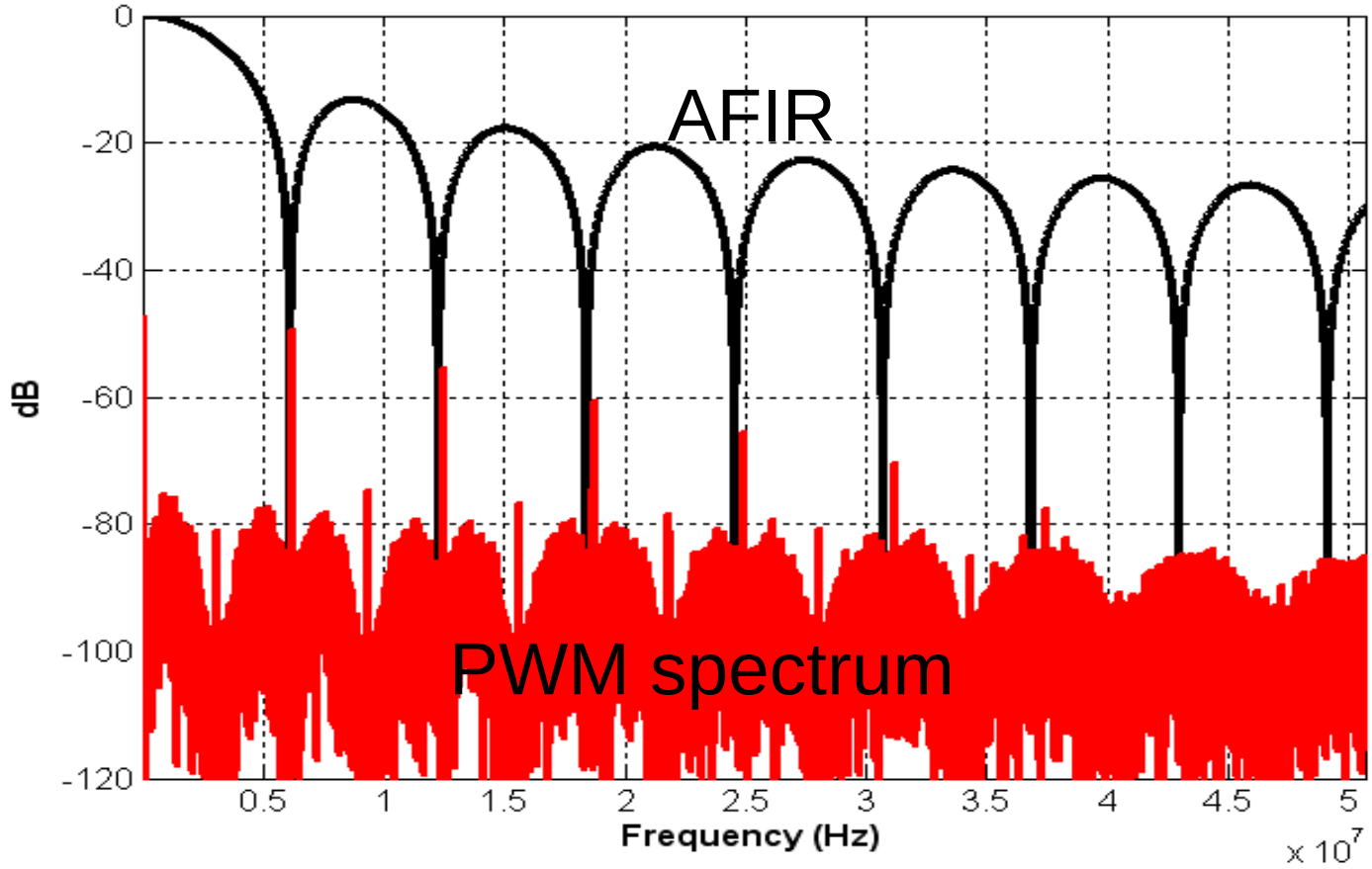
Source of the tone:
- Noise shaping SDM has idle tones, activity created by "Mismatch shaping loop" amplifies these idle tones.

Solution:
- Tonal free SDM design with dither or chaos.

Source of the tone:
- Mismatch shaper has idle tones, this loop combined with ISI introduces FM modulated tones specially at small signal swings.

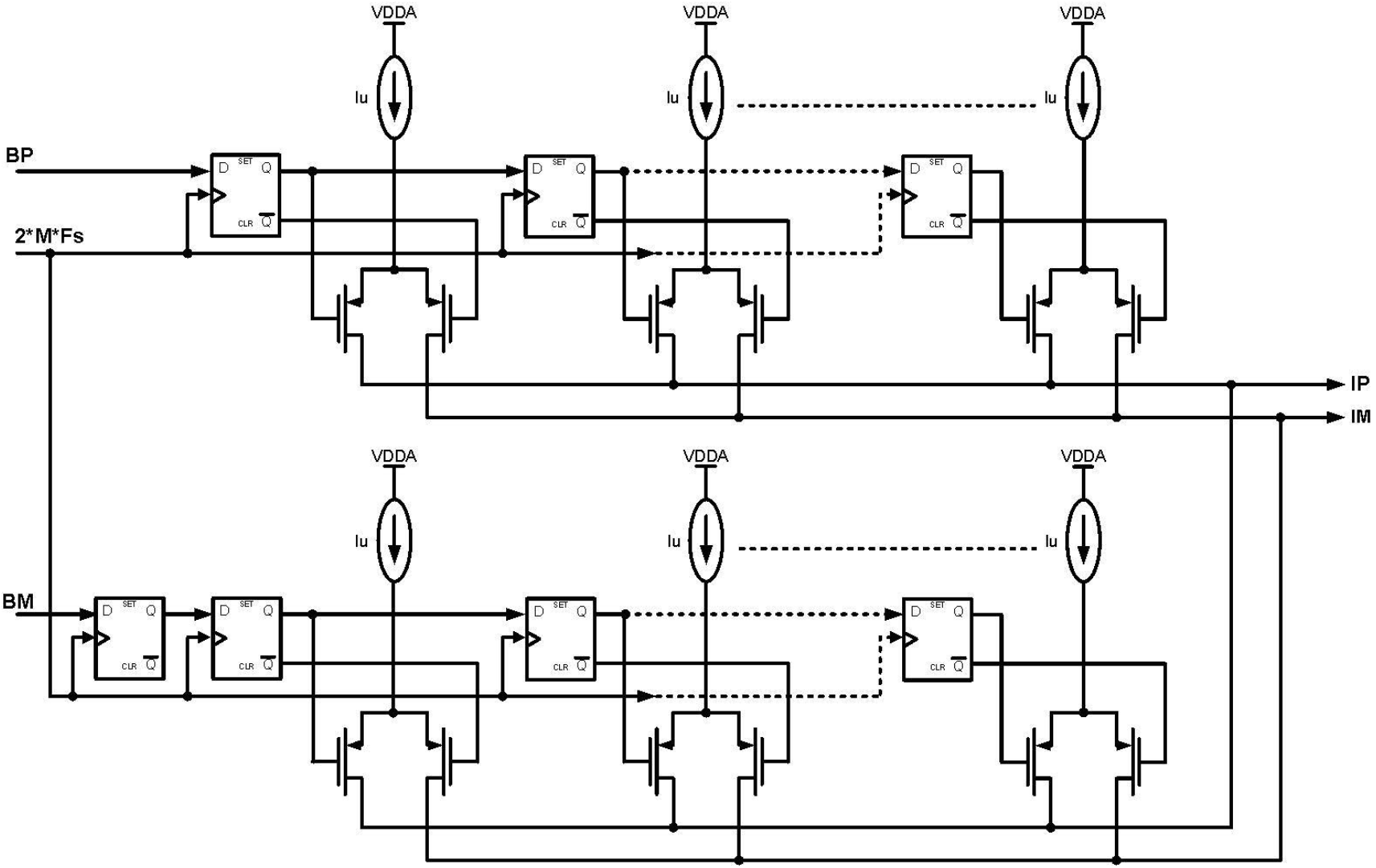
Solution:
- Dithering in SDM does not help, dithering here reduces the effect if static mismatch shaping.
- We can add DC tone and move the tones outside the audio band.

AFIR and PWM Spectrum

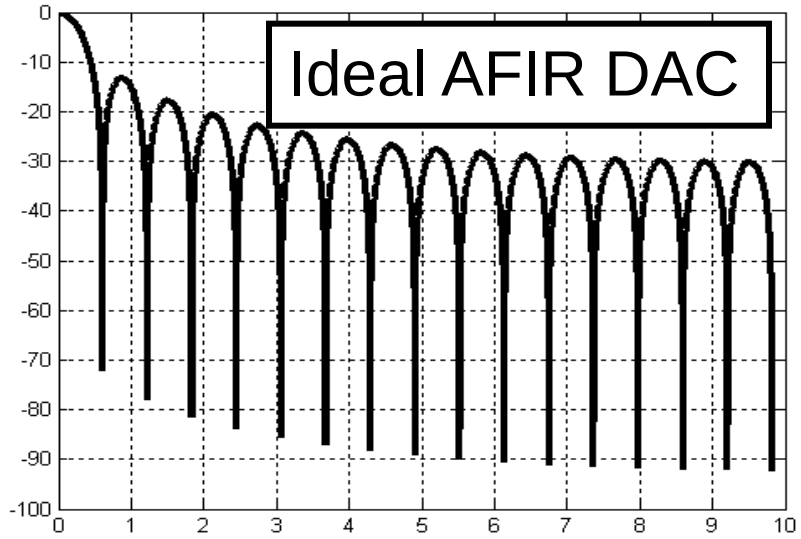


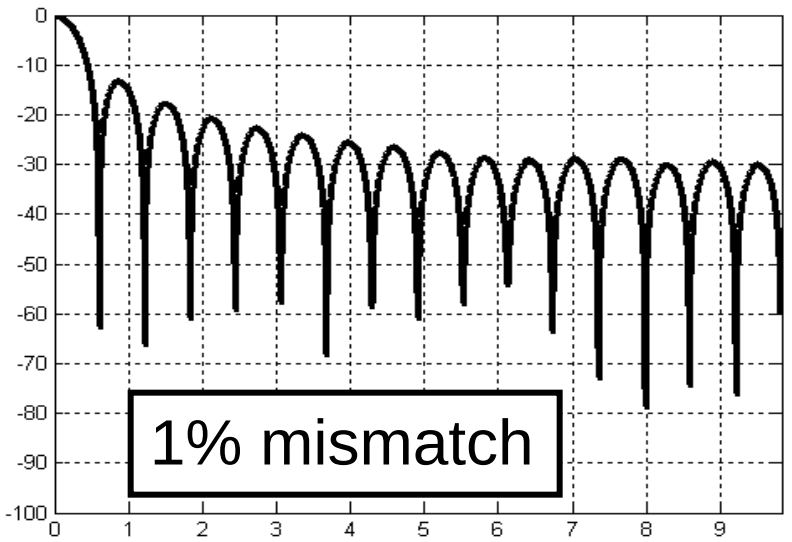
- AFIR notch locations align with PWM harmonics

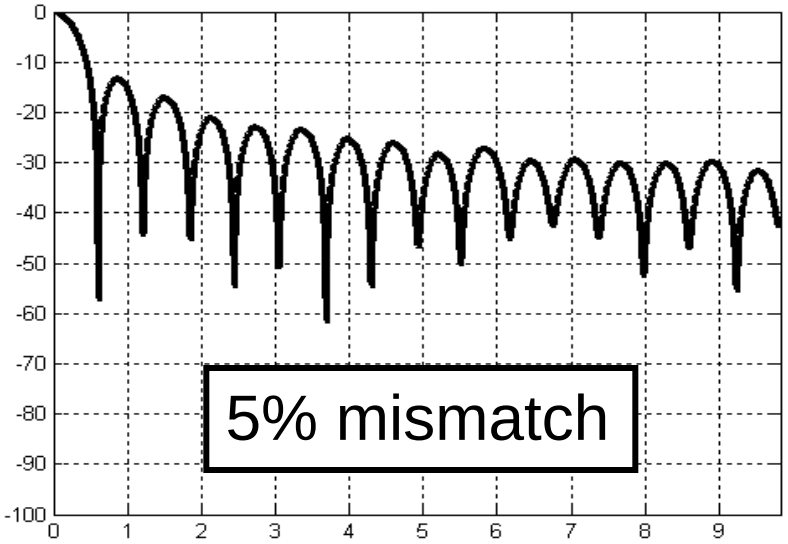
AFIR DAC Circuit

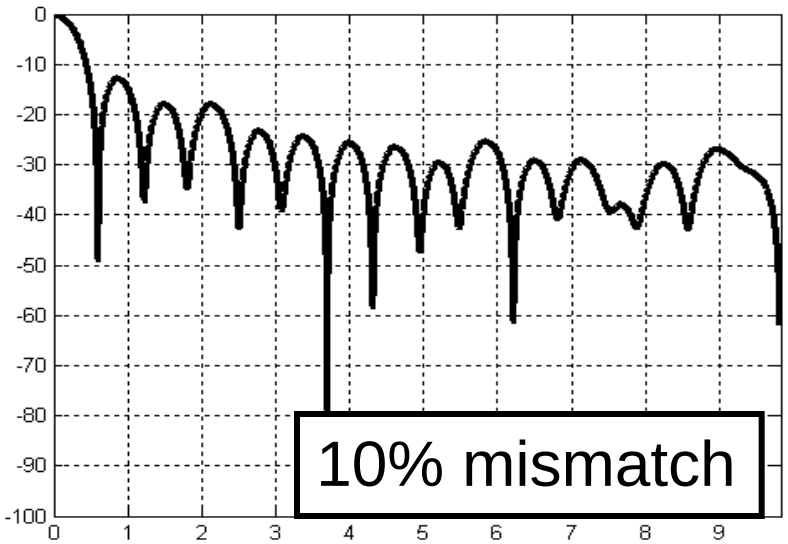


Effect of Mismatch on AFIR

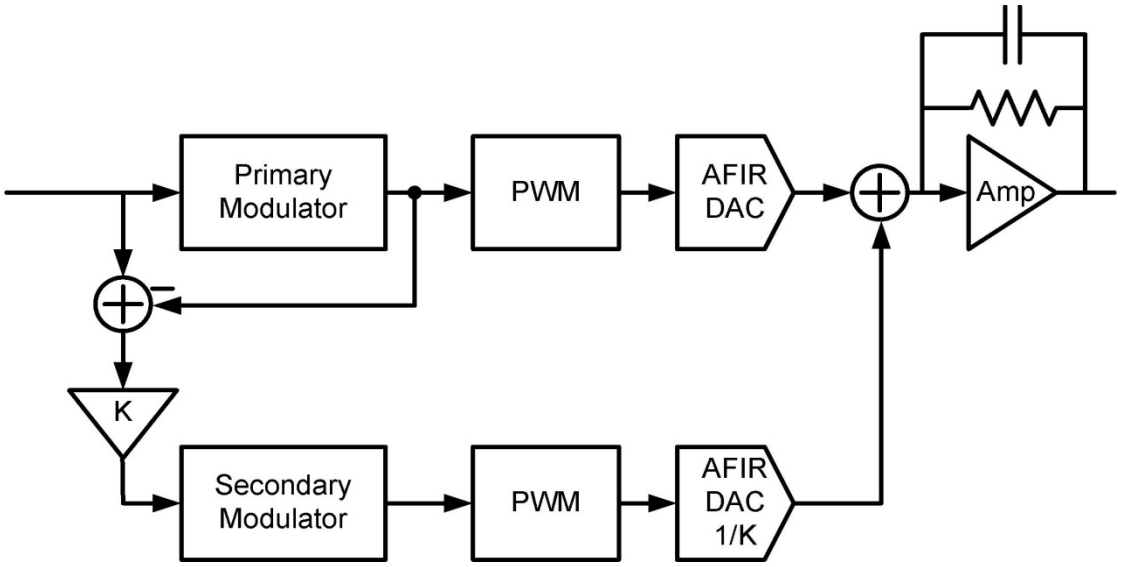




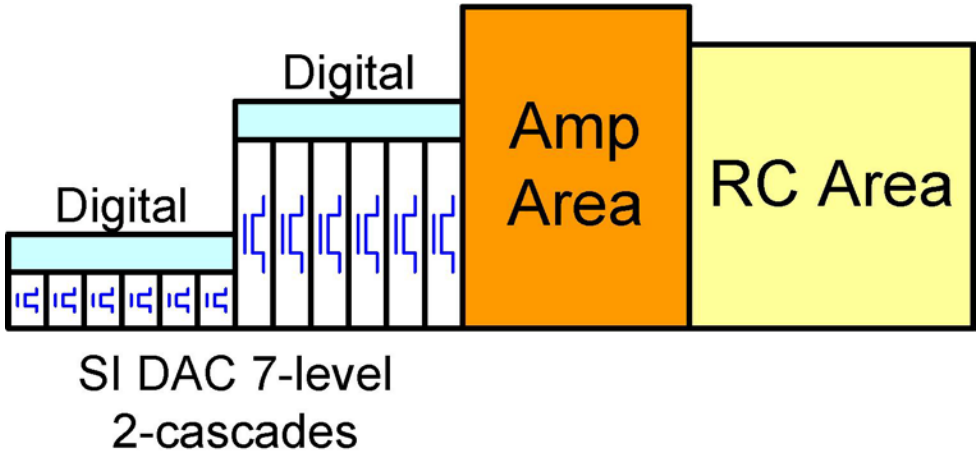




Impact of PWM on Area

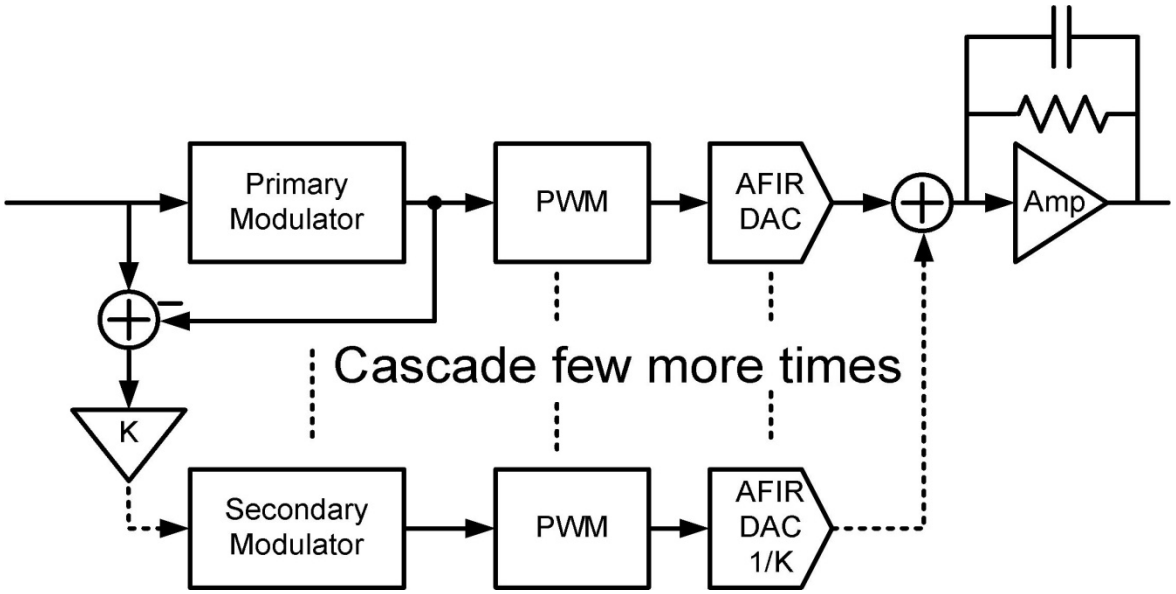


2-level Cascaded architecture with PWM and AFIR

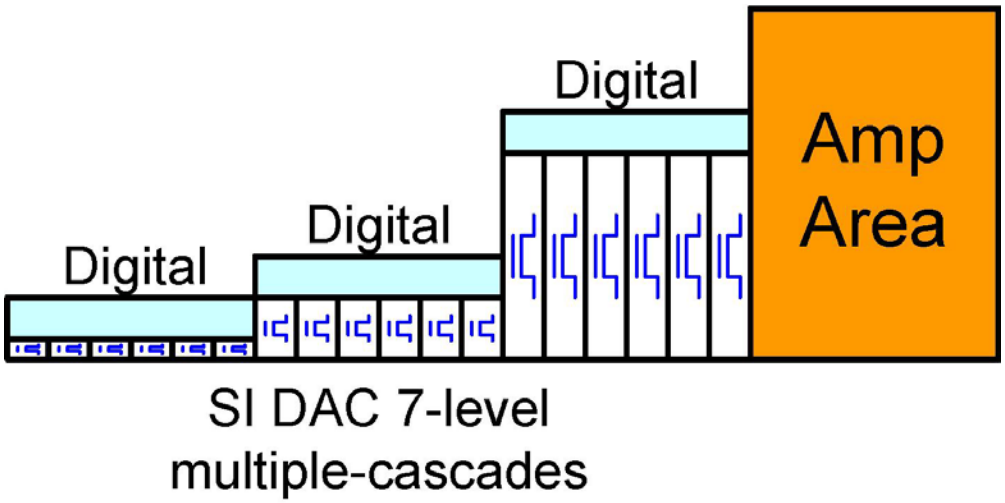


- Digital PWM costs nothing in gates.
- Resistant to mismatch and ISI
- Clock faster

Keep Cascading

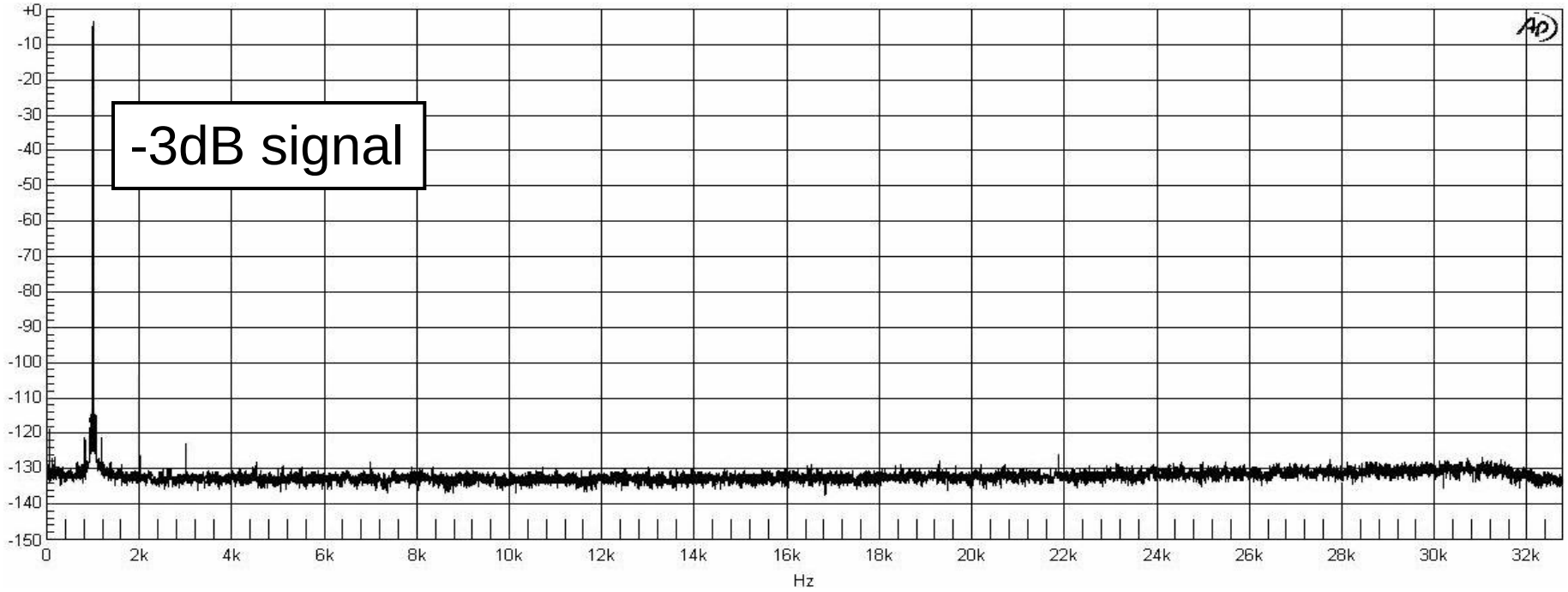


Multiple cascades combined with PWM and AFIR



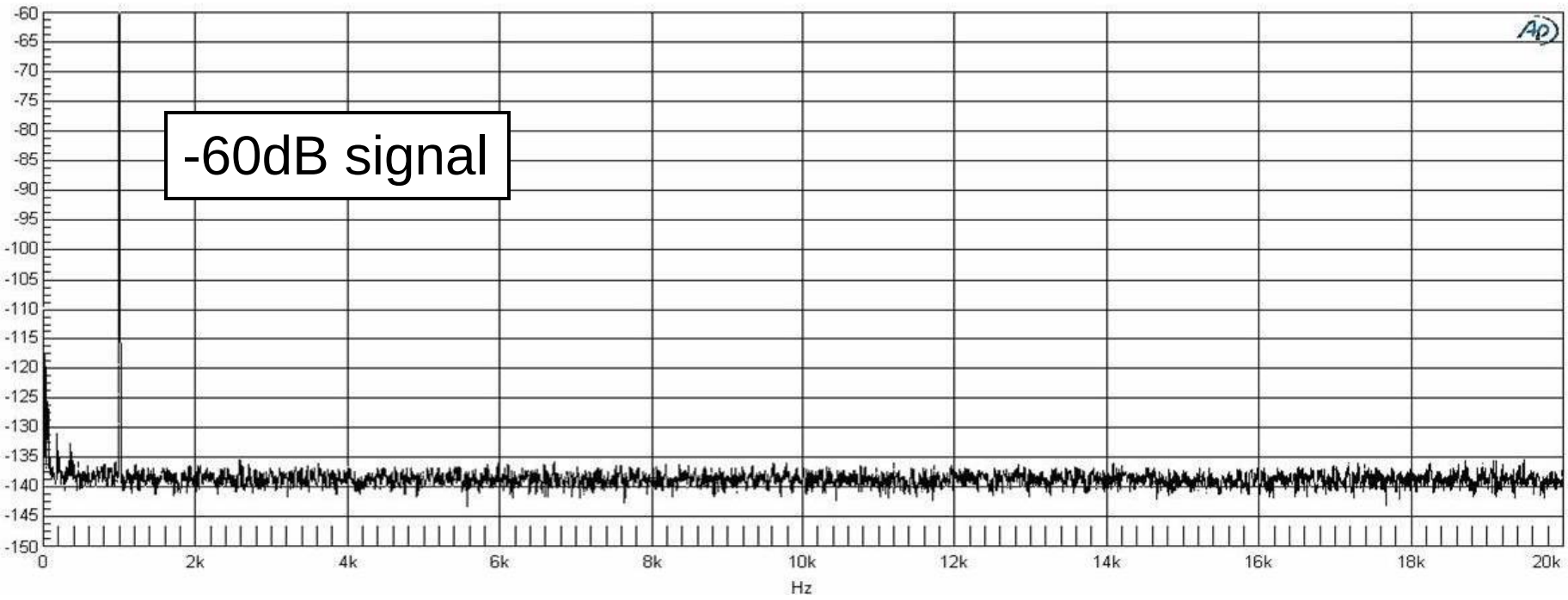
Can eliminate Cap area completely

Measurement Results



- Very low distortion at -3dB signal
- 2nd harmonic is down by 120dB
- 3rd harmonic is down by 118dB
- 60 Hz is visible around signal and DC

Measurement Results



- No spurs and idle tones visible at low signal swing either
- 60 Hz and its harmonics is still visible around DC

Performance Summary

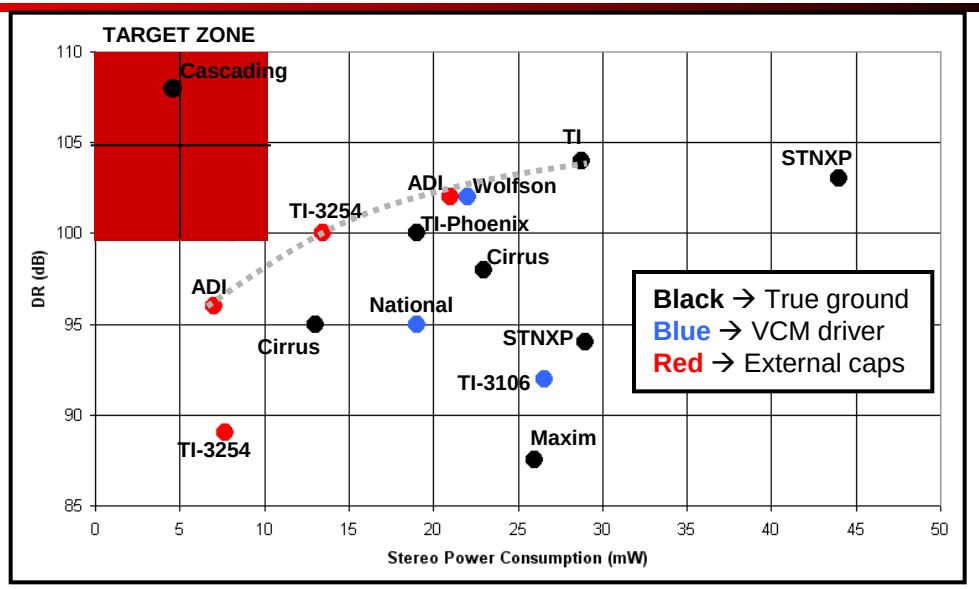
Process	45nm CMOS
Supplies	1.4V Analog/1.1V Digital
Full-scale differential output	176uA peak to peak
Digital power/DAC	0.1mW
Analog power/DAC	0.4mW
Total DAC area	0.045mm2
OSR	64
Clock Frequency	3.072MHz modulator clock 202.752MHz DAC clock
Dynamic Range (A-weighted)	110dB
THD+N	-100dB

Summary

- **Cascaded Modulator Architecture reduced out of band noise efficiently**
  - Reduced sensitivity to analog error sources
  - Reduced RC area cost for post filtering
  - Analog amplifier design requirements are relaxed too.
    - Smaller dV/dt transitions allow a slower amplifier with low area and power.

Where does it stand?

Part	Power (mW)	DR (dB)
ADI SSM2602	7	96
ADI SSM2602	21	102
ST-NXP STw5210	29	94
ST-NXP STw5210	44	103
Wolfson WM8980	22	102
Cirrus CS42L5	13	95
Cirrus CS42L5	23	98
Maxim MAX9851	26	87.5
National LM4934	19	95
TI TLV320AIC3254	7.7	89
TI TLV320AIC3254	13.5	100
TI TLV320AIC3106	26.54	92
TI TWL6040	19	100
TI TWL6040	28.8	104
Path2 Now	7	102.3
Path2-R&D	5.2	107
Path3	8	100

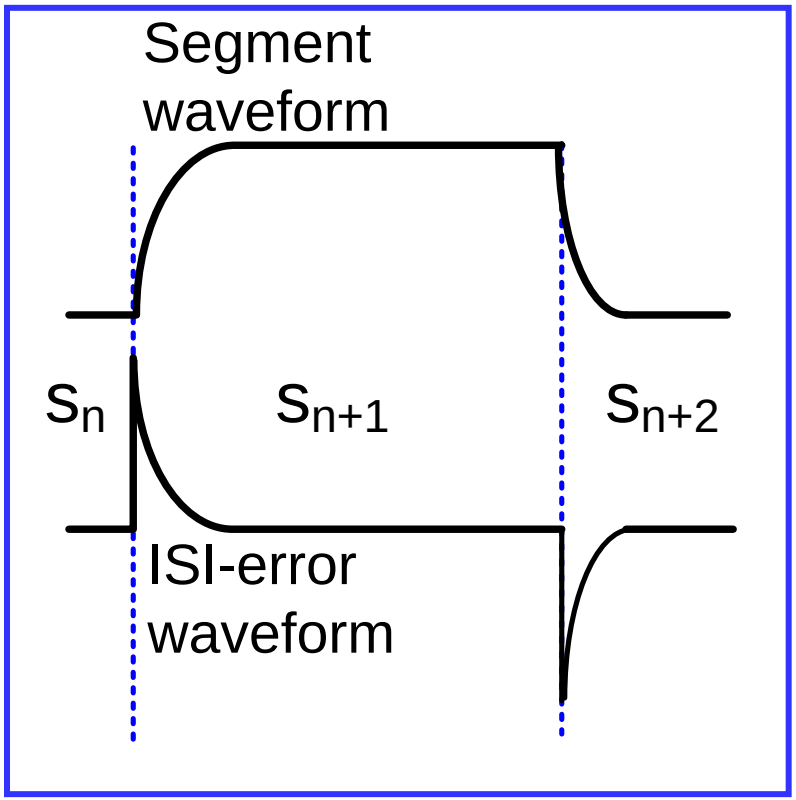


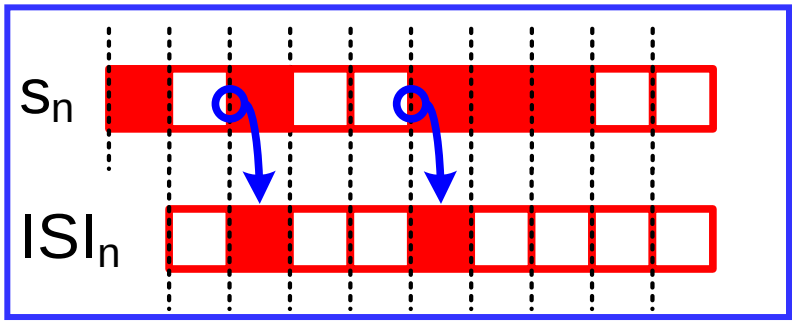
- I don't see a clear indication that ADI is using the 3-level DAC (108dB DR) published in ISSCC08
- ST-NXP is very focused on wireless requirements such as working with 32kHz RTC clock (in fact only one claiming this), true ground swing, implemented in a CMOS process, and ~100dB DR
- Unfortunately process information for most of these are not available.
- TI-TWL6040 (Phoenix) numbers are from the spec document and not silicon data
- **There is sort of a barrier line indicated in green on the graph above for performance and power trade-off when looking at existing designs.**
- **Our proposed architecture today can deliver best in the market performance and will be in a class of its own.**

Smart Signal Processing
How to Linearize a DAC?

It is all in how you use it

ISI-errors and modeling

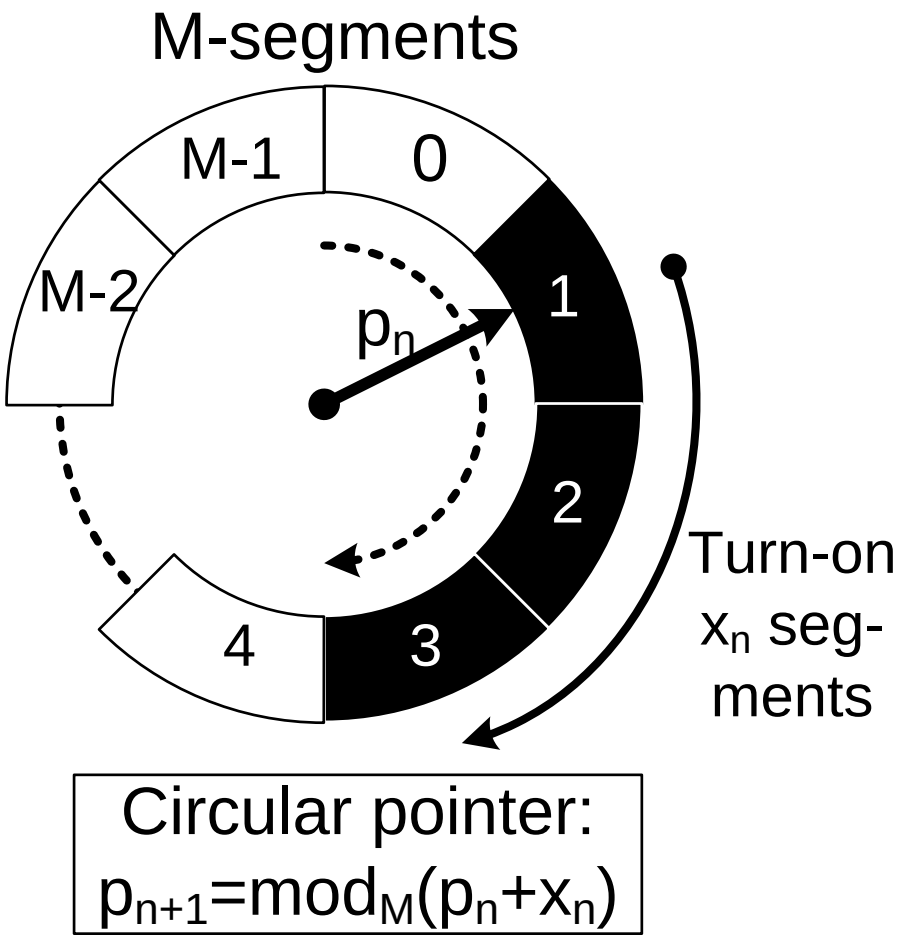




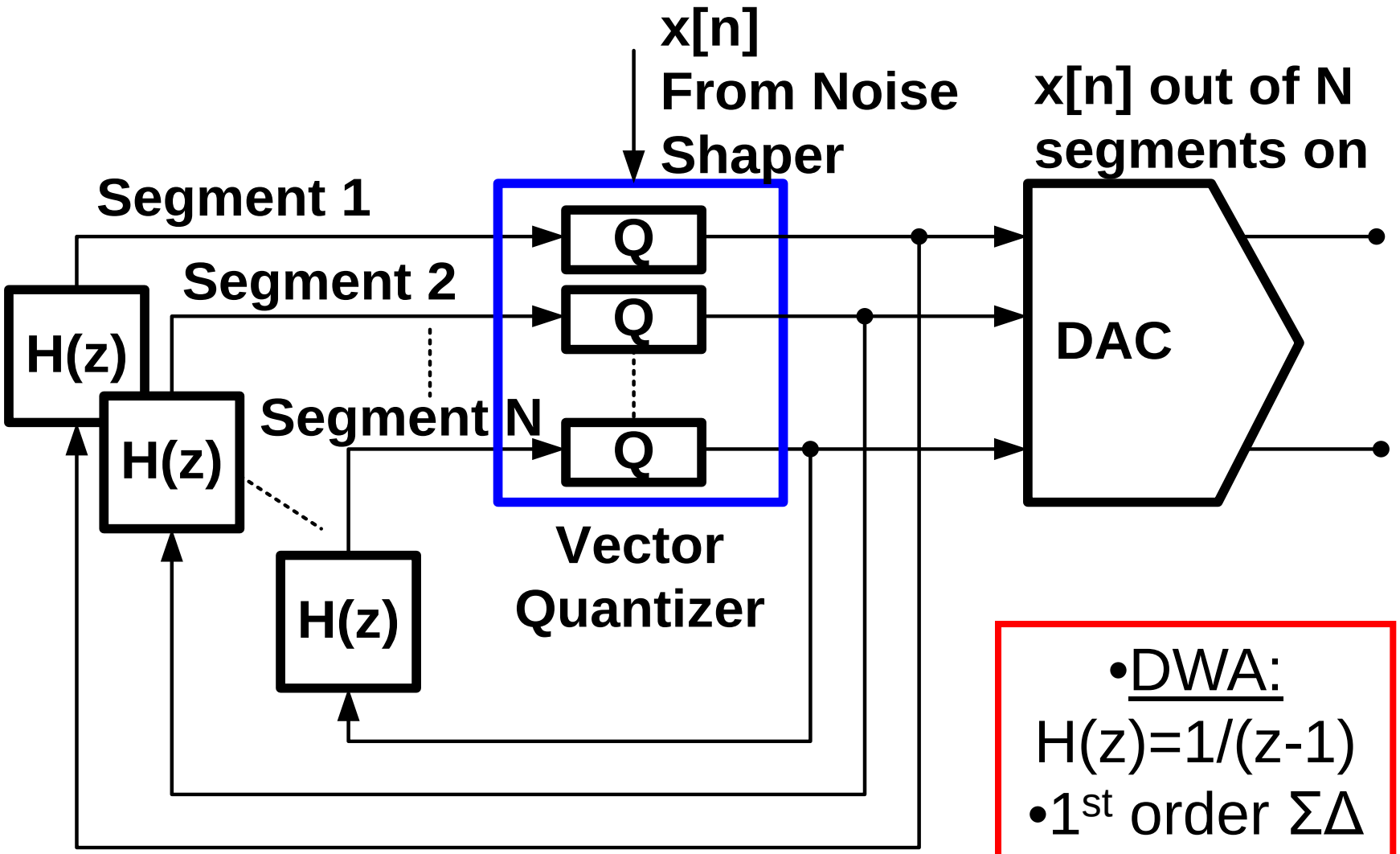
- **Errors depend on the previous symbol**
- **Can be modelled $ISI_n=f(s_n,s_{n-1})$**
- **f() can be linear for symmetrical switching**
  - Shaped by the mismatch shaper (correlated)
- **Non-linear part:**
  - Can be assigned to rising edge only
  - Un-correlated error

The popular DWA a perfect tone generator

- **Simple & popular scheme**
  - Barrel shifter
- **A.k.a ”segment rotation”**
- **Variable rotation speed:**
  - Proportional to the signal x_n
  - ”VCO” operation
  - **F**requency **M**odulated idle tones

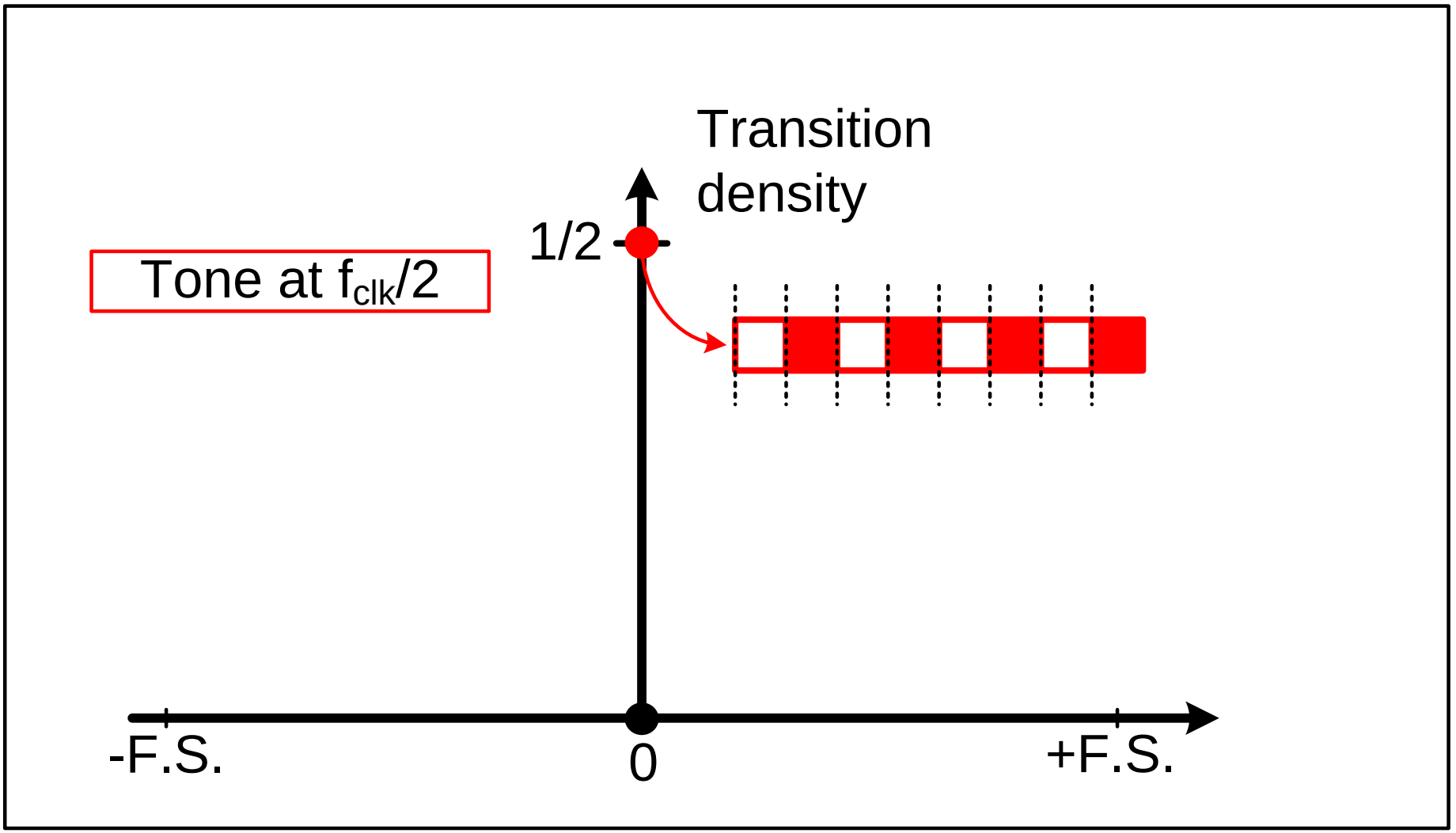


Generic mis-match shaper

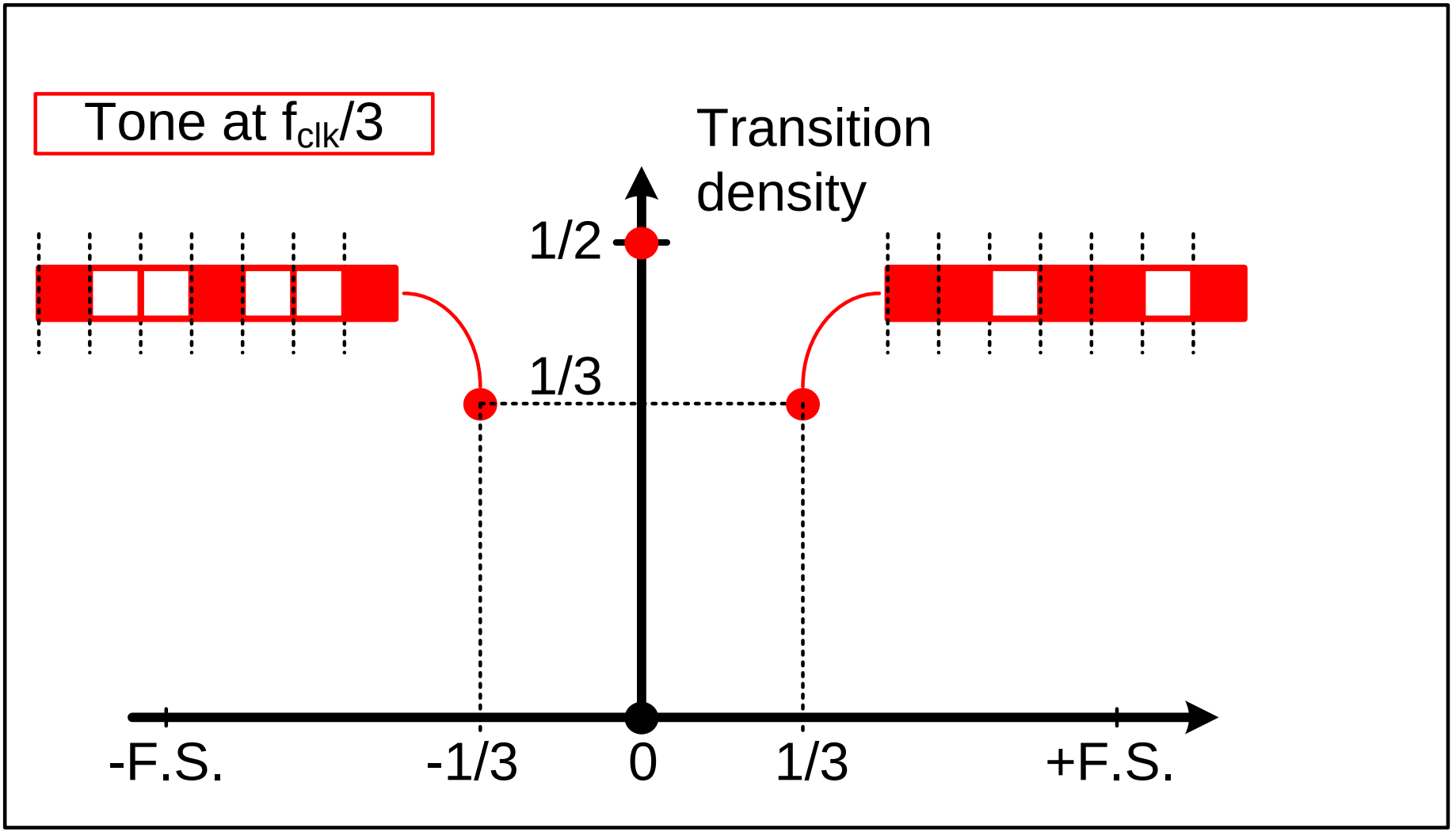


- DWA:
- $H(z)=1/(z-1)$
- 1^{st} order ΣΔ

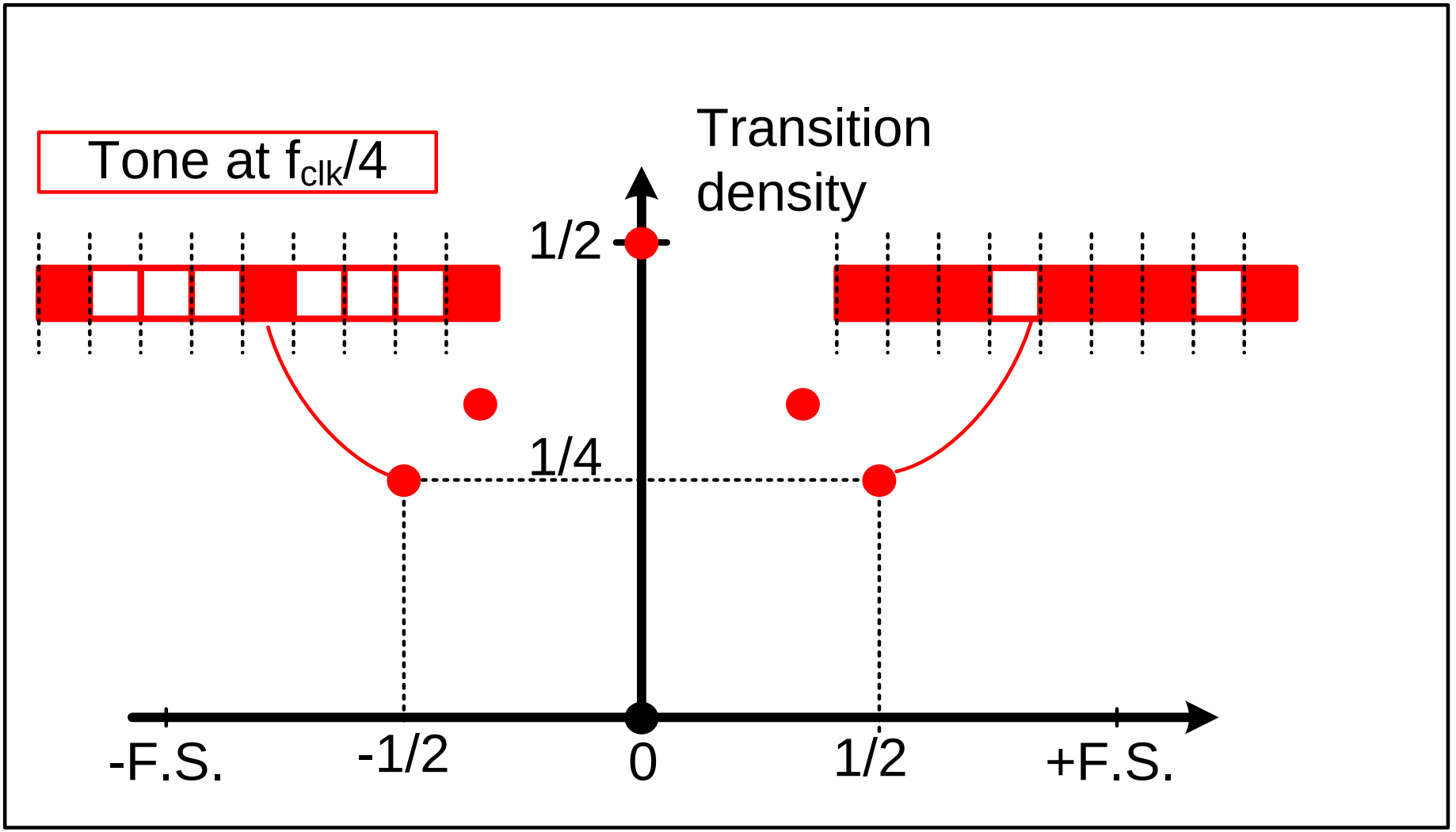
Max. Rate pattern: Midscale



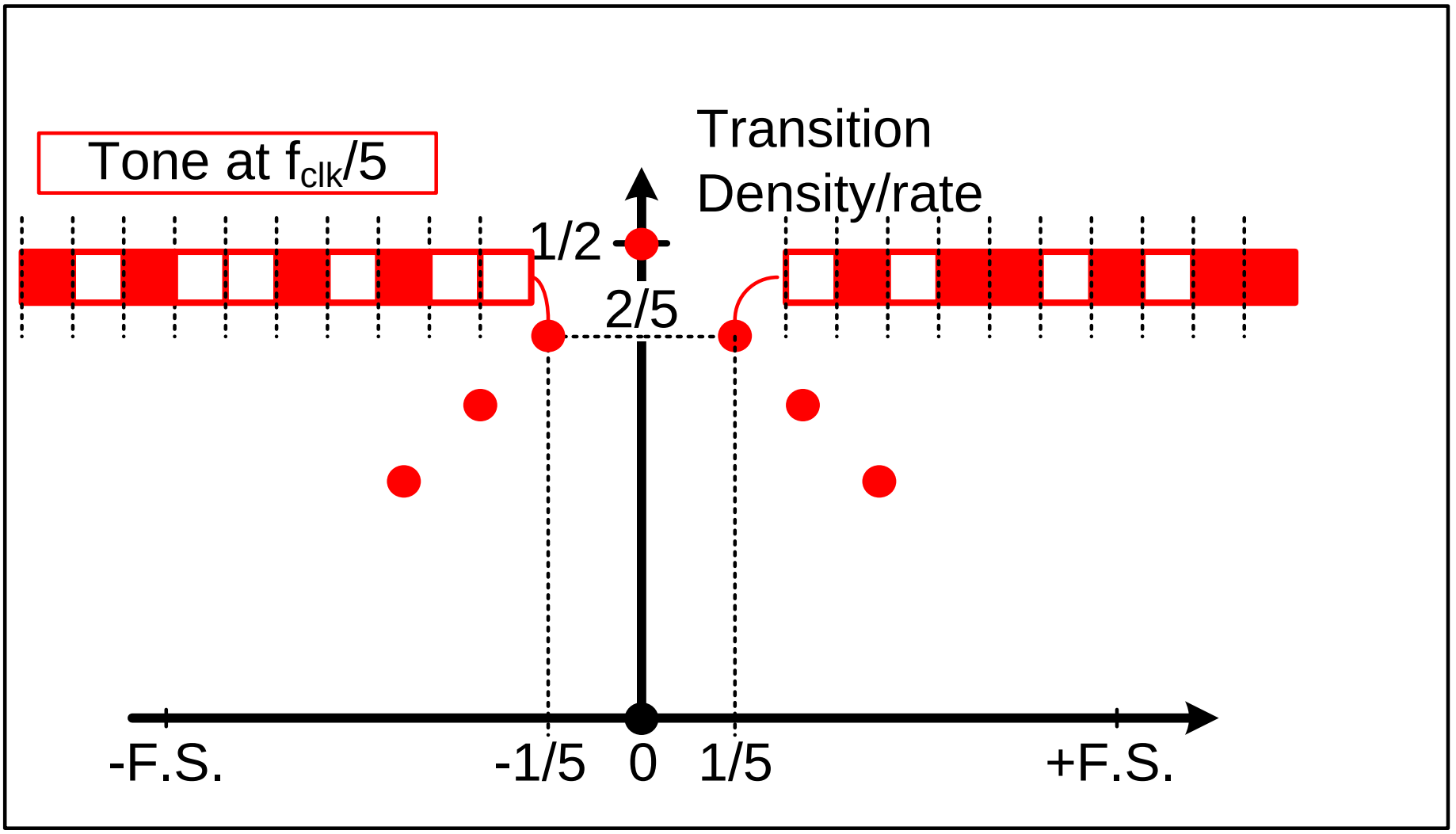
Pattern for ±1/3 Full Scale



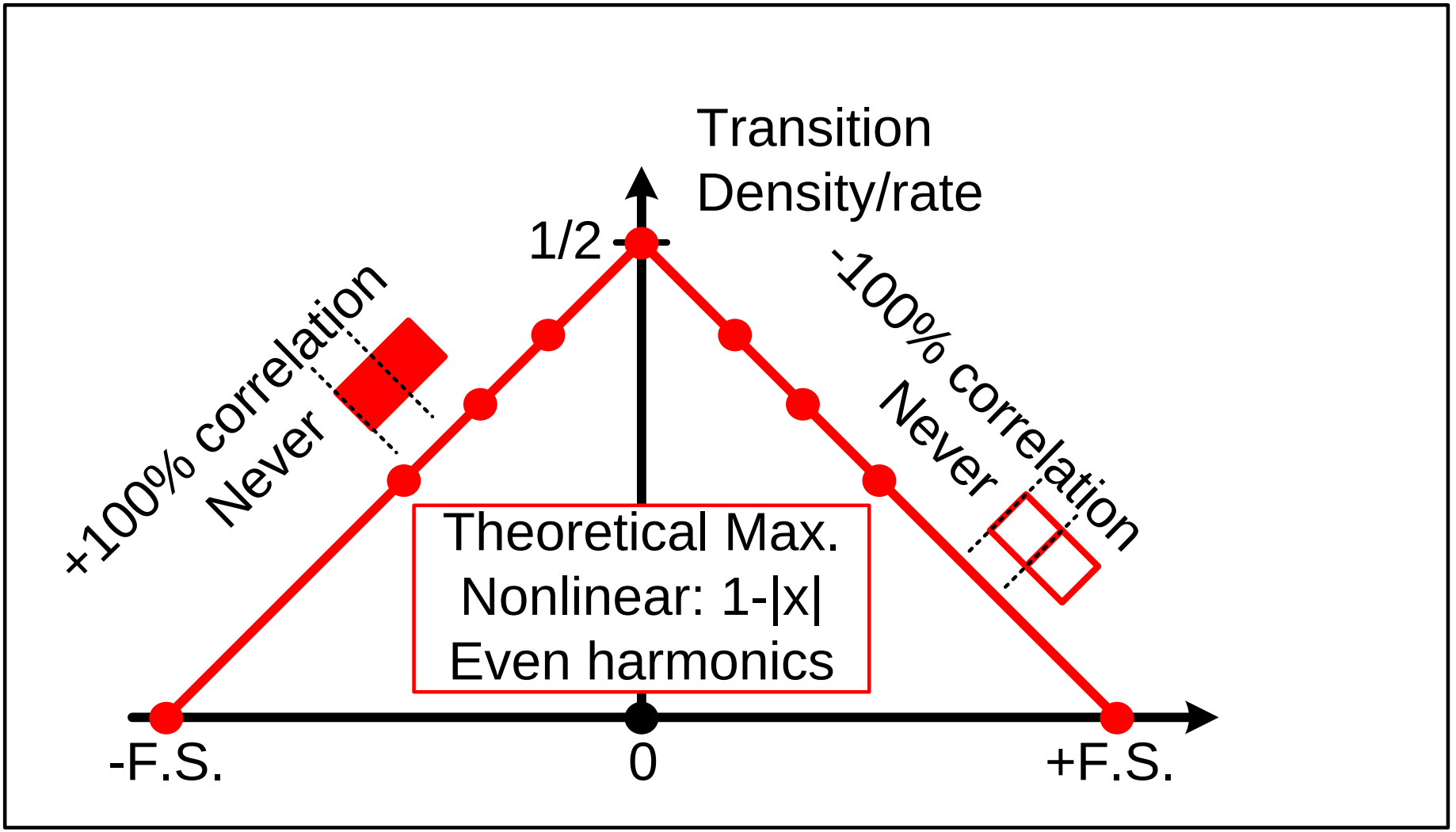
Pattern for ±1/2 Full Scale



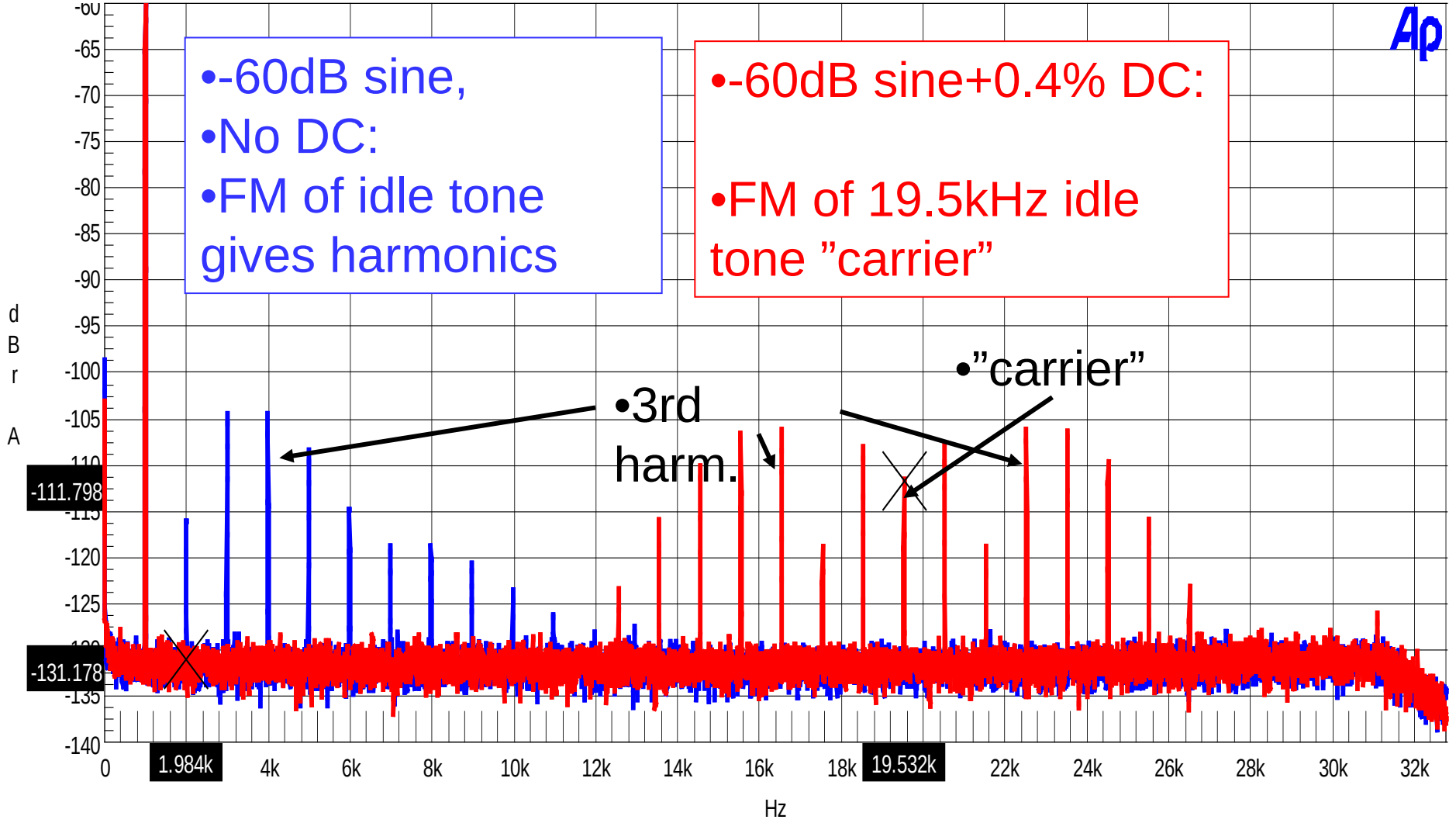
Pattern for ±1/5 Full Scale



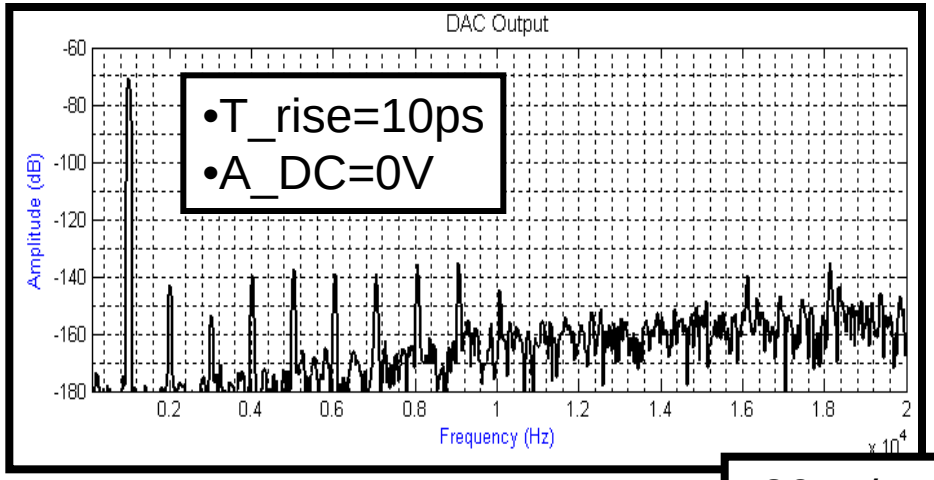
DWA: Max. Theoretical rate

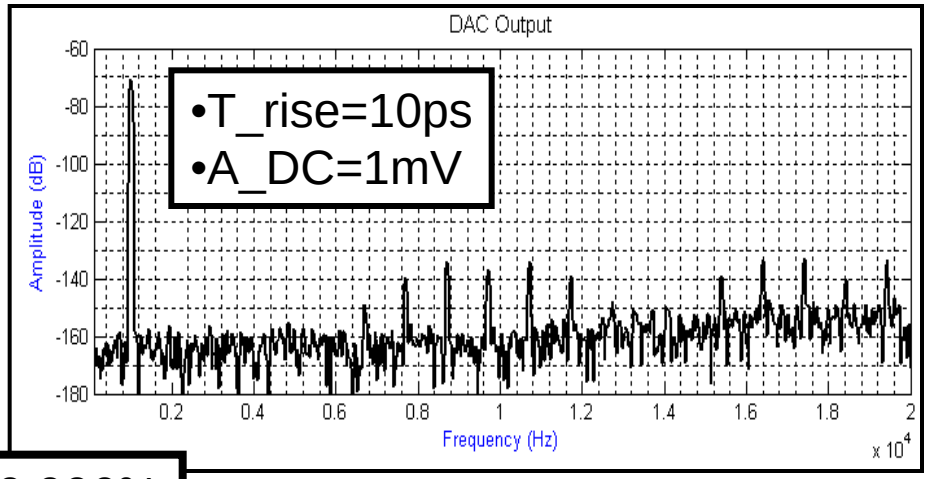


FM idle tones : low level THD issue

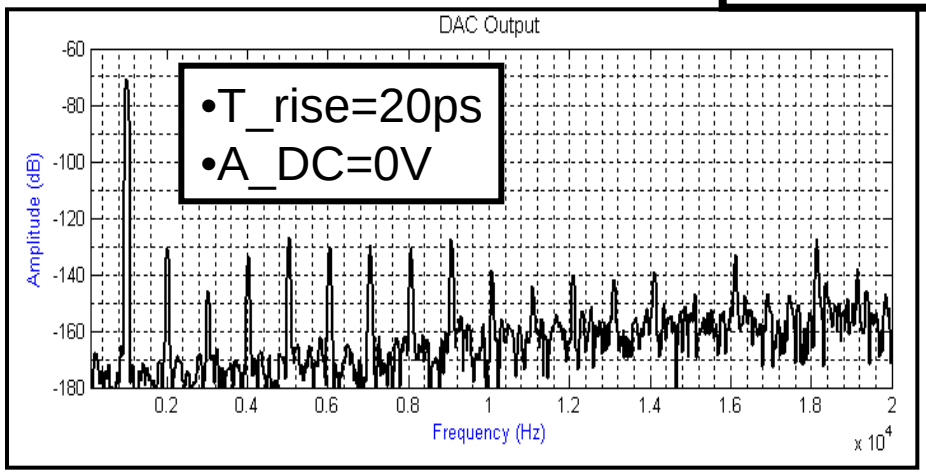


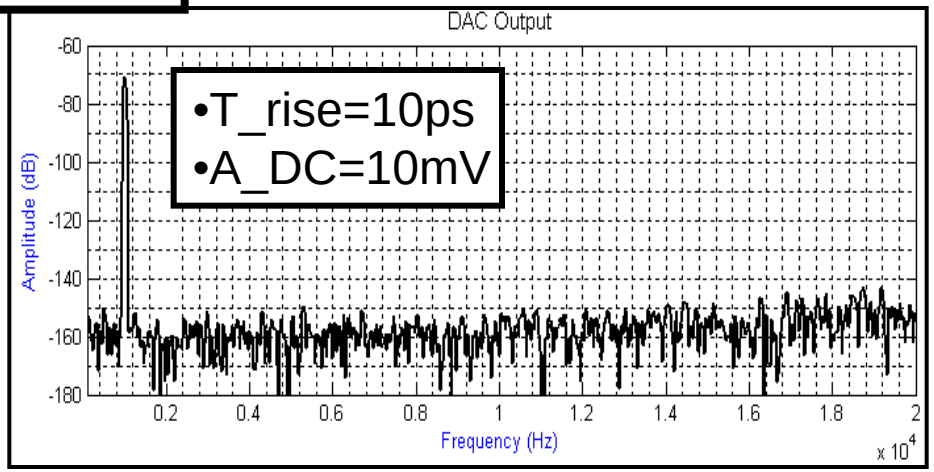
DWA+ISI Simulation examples





•20ps/T_s=0.006%





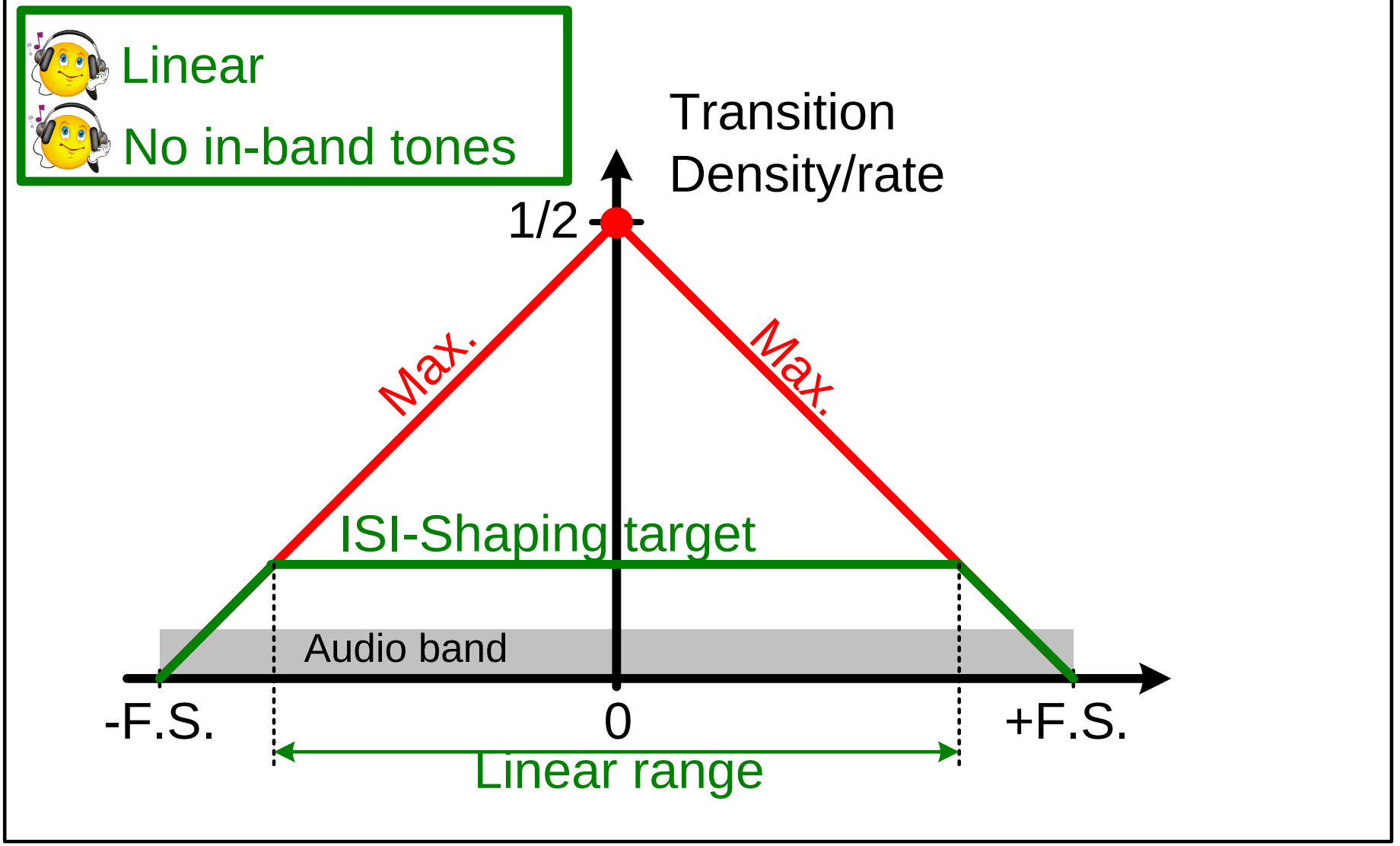
DWA+ISI: a bad cocktail..

- **Large signal:**
  - V-shape transition rate / mean ISI error vs. signal x_n
  - Abs(x_n) type non-linearity - Even-order harmonics
  - Constant THD ratio vs. level
- **Small-signal:**
  - Signal x_n jitters across the midscale point due to the Noise shaper activity
  - De-correlation of the ISI-error: no high-pass shaping
  - FM tone frequency proportional to x_n: (100% mod -> f_{clk})
  - THD due to FM tones – both even and odd order
- **nm-scale design:**
  - Increased clock does not help: ISI goes up and error is concentrated in tones (not spread spectrum)

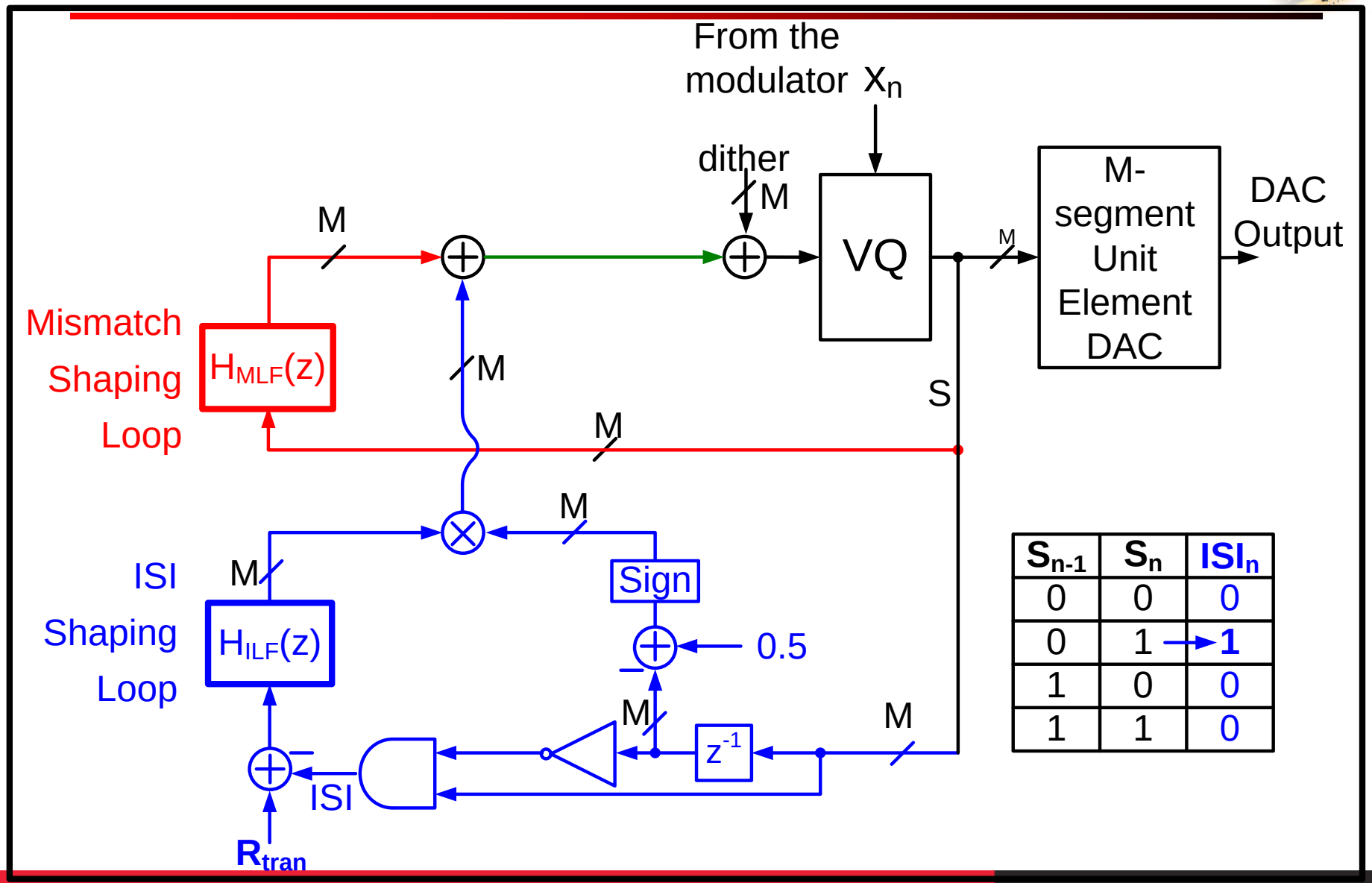
Prior-art solutions to ISI

- **”DC Dither” to shift tones out of band**
  - Popular but just moves the problem
- **Return-to-zero (RTZ)**
  - Increased current, sensitive to timing accuracy/jitter
- **Sample and hold de-glitching**
  - Used to de-glitch R2R DACs in early CD players
- **Mismatch shaping with reduced transition rate[4]**
  - Reduce ISI at the cost of mismatch shaping
- **Pulse Width Modulation (ISSCC’2010)**
  - Great but requires high frequency clock
- **Re-spins and layout tweaking of the analog...**

ISI-Shaper target



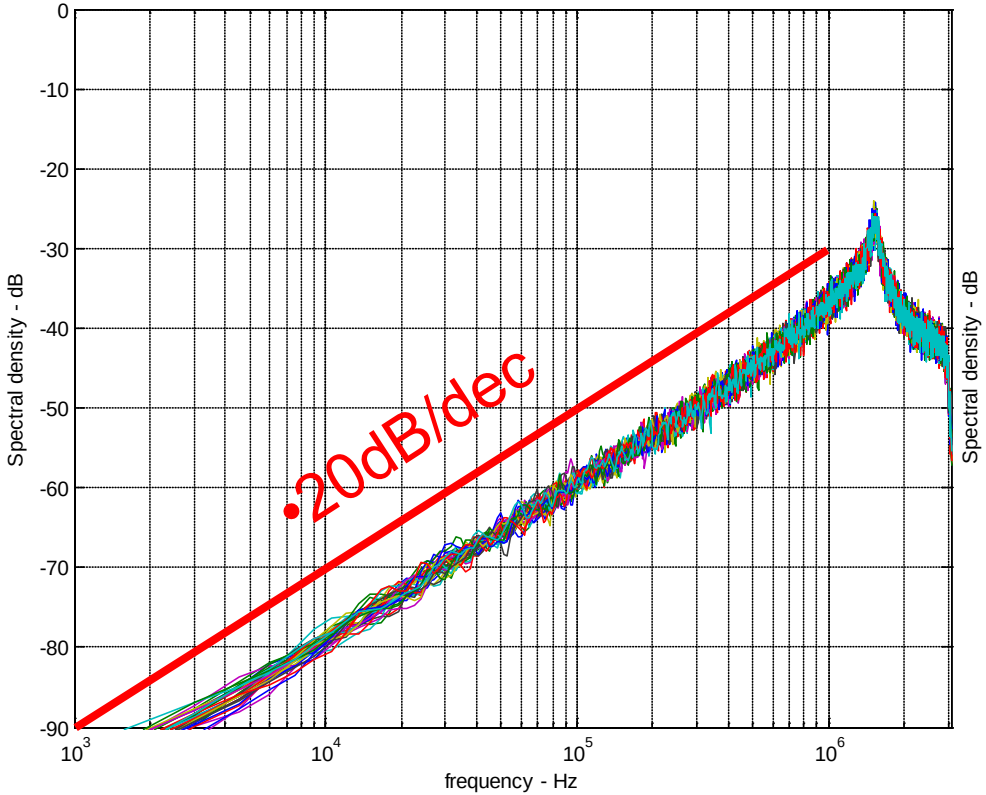
The novel ISI shaping algorithm



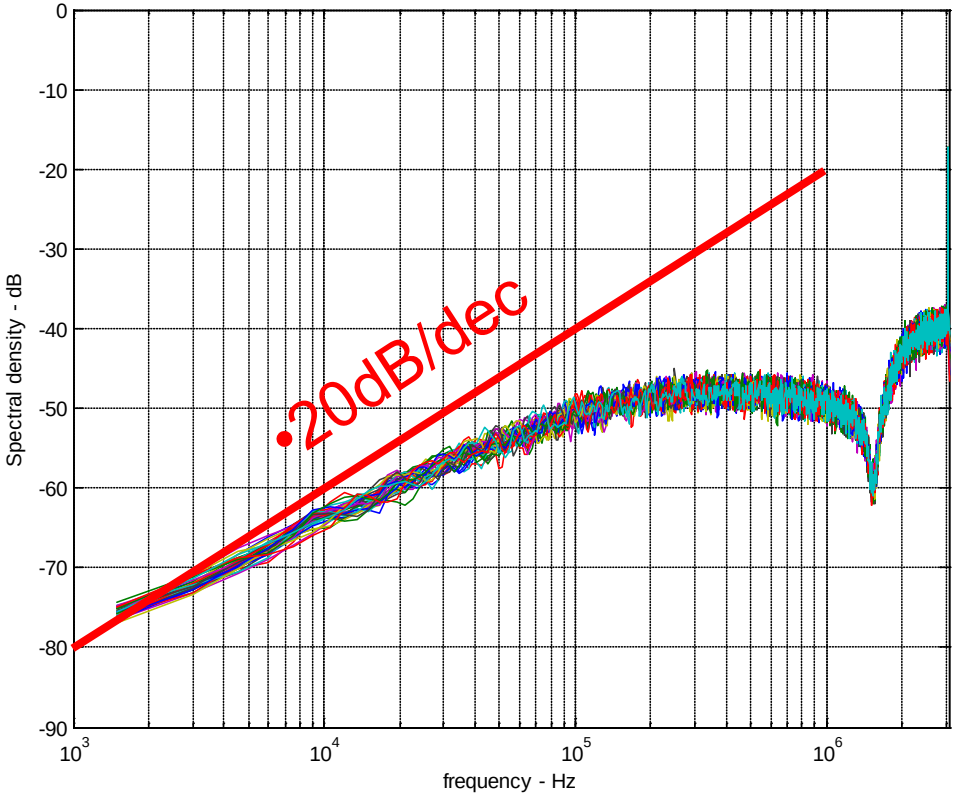
S_{n-1}	S_n	ISI_n
0	0	0
0	1	1
1	0	0
1	1	0

Single segment spectra

- Segment (static mismatch error)

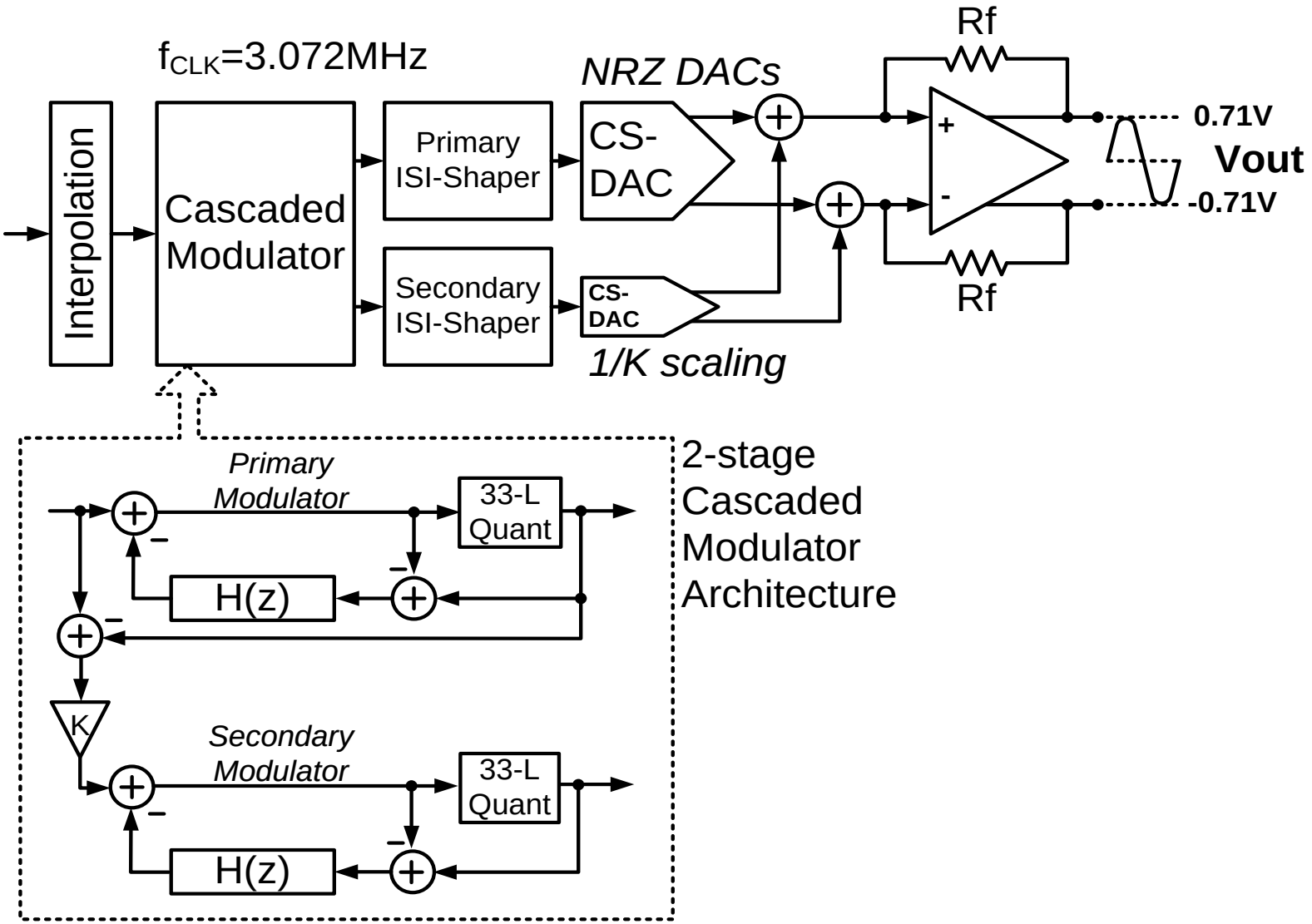


- ISI-error

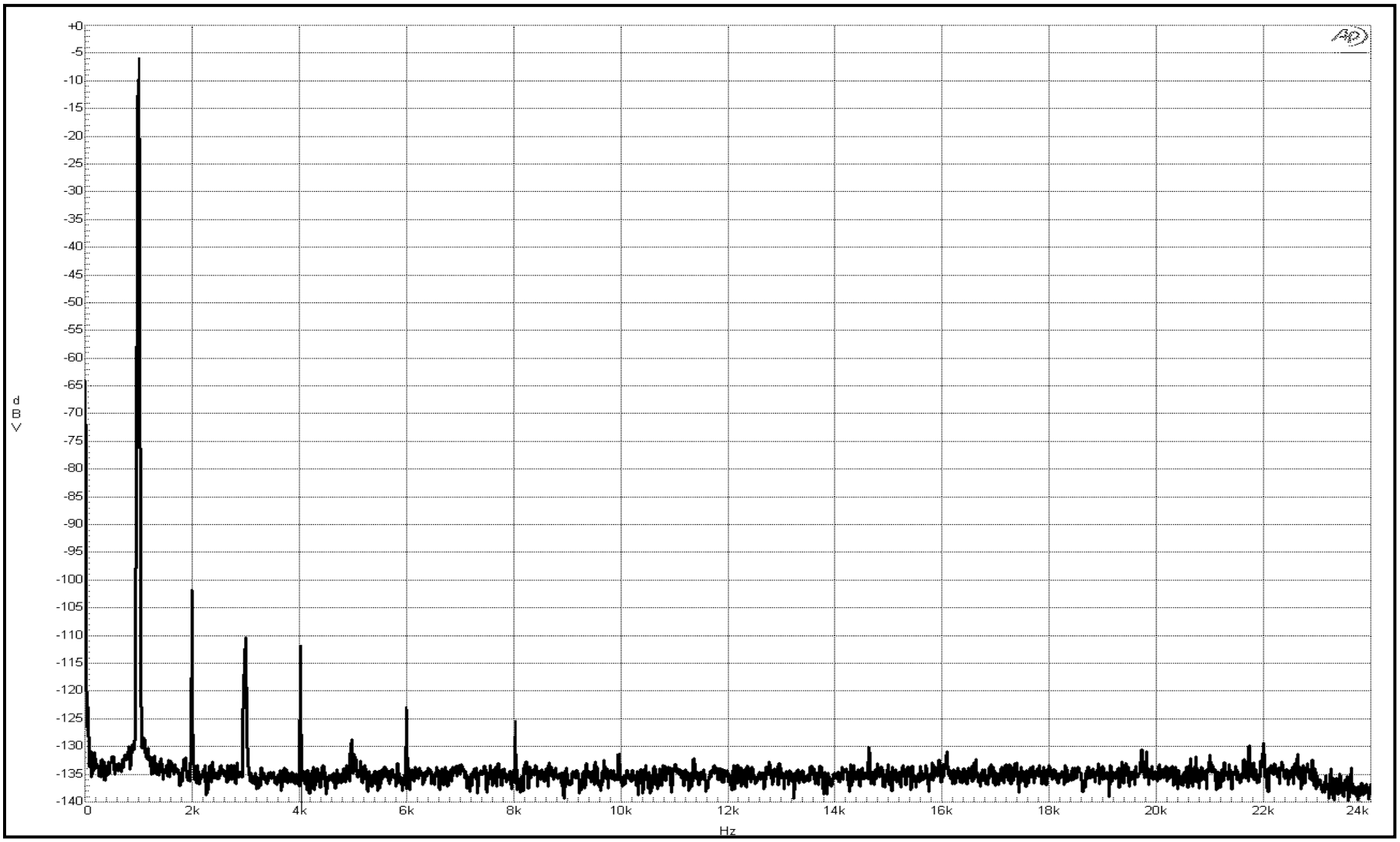


- 1st/1st order ISI-shaper, R_{tran}=0.25

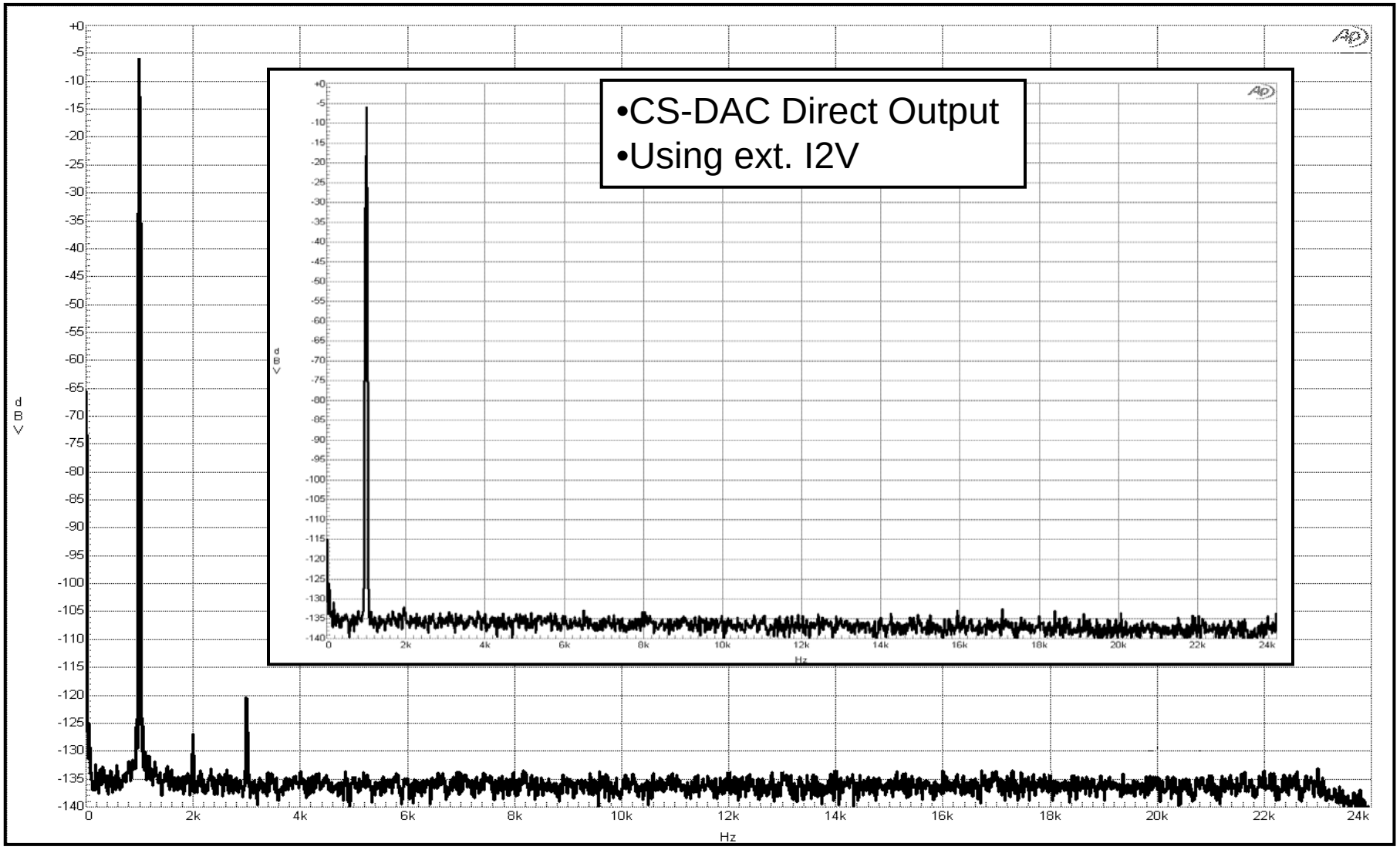
45nm Audio DAC implementation



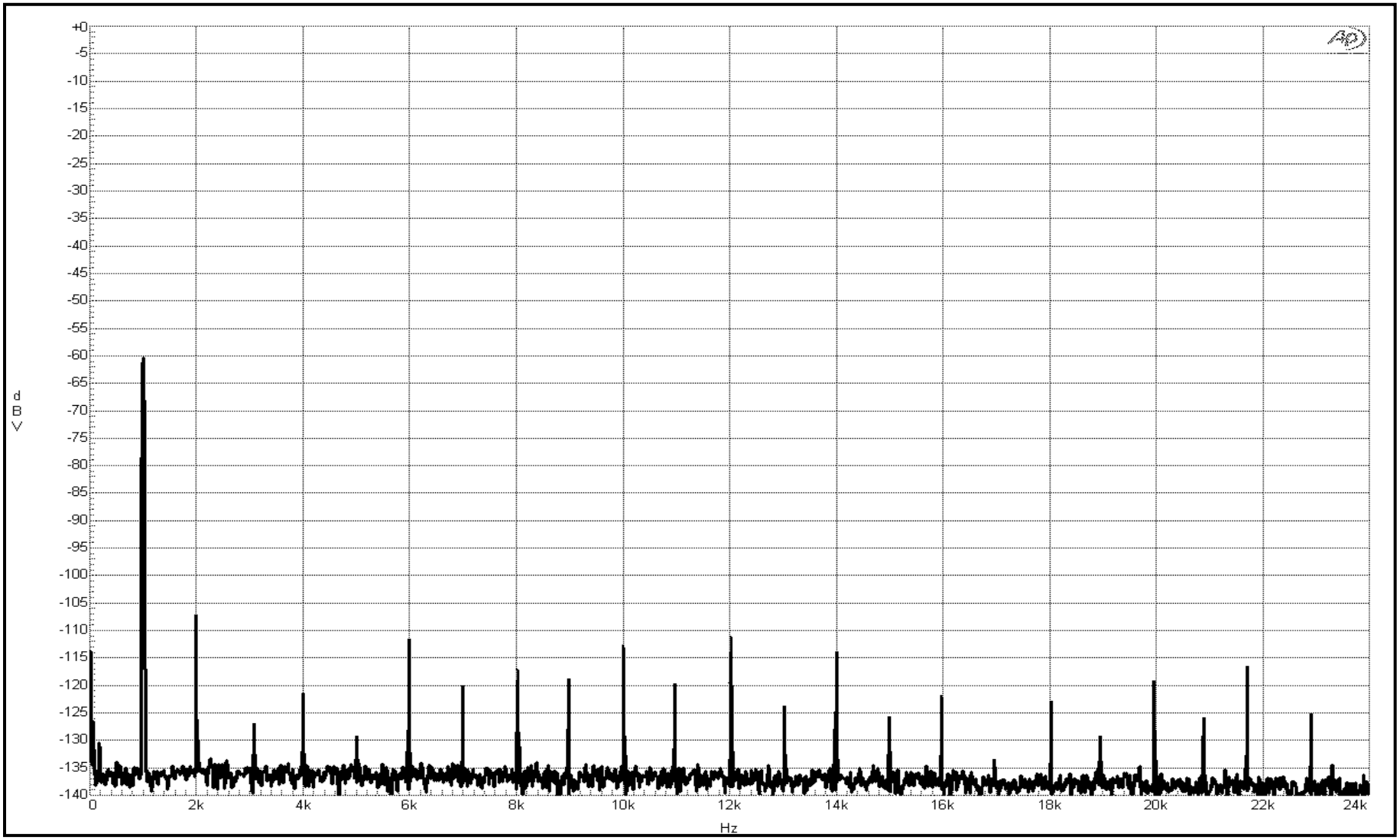
Output at -6dB using DWA



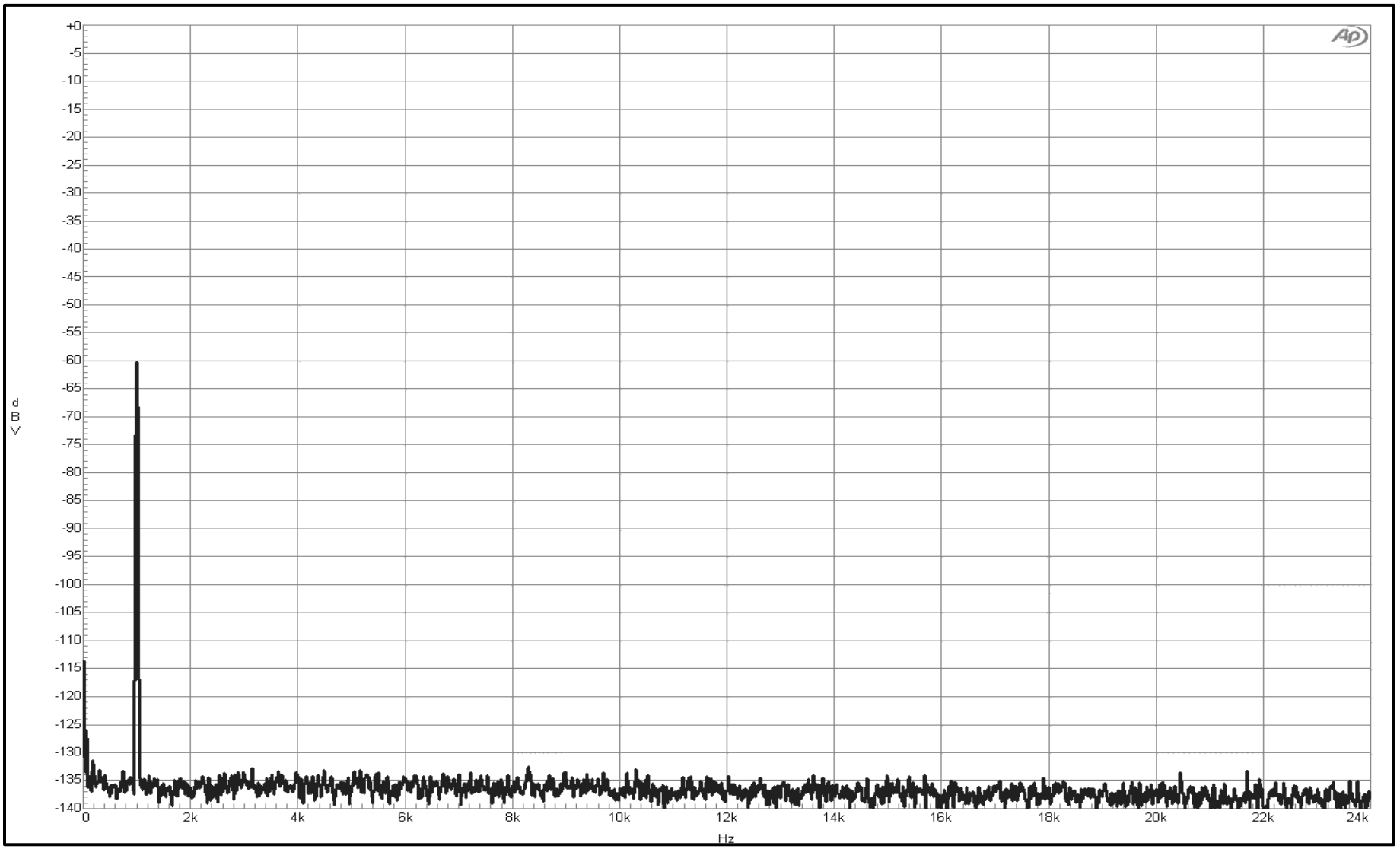
Output at -6dB using ISI Shaper



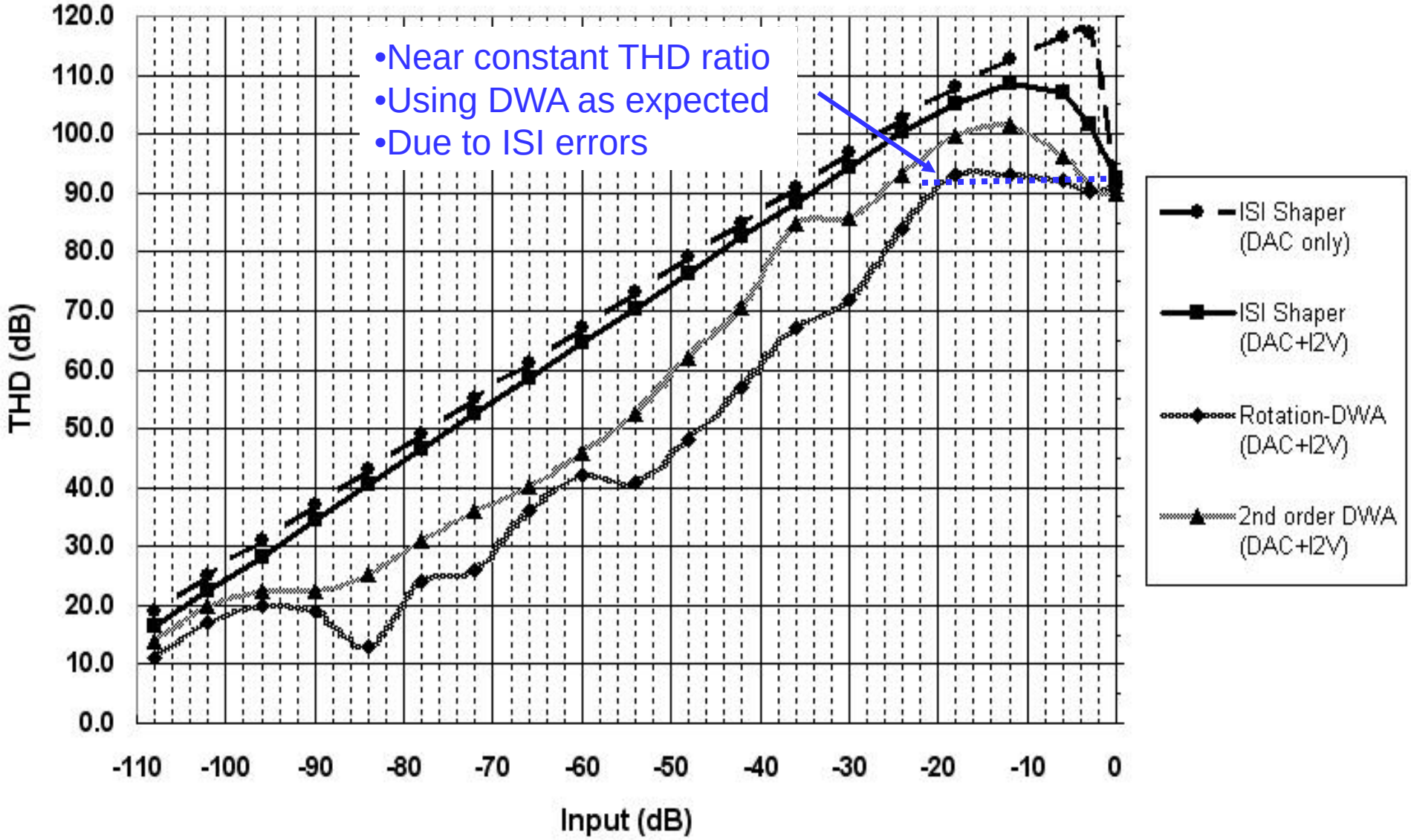
Output at -60dB using DWA



Output at -60 dB using ISI Shaper



45nm DAC: Amplitude sweep



45nm DAC summary

Process	45nm CMOS
Supplies	1.45V Analog 1.1V Digital
Full-scale differential current output	0.176mApp
Full-scale differential voltage output	0.5Vrms
Digital power consumption	0.14 mW
Analog power consumption	0.735 mW
Total area	0.16mm2
OSR	64
Clock Frequency	3.072MHz
Voltage Output Dynamic Range (A-weighted)	108dB
Current Output Total Harmonic Power @-3dB	-120.0dB
Voltage Output Total Harmonic Power @ -3dB	-104.6dB
Voltage Output Total Harmonic Power @ -12dB	-120.6dB
Voltage Output Total Harmonic Power @ -60dB	-124.5dB

Conclusions

- **DWA+ISI gives high amplitude THD and low level tones/noise problems**
  - Concentrates ISI energy in in-band tones
- **ISI is hard to fight using analog techniques**
  - Goes against the desire for fast cycle design of SoCs
  - Goes against the desire to clock fast in nm scale CMOS
- **The novel ISI shaper:**
  - Excellent audio performance – even in 45nm
  - helps fast cycle SoC design
  - Digitally assisted analog solution to fight ISI
  - Provides robustness to analog imperfection