The Design of an Analogue Class-D Audio Amplifier Using Z-Domain Methods

by

Pieter Stephanus Kemp

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Department of Electrical and Electronic Engineering
University of Stellenbosch
Private Bag X1, 7602 Matieland, South Africa

Supervisor: Prof H. du T. Mouton
Co-supervisor: B. Putzeys

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Declaration

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Abstract

The class-D audio power amplifier has found widespread use in both the consumer and professional audio industry for one reason: efficiency. A higher efficiency leads to a smaller and cheaper design, and in the case of mobile devices, a longer battery life.

Unfortunately, the basic class-D amplifier has some serious drawbacks. These include high distortion levels, a load dependent frequency response and the potential to radiate EMI. Except for EMI, the aforementioned issues can be mitigated by the proper implementation of global negative feedback. Negative feedback also has the potential to indirectly reduce EMI, since the timing requirements of the output devices can be relaxed.

This thesis discusses the design of a clocked analogue controlled pulse-width modulated class-D audio amplifier with global negative feedback. The analogue control loop is converted to the z-domain by modelling the PWM comparator as a sampling operation. A method is implemented that improves clip recovery and ensures stability during over-modulation. Loop gain is shaped to provide a high gain across the audio band, and ripple compensation is implemented to minimize the negative effect of ripple feedback. Experimental results are presented.

Uittreksel

Die klas-D klankversterker geniet wydverspreide gebruik in beide die verbruiker en professionele oudio industrie vir een rede: benuttingsgraad. 'n Hoër benuttingsgraad lei tot 'n kleiner en goedkoper ontwerp, en in die geval van draagbare toestelle, tot langer batterylewe.

Ongelukkig het die basiese klas-D klankversterker ernstige tekortkominge, naamlik hoë distorsievlakke, 'n lasafhanklike frekwensierespons en die vermoë om EMI te genereer. Behalwe vir EMI kan hierdie kwessies deur die korrekte toepassing van globale negatiewe terugvoer aangespreek word. Negatiewe terugvoer het ook die potensiaal om EMI indirek te verminder, aangesien die tydvereistes van die skakel stadium verlaag kan word.

Hierdie tesis bespreek die ontwerp van 'n geklokte analoog-beheerde pulswydte-modulerende klas-D klankversterker met globale negatiewe terugvoer. Die analoogbeheerlus word omgeskakel na die z-vlak deur die PWM vlakvergelyker as 'n monster operasie te modelleer. 'n Metode word geïmplementeer wat die stabiliteit van die lus verseker tydens oormodulasie. Die lusaanwins word gevorm om 'n hoë aanwins in die oudioband te verseker en riffelkompensasie word geïmplementeer om die negatiewe effek van terugvoerriffel teen te werk. Eksperimentele resultate word voorgelê.

Acknowledgements

The author would like to thank the following people for their contribution towards this project:

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Contents

Nomenclature

Variables

A_s	sawtooth carrier amplitude
f_s	switching frequency
K	comparator gain
m_a	(amplitude) modulation index
m_f	frequency modulation index
t_d	loop propagation delay
t_{dt}	dead time
V_s	half-bridge power supply rail voltage

Abbreviations

AC	alternating current
DAC	digital to analogue converter
DC	direct current
EMI	electromagnetic interference
ETF	error transfer function
FFT	fast Fourier transform
FPGA	field-programmable gate array
I/O	input/output
LUT	lookup table
MOSFET	metal-oxide-semiconductor field-effect transistor
NSPWM	naturally sampled pulse-width modulation
NSSSPWM	naturally sampled single-sided pulse-width modulation
PAE	pulse amplitude error
PCB	printed circuit board
PLL	phase-locked loop

PSRR	power supply rejection ratio
PTE	pulse timing error
PWM	pulse-width modulation/modulator
RMS	root mean square
STF	signal transfer function
THD	total harmonic distortion

Clarification of Terms

ETF	The error transfer function is normally defined as the transfer function from the error source to the point directly after the error source. However, in this thesis the error transfer function is defined as the transfer function from the error source to the amplifier output.
Linear	The term linear as used in this thesis may refer to three different concepts. Firstly, it may refer to the linearity of a system or process. A linear system is one that mathematically satisfies the superposition principle. In this sense PWM, for example, is non-linear. Secondly, linear may refer to the "linear" operating region of a device. Thirdly, it may refer to something that is distortion free. The context in which the word is used should make its meaning self-explanatory.

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

A class-D audio amplifier is an amplifier in which the power devices are, ideally, either fully on or fully of at any given time. No power is dissipated in the ideal class-D power stage, since the output devices never have a current through and a voltage across them at the same time. This is in contrast to class-A, class-B and other linear amplifier topologies where there is a current through and a voltage across the output devices for significant periods of time. Consequently, the efficiency of class-D amplifiers is superior to that of conventional linear amplifiers.

In its simplest form a class-D amplifier is similar to a DC to AC converter. Figure 1.1 illustrates the basic principle for a half-bridge converter. The MOSFET switches are switched complementary and the gate-signals of the switches are generated through pulse-width modulation (PWM). The simplest way to generate the PWM signal is by comparing a low-frequency reference signal to a high-frequency carrier waveform, typically a sawtooth or triangle wave. This is called naturally sampled PWM (NSPWM), since the switching transition occurs at the natural intersection of the reference and carrier waveforms. Figure 1.2 shows the waveforms associated with NSPWM for a sawtooth carrier $c(t)$ and a sinusoidal reference signal $r(t)$. The amplitude of the carrier and the reference signal is A_c and A_r, respectively. The amplitude modulation index, normally referred to as just the modulation index, is defined as the ratio between the reference and carrier amplitude, or

$$m_a = \frac{A_r}{A_c}.$$

The frequency of the carrier is also the switching frequency, denoted by f_s. The ratio between the reference signal frequency f_r and the carrier frequency f_s is the frequency modulation index, or

$$m_f = \frac{f_r}{f_s}.$$

The amplified PWM waveform $p(t)$ contains an amplified version of the reference waveform (assuming $V_s > A_r$) as well as components at harmonics of the switching frequency and their associated side-bands [5]. The high-frequency components are removed from the signal $p(t)$ by a demodulation filter, which is typically a passive LC low-pass filter.

The DC to AC inverter becomes an audio power amplifier when the sinusoidal reference is replaced by an audio signal. Both the modulation index m_a and the frequency modulation index m_f now varies with time. The switching frequency is chosen significantly higher than the maximum expected audio frequency (generally 20 kHz) in order to minimise the magnitude of the carrier side-bands in the audio band and to allow proper attenuation of the high-frequency components by the filter.

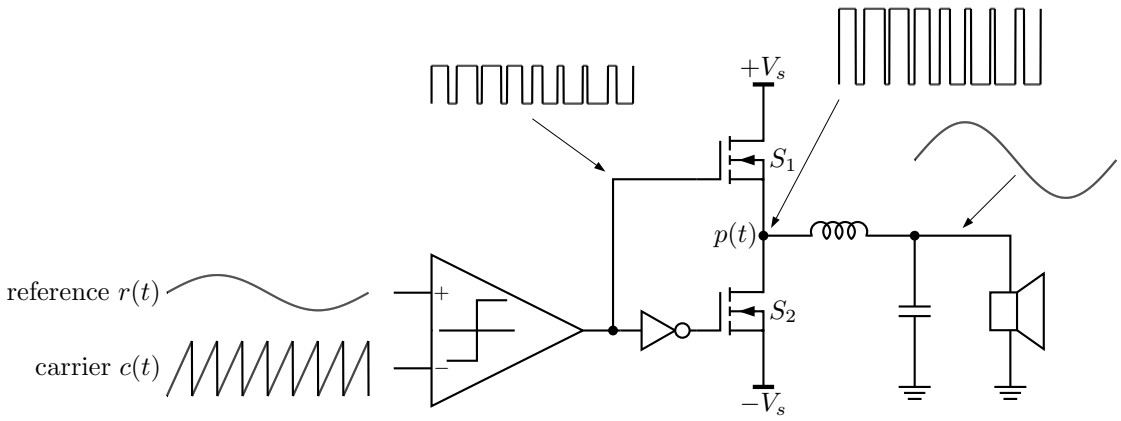


Figure 1.1: Basic class-D operation.

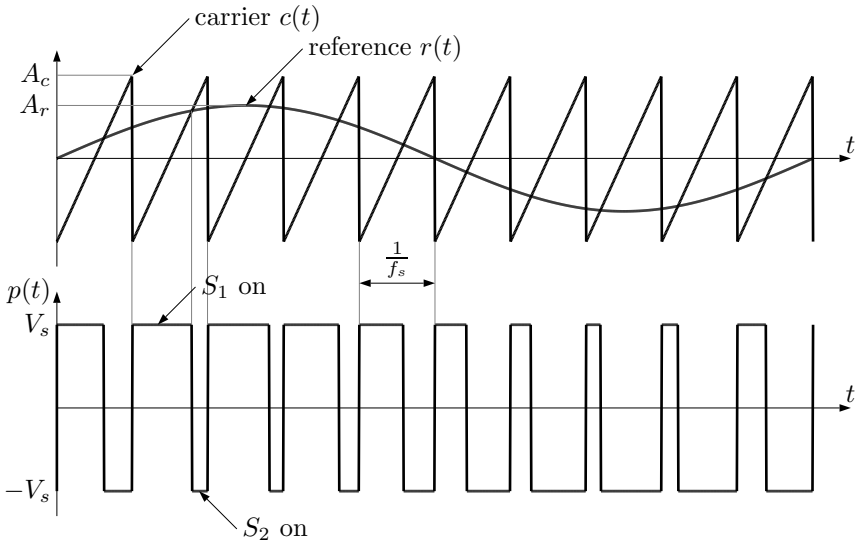


Figure 1.2: NSPWM waveforms for the converter of Figure 1.1.

Unfortunately, the basic class-D topology has some drawbacks. The basic class-D amplifier suffers from the following ailments that degrade sonic performance:

- Pulse timing errors (PTEs) and pulse amplitude errors (PAEs) due to non-ideal switching behaviour. This leads to distortion of the output signal.
- The amplitude of the output signal is modulated by the power supply. Hence power supply rejection is essentially zero.
- The frequency response of the demodulation filter is load dependent and the demodulation filter also contributes to distortion.

The distortion in a class-D power stage is usually dominated by the non-linear PTE caused by dead time [5], which is required to prevent cross-conduction of the switching devices. Decreasing the dead time results in lower distortion, but decreases the efficiency due to increased shoot-through currents.

A class-D amplifier also has the potential to generate significant electromagnetic interference (EMI) due to the high rate of change of voltages and currents in the power switching stage. Radiated EMI can be reduced by reducing the switching speed of the power switches, but this in turn increases PTE related distortion.

The only way to effectively address all of the problems associated with a class-D power stage is through the implementation of global feedback error control. If properly implemented, global negative feedback will mitigate power stage and output filter errors, improve power supply rejection and ensure a less load dependent frequency response. When feedback is applied we can tolerate a higher level of open loop distortion and consequently lower the switching speeds to reduce EMI. Furthermore, we can allow a longer dead time and thereby increase efficiency.

It should be noted, however, that closing a feedback loop around a pulse-width modulator is not without its problems. The comparator behaves like a sampling operation [1] and high-frequency components that are fed back through the loop can alias into the audio band. This has been a topic of much research and recently several techniques to mitigate this effect have emerged [6–9].

Closing a feedback loop around the output stage opens the door to another PWM scheme, which is self-oscillating modulation. A self-oscillating amplifier generates its own carrier by operating in a limit cycle [1]. This obviates the need for external carrier generator circuitry. However, the switching frequency of a self-oscillating amplifier is a function of modulation index. In multichannel audio systems the difference in switching frequency between channels can lead to audible beat tones.

At this point we should make a distinction between digital and analogue with regard to class-D amplifiers. Class-D amplifiers are sometimes referred to as digital amplifiers.

This term can be misleading since the power amplifier itself, consisting of the switching stage and demodulation filter, is inherently analogue and is delivering an analogue signal to the loudspeaker. We can make a distinction between analogue *controlled* and digitally *controlled* class-D amplifiers. In a digitally controlled class-D amplifier the gate signals of the switches are generated digitally. Note that a digitally controlled class-D amplifier also suffers from all the non-idealities mentioned earlier, and as such will benefit greatly from global feedback. Global feedback can be implemented in a digitally controlled class-D amplifier through analogue-to-digital conversion of the amplifier output voltage. Such a design can achieve very good performance, but performance is limited by the analogue-to-digital converter in the feedback path [2].

1.2 Thesis Objectives

The objective of this thesis is to design, simulate, build and measure a high-performance, analogue controlled, clocked (ie. not self-oscillating), class-D amplifier. This is a fairly general statement, but the following is specifically required:

- The design should make use of discrete-time modelling techniques.
- The possibility should be investigated of adapting the method documented in [10] to stabilise a high-order loop during over-modulation for self-oscillating modulators, to clocked modulators.
- The ripple compensation technique described in [2] should be implemented.

In addition to the above, the measured results must be compared to theoretical expectations. In this context, high-performance refers to the audio performance of the amplifier and not the efficiency or EMI performance. The primary research focus is on the control method and not the power converter itself. Note that the performance of the control method is evaluated based on its ability to improve the performance of the amplifier compared to open loop class-D operation, and not on the absolute value of the closed-loop performance measurements.

That being said, we would like the closed-loop amplifier to compare favourably with a high-performance linear amplifier. The following performance targets are set for the closed-loop amplifier:

- Total harmonic distortion and noise (THD+N) $\leq 0.005\%$ in the audio band, and not increasing significantly with frequency inside the audio band.
- Frequency response flat to within 0.1 dB in the audio band.
- Output impedance ≤ 50 mΩ in the audio band.

1.3 Thesis Outline

Chapter 2 discusses the literature that forms the foundation for the remainder of the thesis. This includes, among other topics, the discrete-time modelling of continuous-time PWM loops and ripple compensation.

Chapter 3 covers the design of the class-D output stage, which includes the power switching stage and associated circuitry, and the demodulation filter. Measurements of the open loop class-D amplifier are presented.

Chapter 4 discusses the design of an FPGA-based carrier generator. Carrier data is generated off-line and stored in a lookup table in the FPGA. The data is then clocked to a high-speed digital-to-analogue converter.

Chapter 5 concerns the development of the control loop topology. The analogue circuitry that is required to implement the control loop is discussed and the complete continuous-time loop is presented.

In **Chapter 6** the continuous-time control loop developed in Chapter 5 is converted to the z-domain through the impulse invariant transform. An expression fot the equivalent gain of the comparator is derived by means of Fourier series. Important transfer functions are presented.

Chapter 7 covers the detail design of the control loop. The load that the loudspeaker presents to the amplifier, and its effect on stability, is investigated. A control loop is designed that provides at least 50.8 dB rejection of output stage errors in the audio band.

It should be noted that Chapter 5, Chapter 6 and Chapter 7 are very closely knit and essentially form one unit.

Chapter 8 presents simulation results of the control loop that is designed in the preceding chapters. The simulation results verify the correct operation of the control loop.

Chapter 9 presents and discusses measurements of the complete amplifier. The measurements are compared to theoretical expectations. It is confirmed that the control method effectively mitigates the non-idealities of the open loop system.

This thesis ends with a conclusion in **Chapter 10**. Recommendations for further research are also given.

Chapter 2

Literature Review

This chapter reviews the literature that forms the foundation of the remainder of the thesis.

2.1 The Harmonics of Ideal PWM

In [11] it is shown that an ideal naturally sampled single-sided pulse-width modulating (NSSSPWM) waveform $p(t)$ that is generated by comparing a reference signal $f(t)$ with a sawtooth carrier $st(\omega_s t)$ can be decomposed as the sum of three functions

$$p(t) = f(t) - st(\omega_s t) + st\left(\omega_s t - \pi f(t) + \pi\right), \tag{2.1.1}$$

where

$$st(\theta) = \frac{1}{\pi}\theta \tag{2.1.2}$$

over the interval $-\pi \leq \theta \leq \pi$. The last term in (2.1.1) can be written in terms of its Fourier series expansion to obtain

$$p(t) = f(t) - st(\omega_s t) + \frac{j}{\pi}\sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \frac{1}{m} e^{jm(\omega_s t - \pi f(t))}. \tag{2.1.3}$$

For the special case where $f(t) = m_a \cos(\omega_0 t)$, we can use the Jacobi-Anger identity

$$e^{-jm\pi m_a \cos(\omega_0 t)} = \sum_{n=-\infty}^{\infty} j^n J_n(-m\pi m_a) e^{jn\omega_0 t} \tag{2.1.4}$$

to rewrite (2.1.3) as

$$p(t) = f(t) - st(\omega_s t) - \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{m\pi} J_n(m\pi m_a) \sin\left((n\omega_0 + m\omega_s)t - \frac{n\pi}{2}\right), \tag{2.1.5}$$

where $J_n(x)$ is the n'th order Bessel function of the first kind [11]. Equation (2.1.5) is the well-known double Fourier series expression for a NSSSPWM waveform [12]. Equation (2.1.5) shows that the PWM waveform $p(t)$ contains the following signal components:

- The original reference waveform $f(t)$.
- An inverted sawtooth $-st(\omega_s t)$.
- Sine and cosine components at integer combinations of the reference waveform frequency and the carrier frequency. These primarily manifest as side-band harmonics centred around the carrier harmonics, though some will add to (or subtract from) the carrier harmonics.

Figure 2.1 shows the spectrum of $p(t)$ with a 1 Hz reference signal for a modulation index of $m_a = 0.8$ and a frequency modulation index of $m_f = 50$. It should be clear that, in ideal PWM, only the side-band components contribute to distortion in the audio band, provided that the switching frequency is outside the audio band. Increasing m_f will reduce the magnitude of the side-band components in the audio band.

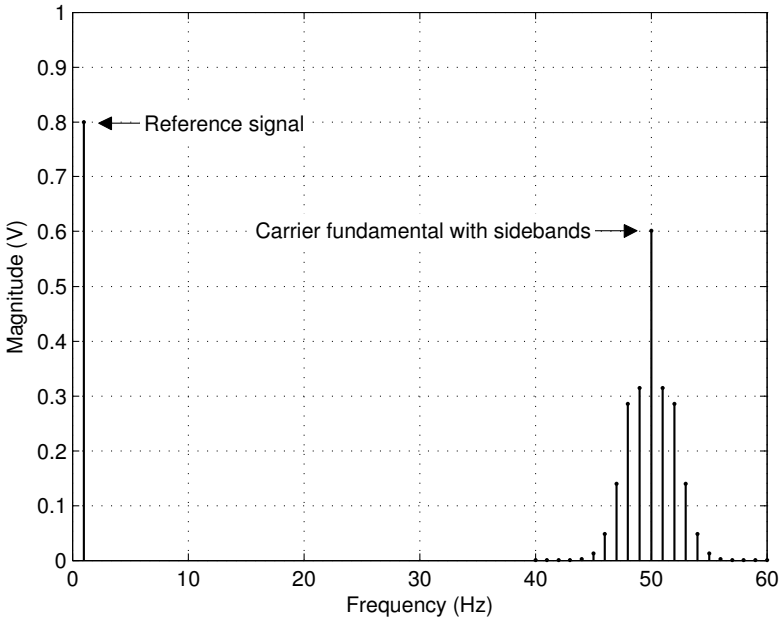


Figure 2.1: Calculated magnitude spectrum of ideal NSSSPWM for $m_a = 0.8$ and $m_f = 50$.

Note that the side-bands in Figure 2.1 decay fairly rapidly. However, non-ideal effects like dead-time and finite switching times will cause the side-bands to decay less rapidly than for ideal PWM [5].

2.2 Class-D Distortion Mechanisms

In an ideal NSPWM class-D amplifier output stage, the only contribution to distortion in the audio band is the carrier side-bands [5]. However, several distortion mechanisms are

present in a practical, non-ideal, class-D amplifier. This section gives a brief overview of the distortion mechanisms present in a class-D amplifier.

2.2.1 Dead Time

As mentioned earlier, the switches in a class-D power stage are switched complementary. However, A MOSFET is not an ideal switch and cannot switch from the on to off state and vice versa instantaneously. For a small time the MOSFET will operate in its linear region, having both a current through it and a voltage across it. To prevent both switches conducting simultaneously during a switching transition, the modulator waits for a time t_{dt} after one switch is off before switching on the next switch. The time in which both switches are off is known as the dead time. Dead time leads to pulse-timing errors (PTEs), and is a major source of distortion in a class-D power stage.

Figure 2.2 shows a simplified half-bridge inverter with ideal switches S_1 and S_2, and ideal diodes D_1 and D_2. Figure 2.3 shows the gate signals of the switches and the unfiltered output voltage v_P. The ideal gate and output waveforms are shown in grey.

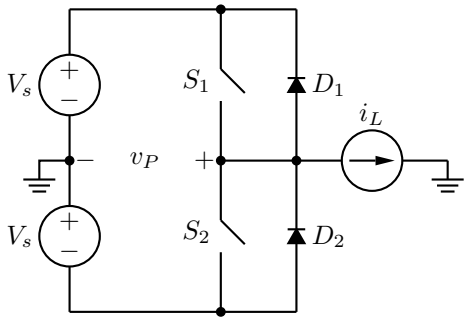


Figure 2.2: Simplified half-bridge inverter with current-source load.

Consider the case when S_1 switches from off to on and S_2 from on to off. If $i_L > 0$, D_2 conducts during the dead time interval and the output voltage is $v_P = -V_s$, while the ideal output voltage at this time is $v_P = V_s$. If $i_L < 0$, D_1 conducts during the dead time interval and the output voltage is $v_P = V_s$, which is the correct output voltage.

In a similar manner, when S_1 switches from on to off and S_2 from off to on the output voltage is correct when $i_L > 0$, and incorrect when $i_L < 0$.

At small values of m_a the inductor current changes polarity twice during a switching cycle and the effect of dead time is reduced to only a time delay of t_{dt}. At larger values of m_a the inductor current polarity is primarily determined by the polarity of the reference signal and is distinctly positive or negative for several switching cycles at a time. The output voltage error now changes with the polarity of the reference signal, which results in distortion of the output waveform inside the audio band.

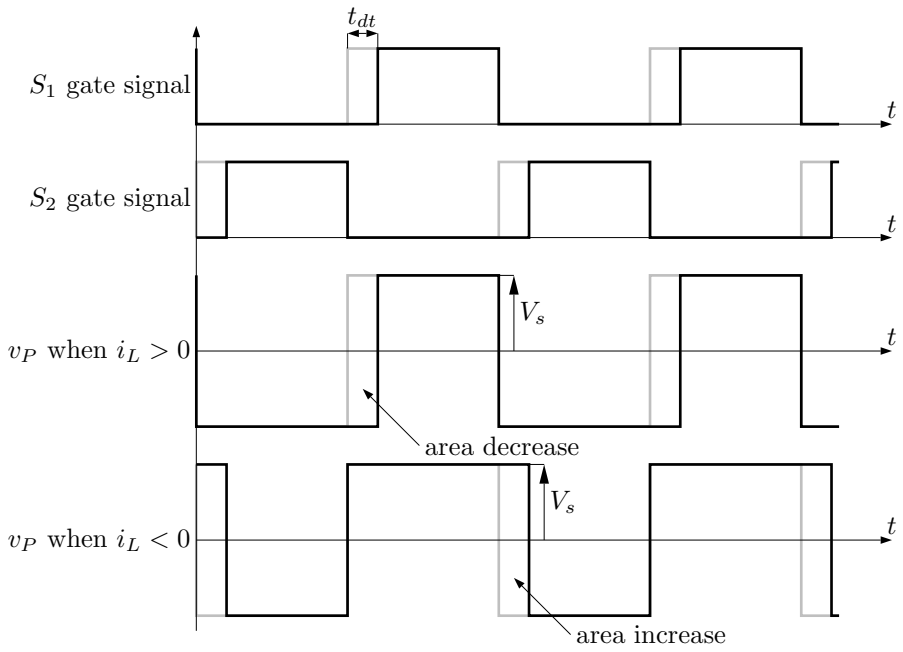


Figure 2.3: The effect of dead time on converter waveforms. Ideal waveforms are shown in grey.

Viewed in isolation, dead time contributes only to odd harmonic distortion in the audio band. However, in [5] it was shown that introducing dead time also increases the magnitude of the side-band switching harmonics inside the audio band for larger values of m_a. Distortion due to dead time increases for increasing values of t_{dt}. Also note that dead time distortion, and distortion due to PTEs in general, increase with an increase in switching frequency.

2.2.2 MOSFET Turn-On and Turn-Off Delays and Non-Zero Switching Transitions

The turn-on and turn-off delays of a MOSFET is a function of the current through the MOSFET [5]. Since the current changes with the reference signal these delays will manifest as PTEs. At low values of m_a, when the current changes polarity twice during a switching cycle, the change in turn-on on turn-off delays is continuous. This continuous change in delays results in even and odd baseband harmonics that decay fairly rapidly with frequency. However, at larger values of m_a when the inductor current is distinctly positive or negative for several switching cycles at a time, the change in delays is discontinuous. The baseband harmonics do not decay as rapidly as was the case with small values of m_a, and results in a significantly higher level of distortion.

As with dead time, the turn-on and turn-off delays also increase the magnitude of the side-band switching harmonics in the audio band at larger values of m_a. Distortion

increases for longer delay times.

Non-linear non-zero switching transitions affect distortion in a similar manner to turn-on and turn-off delays [5].

2.2.3 Parasitics and Reverse Recovery

In [5] it was shown that the ringing of the pulse output waveform due to circuit parasitics and reverse recovery leads to pulse amplitude errors (PAEs), but contributes negligible distortion compared to the PTEs mentioned above. That being said, ringing of the pulse waveform increases radiated EMI and can therefore indirectly increase the distortion in an analogue modulator through self-pollution.

2.2.4 Self-Pollution

The PTEs discussed above can be minimised by increasing the switching speed. However, increasing the switching speed results in higher values of $\frac{di}{dt}$ and $\frac{dv}{dt}$ in the PWM waveform before the demodulation filter. This leads to increased radiated EMI, which can contaminate the signals at the comparator input in an analogue modulator. This can potentially lead to severe distortion of the output waveform, especially at larger values of m_a. A decrease in open-loop distortion due to faster switching times is therefore partially offset by an increase in distortion due to self-pollution.

Note that in an amplifier with a digital modulator, self-pollution will contribute much less to open-loop distortion. Indeed, it was found that a power stage with little regard for EMI performance yielded good distortion measurements in a digital feedback design [2], but was almost completely useless in an analogue control loop. In an analogue modulator the EMI performance of the amplifier directly influences the audio performance. Even though this design is an experimental system and does not officially have to pass any EMI standards, careful attention still has to be paid to EMI performance, if only to maximise the audio performance.

2.2.5 Bus Pumping

In a half-bridge converter the situation can occur where there is a net flow of energy from the load back to a supply rail [13]. Consider the circuit of Figure 2.4. We assume that the filter capacitor C is large enough that the output voltage v_o is approximately constant over a switching cycle. Figure 2.5 (a) shows the idealised inductor and supply current waveforms for a duty cycle of $D = 0.5$ over a single switching cycle. The average inductor current, and load current, is zero. Current flows to and from both sources, but the net energy transfer is zero.

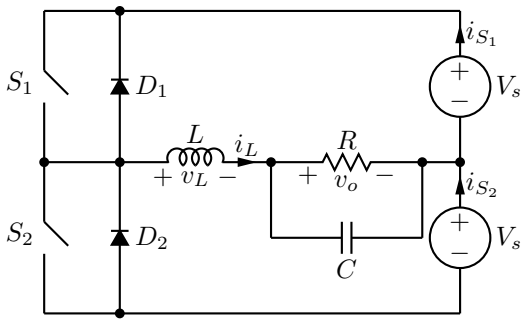


Figure 2.4: Simplified half-bridge converter.

Figure 2.5 (b) shows the same waveforms for a duty cycle of $D = 0.75$. The average inductor current is now greater than zero and energy flows from the positive supply to the load. However, it is observed that there is also a net flow of energy into the negative voltage supply. If the power supply has no way to absorb the energy, as is the case with a passive power supply and most linear supplies, the bus voltage will increase [13]. This is known as "bus pumping". The open-loop gain of the amplifier is proportional to the power supply voltage. If bus pumping causes significant supply voltage fluctuations, this will lead to distortion. However, with a large storage capacitance in the power supply and a control loop that provides error rejection in the audio band the effect of supply pumping should be negligible. This, of course, assumes that the program material does not contain significant power at very low frequencies.

In open-loop tests the effect of bus pumping should be kept in mind. Contrary to an ideal PWM modulator, in a practical amplifier it is unlikely that a carrier with no DC offset will result in a PWM output signal with no DC offset. This is due to the difference in turn-on and turn-off delay times between the top and bottom power switches. In open-loop tests the carrier should be tuned such that the switching stage output signal does not have a significant DC offset, otherwise the supply voltage will increase and the amplifier might get damaged.

2.2.6 Demodulation Filter

The passive components of the demodulation filter are not ideal and can contribute to distortion. Due to the high frequency power signal that enters the demodulation filter, it is necessary to use a ferrite core inductor. Unfortunately a ferrite core is non-linear [14]. The inductor will become increasingly non-linear as the flux density in the core nears the saturation flux density of the core material.

It should be noted that the physical design of the output filter will also have an influence on distortion. The parasitic parallel capacitance of the filter inductor and the parasitic series inductance of the filter capacitor will cause the filter to behave like a high-

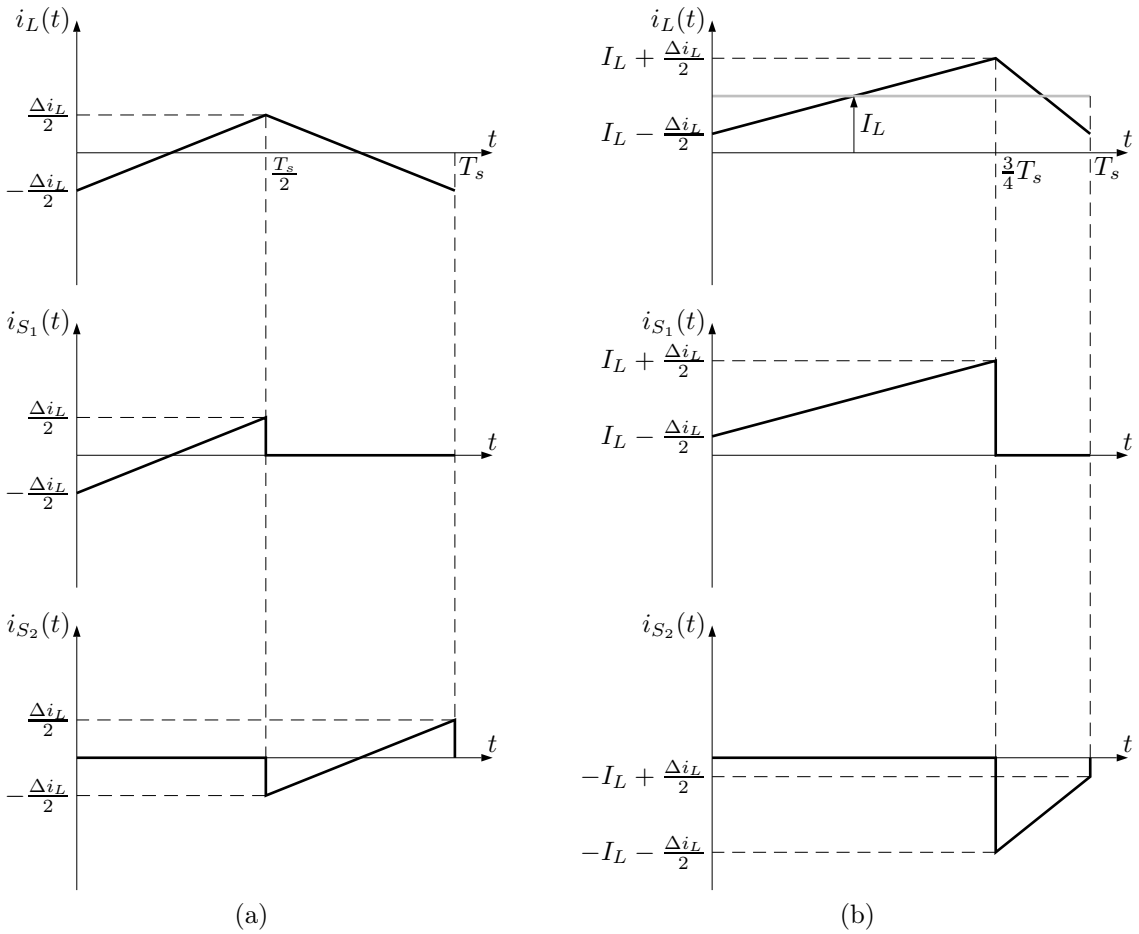


Figure 2.5: Idealised inductor and supply current waveforms for (a) $D = 0.5$ and (b) $D = 0.75$.

pass filter at higher frequencies. If these parasitics are not minimised, the edges of the PWM waveform will show up as voltage spikes in the amplifier output waveform. These high-frequency spikes will radiate off attached cables, leading to increased self-pollution.

2.2.7 Distortion Related to Feedback Error Control

All of the aforementioned distortion mechanisms can be mitigated by applying global negative feedback. However, closing a feedback loop around a class-D power stage introduces additional distortion mechanisms that are not present in an open loop system [7]. If these sources of distortion are not mitigated, they can dominate the overall distortion level.

In [1] it was shown that the comparator is effectively a sampling operation. The PWM waveform that is fed back through the loop to the comparator input contains harmonics of the switching frequency and their associated side-bands. When this signal is sampled at the comparator input, some of these components will alias into the audio band.

Furthermore, the effective comparator gain is a function of the slope of the comparator input signal at the sampling instance [1]. Since the feedback ripple signal is a filtered

PWM waveform, its shape depends on duty cycle. It therefore follows that the slope of the signal at the comparator input, and hence the comparator gain, will depend on duty cycle. This is an additional non-linearity.

Distortion due to ripple feedback can be greatly minimised by implementing the ripple compensation technique described in Section 2.4.

2.3 Discrete-Time Modelling of Continuous-Time Pulse-Width Modulator Loops

In an ideal pulse-width-modulator, the comparator is the only non-linear element and is traditionally linearised into an equivalent gain [14]. However, the linearised continuous-time model fails to account for the high frequency behaviour of the comparator, and stability margins cannot be determined accurately [1, 15].

A very accurate model in which the comparator is modelled as a sampling operation and the continuous-time loop is converted to discrete-time was presented in [1] and [15]. This model accounts for non-linear effects of pulse-width modulation like aliasing and the formation of image components. Furthermore, the comparator frequency response is accurately modelled to above the switching frequency and loop stability can be determined more accurately.

2.3.1 Small-Signal Model of the Ideal Comparator

A small-signal model describes the AC behaviour of a system linearised around a steady-state operating point. A pulse-width modulator operates in steady-state when the modulator output is a 50% duty cycle periodic pulse waveform. Figure 2.6 shows the conceptual small-signal model of an ideal comparator [1]. The small-signal model consists of two identical comparator models. One receives a periodic carrier $c(t)$ as input, while the other receives the same periodic carrier with a small superimposed perturbation signal $y(t)$. The comparator's small-signal response is the difference between the outputs of the two comparators. The ideal comparator and power stage is modelled as a gain G followed by saturation to the power stage supply voltage V_{DD}.

Figure 2.7 shows the waveforms associated with the small-signal model. The carrier $c(t)$ is periodic with frequency f_{sw} and has two uniformly spaced zero crossings per period. For a short time Δt at the zero crossings of $c(t)$ the comparator acts as a linear gain G. Outside this time interval the comparator is saturated and cannot respond to a change in input. The time interval is approximately

$$\Delta t \approx \frac{2V_{DD}}{|\dot{c}_0|G}, \tag{2.3.1}$$

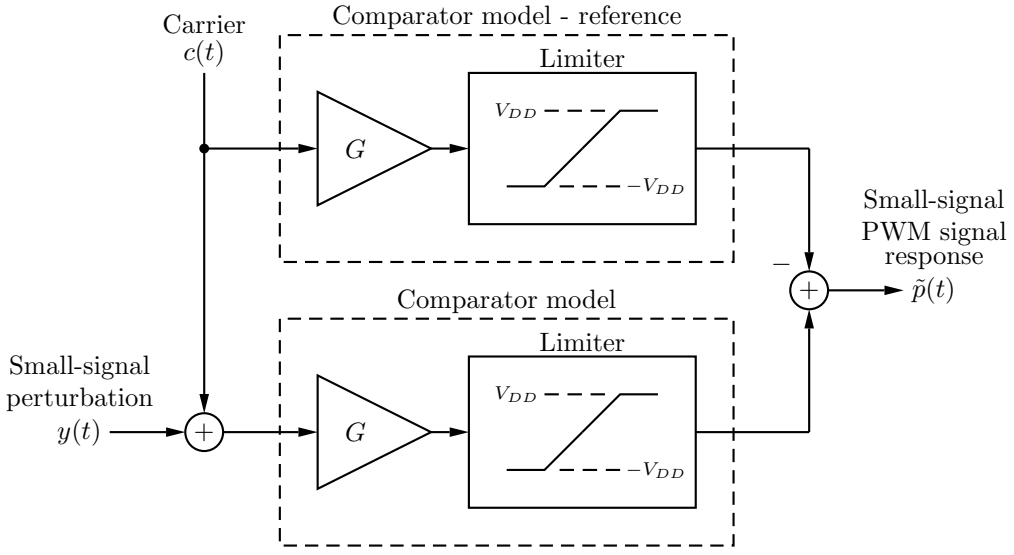


Figure 2.6: Small-signal comparator model [1].

where $\dot{c}_0$ is the slope of the carrier signal $c(t)$ at a zero-crossing. The small-signal PWM response $\tilde{p}(t)$ is effectively the product between $y(t)$ and a pulse train $g(t)$ of amplitude G and pulse duration Δt [1].

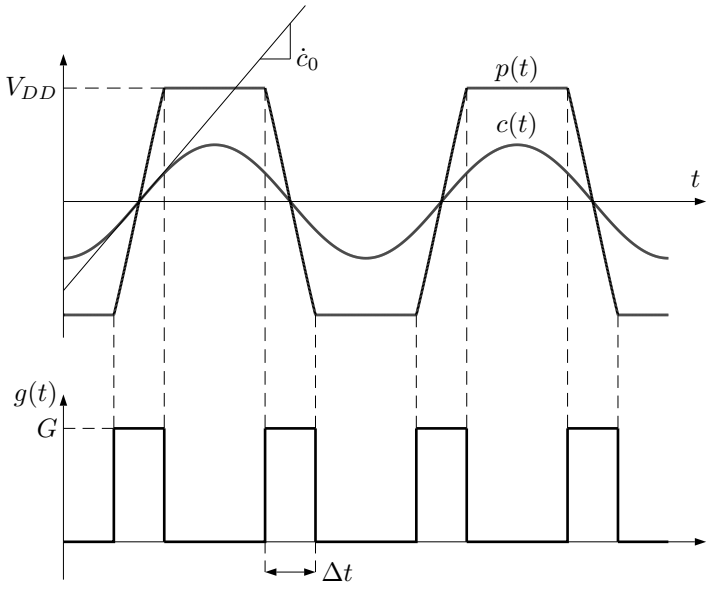


Figure 2.7: Comparator waveforms [1].

The area of each pulse of $g(t)$ is

$$A = G\Delta t \approx \frac{2V_{DD}}{|\dot{c}_0|}. \tag{2.3.2}$$

Note that the area A of a pulse of $g(t)$ is independent of the magnitude G of a pulse and that $\Delta t \approx 0$ for large values of G. The periodic pulse waveform $g(t)$ can therefore be

approximated by a Dirac comb of frequency $2f_{sw}$ [16]. Multiplication by a Dirac comb in the time domain is equivalent to sampling. The comparator therefore acts as a sampling operation with sampling frequency $2f_{sw}$, followed by a gain K which is the mean value of $g(t)$:

$$K = 2f_{sw}A = \frac{4V_{DD}f_{sw}}{|\dot{c}_0|}. \tag{2.3.3}$$

In the case of natural sampling PWM where the carrier $c(t)$ is a triangle or sawtooth wave with amplitude A_c, the comparator gain K is

$$K = \frac{V_{DD}}{A_c}. \tag{2.3.4}$$

2.3.2 Closed-Loop Small-Signal Model

Figure 2.8 shows the comparator model embedded in a feedback loop. $H_s(s)$ is a loop filter and $e_c(t)$ and $e_p(t)$ model noise and distortion that is added at the comparator input and output, respectively.

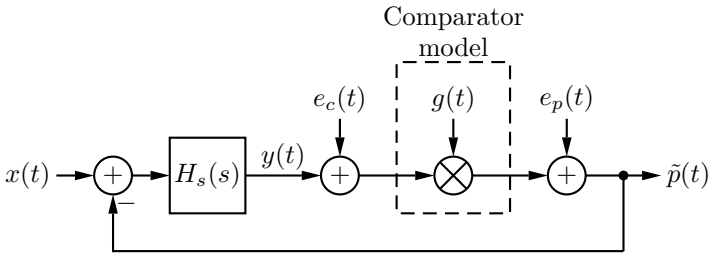


Figure 2.8: Comparator model embedded in a feedback loop.

The small-signal output of the comparator and power stage $\tilde{p}(t)$ approximates a series of delta impulses, or a sampled signal. Since the loop filter is fed by a sampled signal and its output is again sampled by the comparator, we only care about the loop filter response at the sampling instances. Hence the continuous-time loop filter can be replaced by a discrete-time equivalent, as shown in Figure 2.9.

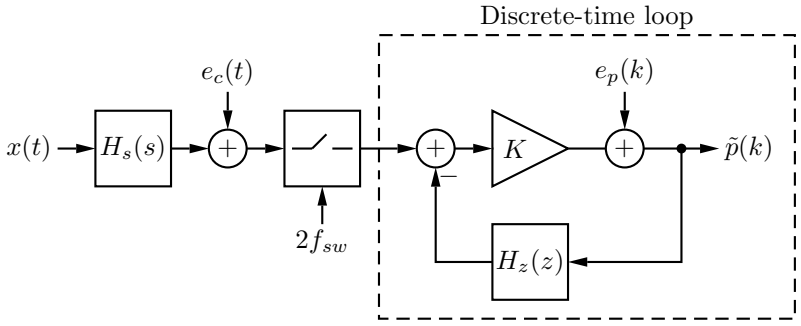


Figure 2.9: Discrete-time comparator model embedded in a feedback loop.

The input reference signal $x(t)$ propagates through the loop filter $H_s(s)$ before reaching the comparator input. Therefore the input reference signal $x(t)$ has to be filtered in continuous-time by $H_s(s)$ before sampling [1]. Similarly, $e_c(t)$ is added in continuous-time. The error source $e_p(t)$ represents timing errors in the power stage and manifests as errors in the values of the Dirac impulses of $\tilde{p}(t)$. Hence the power stage error source $e_p(t)$ is added directly to the discrete-time loop as $e_p(k)$. The signal $\tilde{p}(k)$ is a discrete-time signal that represents the deviation of the modulator from the steady-state operating point.

2.3.3 Conversion to the Z-Domain

As mentioned earlier, the continuous-time loop filter is fed by a sampled signal (a series of Dirac impulses) and its output is again sampled. This operation is similar to the impulse-invariant method of discretisation, which involves taking the z-transform of the sampled impulse-response of a system [17]. Consequently, the continuous-time loop filter $H_s(s)$ can be converted to its discrete-time equivalent $H_z(z)$ through the impulse invariant transform.

Since the real system has to be causal, the comparator can only respond to the loop's response to a previous output sample. This means that the actual system always has at least a one sample delay. This can be taken into account in the impulse-invariant transform by removing the impulse response sample at time zero [1]:

$$H_z(z) = \hat{H}_z(z) - \hat{h}_z(k = 0), \tag{2.3.5}$$

where $\hat{H}_z(z)$ is the direct impulse-invariant transform of $H_s(s)$. In Section 6.2 a slightly different approach to the impulse-invariant transform is suggested.

2.3.4 Effect of Feedback Ripple on Comparator Gain

The effective comparator gain K depends on the slope of the comparator input signal at zero crossings. The large-signal output of the real system is a PWM waveform. The PWM signal is filtered by the loop filter prior to reaching the comparator input and causes a periodic ripple signal $r(t)$ to be added to the carrier. The slope of the comparator input signal at zero-crossings is the sum of the slopes of the carrier and ripple signal. For a triangle wave carrier with amplitude A_t, the comparator gain K is

$$K = \frac{V_{DD}}{A_t + \frac{\dot{r}_{0r-}}{4f_{sw}}}, \tag{2.3.6}$$

where $\dot{r}_{0r-}$ is the slope of the ripple signal $r(t)$ just prior to a rising edge zero crossing of the comparator [1]. It should be noted that the ripple feedback signal reduces the effective comparator gain relative to open-loop operation.

2.4 Ripple Compensation

Closing a feedback loop around a PWM modulator introduces distortion mechanisms that are not present in the open-loop system. The PWM output signal contains components at multiples of the carrier frequency, as well as additional components centred around these. When the output is fed back through the loop to the comparator input, some of these components will be aliased into the audio band due to the sampling nature of the comparator [1, 7, 15]. Aliased components that are harmonically related to the input signal will manifest as harmonic distortion.

In [7] a so-called minimum-aliasing-error loop filter is discussed that reduces the effect of feedback ripple aliasing by cancelling parts of the aliasing error. In [6] the non-linearity is reduced by dynamically modifying the symmetry of the carrier to counteract the phase shift in the effective sampling instances due to ripple feedback. In [8] and [18] a simple and very effective ripple compensation method is presented to reduce the effect of ripple aliasing in pulse-width modulators. A great benefit of the ripple compensation technique is that it gives the designer freedom in designing the transfer function and topology of the control loop. This method is implemented in a digitally-controlled PWM amplifier with state-of-the-art performance in [2]. This section describes the basic operation of the ripple compensation strategy discussed in [2, 8, 18].

Figure 2.10 shows the simplest ripple compensation implementation for a NSSSPWM loop. The loop filter $G(s)$ provides gain for error rejection. The feedback signal is modified

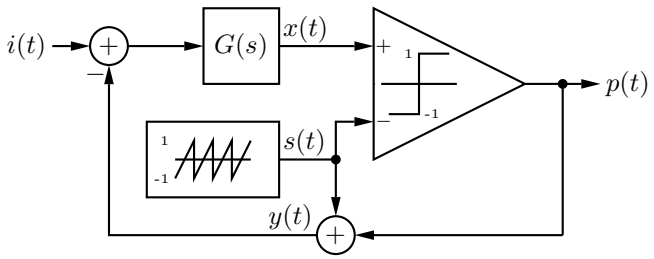


Figure 2.10: Simple PWM feedback loop with ripple compensation [2].

by adding the sawtooth carrier $s(t)$ to the PWM output $p(t)$. This has the effect of cancelling the unmodulated edge of the PWM waveform, thereby making the ripple signal reaching the comparator input largely independent of duty cycle and reducing the effect of the ripple feedback to only a DC offset. From a frequency domain perspective, this means that only components related to the carrier are aliased into the audio band.

Figure 2.11 shows the waveforms associated with the modulator loop of Figure 2.10 for a first-order integrating loop filter. The signal $y(t)$, which is the sum of the PWM

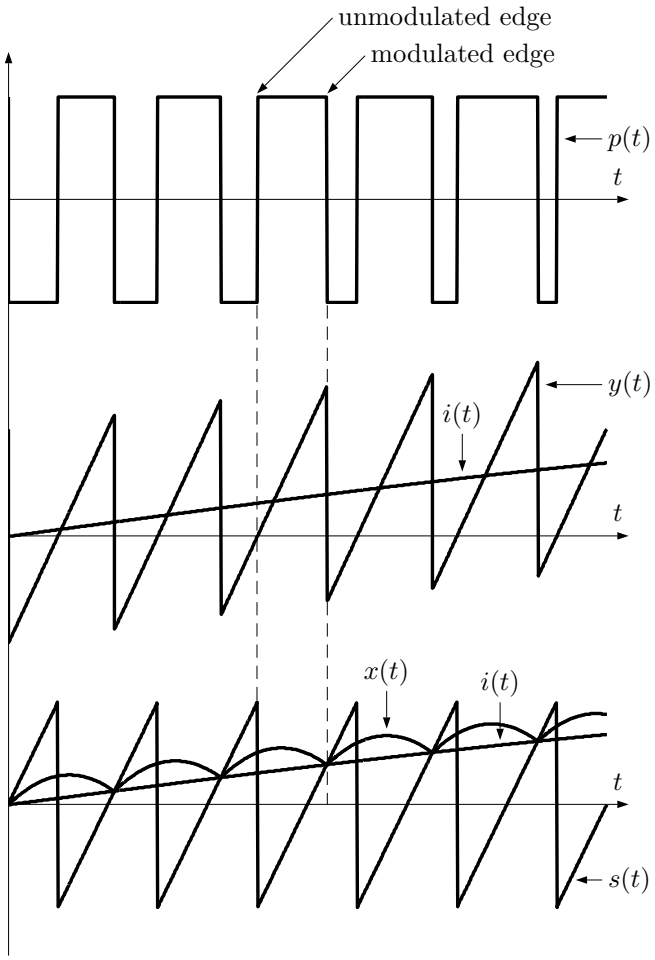


Figure 2.11: Ripple compensation waveforms for a first-order loop [2].

signal $p(t)$ and the carrier $s(t)$, is a sawtooth waveform of which the time average over a switching period is equal to that of $p(t)$.

The feedback loop ensures that the crossings of $i(t)$ and $s(t)$ coincide with the crossings of $x(t)$ and $s(t)$. It is observed that the ripple component of $x(t)$ is largely independent of the average value of $x(t)$. This greatly reduces the non-linearity associated with ripple aliasing. It was noted in Section 2.3 that the effective comparator gain is a function of the slope of the feedback ripple signal which, without ripple compensation, depends on the duty cycle. Consequently, ripple compensation also makes the comparator gain independent of duty cycle.

Figure 2.12 shows three equivalent implementations of the ripple compensation technique. Figure 2.12 (a) is a direct adaptation of Figure 2.10, with the inclusion of an equivalent power stage gain A and a demodulation filter $F(s)$. However, the implementation of Figure 2.12 (a) is not feasible, since it involves adding an amplified carrier to the PWM signal before the demodulation filter. Figures 2.12 (b) and (c) are equivalent to Figure 2.12 (a), but can be implemented practically. The implementation of Figure 2.12 (c)

is especially suitable if the carrier is generated digitally, since a pre-filtered carrier can be generated off-line and stored in a lookup table.

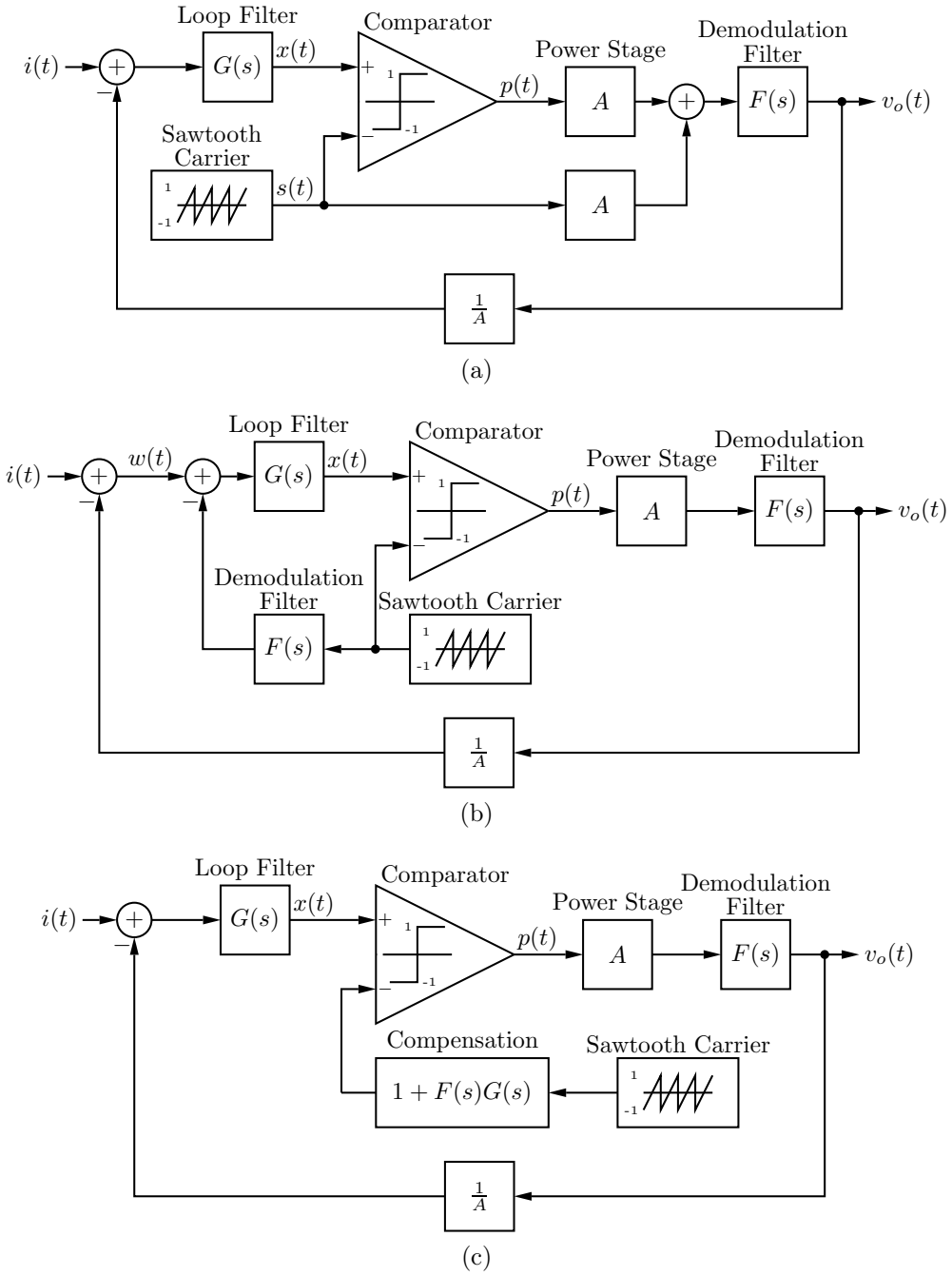


Figure 2.12: Three equivalent implementations of the ripple compensation technique obtained through block diagram manipulation [2].

2.5 Stabilising a High-Order Modulator Under Overload Conditions

2.5.1 The Deviation Detector

When a loop is optimised for gain, it will tend to be conditionally stable. A conditionally stable loop will become unstable when loop gain collapses, as is the case during over-modulation. This is not a problem for a digital controller, in which the input signal range is a known variable and can be restricted to a value that would not lead to over-modulation.

A method to stabilize an over-modulated conditionally stable loop is to modify the loop to become unconditionally stable during over-modulation. This can be achieved by reducing the loop order during over-modulation [10]. In a higher-order loop, the loop filter will typically consist of a chain of integrators [2, 19–21]. When over modulation occurs, the difference between input and output is large. Since the amplifier output during over-modulation is primarily DC, the integrators will produce large output signals. One method of returning the loop to a stable condition when loop gain collapses is to limit the voltage range of each integrator [20]. When an integrator saturates, the loop order is effectively decreased by one. The loop should be designed to be unconditionally stable when the order is reduced.

However, there is a problem with this method. Saturating the integrators is only effective if the integrator output is limited to a level significantly smaller than the unstable output level [10]. The problem is that the integrator output of an unstable amplifier with no input signal could be smaller than that of a stable amplifier under maximum modulation [10]. Hence the integrators will saturate during normal operation, reducing performance.

In [10] a method was proposed to stabilize a conditionally stable loop during over-modulation, without saturating the integrator during normal operation. The method was specifically applied to a self-oscillating class-D device, but it can be adapted for a clocked modulator loop.

Figure 2.13 shows a generic feedback loop with loop filter $H(s)$ and inverting output stage $K(s)$. The error term $E(s)$ represents output stage errors.

The output of the loop filter is given by

$$X(s) = \frac{H(s)}{1 - H(s)K(s)}[V_i(s) + E(s)]. \tag{2.5.1}$$

Equation (2.5.1) shows that the loop filter output contains components from both the output stage error and the loop input. When the modulation index is large, the input

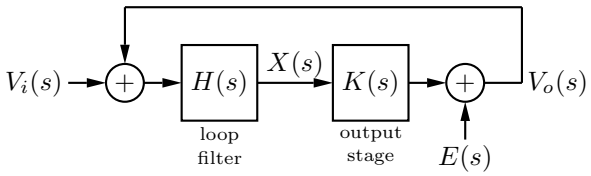


Figure 2.13: Generic output stage embedded in a feedback loop.

term $V_i(s)$ will dominate the loop filter output. The goal is to make the loop filter output independent of the input signal.

Now consider the modified loop of Fig. 2.14. $K'(s)$ is a deviation detection transfer function that approximates the transfer function of the output stage $K(s)$. Assuming $K'(s)$ matches $K(s)$ well, during stable operation the only difference between the output of $K(s)$ and $K'(s)$ is the small error term. The loop filter output can therefore be limited to a very low level. The low saturation limit also has the benefit of improving clip-recovery. When over-modulation or instability occurs, the difference between the output of $K(s)$ and $K'(s)$ is large, and the loop filter saturates. From a dynamic perspective the saturated loop filter acts as an open circuit. The output stage now receives only the direct input signal. When the amplifier comes out of over-modulation the loop filter resumes normal operation.

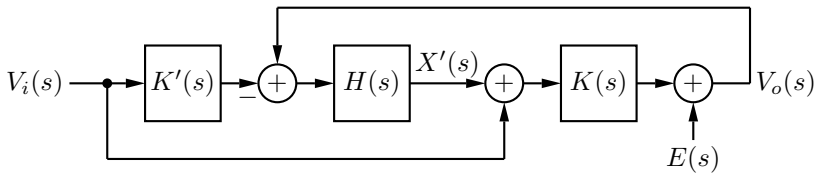


Figure 2.14: Modified control loop with deviation detection filter.

The output of the loop filter in Fig. 2.14 is given by

$$X'(s) = \frac{H(s)}{1 - H(s)K(s)}\Big(V_i(s)[K(s) - K'(s)] + E(s)\Big). \tag{2.5.2}$$

Clearly, if $K'(s)$ approximates $K(s)$ well, the loop filter output will consist primarily of components related to the output stage error term.

For this method to work reliably we need $K'(s)$ to approximate $K(s)$ accurately in the audio band. However, if the output stage $K(s)$ is a switching power stage followed by a demodulation filter the frequency response will vary depending on load. To remedy this, a simple passive lead network is added around the switching stage and output filter, as depicted in Figure 2.15. This circuit replaces $K(s)$ in Figure 2.14. The amplifier now has two feedback loops: an unconditionally stable inner loop to make the frequency response

of the power stage and demodulation filter insensitive to load variations, and an outer loop to increase loop gain in the audio band.

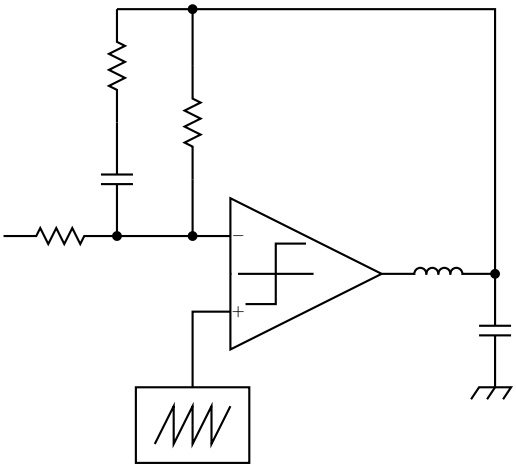


Figure 2.15: Output stage with passive lead network.

Note that any control network that provides enough loop gain to make the frequency response of the output stage relatively insensitive to load variations and is unconditionally stable will be sufficient for the inner loop. Figure 2.15 simply shows a very simple implementation.

2.5.2 Loop Filter Saturation

Saturation of the loop filter can be implemented in several ways [10]. An operational amplifier (op-amp) loop filter has an inherent saturation limit due to its finite output voltage swing. Scaling the system gains such that the loop filter output voltage is large enough to operate close to this saturation limit is not practical. The op-amp closed-loop gain will have to be very large, and the op-amp itself will contribute significantly to distortion.

Another method is to place back-to-back zener diodes in the op-amp feedback path [20]. However, the non-linear capacitance and leakage current of the zener diodes will introduce distortion even if the clipping circuit is not operating.

Figure 2.16 shows an alternative limiting circuit. The loop filter is shown as a simple active RC integrator, but the principle applies to any inverting op-amp circuit. If the op-amp output voltage is positive and high enough Q_3 will start to turn on, sinking collector current through R_1. The resultant voltage drop across R_1 turns on the current mirror consisting of Q_1 and Q_2. The current flowing from the collector of Q_1 into the virtual ground node of the op-amp reduces the magnitude of the current flowing through the feedback impedance, thereby reducing the magnitude of the op-amp output voltage.

Operation is similar for a negative op-amp output voltage. This circuit is not as simple as the zener limiter, but its distortion performance is superior.

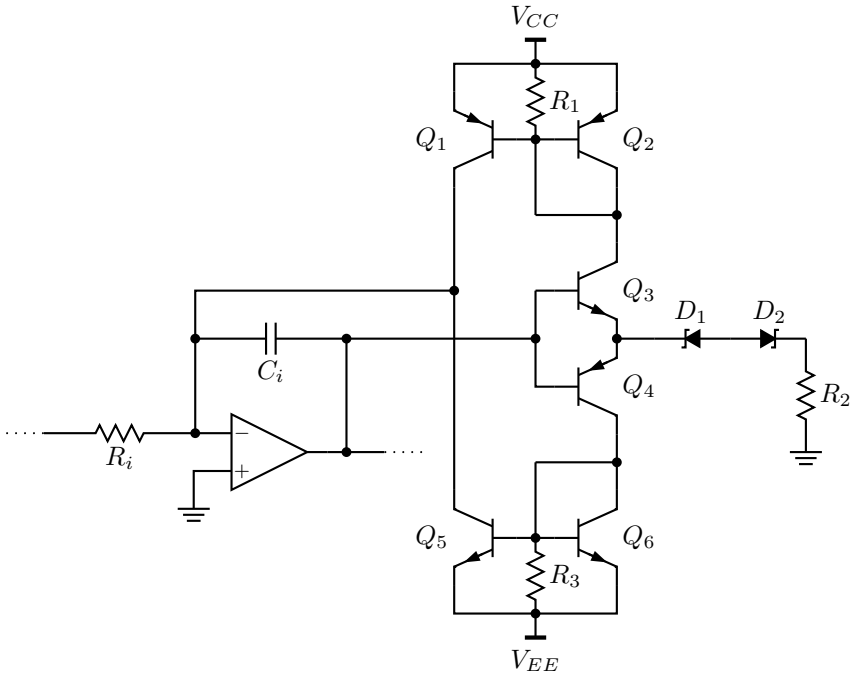


Figure 2.16: Transistor-based loop filter saturation circuit.

Assuming the transistors and zener diodes are ideal, the onset of saturation occurs at a voltage of

$$V_{sat} = V_{zf} + V_{zr} + V_{BE(on)}, \tag{2.5.3}$$

where V_{zf} is the zener forward voltage, V_{zr} is the zener reverse voltage and $V_{BE(on)}$ is the transistor base-emitter on-voltage of Q_3 and Q_4. Note that if zener diodes D_1 and D_2 are omitted, the minimum saturation limit achievable with this circuit is limited by the base-emitter on-voltage of Q_3 and Q_4.

2.6 Contribution to Existing Literature

The fundamental concepts on which the design is based are not new. However, to the best knowledge of the author, an analogue controlled class-D amplifier design incorporating all of the following concepts and properties, is as yet undocumented:

- Global (post-filter) feedback
- Ripple compensation
- The stabilisation method of [10], adapted to a clocked modulator

- Design and analysis of the continuous-time control circuit using discrete-time modelling

These concepts are all essential to realise a control method that achieves the level of performance of the one documented in this thesis.

Chapter 3

Output Stage Design

3.1 Introduction

Initially the comparator and power stage of a commercial class-D amplifier module was used and very good closed-loop measured results were obtained [22]. Unfortunately, the power stage of the commercial module has a minimum pulse width that results in reduced output at the fairly high switching frequency of 768 kHz. It was therefore decided to design a power stage without this limitation.

This chapter focuses on the detail design of the power converter. This includes the design of the gate drive circuitry, thermal design and snubber design. Component selection for the demodulation filter is also discussed. Measurements are presented to confirm the correct operation of the converter.

3.2 Overview

Generally, the converter topology is selected based on power level. In most cases a half-bridge topology is the most economical and compact choice. For large power levels where the voltage stress on the switches becomes significant, a full-bridge topology will be more appropriate. For the purposes of this project a high power amplifier is not required and therefore a half-bridge topology was selected.

Figure 3.1 shows a simplified half-bridge power stage with an LC demodulation filter and output load R_o. For the design of the converter we assume a resistive load equal to the nominal impedance of the loudspeaker. This will typically be 4 Ω or 8 Ω. The loudspeaker is, of course, not purely resistive and in the control design chapter the effect of a non-resistive load will be considered.

The half-bridge topology requires the use of a split-supply to deliver a ground-referenced output signal with no DC component to the load. In some implementations a half-bridge

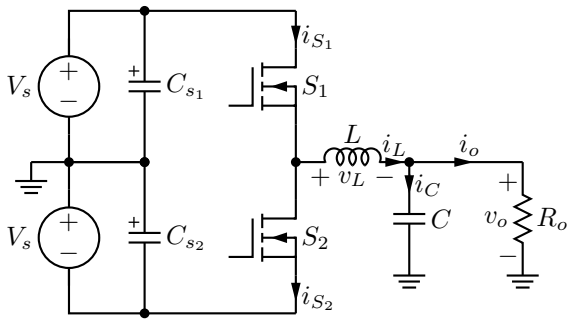


Figure 3.1: Half-bridge topology.

power stage is operated from a single supply [23]. However, this requires the use of an output DC blocking capacitor in series with the load. Placing a capacitor in series with the load is less than optimal since it leads to increased levels of distortion [24] and, unless the capacitor value is very large, a modified frequency response. Depending on the power level of the amplifier, the capacitor will also be physically large.

The drawback when using a split supply is that the gate-drive circuitry operates relative to the negative supply rail. Level-shifting circuitry is needed for the gate-drive circuitry to interface with the control circuitry, which typically operates relative to ground potential. The IRS20957S integrated half-bridge driver from International Rectifier has a floating PWM input which simplifies the half-bridge implementation [4]. The IRS20957S is selected as gate driver.

It was decided to operate the power stage from a standard regulated laboratory power supply capable of providing two supply rails of 30 V each. For an ideal power stage this results in a maximum continuous power output of 56.3 W into 8 Ω or 112.5 W into 4 Ω.

The IRFI4019H-117P integrated half-bridge from International Rectifier is selected for the switching stage. It is specifically designed for class-D audio applications and contains two power MOSFETs connected in a half-bridge configuration in a 5-pin isolated TO-220 package [3]. Table 3.1 shows some of the characteristic values of the MOSFET.

A drawback of the isolated package is its high thermal resistance of $R_{\theta JC} = 6.9$ K/W. The amplifier will not be able to deliver a full-scale sinusoidal output voltage continuously to a 4 Ω load, even if the heat-sink was infinitely large. However, unlike with a conventional DC to AC inverter, a class-D amplifier reference signal is normally not a sinusoidal signal, but an audio signal. Due to the dynamic nature of music and speech, the RMS value of a typical audio signal is less than that of a sinusoidal signal with the same peak amplitude. This assumes that the audio signal is not severely distorted, which is a reasonable assumption in a high-fidelity application. Therefore, for the thermal design of the converter we will assume a full-scale sinusoidal output signal and an 8 Ω load, while for the rest of the design we will assume a 4 Ω load. The resulting amplifier will be perfectly

Table 3.1: IRFI4019H-117P characteristic values [3].

Parameter	Desciption	Value
BV_{DSS}	Drain-to-source breakdown voltage	150 V
$I_{D(max)}$	Maximum continuous drain current	8.7 A
$I_{D(pulsed)}$	Maximum pulsed drain current	34 A
$R_{DS(on)}$	Static drain-to-source on-resistance	80 mΩ
$V_{GS(th)}$	Gate threshold voltage	4.1 V
Q_g	Maximum total gate charge	20 nC
Q_{gd}	Gate-to-drain charge	3.9 nC
Q_{sw}	Switch charge	4.7 nC
$R_{G(int)}$	Internal gate resistance	2.5 Ω
V_{SD}	Diode forward voltage	1.3 V
$R_{\theta JC}$	Junction-to-case thermal resistance	6.9 K/W

capable of delivering a full-scale audio signal continuously into a 4 Ω load.

3.3 Gate Drive Circuitry

3.3.1 Overview

Figure 3.2 shows the IRS20957 half-bridge driver and its associated circuitry. Table 3.2 shows some of the characteristic values of the IRS20957. Power is provided to the PWM input circuitry from the positive supply $+V_s$ through the combination of resistor R_1 and an internal 10.2 V zener diode between pins VDD and VSS. Capacitors C_1 and C_4 are bypass capacitors. Capacitor C_2 determines the start-up delay time and the time it takes the circuit to resume operation after an over-current condition has occurred. Resistors R_2 and R_3 set the low-side over-current limit and resistors R_4 and R_5 set the high-side over-current limit. Diode D_2 and resistor R_6 also form part of the high-side current sensing circuitry. Resistors R_8 and R_9 determine the dead-time setting. The low-side circuitry is powered from a voltage supply V_{CC} referenced to the negative supply rail $-V_s$. Power is provided to the high-side circuitry through the bootstrapping components D_3 and C_3, as well as R_7. Diode D_1 prevents the voltage at the COM pin from being significantly higher than the voltage at the VSS pin, which would damage the IC. This could happen if the negative voltage supply is missing or if the power MOSFETs fail. All diodes are ES1D fast recovery diodes from Fairchild Semiconductor.

3.3.2 Bootstrap Components

When S_2 conducts, the bootstrap capacitor C_3 is charged by the low-side supply V_{CC} through the bootstrap diode D_3. The stored energy in the bootstrap capacitor then

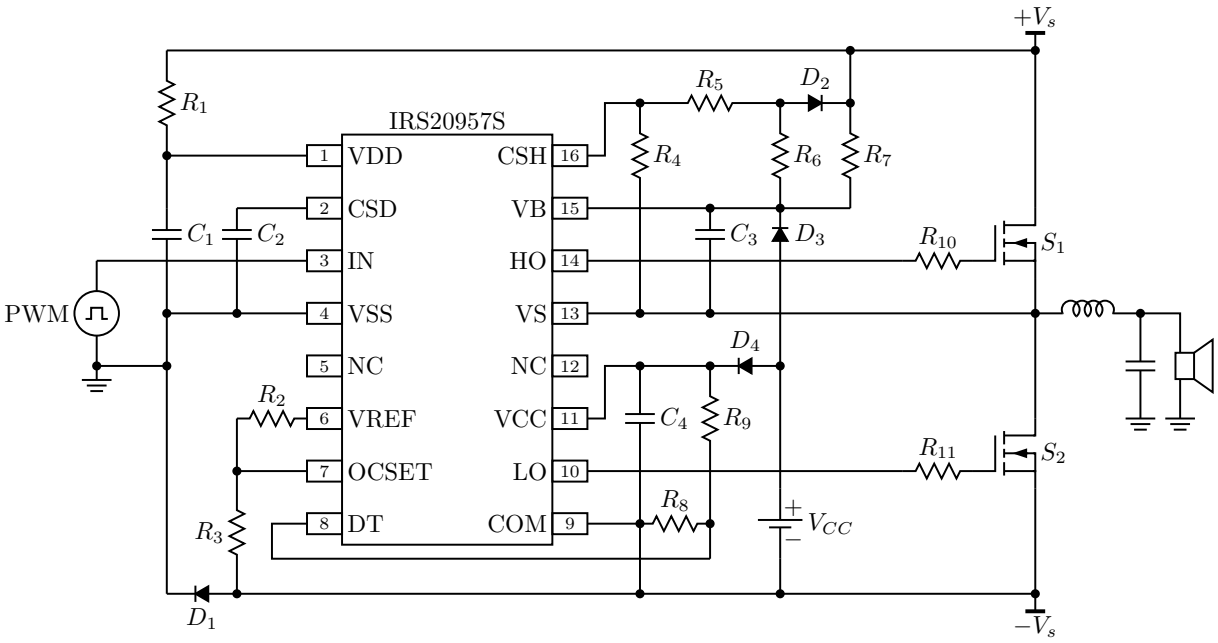


Figure 3.2: IRS20957S gate driver implementation.

Table 3.2: Gate driver characteristic values [4].

Parameter	Description	Value
$V_{B(max)}$	Maximum high side floating supply voltage	214 V
$UV_{BS(max)}$	Maximum high side under-voltage threshold	9 V
I_{QBS}	High side quiescent current	1 mA
I_{QCC}	Low side quiescent current	3 mA
R_{OUT}	Gate driver output impedance	10 Ω

powers the high-side gate-drive circuitry when S_2 is off.

The situation might occur where the bootstrap capacitor is not fully charged and the control loop wants the top switch S_1 to be on and the bottom switch S_2 to be off. This could happen during start-up when the loop has not yet stabilised. If the loop enters this condition it is likely to stay there indefinitely, since the bootstrap capacitor can only charge while the bottom switch is on, but the control loop is trying to turn on the top switch. The IRS20957S contains an internal 15.3 V zener diode clamp between pins VB and VS. Connecting a resistor R_7 between $+V_s$ and pin VB allows the bootstrap capacitor to be charged even if S_2 is not conducting. Resistor R_7 should be small enough to supply the necessary current to the bootstrap capacitor and high-side circuitry, and large enough that it does not drain significant charge from the bootstrap capacitor when S_1 is on. Assuming both switches S_1 and S_2 are off and the amplifier output voltage is at 0 V, the maximum value of R_7 is given by

$$R_{7(max)} = \frac{V_s - V_{clamp}}{I_{QBS}}, \tag{3.3.1}$$

where V_{clamp} is the internal zener diode clamp voltage. With $V_s = 30$ V, $V_{clamp} = 15.3$ V and $I_{QBS} = 1$ mA, we get $R_{7(max)} = 14.7$ kΩ. Charging resistor R_7 is chosen as $R_7 = 8.2$ kΩ. When S_1 conducts, the current flowing from the bootstrap capacitor into R_7 is approximately

$$\begin{aligned} I_{R_7} &\approx \frac{V_{CC} - V_F}{R_7} \\ &= 1.439\,\text{mA}. \end{aligned} \tag{3.3.2}$$

Resistor R_6, which is part of the high-side over-current sensing circuitry and has a value of 8.2 kΩ, also drains charge from the bootstrap capacitor when S_1 is on. The current through R_6 when S_1 is on is approximately

$$\begin{aligned} I_{R_6} &\approx \frac{V_{CC} - 2V_F}{R_6} \\ &= 1.293\,\text{mA}. \end{aligned} \tag{3.3.3}$$

Normal procedure is to design C_3 for a maximum allowable voltage drop in the bootstrap supply over a switching cycle [25]. However, in an analogue modulator the possibility of over-modulation exists. During over-modulation the switches will remain in a certain state for more than one switching cycle, and the bootstrap capacitor needs to have enough stored charge to power the high-side circuitry during this time. The amount of time spent in this condition depends on the degree of over-modulation and the frequency of the modulator input reference waveform. For the bootstrap capacitor design we will assume a worst-case scenario in which the modulator is severely over-modulated with a 10 Hz reference signal. In this situation the bootstrap capacitor has to power the high-side circuitry for 50 ms.

The value of the bootstrap capacitor is given by

$$C_3 = \frac{\Delta Q}{\Delta V_{BS}}, \tag{3.3.4}$$

where ΔQ is the charge drawn from the capacitor while S_1 is on and ΔV_{BS} is the bootstrap supply voltage drop due to the reduction in the capacitor charge. Due to the long on-time of S_1 the charge drained from C_3 will be dominated by the quiescent current supplied by the bootstrap capacitor while S_1 is on. The charge ΔQ is therefore approximately given by

$$\Delta Q \approx (I_{QBS} + I_{R_6} + I_{R_7}) t_{H(on)}, \tag{3.3.5}$$

where I_{QBS} is the high-side supply quiescent current and $t_{H(on)}$ is the time that S_1 is on. For $I_{QBS} = 1$ mA, $I_{R_6} = 1.293$ mA, $I_{R_7} = 1.439$ mA and $t_{H(on)} = 50$ ms, we get $\Delta Q = 186.6$ μC.

The maximum allowable voltage drop in the bootstrap supply is given by

$$\Delta V_{BS} = V_{CC} - V_F - I_{D(max)} R_{DS(on)} - UV_{BS(max)}, \tag{3.3.6}$$

where V_F is the bootstrap diode forward voltage, $I_{D(max)}$ is the maximum low-side MOSFET drain current, $R_{DS(on)}$ is the low-side MOSFET on-resistance and $UV_{BS(max)}$ is the maximum under-voltage-lockout voltage of the high-side driver. The maximum drain current $I_{D(max)}$ is equal to the maximum amplifier output current, which for a 4 Ω load is $I_o = 7.5$ A. For $V_{CC} = 12.4$ V, $V_F = 0.6$ V, $I_{D(max)} = 7.5$ A, $R_{DS(on)} = 80$ mΩ and $UV_{BS(max)} = 9$ V, we get $\Delta V_{BS} = 2.2$ V. Substituting $\Delta Q = 186.6$ μC and $\Delta V_{BS} = 2.2$ V into (3.3.4), we get $C_3 = 84.8$ μF. This is the absolute minimum required bootstrap capacitor value and it is recommended that the actual bootstrap capacitor be made significantly larger [26]. Capacitor C_3 is chosen as the parallel combination of a 470 μF electrolytic and a 100 nF ceramic capacitor.

3.3.3 Low-Side Voltage Supply

The low-side drive circuitry of the IRS20957S requires a voltage supply V_{CC} referenced to the negative supply rail $-V_s$. The V_{CC} supply is shown as a battery in Figure 3.2 and is realised by the simple linear regulator circuit of Figure 3.3 [27]. Resistor R_z biases the

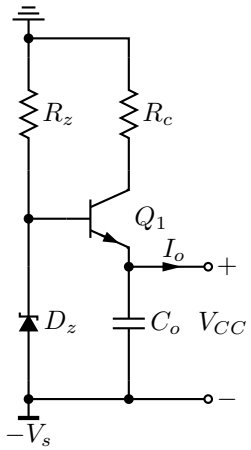


Figure 3.3: Low-side V_{CC} supply.

zener diode D_z. The voltage over the zener is buffered by a PZT2222A NPN transistor Q_1. Capacitor C_o is a decoupling capacitor consisting of the parallel combination of a 47 μF electrolytic and 100 nF ceramic capacitor. Resistor R_c limits the collector and emitter current of the transistor. The output voltage V_{CC} is equal to

$$V_{CC} = V_z - V_{BE(on)}, \tag{3.3.7}$$

where V_z is the zener voltage and $V_{BE(on)}$ is the base-emitter on-voltage of Q_1. D_z is chosen as a 13 V zener, which results in an output voltage of $V_{CC} = 12.4$ V if we assume $V_{BE(on)} = 0.6$ V.

The maximum average output current I_o that the supply has to deliver is approximately given by [25]

$$I_o = I_{QCC} + I_{QBS} + 2Q_g f_s, \tag{3.3.8}$$

where I_{QCC} is the low-side quiescent supply current. For $I_{QCC} = 3$ mA, $I_{QBS} = 1$ mA, $Q_g = 20$ nC and $f_s = 768$ kHz, we get $I_o = 34.7$ mA. If we assume a worst-case transistor current gain of $h_{FE} = 50$, the minimum required zener diode bias current is

$$\begin{aligned} I_z &= \frac{I_o}{h_{FE}} \\ &= 694\,\mu\text{A}, \end{aligned} \tag{3.3.9}$$

and the maximum value of the bias resistor R_z is

$$\begin{aligned} R_z &= \frac{V_s - V_z}{I_z} \\ &= 24.5\,\text{k}\Omega. \end{aligned} \tag{3.3.10}$$

We choose $R_z = 15$ kΩ. Assuming transistor Q_1 is ideal, the value of the current limiting resistor R_c is given by

$$R_c = \frac{V_s}{I_{lim}}, \tag{3.3.11}$$

where I_{lim} is the maximum allowable capacitor inrush current. Choosing $R_c = 100\ \Omega$ limits the inrush current to 300 mA.

The current limiting resistor R_c is effectively in series with the V_{CC} load, and its power dissipation has to be considered. Worst-case power dissipation in R_c is $P_{R_c} = 120.4$ mW. R_c is chosen as an 0102 MELF resistor, which has a power rating of 200 mW.

The power dissipation in Q_1 is given by

$$P_{Q_1} \approx (V_s - I_o R_c - V_{CC}) I_o \tag{3.3.12}$$

$$= 490\,\text{mW}. \tag{3.3.13}$$

The junction temperature of Q_1 will increase by

$$\Delta T_j = P_{Q_1} R_{\theta JA}, \tag{3.3.14}$$

where $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the transistor package. For the SOT223 package of the PZT2222A, $R_{\theta JA} = 109$ K/W. From (3.3.14) it follows that $\Delta T_j = 53.4$ K. This is a significant, though not destructive, temperature rise and can be lowered by connecting a thermal copper plane on the PCB to the collector pad of the package.

The charge in the low-side supply decoupling capacitor C_4 is continuously replenished by the V_{CC} supply. Consequently, it does not have to be as large as the bootstrap capacitor. C_4 is chosen to consist of a 47 μF electrolytic capacitor in parallel with a 100 nF ceramic capacitor. Diode D_4 ensures that the bootstrap capacitor does not receive its energy from the low-side supply decoupling capacitor C_4, but only from V_{CC}.

3.3.4 Gate Resistors

Figure 3.4 shows a graph of gate charge versus gate-to-source voltage for the IRFI4019H-117P MOSFET.

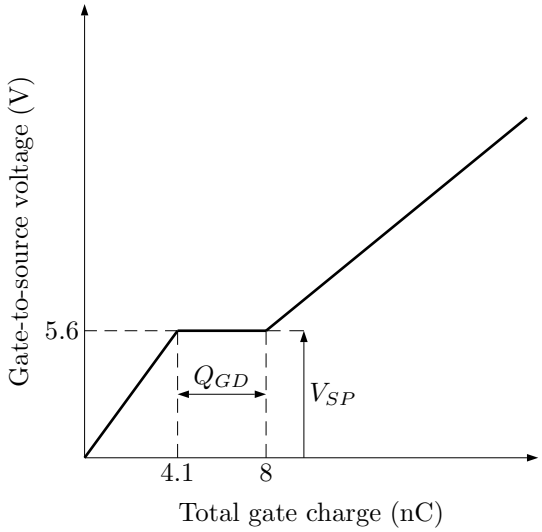


Figure 3.4: IRFI4019H-117P gate charge versus gate-to-source voltage [3].

The MOSFET voltage fall time is given by [28]

$$t_{vf} = \frac{Q_{GD} R_{G(tot)}}{V_{OH} - V_{SP}}, \tag{3.3.15}$$

where $R_{G(TOT)}$ is the total gate resistance, V_{OH} is the high level output voltage of the gate driver and V_{SP} is the switching-point voltage as defined in Figure 3.4. The MOSFET voltage rise time is given by [28]

$$t_{vr} = \frac{Q_{GD} R_{G(tot)}}{V_{SP} - V_{OL}}, \tag{3.3.16}$$

Where V_{OL} is the low level output voltage of the gate driver. The total gate resistance $R_{G(tot)}$ is the sum of the gate driver output resistance R_{OUT}, the external gate resistor R_G and the internal gate resistance $R_{G(int)}$ of the MOSFET. The high level output voltage V_{OH} is 1.4 V lower than the voltage at pin VCC and the low level output voltage is $V_{OL} = 0.1$ V [4]. In this case

$$V_{OH} = V_{CC} - V_F - 1.4 = 10.4\,\text{V}. \tag{3.3.17}$$

Theoretically, reducing the MOSFET switching transition times will reduce open-loop distortion [5]. However, faster switching transitions will lead to increased radiated EMI. When EMI from the power stage couples into the analogue modulator self-pollution occurs, resulting in increased distortion at larger values of modulation. The gate resistors are therefore not designed to yield the fastest possible switching times. It was decided to design for voltage rise and fall times of around 25 ns. Choosing $R_G = 22\ \Omega$ results in $t_{vf} = 28$ ns and $t_{vr} = 24.5$ ns.

3.3.5 Miscellaneous

Capacitor C_2 sets the start-up time of the IRS20957S, as well as the self-reset time after an over-current condition. The data sheet recommends a value of 10 μF, which gives a start-up time of 714 ms and a self-reset time of 1.122 s.

Resistors R_8 and R_9 set the gate driver blanking time. To avoid a negative dead-time and consequent cross-conduction of the power MOSFETs, the blanking time has to be greater than t_{vf} and t_{vr}. Choosing $R_8 = 3.3$ kΩ and $R_9 = 8.2$ kΩ sets the blanking time to 35 ns. It should be noted that in an amplifier design in which audio performance has a higher priority than efficiency a certain amount of transistor cross-conduction is tolerated. The blanking time of 35 ns is only an initial value and the final value will be determined through measurement.

Resistors R_2 and R_3 set the low-side current limit; R_4 and R_5 set the high-side current limit. The current limit was chosen to be 10 A. Choosing $R_2 = 8.2$ kΩ, $R_3 = 1.5$ kΩ, $R_4 = 8.2$ kΩ and $R_5 = 1.5$ kΩ sets the low-side and high-side current limits to 10.24 A and 9.86 A, respectively. Resistor R_6 and diode D_2 prevents high voltages reaching the CSH pin when S_2 is on.

Power is provided to the floating PWM input circuitry through resistor R_1 and the internal zener diode clamp, as shown in Figure 3.5. Resistor R_1 is chosen as $R_1 = 8.2$ kΩ, based on the recommendations in the data sheet [4]. C_1 is chosen as a 47 μF electrolytic in parallel with a 100 nF ceramic capacitor.

3.4 MOSFET Power Loss

For power loss calculations, the inductor current is approximated by a current source with value

$$i_L(t) = I_o \sin(2\pi f_1 t), \tag{3.4.1}$$

where I_o is the peak value of the sinusoidal load current and f_1 is the frequency of the amplifier output signal. Figure 3.6 shows the idealised current through switch S_1, if it is assumed that the parasitic diode of the MOSFET does not become forward biased due

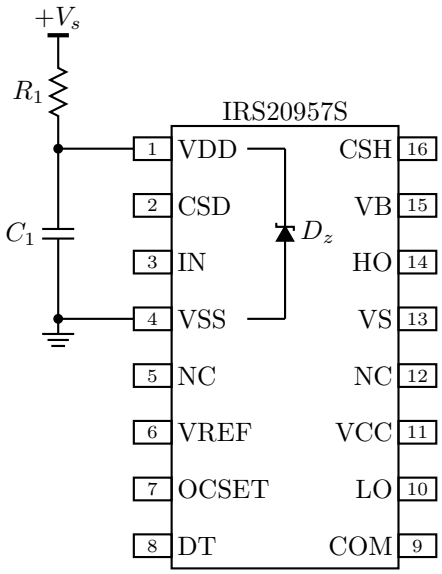


Figure 3.5: IRFI4019H-117P floating input voltage supply [3].

to the voltage drop over $R_{DS(on)}$. When the amplifier delivers a 30 V output signal into a 4 Ω load the voltage drop over $R_{DS(on)}$ is $V_{RDS} = 600$ mV. This is less than the diode forward voltage of 1.3 V. It is assumed that the conduction loss of the diodes are negligible compared to the conduction loss of the MOSFETs, since the diodes only conduct during dead-time. Ideal diodes are assumed.

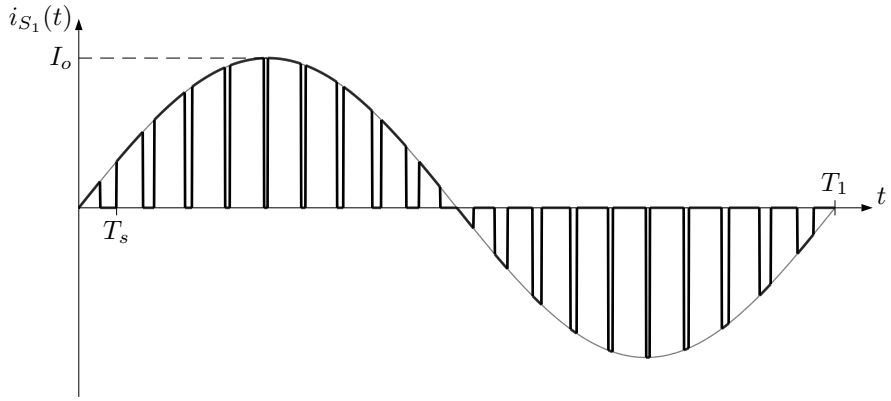


Figure 3.6: Current through MOSFET S_1 with a sinusoidal current source as load.

3.4.1 Conduction Loss

The power dissipated in MOSFET S_1 due to its non-zero on-resistance $R_{DS(on)}$ is given by

$$P_{S_1(cond)} = I^2_{S_1(rms)} R_{DS(on)}, \tag{3.4.2}$$

where $I_{S_1(rms)}$ is the RMS current through the MOSFET. Figure 3.7 shows the square of the current through S_1 over three switching cycles. Each pulse is approximated by a rectangular pulse when calculating the area of a pulse, as indicated in Figure 3.7.

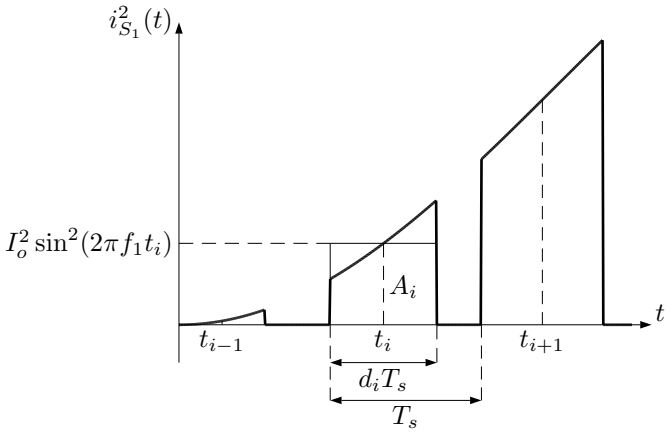


Figure 3.7: Square of the current through MOSFET S_1 with a sinusoidal current source as load. Three switching cycles are shown.

The area A_i of rectangular pulse i is given by

$$A_i = d_i T_s I_o^2 \sin^2(2\pi f_1 t_i), \tag{3.4.3}$$

where

$$d_i = \frac{1}{2}\left(1 + m_a \sin(2\pi f_1 t_i)\right). \tag{3.4.4}$$

Consequently, the average value of $i^2_{S_1}(t)$, or the square of the RMS current through S_1, is approximately given by

$$I^2_{S_1(rms)} = \frac{1}{T_1}\sum_{i=1}^{N} \frac{1}{2}\left(1 + m_a \sin(2\pi f_1 t_i)\right) T_s I_o^2 \sin^2(2\pi f_1 t_i), \tag{3.4.5}$$

where N is the number of switching cycles during time T_1. Equation (3.4.5) can be approximated by the integral [29]

$$I^2_{S_1(rms)} \approx \frac{1}{T_1}\int_0^{T_1} \frac{1}{2}\left(1 + m_a \sin(2\pi f_1 t)\right) I_o^2 \sin^2(2\pi f_1 t)\, dt \tag{3.4.6}$$

$$= \frac{I_o^2}{4}. \tag{3.4.7}$$

Substituting (3.4.7) into (3.4.2) we obtain

$$P_{S_1(cond)} = \frac{I_o^2}{4} R_{DS(on)}. \tag{3.4.8}$$

3.4.2 Switching Loss

Figure 3.8 shows the current through S_1 with a sinusoidal current source as load for three switching cycles. Figure 3.9 shows the idealised MOSFET turn-on and turn-off transitions. During time t_{on} and t_{off} the switch has both a voltage over it and a current through it.

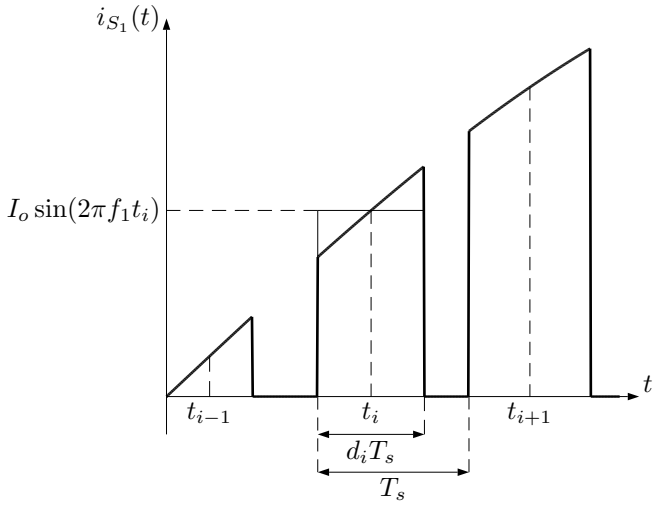


Figure 3.8: Current through MOSFET S_1 with a sinusoidal current source as load. Three switching cycles are shown.

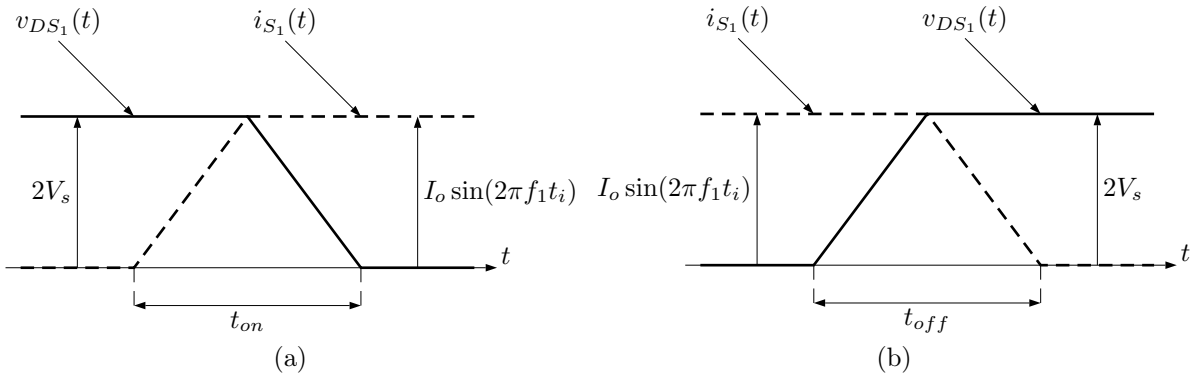


Figure 3.9: Idealised MOSFET switching waveforms during (a) turn-on and (b) turn-off.

Assuming ideal diodes, the energy dissipated in a switching cycle is approximately given by

$$E_{i(switch)} = V_s I_o \sin(2\pi f_1 t_i)(t_{on} + t_{off}), \tag{3.4.9}$$

where t_{on} and t_{off} are the on- and off transition times of the MOSFET, respectively. The average switching loss is the average energy dissipated over time T_1. It therefore follows

that

$$P_{S_1(switch)} \approx \frac{1}{T_1}\sum_{i=1}^{N} V_s I_o \sin(2\pi f_1 t_i)(t_{on} + t_{off}). \tag{3.4.10}$$

In the negative half-cycle of $i_L(t)$ diode D_1 is forced into conduction during dead-time, limiting the voltage over S_1 to the forward voltage of the diode. Consequently, the switching energy dissipated in S_1 during the negative half-cycle of $i_L(t)$ is negligible compared to that of the positive half-cycle. Therefore, unlike with the calculation of the conduction loss, N is now the number of switching cycles during time $\frac{T_1}{2}$. Equation (3.4.10) can be approximated by the integral

$$P_{S_1(switch)} \approx \frac{1}{T_1 T_s}\int_0^{\frac{T_1}{2}} V_s I_o \sin(2\pi f_1 t_i)(t_{on} + t_{off})\, dt \tag{3.4.11}$$

$$= \frac{f_s}{\pi} V_s I_o (t_{on} + t_{off}). \tag{3.4.12}$$

The switching transition times are approximately given by [28]

$$t_{on} = \frac{Q_{SW} R_{G(tot)}}{V_{OH} - V_{SP}} \tag{3.4.13}$$

and

$$t_{off} = \frac{Q_{SW} R_{G(tot)}}{V_{SP}}, \tag{3.4.14}$$

where Q_{SW} is the switching charge, $R_{G(tot)}$ is the total gate resistance, V_{OH} is the gate driver output-high voltage and V_{SP} is the switching point voltage as defined in Figure 3.4.

3.4.3 Total Dissipation

The total dissipation is the sum of the conduction loss and switching loss. Table 3.3 shows the values required for the calculation. A full-scale output voltage into an 8 Ω load results in a peak output current of $I_o = 3.75$ A.

Table 3.3: Circuit and MOSFET parameter values.

Parameter	Value
V_s	30 V
I_o	3.75 A
f_s	768 kHz
Q_{SW}	4.7 nC
$R_{G(tot)}$	37 Ω
V_{OH}	10.4 V
V_{SP}	5.6 V

From (3.4.8), we calculate $P_{S_1(cond)} = 281$ mW. From (3.4.12), (3.4.13) and (3.4.14), we obtain $P_{S_1(switch)} = 1.728$ W. The total power dissipated in S_1 is therefore

$$\begin{aligned} P_{S_1(tot)} &= P_{S_1(cond)} + P_{S_1(switch)} \\ &= 2.01\,\text{W} \end{aligned} \tag{3.4.15}$$

Due to the symmetry of the reference waveform the power dissipation of both MOSFETs are the same, thus $P_{S_2(tot)} = P_{S_1(tot)}$. The total dissipation in the package is $P_{TOT} = P_{S_1(tot)} + P_{S_2(tot)} = 4.02$ W.

3.5 Heat-sink Design

The transistor junction temperature rise due to the power dissipated in the MOSFET package is given by [14]

$$\Delta T = P_{TOT}(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}), \tag{3.5.1}$$

where P_{TOT} is the total power dissipated in the package, and $R_{\theta JC}$, $R_{\theta CS}$ and $R_{\theta SA}$ are the junction-to-case, case-to-sink and sink-to-ambient thermal resistances of the package, respectively. If we design for a maximum temperature rise of $\Delta T = 60°$C and estimate $R_{\theta CS} = 1°$C/W [30], the minimum required thermal resistance of the heat-sink is $R_{\theta SA} = 7.05°$C/W. This is approximately the thermal resistance of a 80 mm $\times$ 80 mm aluminium plate of 1 mm thickness. Due to the circuit layout the actual heat-sink is smaller than this. However, the heat-sink has an L-shape and provision is made to attach an off-board heat-sink to one of the sides of the on-board heat-sink, thereby decreasing the overall thermal resistance.

3.6 Snubber Design

The resonance caused by the parasitic series inductance and parallel output capacitance of each MOSFET leads to overshoot and ringing of the switching waveform. This in turn leads to greater stress on the switches and increased EMI. The voltage overshoot will not damage the IRFI4019-117P MOSFETs, since their voltage ratings are substantially larger than the voltages in the circuit. However, the increased EMI will lead to increased distortion in the analogue modulator due to self-pollution.

A simple RC snubber is added over each MOSFET to absorb the energy stored in the parasitics. When the snubber resistor is selected to be equal to the characteristic impedance of the resonant circuit the resonance is critically damped, and theoretically there will be no overshoot [31]. The snubber capacitor must be larger than the parasitic

capacitance, which is normally dominated by the output capacitance C_{oss} of the MOSFET. The characteristic impedance of the resonant circuit is given by

$$Z_i \approx \sqrt{\frac{L_s}{C_{oss}}}, \tag{3.6.1}$$

where L_s is the series inductance of the MOSFET. The parasitic series inductance includes the inductance of tracks and vias and the internal inductance of the package, and is estimated to be $L_s \approx 20$ nH [32]. With $C_{oss} = 97$ pF, we get $Z_i = 14.36\ \Omega$.

Ideally, the snubber capacitor should be able to store the energy stored in the parasitic inductance [33]. This means that

$$\begin{aligned} \frac{1}{2}C_s(2V_s)^2 &> \frac{1}{2}L_s I_o^2 \\ \Rightarrow C_s &> \frac{L_s I_o^2}{4V_s^2}. \end{aligned} \tag{3.6.2}$$

For $L_s = 20$ nH, $I_o = 3.75$ A and $V_s = 30$ V, (3.6.2) evaluates to $C_s > 78$ pF. We have already stated that the snubber capacitor should be larger than the MOSFET output capacitance of $C_{oss} = 97$ pF, so (3.6.2) will be satisfied. However, we also need to consider the power dissipation in the snubber resistor when choosing a snubber capacitor value.

The worst-case power dissipated in the snubber resistor can be estimated by [31]

$$P_{R_s} \approx 4 f_s C_s V_s^2. \tag{3.6.3}$$

According to [31] the optimal value for the snubber capacitor is approximately three times the MOSFET output capacitance, which in this case gives a snubber capacitor of 291 pF. A snubber capacitor of 291 pF will result in 805 mW being dissipated in the snubber resistor, which is too high. This is mainly due to the high switching frequency. The snubber capacitor was chosen as $C_s = 150$ pF. This gives a dissipation of 418 mW in the snubber resistor. The snubber resistor was chosen as the parallel combination of two 27 Ω 0805 0.25 W Panasonic anti-surge resistors, effectively creating a 13.5 Ω 0.5 W resistor. Note that the snubber capacitor has to withstand a voltage of $2V_s = 60$ V.

3.7 Demodulation Filter

The PWM signal produced by the power switching stage contains an amplified version of the reference (audio) signal, as well as harmonics of the switching frequency and their associated side-bands [5]. The purpose of the demodulation filter is to remove the energy outside the audio band from the PWM signal.

The demodulation filter is commonly realised by a second order LC low-pass filter. Unfortunately, placing a passive filter between the PWM output and the loudspeaker

introduces several non-idealities into the system. These include a load dependent frequency response, high output impedance and restricted bandwidth. The demodulation filter also introduces distortion, since a ferrite core inductor is inherently non-linear. In an open-loop or pre-filter feedback design most of these non-idealities are mitigated by increasing the resonant frequency of the filter. However, this reduces the ability of the filter to perform its primary purpose. In a global feedback design the open loop non-idealities are mitigated by the control loop. The result is that the resonant frequency of the demodulation filter can be much lower than in an open loop or pre-filter feedback design. Choosing the resonant frequency of the demodulation filter as low as possible is also important from a control perspective. A lower cut-off frequency will result in a lower unity gain crossover frequency, which increases phase margin.

Typically, we want the inductor value to be as small as possible. There are several reasons for this. We want to keep the peak flux density in the inductor core as small as possible to minimise distortion and we want as few turns as possible to minimise parasitic winding capacitance. For a given ferrite core this means that the inductor value should be as low as possible. Furthermore, if the inductor ripple current is large enough that it changes polarity twice during every switching cycle, the distortion resulting from dead-time is much reduced [5].

For a given resonant frequency a smaller inductor value will necessarily result in a larger capacitor value. However, there is a limit on the physical size and the capacitance value of the capacitor. A physically large capacitor will have a large parasitic inductance. The parasitic parallel capacitance of the inductor and the parasitic series inductance of the capacitor causes the inductor and capacitor to each have a self-resonant frequency. Above these resonant frequencies the capacitor is inductive and the inductor is capacitive. Consequently the LC low-pass filter is an LC high-pass filter at high frequencies. From an EMI perspective it is therefore important to minimise these parasitics. This means that we require a physically small capacitor. A polyester dielectric capacitor is a good choice, since they have good high frequency behaviour and are physically small for a given capacitance value. The problem with polyester capacitors is that their RMS voltage handling capability reduces with frequency. This phenomenon gets worse for higher capacitance values. This places a limit on the maximum capacitance value and therefore on the minimum inductor value.

Selecting the inductor and capacitor of the demodulation filter is a compromise between all of the aforementioned factors. Three parallel 680 nF, 5 mm pitch, polyester capacitors are used in the filter. The inductor is a modified version of the inductor found on a commercial UcD180LP class-D module from Hypex Electronics. The UcD180LP inductor has an 18 turn copper foil winding and a nominal value of 30 μH. Three turns

were removed to obtain a value of 20.83 μH. Figure 3.10 shows the calculated frequency response of the filter for various output loads. The resonant frequency of the ideal filter is 24.4 kHz and it has a Q factor of 2.57 into an 8.2 Ω load.

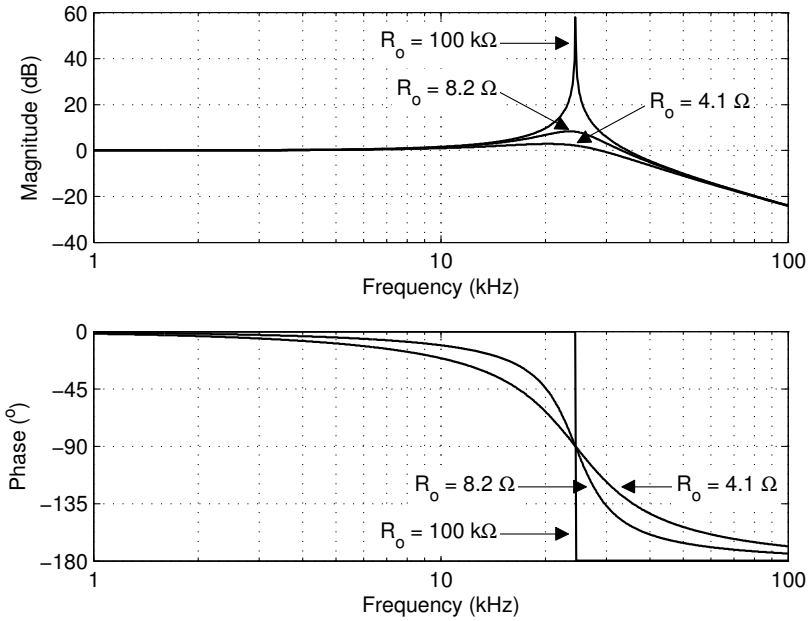


Figure 3.10: Calculated frequency response of the ideal demodulation filter for various output loads.

3.8 Circuit Board Layout

The high frequency currents associated with a class-D power stage requires us to pay careful attention to the printed circuit board (PCB) layout. An ill-conceived PCB layout will greatly increase EMI. There are a few basic principles that have to be adhered to in the PCB design [34]:

- The PCB should have a single contiguous ground plane.
- Connections should be kept together.
- Current loop areas should be minimised.

Figure 3.11 and Figure 3.12 show the top layer and bottom layer of the power stage PCB, respectively. Surface mount components are mounted on the bottom layer and the ground plane is on the top layer.

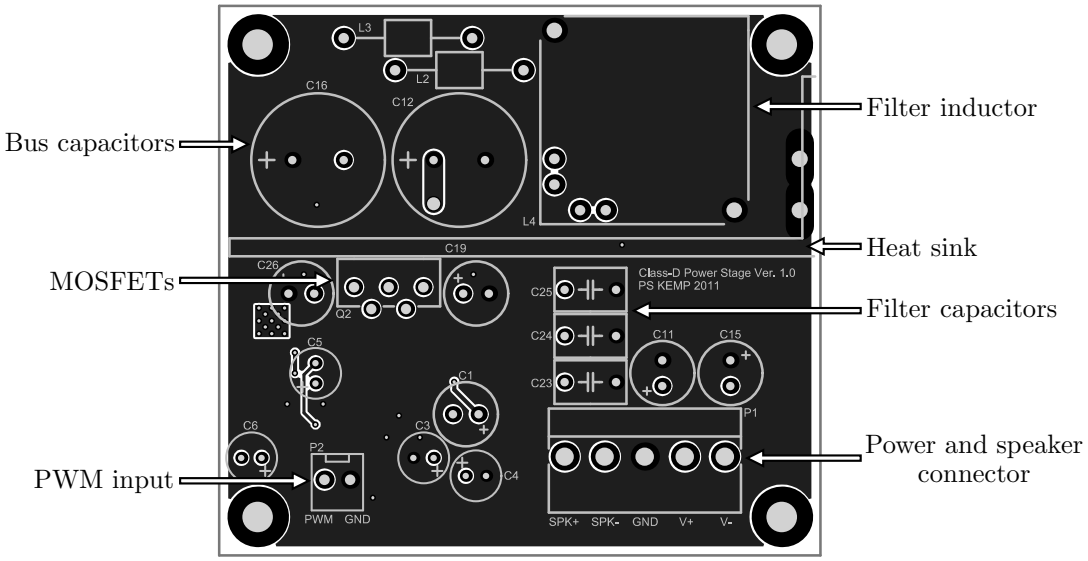


Figure 3.11: Top layer of PCB.

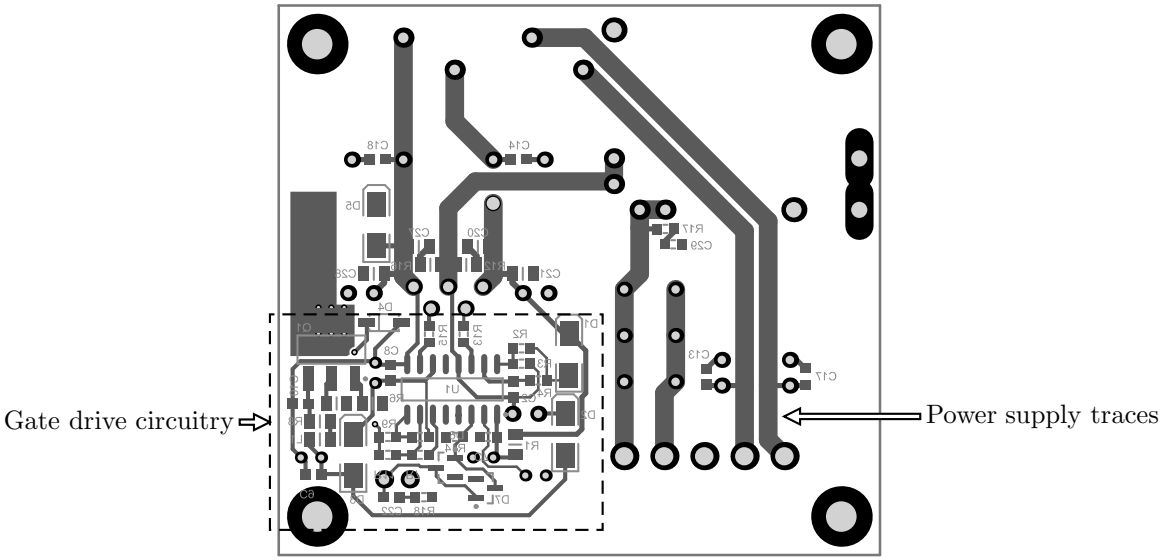


Figure 3.12: Bottom layer of PCB.

3.9 Adjustments

This section describes the modifications that were made to the original power stage design after initial measurements were taken.

3.9.1 Dead Time and Gate Resistor Selection

To minimise distortion the final value of the blanking-time is selected by decreasing the dead-time until the contribution of the shoot-through current of the output devices to the idle loss of the amplifier is about 2% of the rated maximum power of the amplifier. For

a 100 W amplifier operated from $V_s = 30$ V rails, this corresponds to an average current of 33.3 mA drawn from each supply rail. This should be measured through the positive supply rail, because the negative rail also sinks current from the gate driver V_{CC} supply.

The blanking time of the gate driver was decreased to its minimum value of 15 ns by removing resistor R_8 in Figure 3.2. The effective dead-time was further decreased by increasing the value of the gate resistors from 22 Ω to 27 Ω. This reduces the switching time which decreases the effective dead-time. With a blanking time of 15 ns and gate resistors of $R_G = 27$ Ω the average current drawn from the supply due to shoot-through is measured as 32 mA.

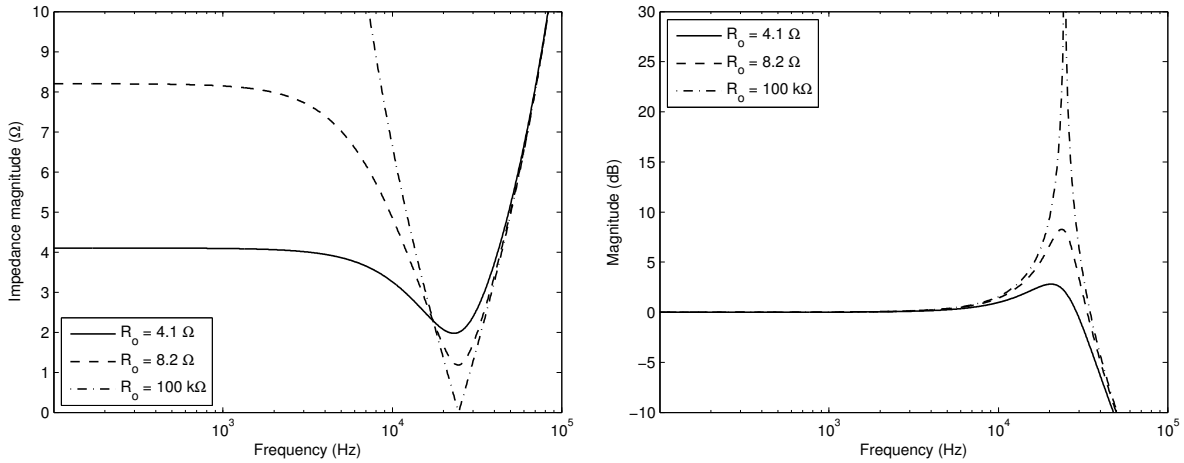
3.9.2 Current Limit Setting

The over-current protection of the IRS20957 gate driver triggered regularly during initial measurements. A factor that was not taken into account during the initial design phase is the decreasing impedance of the demodulation filter capacitor at higher frequencies. In a conventional design in which the resonant frequency is significantly higher than 20 kHz this is not a problem. However, in this design the resonant frequency of the output filter is 24.4 kHz. The current flowing into the filter capacitor becomes significant at higher audio frequencies. In the open loop system this situation is aggravated when the filter is not well damped, for example under no-load conditions.

Figure 3.13 (a) shows the calculated magnitude of the input impedance of the demodulation filter as a function of frequency for various output load resistances. Figure 3.13 (b) shows the calculated magnitude response of the demodulation filter. Ideal components are assumed. The input impedance at 20 kHz is down to 2.1 Ω for a 4.1 Ω load and 1.3 Ω for a 100 kΩ load. Figure 3.14 (a) shows the calculated demodulation filter input current for $m_a = 1$ and no feedback. The 10 A current limit of the gate driver is reached at about 12 kHz for a 4 Ω load. For a load resistance of $R_o = 100$ kΩ the current at 20 kHz is 20 A, even though the load resistance is very large.

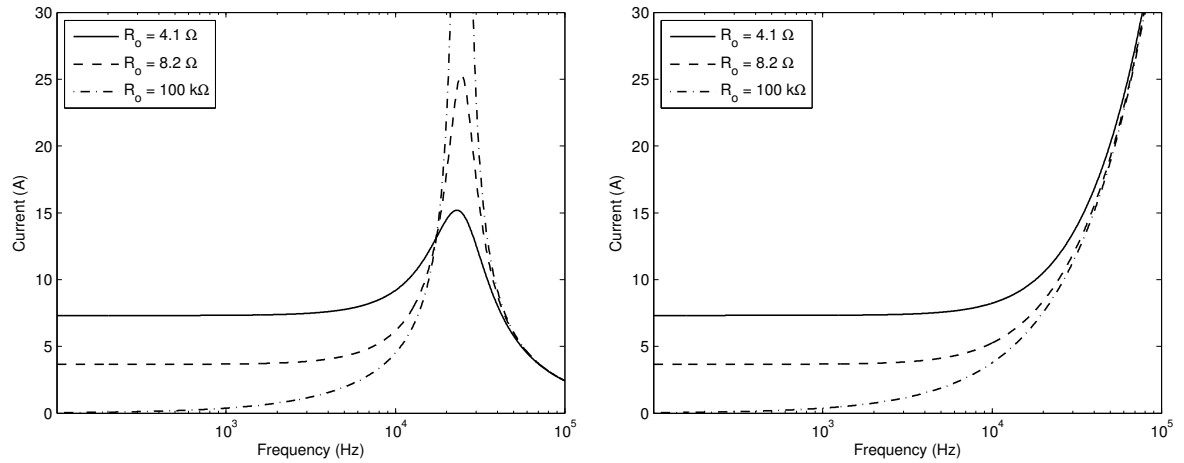
Figure 3.14 (b) shows that when the output voltage of the filter is kept constant by a feedback control loop, the situation is markedly different. The filter input current still increases with frequency, but only rises to 10.5 A at 20 kHz for a 4 Ω load and 7.5 A for a 100 kΩ load.

It was decided to raise the current limit of the gate driver from 10 A to approximately 15 A. This ensures that the current limiting will not be triggered unnecessary in the closed loop amplifier and it enables the open loop system to be sufficiently measured. However, making high power measurements in the upper part of the audio band will not be possible with the open loop power stage. The new values for the current limiting components in



(a) (b)

Figure 3.13: (a) Calculated input impedance of the demodulation filter. (b) Calculated magnitude response of the demodulation filter.



(a) (b)

Figure 3.14: Calculated demodulation filter input current for an output voltage of 30 V at 1 kHz for (a) the open loop converter and (b) the closed loop converter.

Figure 3.2 are $R_2 = 6.8$ kΩ, $R_3 = 2.2$ kΩ, $R_4 = 6.8$ kΩ and $R_5 = 2.7$ kΩ. This results in a high-side current limit of 14.7 A and a low-side current limit of 15.6 A.

3.10 Open Loop Measurements

The open loop system has to be characterised through measurements before an optimal control loop can be designed. The PWM input signal for the power stage is generated by comparing a sawtooth carrier of frequency $f_s = 768$ kHz and amplitude $A_s = 300$ mV to a sinusoidal reference waveform. The sawtooth carrier is generated by the FPGA waveform generator described in Chapter 4. A DC offset of 13 mV is added to the carrier

to compensate for the unequal on- and off-times of the switches which would otherwise lead to a DC offset in the amplifier output signal. The comparator circuit is discussed in Chapter 7.

Figure 3.15 shows the differential mode amplifier output signal with no applied reference input. With ideal filter components the demodulation filter output signal should be approximately sinusoidal. The measurement shows that this is not entirely the case and some of the high frequency components of the PWM signal are still present in the output signal. These high frequency spikes correspond to the switching transition of the switching stage and will radiate from attached cables and cause EMI. It should be noted, however, that these spikes are small in amplitude (20 mV peak-to-peak common mode). There are some class-D amplifiers on the market that perform better in this regard, but there are also some that perform substantially worse [35].

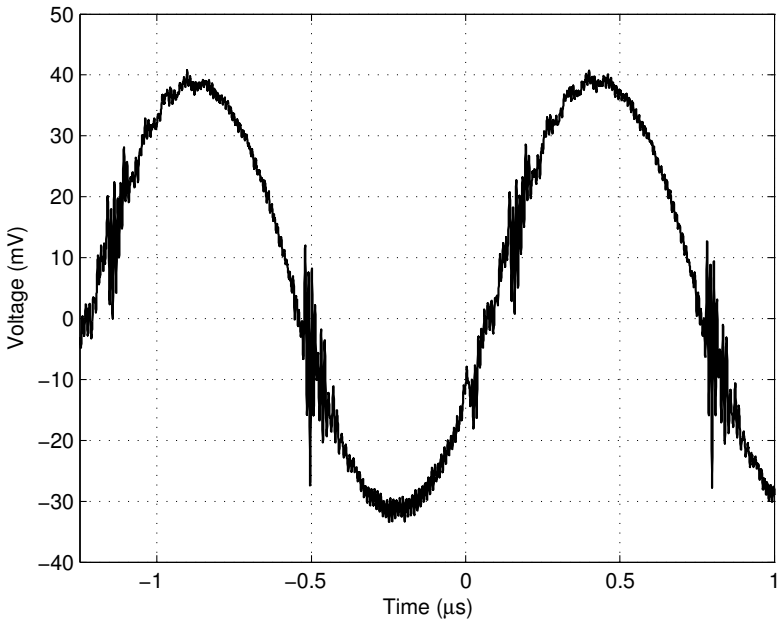


Figure 3.15: Oscilloscope measurement of the amplifier output signal with no input reference signal. Measurement bandwidth is 100 MHz.

Figure 3.16 shows the switching node voltage with and without the RC snubber. Without the snubber there is some overshoot and significant ringing. The snubber effectively reduces the ringing.

The following measurements were performed with an Audio Precision SYS-2722 analyser through an AUX-0025 switching amplifier measurement filter. Unless otherwise stated, the AES-17 20 kHz filter of the analyser was enabled. To make the measurements between different output loads comparable, power is measured relative to an 8.2 Ω

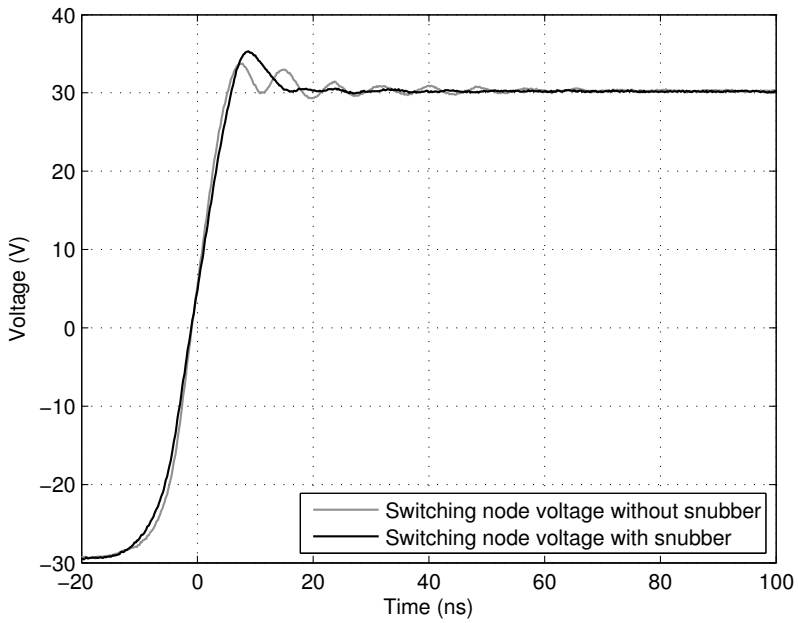


Figure 3.16: Oscilloscope measurement of switching node voltage with and without RC snubber.

load. Note that this means the actual power into a 4.1 Ω load is twice the indicated amount.

Figure 3.17 shows a measurement of total harmonic distortion and noise (THD+N) as a function of output power for a 4.1 Ω and 8.2 Ω load. The frequency of the test signal is 1 kHz. A measurement of the commercial power stage is shown in grey for reference. Note the decrease in distortion with an increase in output power at lower power levels. Normally this shows that the measurement is dominated by noise over the specific power range. For the measurement of Figure 3.17 this is not the case. Figure 3.18 shows an FFT of the output when the amplifier is delivering 100 mW into an 8.2 Ω load. The measurement is clearly not dominated by noise. The dominant source of distortion, namely dead time distortion, decreases with an increase in m_a [5]. However, at 100 mW the inductor current changes polarity twice during each switching cycle and the distortion due to dead time should be very low [5]. The source of the low-level distortion is unclear. Note that the THD+N of the commercial power stage is greater than the designed power stage above 1 W.

Above 10 W there is an increase in even harmonic distortion. This increase in even harmonic distortion is due to the DC offset in the carrier waveform causing unsymmetrical over-modulation. Self-pollution also contributes to the increase in even harmonic components at higher levels of m_a.

Figure 3.19 shows a measurement of THD+N over frequency at 10 W output power. The rise in distortion with frequency for the 8.2 Ω load is due to the demodulation filter

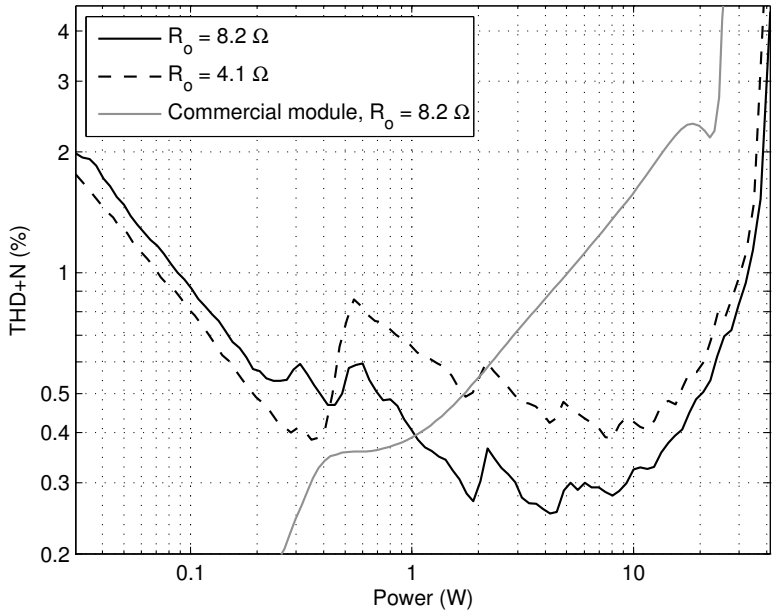


Figure 3.17: Open loop THD+N versus output power for $R_o = 4.1\ \Omega$ and $R_o = 8.2\ \Omega$ with a 1 kHz test signal.

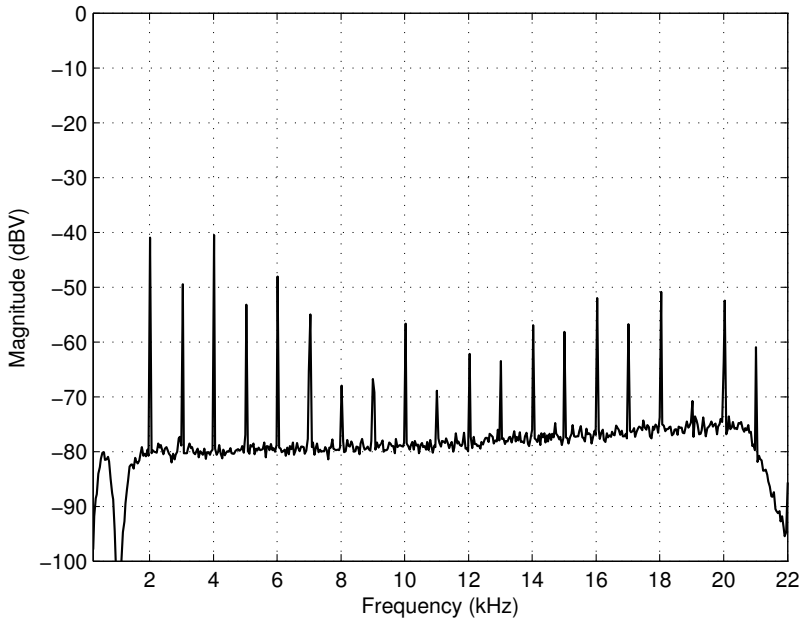


Figure 3.18: FFT of distortion residue with 100 mW into 8.2 Ω. The suppressed fundamental is at 0 dBV.

that amplifies the harmonics at higher frequencies. With a 4.1 Ω load the filter is better damped and there is less of a rise in distortion with frequency. The drop in distortion at 6.6 kHz is due to the third harmonic falling outside the passband of the AES-17 20 kHz filter. Above 10 kHz all harmonics fall outside the measurement bandwidth and only noise contributes to the THD+N measurement.

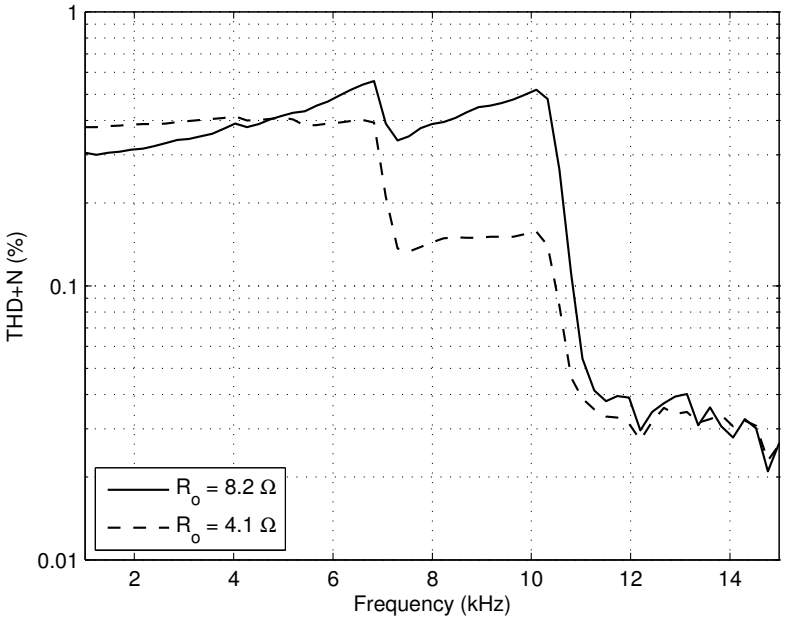


Figure 3.19: Open loop THD+N versus frequency for 10 W into 4.1 Ω and 8.2 Ω.

Figure 3.20 shows the measured frequency response of the open loop amplifier for various output loads. This measurement was performed without the AUX-0025 and AES-17 filter. Note that the 100 kΩ load is the input impedance of the analyser. The theoretical low-frequency gain of the open loop amplifier is $A_{V(open)} = \frac{V_s}{A_s} = 100\,\mathrm{V/v}$, or 40 dB. The measured gain is in accordance with the theoretical value, although there is some variation in low frequency gain due to the output resistance of the power stage. Most of the output resistance is in series with the filter inductor and is a combination of the resistance of the power supply rail, the on-resistance of the MOSFET and the series resistance of the filter inductor. We model these resistances as a single resistance R_L in series with the filter inductor. The value of R_L can be calculated from the measured change in low frequency amplifier gain due to an applied output load. The value of the equivalent inductor series resistance is $R_L = 0.45\ \Omega$.

The value of the filter inductor and capacitor was measured as $L = 20.4\ \mu$H and $C = 2.13\ \mu$F, respectively. The propagation delay of the comparator and power stage was measured as 160 ns and 122 ns for a rising and falling edge of the switching node voltage, respectively.

3.11 Summary

This chapter discussed all the aspects of the detail design of the output stage. The IRS20957S was selected as gate driver and the IRFI4019H-117P integrated half-bridge as power MOSFET. Total harmonic distortion and noise at 1 kHz was measured as 0.3%

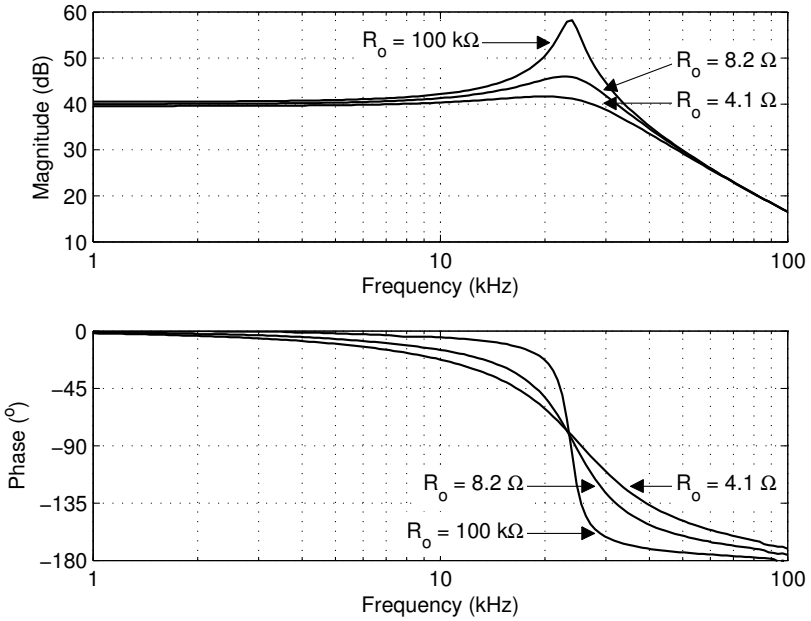


Figure 3.20: Measured open loop frequency response for various output loads. Bandwidth is >500 kHz.

with 10 W into 8.2 Ω and 0.4% with 20 W into 4.1 Ω. This is not very low, but it should be kept in mind that the output stage is not designed for open loop operation.

Chapter 4

Carrier Generator

4.1 Introduction

It was decided to use an FPGA-based arbitrary waveform generator for carrier generation, since this allows easy manipulation of the carrier waveform. Figure 4.1 shows a block-diagram of the FPGA-based carrier generator. The carrier data is generated off-line and stored in a lookup table (LUT) in the FPGA. The LUT data is clocked to a high speed parallel input digital to analogue converter (DAC), which converts the digital data to an analogue differential current. The DAC is followed by a filter and buffer stage that converts the differential current to a differential voltage.

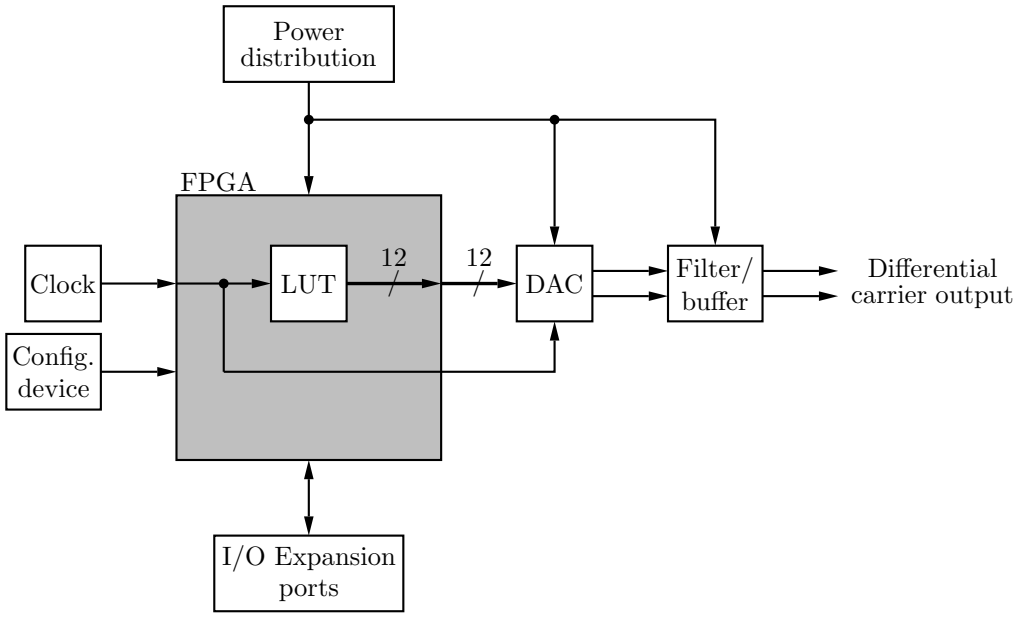


Figure 4.1: Block-diagram of the FPGA-based carrier generator.

4.2 FPGA

The programmable logic of the FPGA allows us to retrieve data from the LUT in a single clock cycle, provided that the timing requirements of the FPGA are met. The FPGA does not require many logic elements or a large amount of memory, because the carrier is generated off-line and only the data of one cycle is stored in memory. The FPGA is an Altera Cyclone III EP3C10E144C8. It is one of the smallest FPGAs in the Cyclone series and has 10 320 logic elements, 414 Kb memory and 94 I/O pins [36]. The system clock is a 98.304 MHz low-jitter oscillator from Crystek.

The FPGA is configured through a download cable by means of a JTAG interface. The FPGA can also be configured by programming a non-volatile serial configuration device through the JTAG interface. Configuration data is then transferred from the serial configuration device to the FPGA at system start-up.

4.3 DAC

The quantization noise of the DAC will be greatly attenuated by the control loop. Hence a high-resolution DAC is not required. However, since this is an experimental system the assumption cannot be made that the entire output range of the DAC will be utilized. The 12-bit, 165 MSPS, advanced segmentation, DAC902 from Texas Instruments was selected. The DAC902 is also pin-compatible with the 8-, 10- and 14-bit DAC908, DAC900 and DAC904, respectively. The DAC902 provides a differential current output, with the full-scale current set to 18.04 mA by an external resistor.

The output of the DAC feeds into the differential low-pass filter and output buffer shown in Figure 4.2. The component values for the circuit in Figure 4.2 are shown in Table 4.1. The purpose of the filter is twofold. Firstly, it converts the differential current output of the DAC to a differential voltage. Secondly, it attenuates unwanted image frequency components present in the DAC output signal and prevents slew-rate limiting of the buffer op-amps. The filter is a matched impedance, 5th order, Bessel low-pass filter with a resonant frequency of 30 MHz [37]. The filter converts the 18.04 mA full-scale DAC output current to a 505 mV differential voltage.

A Bessel filter is chosen, because it has a very good transient response with no overshoot to a pulse input [38]. The superior transient response of the Bessel filter can be seen in Figure 4.3, which shows the calculated output of a Bessel and Butterworth filter with a sawtooth as input. The downside of a Bessel filter is its slow rate of attenuation above the cut-off frequency [38]. The image frequency components present in the DAC output signal will therefore not be as well rejected as would be the case for a Butterworth or Chebychev filter of the same order. This is not a problem, because the comparator itself has a finite

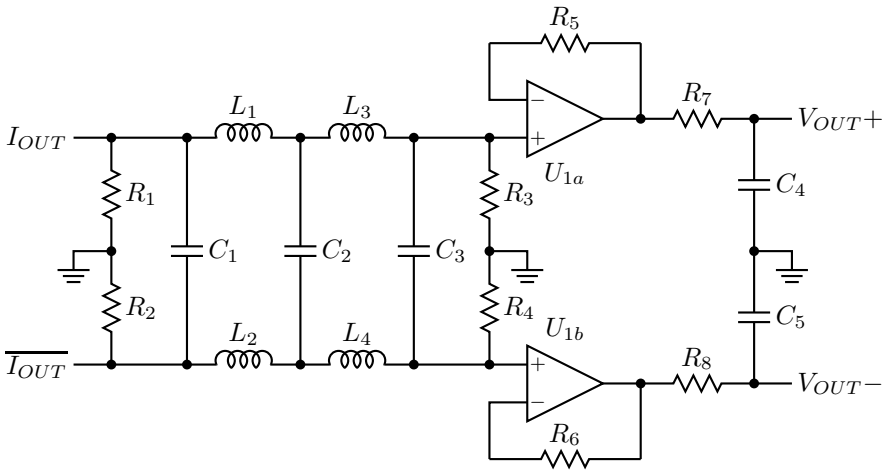


Figure 4.2: DAC output filter and buffer.

Table 4.1: Component values for the DAC post-filter and buffer.

Component	Value
$R_1 - R_4$	56 Ω
R_5, R_6	27 Ω
R_7, R_8	22 Ω
$L_1 - L_4$	220 nH
C_1	12 pF
C_2	120 pF
C_3	18 pF
C_4, C_5	82 pF

bandwidth and will not respond to the very high frequency content in the carrier signal. For example, the LM306 comparator used in this design has an approximate bandwidth of 18.5 MHz [1]. Figure 4.4 shows the calculated frequency response of the DAC output filter.

Refer to Figure 4.2. U_1 is an OPA2690 high-bandwidth, low noise, dual op-amp from Texas Instruments. Resistors R_5 and R_6 isolate the inverting input capacitance from the output pin and provides DC-bias current cancellation [39].

A capacitive load decreases the phase margin of an op-amp due to an additional pole in the feedback path created by the output resistance of the op-amp and the capacitive load [40]. Resistor R_7 shifts the pole and introduces a zero that cancels the phase lag of the capacitive pole, thereby improving stability [39]. The data sheet of the OPA2690 provides a graph of the recommended resistance value for a specified load capacitance. The lower the load capacitance, the higher the recommended resistance value. The carrier generator will not drive a very large capacitive load. To minimise the required output resistance, we intentionally increase the load capacitance by adding C_4 and C_5. Note that

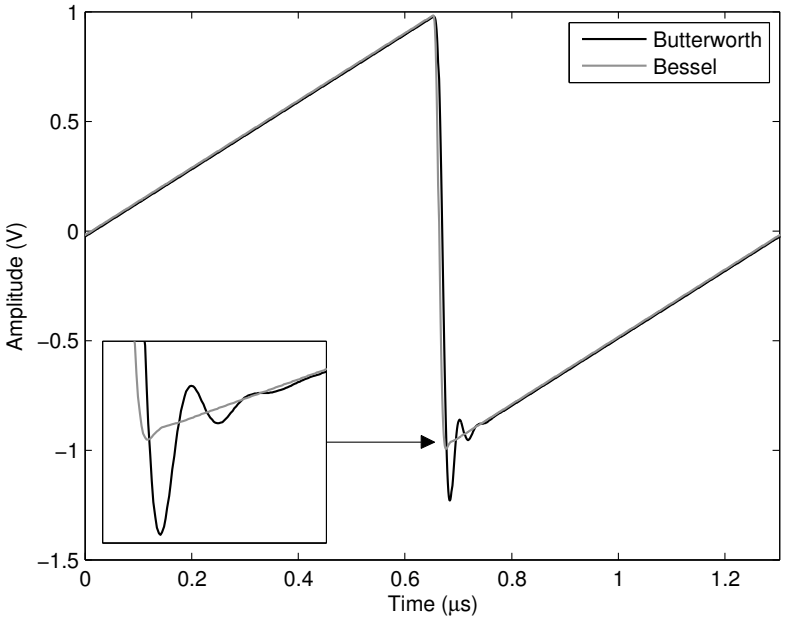


Figure 4.3: Filtered sawtooth signal for a 5th order Bessel and Butterworth filter.

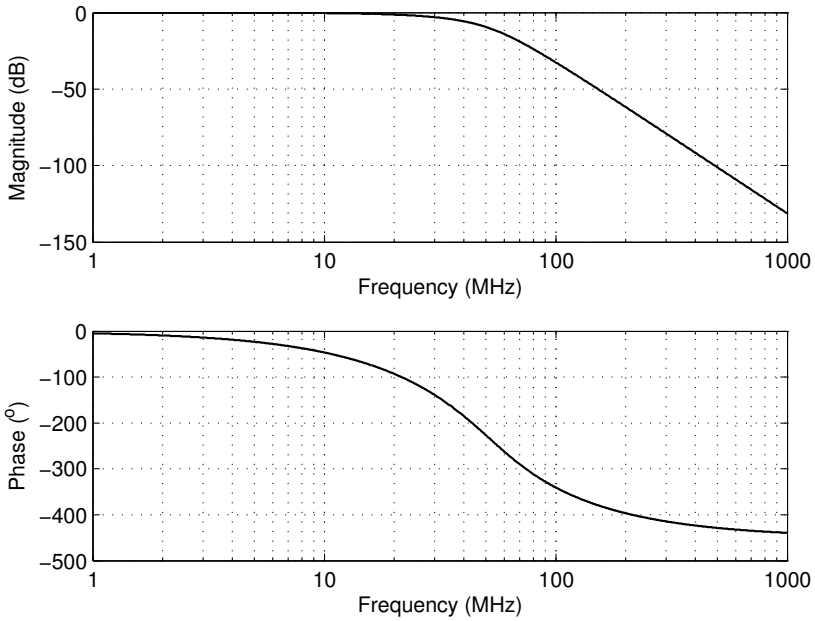


Figure 4.4: Frequency response of the DAC output filter.

the addition of R_7 and C_4, and R_8 and C_5, reduces the bandwidth of the buffer stage. Choosing $R_7 = R_8 = 22\ \Omega$ and $C_4 = C_5 = 82$ pF limits the bandwidth of the buffer stage to 88 MHz. This will not have a significant impact on the carrier signal.

It should be noted that the output current of the DAC is limited to positive values only. The output voltage will therefore have a common-mode DC-offset. However, this should not be a problem as we are working differentially.

4.4 Power Distribution

The carrier generator PCB contains nine linear voltage regulators, as shown in Figure 4.5. The internal logic and PLL's of the FPGA require a 1.2 V and 2.5 V supply, respectively. The FPGA has eight I/O banks and each I/O bank can operate at a different voltage level depending on the circuitry a particular bank has to interface with. The clock operates at 1.8 V, hence there is a 1.8 V I/O bank. There is also a 3.3 V bank for an I/O expansion interface. It was decided to interface with the DAC through 3 V LVCMOS logic, since the maximum output toggle rate of the 3 V logic is significantly faster than that of the 3.3 V logic [36]. The DAC is provided with a 3 V and 5 V digital and analogue supply, respectively. The output buffer op-amps receive a bipolar supply of 5 V per supply rail.

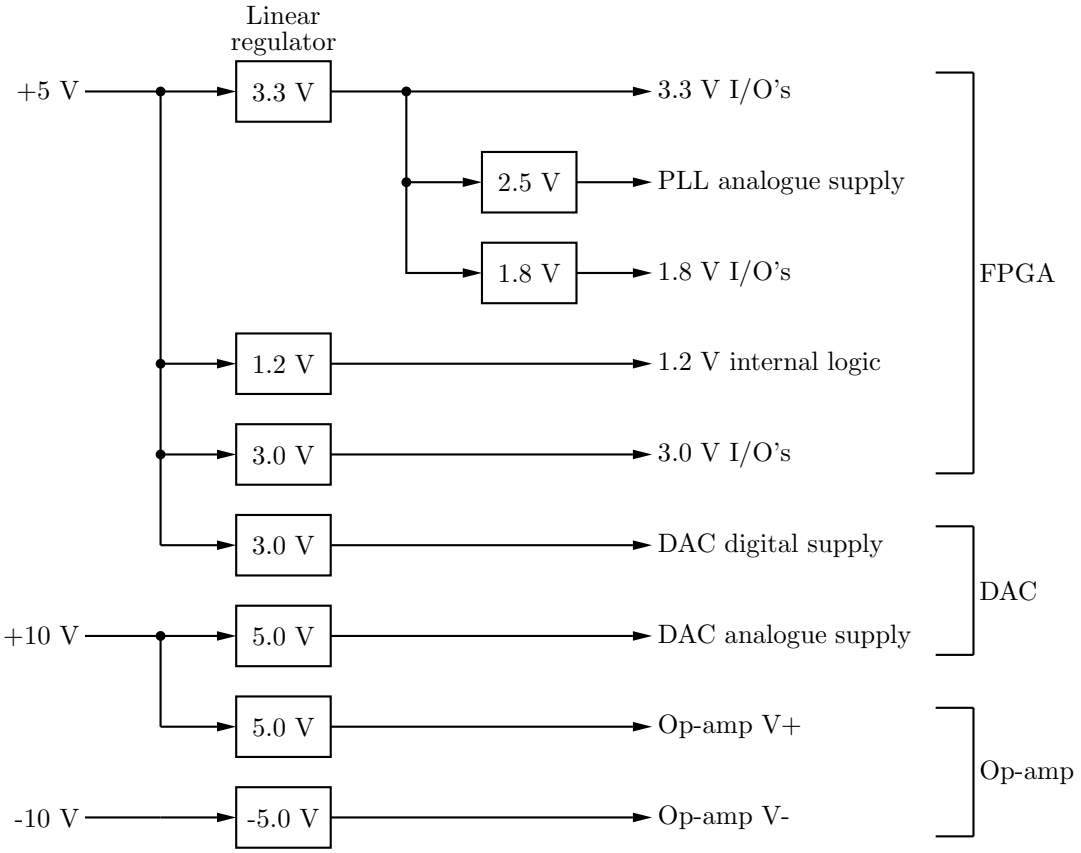


Figure 4.5: Power distribution of the carrier generator board.

4.5 Carrier Data Generation

With reference to Section 2.4, ripple compensation is implemented by filtering the sawtooth carrier by the loop transfer function and adding the resultant signal to the original sawtooth. Additional filtering is required to cancel the effect of the pre-filtering of the

passive inner control loop, as discussed in Section 5.2. The details of the filtering transfer function is discussed in Section 7.9. For now we will assume the sawtooth carrier has to be filtered by an arbitrary transfer function $Q(s)$. The Fourier series of a sawtooth with fundamental frequency f_s is given by [16]

$$c(t) = -\frac{2}{\pi}\sum_{k=1}^{N}\frac{\sin(2\pi k f_s t)}{k}. \tag{4.5.1}$$

Consequently, the Fourier series of the filtered sawtooth is given by

$$c_f(t) = -\frac{2}{\pi}\sum_{k=1}^{N}|Q(j2\pi k f_s)|\frac{\sin(2\pi k f_s t + \angle Q(j2\pi k f_s))}{k}. \tag{4.5.2}$$

The filtered sawtooth is approximated by calculating the Fourier summation up to $N = 63$. The DAC clock frequency of 98.304 MHz is 128 times the fundamental frequency of the sawtooth. Limiting the Fourier summation to 63 terms ensures that the carrier contains no frequency components above the Nyquist frequency, thereby avoiding aliasing. The resulting waveform is discretised in time and quantised to 12 bits.

4.6 Measurements

Figure 4.6 shows the measured output of the waveform generator for a sawtooth carrier. The signal is measured between V_{OUT+} (see Figure 4.2) and ground. The differential amplitude of the sawtooth, measured between V_{OUT+} and V_{OUT-}, is 800 mV peak-to-peak. The Fourier summation is limited to $N = 63$ terms. Note that the ringing at the peaks of the waveform is due to the finite number of Fourier terms included in the summation.

Figure 4.7 shows the output of the waveform generator when $N = 10,000$. Notice that the peaks are now free of ringing. Theoretically the sawtooth waveform generated with $N = 10,000$ contains aliasing components. However, the Nyquist frequency of 49.152 MHz is significantly higher than the fundamental frequency $f_s = 768$ kHz of the sawtooth waveform and the magnitude of the aliased components is small. For the closed-loop amplifier there was no measurable difference between using $N = 63$ or $N = 10,000$.

4.7 Summary

This chapter presented the details of the FPGA-based waveform generator that was designed for generating the carrier signal. Carrier data is generated off-line in MATLAB, stored in a lookup table in the FPGA, and clocked to a high-speed DAC. Measurements were presented that confirmed the operation of the waveform generator.

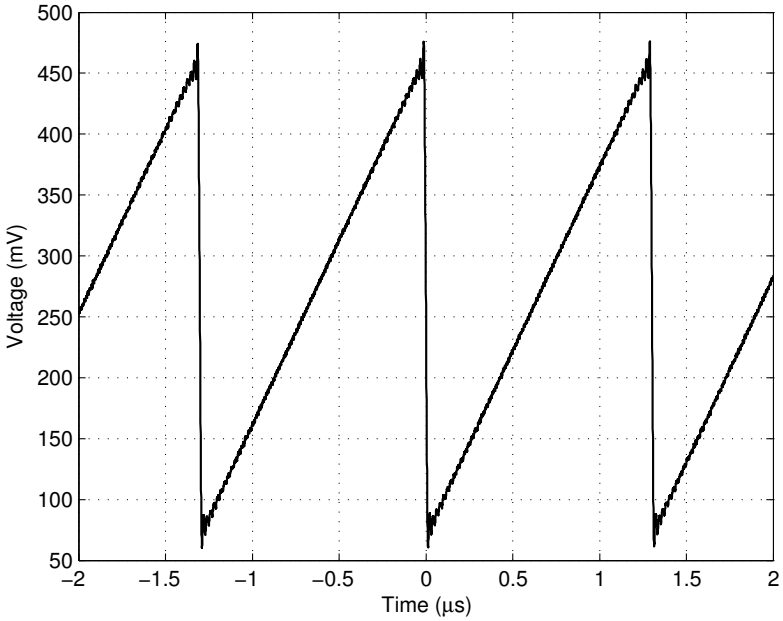


Figure 4.6: Measured carrier generator output at V_{OUT+} for a sawtooth waveform. The Fourier summation is limited to $N = 63$ terms.

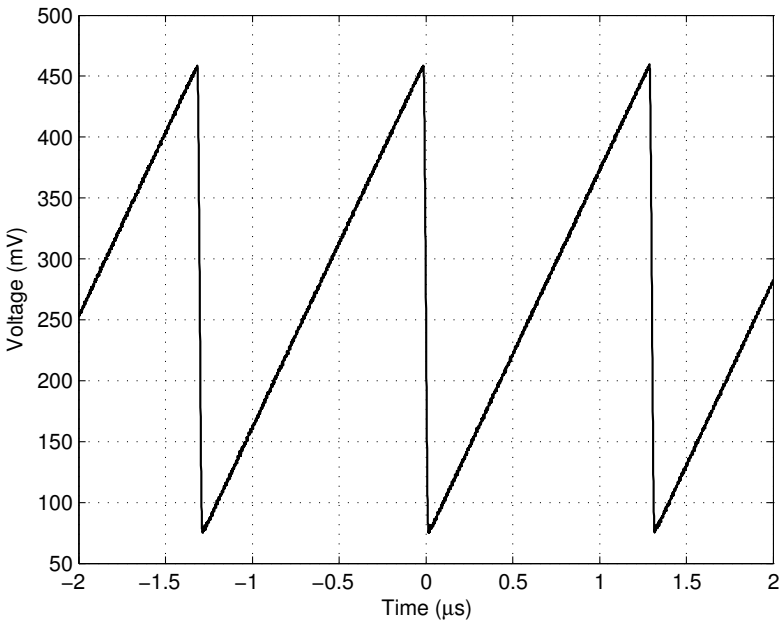


Figure 4.7: Measured carrier generator output at V_{OUT+} for a sawtooth waveform. The Fourier summation is limited to $N = 10,000$ terms.

Chapter 5

Developing the Control Loop Topology

5.1 Introduction

The basic control loop structure follows from Section 2.5 and is shown in Figure 5.1. $K(s)$ contains the power stage and demodulation filter as well as an unconditionally stable control loop. $H(s)$ is a loop filter that provides high gain throughout the audio band. $K'(s)$ is a deviation detector, or estimation filter, that approximates the behaviour of $K(s)$ in the audio band.

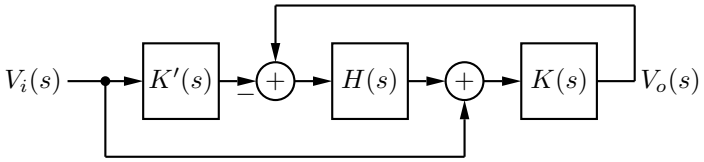


Figure 5.1: Basic control loop structure.

Implementing the control system of Figure 5.1 with actual analogue circuitry requires us to introduce a few additional control blocks. This chapter will expand the basic control loop of Figure 5.1 to include elements that are required for practical implementation. Section 5.2 introduces the basic control system building blocks based on the underlying analogue circuitry. The complete control loop is presented in Section 5.3.

Note that for simplicity all circuits are shown as single-ended implementations. The final implementation, however, will be balanced to improve the rejection of ground noise and other external noise sources. This requires the single-ended equivalent circuits to use shunt feedback. Conversion to a balanced circuit is simply a matter of "mirroring" the passive components with regard to ground. Figure 5.2 illustrates the basic principle for a simple inverting op-amp circuit. A similar transformation applies if fully differential op-amps are used.

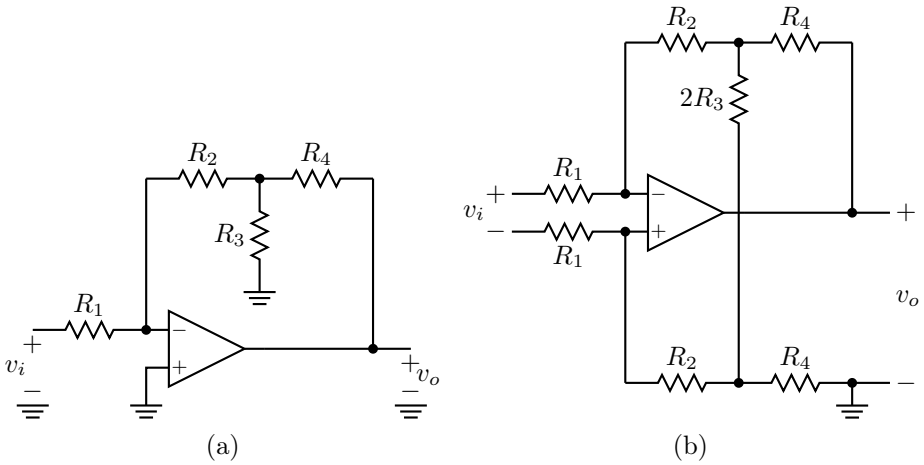


Figure 5.2: Shunt voltage feedback op-amp circuit (a) and its balanced equivalent (b).

5.2 Building Blocks

5.2.1 Output Stage and Inner Feedback Loop

For the control scheme to work effectively the frequency response of $K(s)$, which includes the power stage and demodulation filter, has to be relatively load independent. The frequency response is made load independent by closing a feedback loop around the power stage and demodulation filter. A simple passive lead compensator, as shown in Figure 5.3, is sufficient for this purpose [41]. The circuit receives three input signals: a control input signal from the output of the loop filter, a feed-forward signal from the main amplifier input and the carrier signal. The input summation resistors are selected to be of equal value to simplify design.

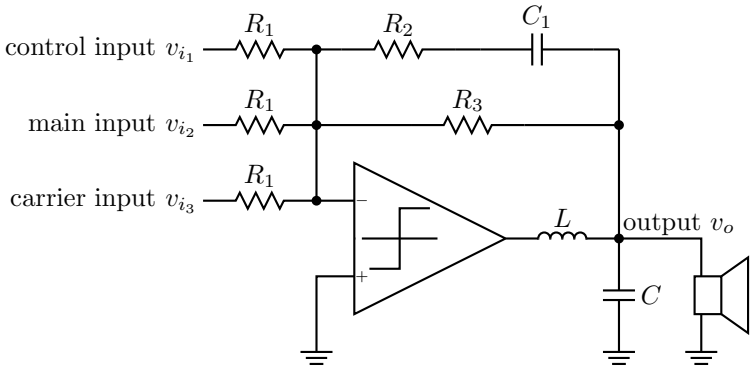


Figure 5.3: Output stage with passive lead compensation.

Figure 5.4 shows the equivalent control system block-diagram of Figure 5.3. We will refer to the feedback loop in Figure 5.4 as the inner loop, and to $H_1(s)$ as the inner loop filter. Note that the passive compensation network causes the input terms to be filtered

by $\frac{1}{3}[1 - H_1(s)]$. The carrier will have to be pre-distorted to compensate for this. V_s is the power stage supply voltage and $F(s)$ is the demodulation filter transfer function.

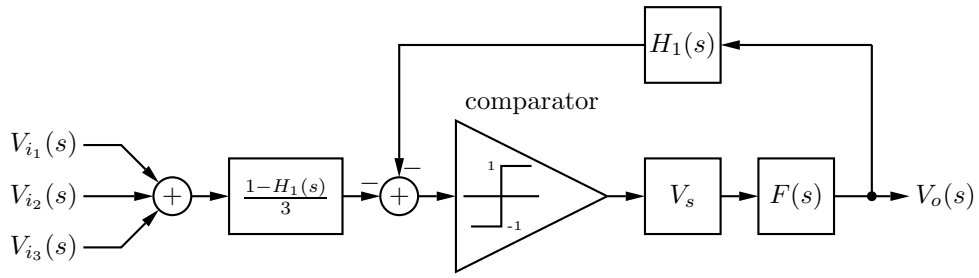


Figure 5.4: Control system block-diagram of output stage with passive compensation.

For the circuit of Figure 5.3 the transfer function of the inner loop filter $H_1(s)$ is given by

$$H_1(s) = \frac{R_1(R_2+R_3)}{3R_2R_3 + R_1(R_2+R_3)} \cdot \frac{s + \dfrac{1}{C_1(R_2+R_3)}}{s + \dfrac{1}{C_1}\dfrac{3R_3+R_1}{3R_2R_3+R_1(R_2+R_3)}} \tag{5.2.1}$$

$$= G_1 \frac{s+\omega_z}{s+\omega_p}, \tag{5.2.2}$$

with $G_1 < 1$ and $\omega_z < \omega_p$.

Assuming the demodulation filter $F(s)$ is an ideal LC filter with a resistive load R_o, its transfer function is given by

$$F(s) = \frac{\frac{1}{LC}}{s^2 + s\frac{1}{R_oC} + \frac{1}{LC}}. \tag{5.2.3}$$

5.2.2 Outer Loop Filter

$K(s)$ includes a feedback loop, with the inner loop filter $H_1(s)$, around the power stage and demodulation filter. We will therefore refer to the loop filter $H(s)$ in Figure 5.1 as the outer loop filter and name it $H_2(s)$. The purpose of the outer loop filter is to improve error rejection by providing an increase in loop gain throughout the audio band. The amount of loop gain achievable is limited by the order of the loop filter and the required stability margins.

The outer loop filter can be implemented in several ways. The simplest loop filter is a single integrator. However, a single integrator is not a very good loop filter because of its limited gain at the upper end of the audio band. The most common approach when implementing a higher order loop filter, is to realise it with a series of integrators [2, 19, 21, 42, 43]. Figure 5.5 shows a typical third-order loop filter topology. Note that

the loop filter can also be extended to higher orders and is similar to that of a $\Sigma\Delta$ modulator [44, 45].

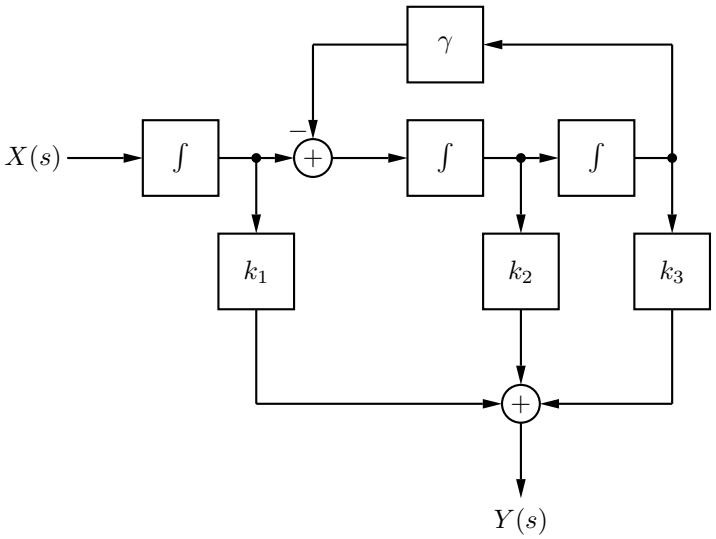


Figure 5.5: Third-order integrating loop filter with local feedback and feed-forward summation.

The transfer function of the loop filter of Figure 5.5 is given by

$$\frac{Y(s)}{X(s)} = \frac{k_1 s^2 + k_2 s + k_3 + k_1\gamma}{s(s^2+\gamma)}. \tag{5.2.4}$$

The loop filter of Figure 5.5 is easy to implement with three active RC op-amp integrators. However, for the third-order case a much simpler circuit yields a similar transfer function. Consider the active filter circuit of Figure 5.6.

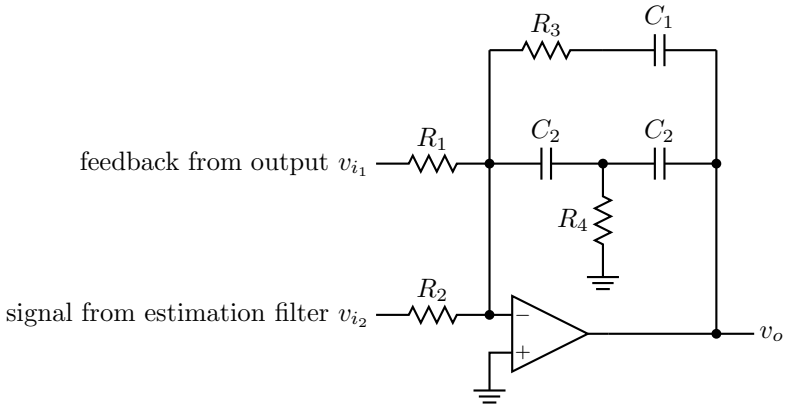


Figure 5.6: Single op-amp third-order integrating loop filter.

The output of the circuit of Figure 5.6 is given by

$$V_o(s) = -\frac{2}{C_2 s}.\frac{\left(s+\frac{1}{2C_2R_4}\right)\left(s+\frac{1}{C_1R_3}\right)}{s^2+\left(\frac{1}{C_1R_3}+\frac{2}{C_2R_3}\right)s+\frac{1}{C_2^2R_3R_4}}.\left[V_{i_1}(s)\frac{1}{R_1}+V_{i_2}(s)\frac{1}{R_2}\right] \tag{5.2.5}$$

$$= -H_2(s)\left[V_{i_1}(s)A + V_{i_2}(s)B\right], \tag{5.2.6}$$

where

$$H_2(s) = \frac{2}{C_2 s}.\frac{\left(s+\frac{1}{2C_2R_4}\right)\left(s+\frac{1}{C_1R_3}\right)}{s^2+\left(\frac{1}{C_1R_3}+\frac{2}{C_2R_3}\right)s+\frac{1}{C_2^2R_3R_4}} \tag{5.2.7}$$

$$= \frac{G_2}{s}.\frac{(s+\omega_{z1})(s+\omega_{z2})}{s^2+\beta_p s+\omega_p^2}, \tag{5.2.8}$$

$$A = \frac{1}{R_1} \tag{5.2.9}$$

and

$$B = \frac{1}{R_2}. \tag{5.2.10}$$

Equation (5.2.8) is similar to (5.2.4), except that the zeros of (5.2.4) can be complex and the complex pole pair of (5.2.4) is fully imaginary. It was decided to use the circuit of Figure 5.6 as outer loop filter due to its simplicity compared to the circuit of Figure 5.5.

Figure 5.7 shows the equivalent control system block-diagram of Figure 5.6, based on (5.2.6). Note that higher order implementations can easily be obtained by cascading multiple circuits.

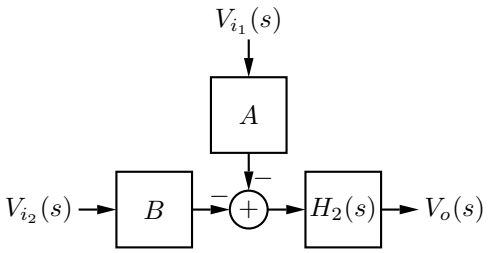


Figure 5.7: Control system block diagram of single op-amp third-order integrating loop filter.

5.2.3 Estimation Filter

The final circuit topology of the estimation filter $K'(s)$ will depend on the closed-loop transfer function of the inner loop. However, if $K'(s)$ is an active filter, the only modification required to the basic loop is the inclusion of an additional gain term b in the

estimation filter. This gives us more freedom in choosing the gain of the estimation filter stage. If we select $bB = A$, the output of the outer loop filter $H_2(s)$ will consist only of components related to the output stage error. However, if the circuit that is responsible for limiting the output of the outer loop filter cannot saturate to a very low level it will be necessary to scale the output level of the loop filter to improve clip recovery. This is done by increasing the magnitude of the loop filter output signal component that is related to the input signal by introducing a mismatch between bB and A.

5.3 The Complete Continuous-Time Control Loop

We can now construct the complete control loop by incorporating Figure 5.4 and Figure 5.7 into Figure 5.1. Figure 5.8 shows the complete control loop. Gain A is chosen to realise the desired loop gain. Gain b is chosen to realise the desired estimation filter stage gain. Gain B is chosen to obtain the desired magnitude of the input signal component present in the outer loop filter output signal. If $B = \frac{A}{b}$, the outer loop filter output will contain only signals related to the output stage error.

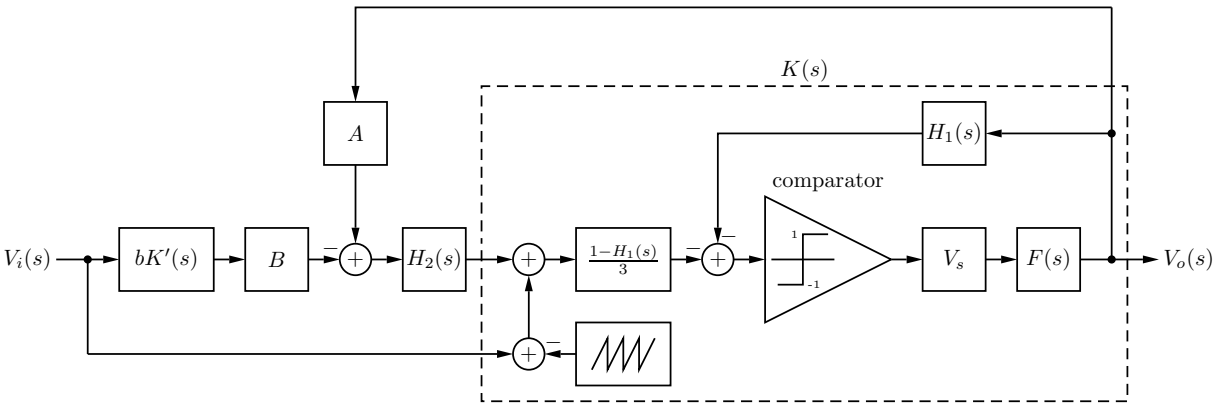


Figure 5.8: Complete control system diagram.

Note that the estimator $K'(s)$ and associated gains b and B are not enclosed in a feedback loop. This means that we can scale the outer loop filter output level without directly affecting the stability and loop gain of the control system. However, this also means that any noise and distortion present in the estimation filter cannot be attenuated by the loop and will be reproduced at the amplifier output.

5.4 Summary

In this chapter the analogue circuitry that is required to implement the control loop was discussed. The control circuit consists of a passive first-order inner loop around the

power switching stage and demodulation filter, and a single op-amp third-order loop filter around the inner loop. The various analogue circuit building blocks were converted to control system blocks and the original general control circuit was expanded to include these additional control blocks.

Chapter 6

Conversion to the Z-Domain

6.1 Introduction

In this chapter the s-domain feedback loop described in Chapter 5 is converted to the z-domain. In Section 6.2 an expression is derived for the transformation between the s- and z-domain. Section 6.3 discusses the calculation of the equivalent gain of the comparator when ripple compensation is implemented. In Section 6.4 the discrete-time comparator model is embedded in the control loop and expressions for the most important transfer functions are derived. The final control loop is a function of both s- and z-domain parameters, with the feedback being only in the z-domain.

6.2 The Impulse Invariant Transform

In Section 2.3 it was said that the continuous-time loop can be converted to its discrete-time equivalent through the impulse invariant transform. The impulse invariant transform involves taking the z-transform of the discretised impulse response of a system. Figure 6.1 illustrates the basic principle.

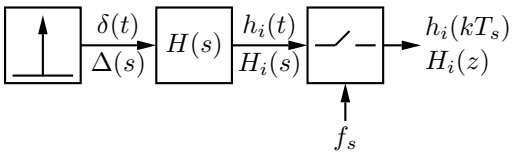


Figure 6.1: Block diagram illustration of the impulse invariant method.

We will assume that the system transfer function is of the form $H(s) = e^{-st_d}\frac{1}{s+a}$, where t_d accounts for a delay in the system. The continuous-time impulse response of $H(s)$ is [17]

$$h_i(t) = e^{-a(t-t_d)}\mu(t-t_d), \tag{6.2.1}$$

where

$$\mu(\tau) = \begin{cases} 0 & \text{if } \tau < 0 \\ 1 & \text{if } \tau \geq 0 \end{cases} \tag{6.2.2}$$

The corresponding discrete-time impulse response is obtained by letting $t = kT_s$:

$$h_i(kT_s) = e^{-a(kT_s - t_d)}\mu(kT_s - t_d), \quad k = 0, 1, 2, ... \tag{6.2.3}$$

Figure 6.2 shows the continuous- and discrete-time impulse responses of $H(s)$. As noted in Section 2.3, the time delay t_d causes the first sample of the discrete-time impulse response to be zero.

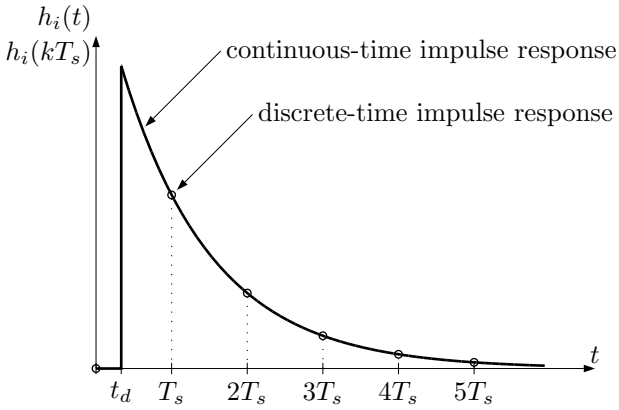


Figure 6.2: Continuous-time and discrete-time impulse responses.

Assuming $0 < t_d < T_s$, the z-transform of (6.2.3) is given by

$$\begin{aligned} H_i(z) &= \sum_{k=0}^{\infty} h_i(kT_s)z^{-k} \\ &= \sum_{k=0}^{\infty} e^{-a(kT_s - t_d)}\mu(kT_s - t_d)z^{-k} \\ &= 0 + e^{-a(T_s - t_d)}\mu(T_s - t_d)z^{-1} + e^{-a(2T_s - t_d)}\mu(2T_s - t_d)z^{-2} + \\ &\quad e^{-a(3T_s - t_d)}\mu(3T_s - t_d)z^{-3} + ... \\ &= e^{-aT_s}e^{at_d}z^{-1} + e^{-2aT_s}e^{at_d}z^{-2} + e^{-3aT_s}e^{at_d}z^{-3} + ... \\ &= e^{at_d}\left[-1 + 1 + (e^{-aT_s}z^{-1}) + (e^{-aT_s}z^{-1})^2 + (e^{-aT_s}z^{-1})^3 + ...\right] \\ &= e^{at_d}\left(-1 + \sum_{k=0}^{\infty}(e^{-aT_s}z^{-1})^k\right). \end{aligned} \tag{6.2.4}$$

The infinite series sum in (6.2.4) can be expressed in a closed form [46]:

$$\sum_{k=0}^{\infty}(e^{-aT_s}z^{-1})^k = \frac{1}{1 - e^{-aT_s}z^{-1}}. \tag{6.2.5}$$

Substituting (6.2.5) into (6.2.4) and simplifying yields

$$H_i(z) = e^{at_d}\frac{e^{-aT_s}}{z - e^{aT_s}} \tag{6.2.6}$$

We now have a transformation between the s-domain and z-domain:

$$e^{-st_d}\frac{1}{s+a} \Leftrightarrow e^{at_d}\frac{e^{-aT_s}}{z - e^{-aT_s}} \tag{6.2.7}$$

Note that even though it was assumed that $0 < t < T_s$, it can be shown that (6.2.7) is also valid for $t_d = 0$. Since the z-transform is a summation, (6.2.7) can be expressed in a more general form as

$$e^{-st_d}\sum_{i=1}^{n}\frac{1}{s+a_i} \Leftrightarrow \sum_{i=1}^{n} e^{a_i t_d}\frac{e^{-a_i T_s}}{z - e^{-a_i T_s}} \tag{6.2.8}$$

For loop design and analysis purposes, it will be convenient to match the DC gain of the transfer function in the s- and z-domain. This is done by multiplying the z-domain transfer function with the sample period T_s:

$$e^{-st_d}\sum_{i=1}^{n}\frac{1}{s+a_i} \Leftrightarrow T_s\sum_{i=1}^{n} e^{a_i t_d}\frac{e^{-a_i T_s}}{z - e^{-a_i T_s}} \tag{6.2.9}$$

Transfer functions that can be written in the form

$$\sum_{i=1}^{n}\frac{r_i}{s+a_i} \tag{6.2.10}$$

can be transformed to the z-domain using (6.2.9). Transfer functions of the form

$$G(s) = \frac{s^m + \beta_{m-1}s^{m-1} + ... + \beta_1 s + \beta_0}{s^n + \alpha_{n-1}s^{n-1} + ... + \alpha_1 s + \alpha_0} \tag{6.2.11}$$

can be written in the form of (6.2.10) by means of partial fraction expansion if $M < N$ and if the poles are distinct [47].

6.3 Calculating the Comparator Gain

In Section 2.3 it was shown that the ideal comparator can be modelled by a sampling operation followed by a gain K. For a triangle carrier the equivalent comparator gain K is given by

$$K = \frac{4V_s f_s}{|\dot{r}_0|}. \tag{6.3.1}$$

For a triangle carrier the reference signal is sampled twice in a single cycle of the carrier waveform. However, when a sawtooth carrier is used, the reference signal is sampled only once per carrier cycle. It therefore follows that, for a sawtooth carrier,

$$K = \frac{2V_s f_s}{|\dot{r}_0|}. \tag{6.3.2}$$

Since ripple compensation involves the modification of the ripple feedback signal, it will have an influence on the equivalent comparator gain. Figure 6.3 shows a feedback loop with ripple compensation. The power stage, demodulation filter and inner loop filter are all incorporated into $L(s)$. It is assumed that the demodulation filter is of second order and that the loop filter has at least as many poles as zeros. The gain A_s sets the amplitude of the carrier at the comparator input. We will now proceed to calculate the value of K for the loop of Figure 6.3.

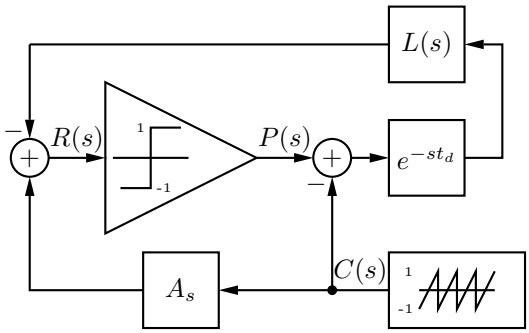


Figure 6.3: Block diagram for comparator gain calculation.

The Fourier series representation of the sawtooth carrier and steady-state comparator output, which is a square wave, is given by [46]

$$c(t) = -\frac{2}{\pi}\sum_{k=1}^{\infty}(-1)^k\frac{\sin 2\pi f_s kt}{k} \tag{6.3.3}$$

and

$$p(t) = \frac{4}{\pi}\sum_{k=1,3,5,\ldots}^{\infty}\frac{\sin 2\pi f_s kt}{k}, \tag{6.3.4}$$

respectively.

The steady-state output of an LTI system with transfer function $H(s)$ and input $x(t) = A\cos(\omega t + \phi)$ is

$$y_{ss}(t) = A|H(j\omega)|\cos[\omega t + \phi + \theta(\omega)], \tag{6.3.5}$$

where $\theta(\omega)$ is the angle of $H(j\omega)$ [16].

Using (6.3.5) we can express the steady-state input to the comparator as

$$r_{ss}(t) = r_1(t) + r_2(t) + r_3(t), \tag{6.3.6}$$

with

$$r_1(t) = -\frac{2A_s}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^k}{k}\sin 2\pi f_s kt, \tag{6.3.7}$$

$$r_2(t) = -\frac{2}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^k}{k}|L(j2\pi f_s k)|\sin[2\pi f_s k(t-t_d) + \theta_L(kf_s)], \tag{6.3.8}$$

and

$$r_3(t) = -\frac{4}{\pi}\sum_{k=1,3,5,\ldots}^{\infty}\frac{1}{k}|L(j2\pi f_s k)|\sin\left[2\pi f_s k(t-t_d)+\theta_L(kf_s)\right]. \tag{6.3.9}$$

Note that $r_1(t)$ is an amplitude scaled version of the carrier, $r_2(t)$ is the carrier propagated through the loop and $r_3(t)$ is the comparator output propagated through the loop.

We now need to find the derivative of $r_{ss}(t)$ and evaluate it at $t = 0$. Note that $p(t)$ is discontinuous at $t = 0$ and therefore its derivative is undefined at $t = 0$. However, the signal $r_3(t)$ arriving at the comparator input is delayed by t_d and therefore its derivative does exist at $t = 0$. The slope of the sawtooth waveform that adds directly at the comparator input does not have to be approximated, and is given by

$$\left.\frac{dr_1(t)}{dt}\right|_{t=0} = 2A_s f_s. \tag{6.3.10}$$

The slope of the filtered carrier and comparator output signal is given by

$$\left.\frac{dr_2(t)}{dt}\right|_{t=0} = -4f_s\sum_{k=1}^{\infty}(-1)^k|L(j2\pi f_s k)|\cos[\theta_L(kf_s)-2\pi f_s k t_d] \tag{6.3.11}$$

and

$$\left.\frac{dr_3(t)}{dt}\right|_{t=0} = -8f_s\sum_{k=1,3,5,\ldots}^{\infty}|L(j2\pi f_s k)|\cos[\theta_L(kf_s)-2\pi f_s k t_d], \tag{6.3.12}$$

respectively. We can now calculate $\dot{r}_0$:

$$\dot{r}_0 = \left.\frac{dr_1(t)}{dt}\right|_{t=0} + \left.\frac{dr_2(t)}{dt}\right|_{t=0} + \left.\frac{dr_3(t)}{dt}\right|_{t=0}. \tag{6.3.13}$$

The transfer function $L(s)$ contains the second order demodulation filter and the loop filter. The signals $p(t)$ and $c(t)$ will see the pole pair of the demodulation filter as a double integrator. Hence the signals $r_2(t)$ and $r_3(t)$ will be approximately sinusoidal and we can approximate them by their fundamental components. The first-order approximation for the derivative of $r_{ss}(t)$ when the comparator output changes state is

$$\dot{r}_{0_1} = 2f_s\left(A_s - 2|L(2\pi f_s)|\cos\left[2\pi f_s t_d - \theta_L(f_s)\right]\right). \tag{6.3.14}$$

Substituting (6.3.14) into (6.3.2), we obtain

$$K_1 = \frac{V_s}{|A_s - 2|L(2\pi f_s)|\cos\left[2\pi f_s t_d - \theta_L(f_s)\right]|} \tag{6.3.15}$$

An important point that should be noted is that the outer loop will have a negligible effect on the comparator gain. This is because the outer loop filter has a low-pass filter characteristic, while the inner loop filter does not. Consequently, the ripple component at the output of the outer loop filter will be negligible compared to the ripple component at the output of the inner loop filter.

6.4 Embedding the Discrete-Time Comparator Model in the Control Loop

We will assume that the carrier has been pre-filtered by a transfer function $\frac{3}{1-H_1(s)}$. This cancels the filtering of the carrier by the passive compensation network so that the carrier is effectively added directly at the comparator input.

Figure 6.4 shows the continuous-time inner loop. Error source $E_p(s)$ models timing errors in the power switching stage, which is the dominant source of distortion in an open-loop class-D amplifier. The power stage supply voltage V_s and the propagation delay t_d of the active electronics are integrated into the comparator.

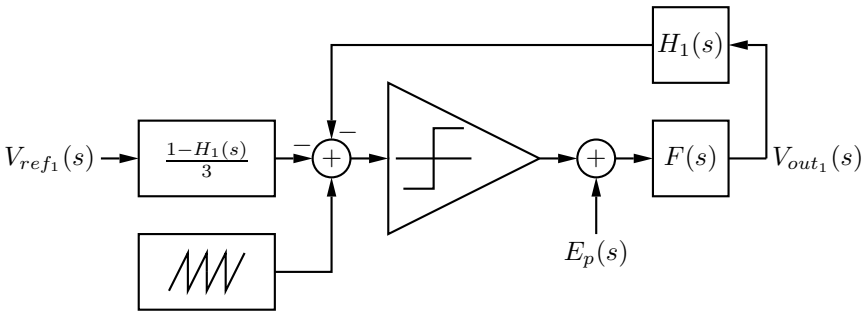


Figure 6.4: Continuous-time inner loop.

Figure 6.5 shows the loop of Figure 6.4 converted to the z-domain as per Section 2.3, with the only difference being the addition of an impulse reconstructor. The impulse reconstructor is effectively a DAC that converts the discrete-time impulses to continuous-time impulses. The impulse reconstructor is followed by the propagation delay t_d and the demodulation filter $F(s)$.

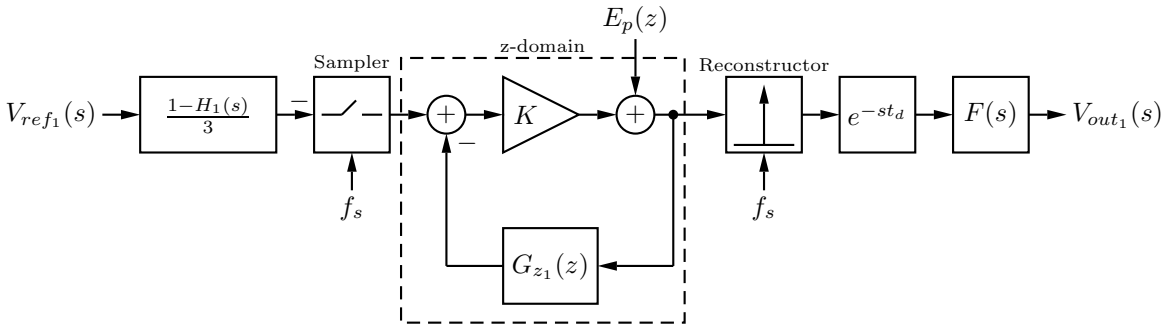


Figure 6.5: Inner loop with sampling comparator model.

In Figure 6.5, $G_{z1}(z)$ is the impulse-invariant transform of $F(s)H_1(s)e^{-st_d}$, or

$$G_{z_1}(z) = \mathcal{Z}_i\{F(s)H_1(s)e^{-st_d}\}. \tag{6.4.1}$$

The transfer function from input $V_{ref_1}(s)$ to output $V_{out_1}(s)$ is given by

$$\begin{aligned} STF_1(f) &= \frac{V_{out_1}(f)}{V_{ref_1}(f)} \\ &= -\frac{1-H_{s_1}(s)}{3}.\frac{KF_s(s)e^{-st_d}}{1+KG_{z_1}(z)}\bigg|_{s=j2\pi f,\, z=e^{j2\pi fT_s}}. \end{aligned} \tag{6.4.2}$$

Note that the transfer function of the estimation filter $K'(s)$ has to approximate $STF_1(f)$ in the audio band. The transfer function from error source $E_p(z)$ to output $V_{out_1}(s)$ is given by

$$\begin{aligned} ETF_1(f) &= \frac{V_{out_1}(f)}{E_p(f)} \\ &= \frac{F(s)e^{-st_d}}{1+KG_{z_1}(z)}\bigg|_{s=j2\pi f,\, z=e^{j2\pi fT_s}}. \end{aligned} \tag{6.4.3}$$

Figure 6.6 shows the complete continuous-time control loop and Figure 6.7 its discrete-time equivalent. In Figure 6.7, $G_{z_1}(z)$ is given by (6.4.1) and $G_{z_2}(z)$ is given by

$$G_{z_2}(z) = \mathcal{Z}_i\left\{\frac{A}{3}F(s)\left[1-H_1(s)\right]H_2(s)e^{-st_d}\right\}. \tag{6.4.4}$$

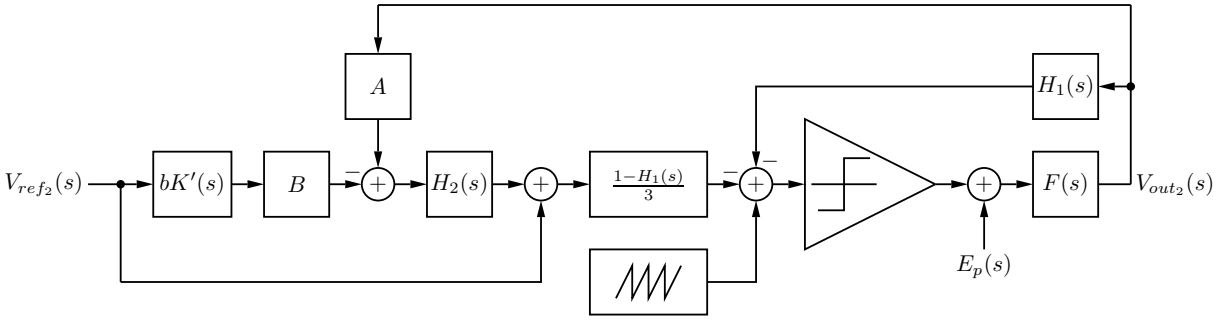


Figure 6.6: Continuous-time complete loop.

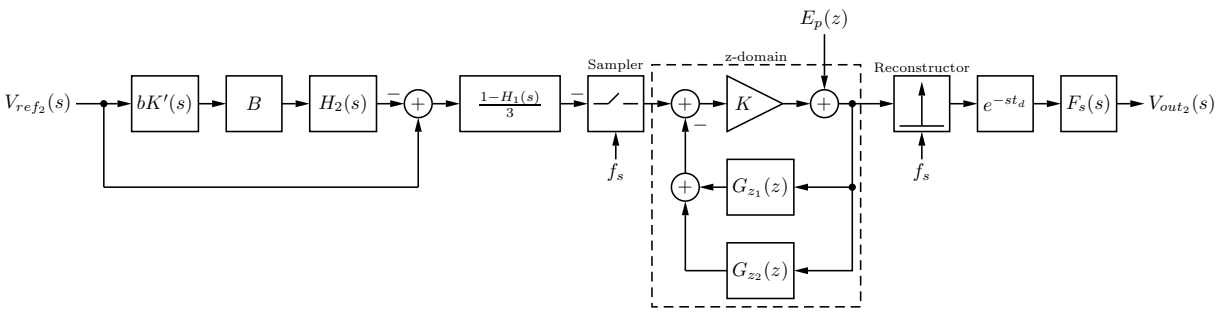


Figure 6.7: Complete loop with sampling comparator model.

The transfer function from input $V_{ref_2}(s)$ to output $V_{out_2}(s)$ is given by

$$STF_2(f) = \frac{V_{out_2}(f)}{V_{ref_2}(f)} \tag{6.4.5}$$

$$= -\frac{K}{3}.\frac{[1 - bBK'(s)H_2(s)][1 - H_1(s)]F(s)e^{-st_d}}{1 + K[G_{z_1}(z) + G_{z_2}(z)]}\bigg|_{s=j2\pi f,\, z=e^{j2\pi fT_s}}. \tag{6.4.6}$$

The transfer function from error source $E_p(z)$ to output $V_{out_2}(s)$ is given by

$$ETF_2(f) = \frac{V_{out_2}(f)}{E_p(f)}$$

$$= \frac{F(s)e^{-st_d}}{1 + K[G_{z_1}(z) + G_{z_2}(z)]}\bigg|_{s=j2\pi f,\, z=e^{j2\pi fT_s}}. \tag{6.4.7}$$

Inspection of (6.4.3) and (6.4.7) shows that we need to maximise the comparator gain and the gain of the loop filters to reduce the magnitude of the error transfer functions. Note that since the inner loop filter is passive, the comparator, which includes the power stage, is the only element that contributes gain to the inner loop.

6.5 Summary

In this chapter the discrete-time comparator model was embedded into the control loop developed in Chapter 5. The feedback loops are converted to discrete-time through the impulse invariant transform. The effect of ripple compensation on comparator gain was considered and a first-order approximation to the comparator gain was derived. General forms of the signal transfer functions (STFs) and error transfer functions (ETFs) for both the inner loop and complete loop were presented.

Chapter 7

Control Loop Design

7.1 Introduction

This chapter covers the design of the control loop. The load presented to the amplifier by the loudspeaker, and how it affects stability, is investigated. Thereafter an optimal control loop is designed and analysed. Component values for the control circuitry are calculated. Finally, the carrier pre-distortion transfer function is presented.

7.2 The Load and its Effect on Stability

The frequency response of the demodulation filter is load dependent. Since the demodulation filter is enclosed in the feedback loop, we need to consider how a change in load will affect stability. If we model the load as a resistor R and take the effect of the equivalent series resistance R_L of the inductor into account, the transfer function of the second-order LC demodulation filter is given by

$$F(s) = \frac{R}{R + R_L} \cdot \frac{\left(1 + \frac{R_L}{R}\right)\frac{1}{LC}}{s^2 + s\left(\frac{R_L}{L} + \frac{1}{RC}\right) + \left(1 + \frac{R_L}{R}\right)\frac{1}{LC}} \tag{7.2.1}$$

The resistance R_L forms a voltage divider with the load resistance R, which reduces the overall loop gain. If the loop is unconditionally stable, this reduction in loop gain reduces the gain margin of the system. Lowering the load resistance increases the damping of the demodulation filter. This increases the phase margin since the demodulation filter now contributes less phase shift at the unity-gain frequency of the loop. When the load resistance is increased, the opposite happens: loop gain is increased, which increases gain margin, but phase margin is reduced. Note that the resonant frequency becomes load dependant if $R_L \neq 0$. Compared to the other aforementioned factors, the slight change in resonant frequency does not significantly affect stability.

A loudspeaker is, however, not a purely resistive load. Figure 7.1 shows a simplified equivalent circuit of a moving-coil transducer [48]. Inductance L_E and resistance R_E are the inductance and resistance of the voice coil, respectively. Capacitance C_P, resistance R_P and inductance L_P are the electrical analogies of mechanical properties of the speaker, and are given by

$$C_P = \frac{M_{MS}}{(Bl)^2}, \tag{7.2.2}$$

$$R_P = \frac{(Bl)^2}{R_{MS}} \tag{7.2.3}$$

and

$$L_P = C_{MS}(Bl)^2, \tag{7.2.4}$$

where M_{MS} is the equivalent mass of the cone, C_{MS} is the suspension compliance, R_{MS} is the mechanical resistance of the system and Blu (u is velocity) is the electromotive force due to the movement of the speaker coil through the magnetic field of the motor [48]. Note that the equivalent circuit model of Figure 7.1 neglects eddy currents in the iron core and skin-effect in the coil of the loudspeaker, but it is sufficient for our purposes.

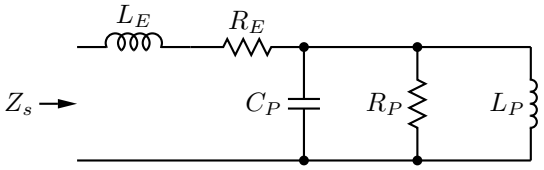


Figure 7.1: Simplified equivalent circuit of a moving-coil transducer.

The loudspeaker impedance Z_s has a low-frequency resonance where the impedances of the parallel capacitor C_P and inductor L_P cancel. At frequencies significantly higher than the resonant frequency the capacitor C_P is effectively a short-circuit and the impedance can be approximated by the series combination of L_E and R_E. Figure 7.2 shows the modelled impedance Z_s of a typical loudspeaker [49], based on Figure 7.1. The first-order approximation, where Z_s is the series combination of L_E and R_E, is also shown. The component values for the equivalent circuit are given in Table 7.1. The quoted nominal impedance of the loudspeaker is 8 Ω [49].

For control purposes, we are concerned with the transfer function of the demodulation filter at frequencies above the audio band, because this is where stability margins will be determined. Inspection of Figure 7.2 shows that we clearly cannot model the loudspeaker as an 8 Ω resistive load when designing the control loop. A high-order control loop designed with tight stability margins for an 8 Ω resistive load will most likely not be

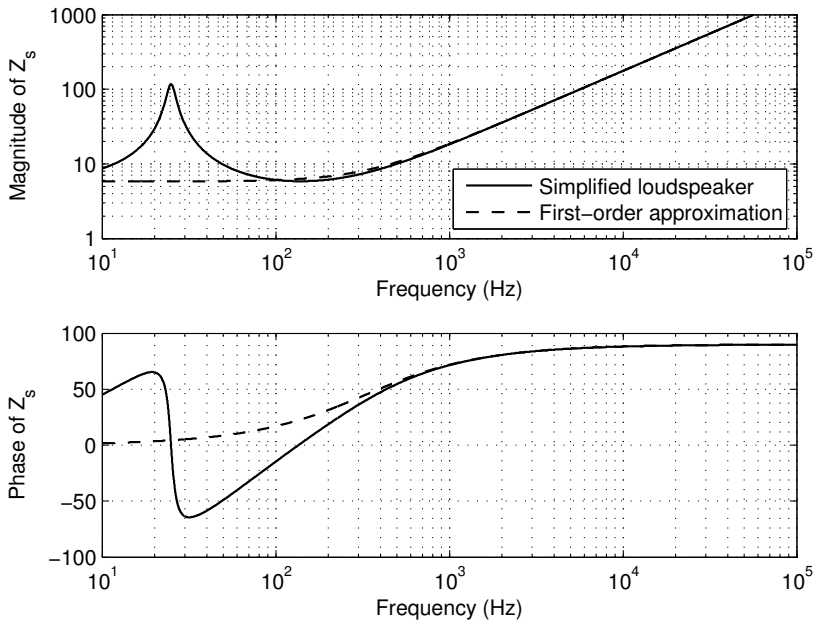


Figure 7.2: Calculated impedance of the simplified loudspeaker and the first-order approximation.

Table 7.1: Component values for loudspeaker equivalent circuit.

Component	Value
L_E	2.8 mH
R_E	5.8 Ω
C_P	511 μF
R_P	112 Ω
L_P	79.7 mH

stable into an actual moving coil transducer rated at 8 Ω. At the unity-gain frequency of the control loop, which will be above 20 kHz, the impedance of the loudspeaker is dominated by the inductance of the voice-coil and is much greater than 8 Ω. In fact, with regard to stability, the loudspeaker looks more like an open-circuit than an 8 Ω load.

Figure 7.3 shows the frequency response of the demodulation filter for different output loads. The frequency response with an 8 Ω loudspeaker load and a 100 kΩ resistive load is indiscernible. The frequency response with an 8 Ω resistive load is shown in grey for comparison. From Figure 7.3 we also see that, if the unity gain crossover frequency of the control loop is below 100 kHz, phase margin will be reduced when an 8 Ω loudspeaker rather than an 8 Ω resistive load is connected to the demodulation filter.

We might consider adding an impedance-correction network in parallel with the loudspeaker to reduce the phase shift at the unity-gain frequency, and thereby increase the phase margin for high-impedance loads. However, in this particular design the resonant

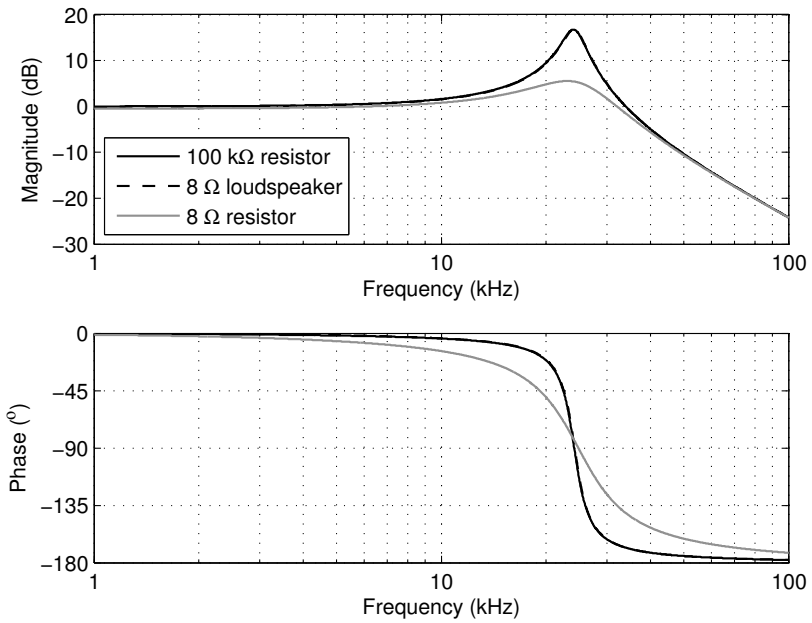


Figure 7.3: Calculated demodulation filter transfer function for a 100 kΩ resistor, an 8 Ω loudspeaker, and an 8 Ω resistor as load, respectively.

frequency of the demodulation filter is not far above the audio band and significant audio-band energy will have to be dissipated in the compensation network if it is to have any effect. Adding an impedance-correction network at the amplifier output is therefore not an option.

Many loudspeaker systems contain more than one transducer and a passive crossover filter network that may or may not flatten the impedance of the loudspeaker system. If the loudspeaker system contains a crossover network with an impedance-correction network, the loudspeaker will more closely represent a resistive load with value equal to the rated impedance of the loudspeaker.

To summarise, the worst-case load with regard to phase margin is an open-circuit, and with regard to gain margin is a low-impedance load. A loudspeaker can present itself as either of these. It was decided to design the amplifier to be stable for all resistive loads from 2 Ω to infinity. This should be enough to ensure that the amplifier is stable into all conventional loudspeaker loads rated 4 Ω and higher.

7.3 Design Strategy

In a high-order control loop there are many free variables and to achieve maximum performance some form of optimisation is required. However, there are a few constraints that have to placed on the optimisation. It is noted that the impulse invariant transform of (6.2.9) provides a direct mapping between s-domain and z-domain poles through the equa-

tion $z_i = e^{-a_i T_s}$, where z_i is the z-domain pole location. However, the mapping of zeros is not so simple and depends on the residues obtained through partial fraction expansion of the transfer function. In fact, the number of zeros in the s-domain and z-domain is not necessarily equal. In an analogue control loop the form of the s-domain equivalent of the z-domain transfer function is dictated by the analogue circuitry. This makes it difficult to design the control loop by placing poles and zeros directly in the z-domain, since the s-domain equivalent will most likely not be implementable. The fact that we have a nested feedback loop makes the process even more complicated. It was therefore decided to design the loop through an iterative process of converting different s-domain loops with the correct form to the z-domain, analysing their z-domain behaviour, and selecting the optimal solution.

Theoretically it is possible to optimise both loops and all free variables simultaneously for a given set of constraints, but to be practical this would require a greatly optimised optimisation algorithm − which is a subject in itself. Instead the inner loop is designed and optimised to meet a set of specifications and the outer loop is then optimised around the inner loop.

The optimisation algorithm works by sweeping selected variables of the s-domain transfer function, analysing the z-domain behaviour, and identifying those solutions that meet or exceed a specified set of requirements. For the inner loop the gain of $H_1(s)$ is chosen and the pole and zero positions are swept from 30 kHz to 384 kHz ($\frac{f_s}{2}$), with the frequency of the pole being greater than the frequency of the zero. For the outer loop the frequency of the complex pole pair is chosen and the positions of the zeros are swept. The one zero is swept from 100 Hz to the frequency of the complex pole pair. The other zero is swept from 30 kHz to 384 kHz. The design requirements that are used as constraints in the optimisation algorithm are listed in Table 7.2. In addition to the requirements in Table 7.2, the inner loop must be unconditionally stable. The requirements in Table 7.2 are for an open-circuit load, since this was found to be the most difficult load with regard to stability. A propagation delay of $t_d = 150$ ns is assumed. Note that the stability of the final loop will have to be verified for all specified loads and possible values of t_d.

It should be noted that the development and implementation of the control loop went through several iterations before arriving at its final form. The values chosen in Table 7.2 are based on the practical evaluation of several design iterations.

In Section 2.5 it was mentioned that the inner loop requires enough loop gain to make its closed-loop frequency response relatively insensitive to load variations. Choosing $|ETF_1(f)|_{max} \leq -25$ dB means that the inner loop will have at least 25 dB of loop gain. To a rough approximation, with 25 dB of loop gain a 6 dB variation in the open loop frequency response will be reduced to a 0.234 dB variation in the closed-loop frequency

Table 7.2: Optimisation constraints.

Parameter	Desciption	Value
$\|ETF_1(f)\|_{max}$	Maximum value of inner loop error transfer function magnitude in the audio band	≤ -25 dB
$\|ETF_2(f)\|_{max}$	Maximum value of complete loop error transfer function magnitude in the audio band	≤ -50 dB
GM_1	Gain margin of inner loop	≥ 5 dB
PM_1	Phase margin of inner loop	$\geq 25°$
GM_2	Gain margin of complete loop	≥ 3 dB
PM_2	Phase margin of complete loop	$\geq 24°$

response, which should be sufficient. Ideally, with $|ETF_2(f)|_{max} \leq -50$ dB we expect the open loop THD+N level of 0.3% for 10 W into 8.2 Ω to be reduced by 50 dB to about 0.0009%.

7.4 Selecting the Switching Frequency

The switching frequency should be significantly higher than the bandwidth of the reference signal, which is 20 kHz. Increasing the switching frequency increases the achievable loop gain for a given set of stability margins. However, a higher switching frequency leads to increased distortion due to PTEs (primarily dead-time) and increased switching losses. In this particular design the switching frequency is selected based on the required loop gain of the inner loop. It was found that a switching frequency of $f_s = 768$ kHz allows us to achieve the gain and stability specifications as listed in Table 7.2. The particular value of $f_s = 768$ kHz is chosen, because it allows the generation of a 128 samples per cycle sawtooth when the FPGA and DAC of the carrier generator is clocked at 98.304 MHz.

7.5 The Optimal Loop

7.5.1 The Inner Loop

Figure 7.4 again shows the passive compensation of the inner loop. The transfer function of the inner loop filter $H_1(s)$ is given by

$$H_1(s) = G_1 \frac{s + \omega_z}{s + \omega_p}. \tag{7.5.1}$$

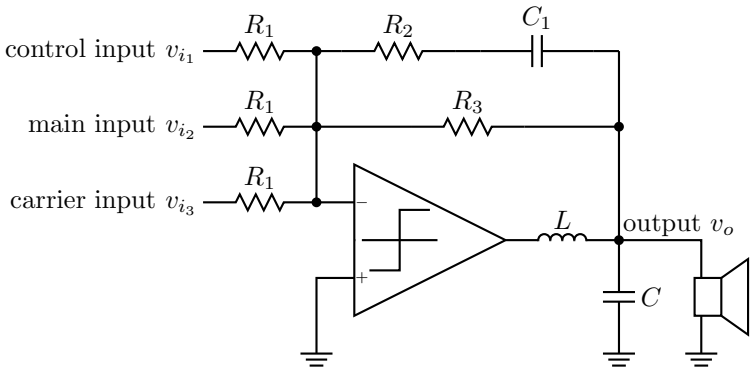


Figure 7.4: Output stage with single pole passive lead compensation.

Due to the passive summation network the input signals are filtered by the transfer function

$$\frac{1-H_1(s)}{3} = \frac{1-G_1}{3}.\frac{s+\frac{\omega_p-\omega_z}{1-G_1}}{s+\omega_p} \tag{7.5.2}$$

$$= A_p P(s), \tag{7.5.3}$$

where

$$A_p = \frac{1-G_1}{3} \tag{7.5.4}$$

and

$$P(s) = \frac{s+\frac{\omega_p-\omega_z}{1-G_1}}{s+\omega_p}. \tag{7.5.5}$$

During carrier generation the carrier is pre-filtered by a transfer function $\frac{1}{P(s)}$, such that the carrier is effectively added directly at the comparator input and scaled by a gain A_p (see Section 7.9). The carrier arriving at the comparator input has an amplitude of $A'_s = A_s A_p$, where A_s is the carrier amplitude at the output of the carrier generator. The component values for the circuit of Figure 7.4 are given by

$$R_1 = \frac{3G_1(\omega_p-\omega_z)}{C_1(G_1\omega_z-\omega_p)^2}, \tag{7.5.6}$$

$$R_2 = \frac{1-G_1}{C_1(\omega_p-G_1\omega_z)} \tag{7.5.7}$$

and

$$R_3 = \frac{\omega_p-\omega_z}{C_1\omega_z(\omega_p-G_1\omega_z)}. \tag{7.5.8}$$

The value of capacitor C_1 can be freely chosen. Note that the resistor values scale inversely proportional to C_1. We want to keep the resistor values as small as possible

to minimise Johnson noise and to minimise the interaction with the non-linear input impedance of the comparator, but large enough to ensure that the preceding stages are not excessively loaded.

The high-frequency gain of the inner loop filter is chosen as $G_1 = 0.26$ and the sawtooth amplitude is chosen as $A_s = 300$ mV. From (7.5.4) it follows that $A_p = 0.247$, and hence the effective carrier amplitude is $A'_s = 74$ mV. The swept parameters for optimisation are ω_z and ω_p. Table 7.3 shows the component values and loop characteristics for the optimal component values and for the selected standard value components. Note that ten terms were used in the Fourier approximation of the comparator gain K.

Table 7.3: Inner loop component and parameter values.

Item	Optimal value	Standard component value
R_1	1.086 kΩ	1.1 kΩ
R_2	1.244 kΩ	1.1 kΩ
R_3	5.98 kΩ	5.6 kΩ
C_1	270 pF	270 pF
G_1	0.26	0.285
ω_z	513 krad/s	553 krad/s
ω_p	2.34 Mrad/s	2.56 Mrad/s
$\lvert ETF_1(f)\rvert_{max}$	-26.4 dB	-27.2 dB
GM_1	5.15 dB	4.59 dB
PM_1	26.6°	25.6°
K	50.9 dB	51.1 dB

7.5.2 The Outer Loop

Figure 7.5 shows the circuit that realises the difference amplifier and outer loop filter. The transfer function of the outer loop filter is given by

$$H_2(s) = \frac{G_2}{s}.\frac{(s+\omega_{z1})(s+\omega_{z2})}{s^2+\beta_p s+\omega_p^2}. \tag{7.5.9}$$

The component values for the circuit of Figure 7.5 are given by

$$R_1 = \frac{1}{A} \tag{7.5.10}$$

$$R_3 = \frac{2\omega_{z_1}}{C_2\omega_0^2} \tag{7.5.11}$$

$$R_4 = \frac{1}{2C_2\omega_{z_1}} \tag{7.5.12}$$

and

$$C_1 = \frac{C_2\omega_0^2}{2\omega_{z_1}\omega_{z_2}}. \tag{7.5.13}$$

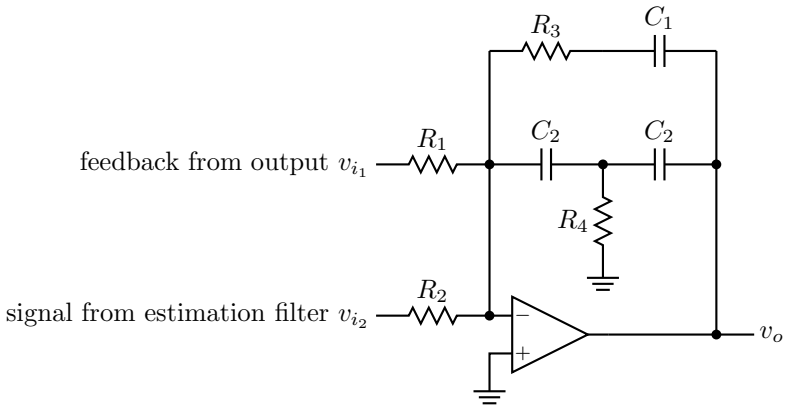


Figure 7.5: Single op-amp third-order integrating loop filter.

Capacitor C_2 can be freely chosen. The value of resistor R_2 is selected to optimise the clipping behaviour of the amplifier and is determined in Section 7.7. The frequency of the complex pole pair is chosen as $\omega_0 = 94.2$ krad/s. The swept parameters are ω_{z_1} and ω_{z_2}, as well as the product of the feedback gain term A and G_2. Table 7.4 shows the component values and loop characteristics for the optimal component values and for the selected standard value components. Note that a negative gain margin indicates conditional stability.

Table 7.4: Complete loop component and parameter values.

Item	Optimal value	Standard component value
R_1	18.45 kΩ	18 kΩ
R_3	51.8 kΩ	51 kΩ
R_4	449 Ω	470 Ω
C_1	3.34 nF	3.9 nF
C_2	2.2 nF	2.2 nF
AG_2	49.3×10^3	50.5×10^3
ω_{z_1}	506 krad/s	484 krad/s
ω_{z_2}	5.77 krad/s	5.03 krad/s
ω_0	94.2 krad/s	92.8 krad/s
$\lvert ETF_2(f)\rvert_{max}$	-51.2 dB	-50.8 dB
GM_2	-3.02 dB	-3.43 dB
PM_2	24.1°	23.9°

7.6 Estimation Filter

Figure 7.6 shows the second-order multiple feedback active low-pass filter that realises the estimation filter stage $bK'(s)$.

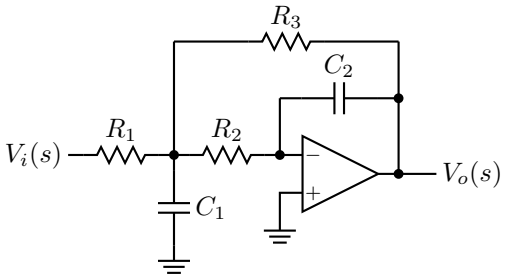


Figure 7.6: Estimation filter stage circuit.

The transfer function of the circuit of Figure 7.6 is given by

$$bK'(s) = \frac{V_o(s)}{V_i(s)} \tag{7.6.1}$$

$$= -\frac{R3}{R1}.\frac{\frac{1}{C_1C_2R_2R_3}}{s^2 + \left(\frac{1}{C_1R_1} + \frac{1}{C_1R_2} + \frac{1}{C_1R_3}\right)s + \frac{1}{C_1C_2R_2R_3}} \tag{7.6.2}$$

We choose the DC gain of the estimation filter stage as $b|K'(0)| = 1$. Since we are designing $K'(s = j2\pi f) \approx STF_1(f)$, we can calculate b as

$$b = \frac{1}{|STF_1(f = 0)|}. \tag{7.6.3}$$

The component values for the estimation filter stage are chosen as $R_1 = 1$ kΩ, $R_2 = 3$ kΩ, $R_3 = 1$ kΩ, $C_1 = 2 \times 820$ pF and $C_2 = 220$ pF. Capacitor C_1 is chosen as $C_1 = 2 \times 820$ pF, such that when the circuit is converted to its differential form, C_1 will be a single 820 pF capacitor. The resultant low-pass filter has a complex pole pair at 153 kHz with a damping ratio of 0.74.

Figure 7.7 shows a bode plot of the transfer function $STF_1(f)$ for various output loads, as well as a bode plot of the transfer function of the estimation filter $K'(s)$. The value of b is calculated for an 8.2 Ω load and is 0.206. Figure 7.7 confirms that the inner loop has enough loop gain in the audio band to make $STF_1(f)$ insensitive to load variations. The maximum audio band change in the magnitude of $STF_1(f)$ between a 4.1 Ω and a 100 kΩ output load is 0.07 dB, while the maximum change in phase is 1.2°. The estimation filter $K'(s)$ matches the inner loop transfer function $STF_1(f)$ to within 0.03 dB and 0.9° in the audio band.

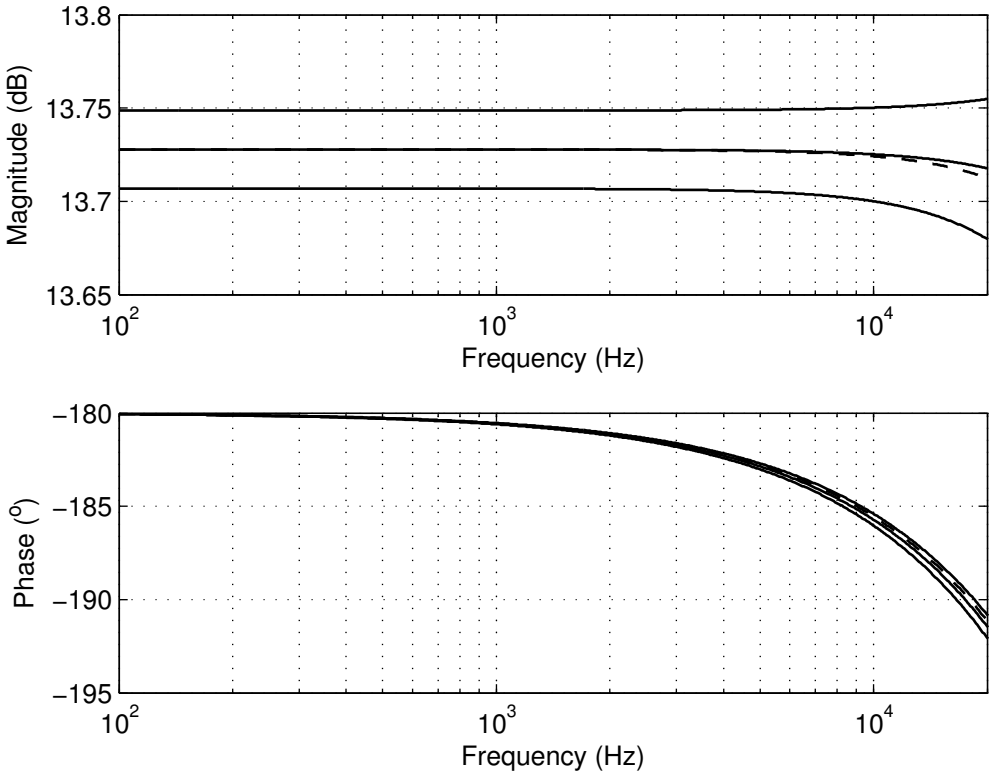


Figure 7.7: Calculated closed-loop transfer function $STF_1(f)$ of the inner loop for various output loads R_o. From top to bottom: $R_o = 100$ kΩ, $R_o = 8.2$ Ω and $R_o = 4.1$ Ω. The dotted line is the transfer function $K'(f)$ of the estimation filter.

7.7 Scaling the Loop Filter Output Level

Consider the continuous-time control loop of Figure 7.8. $K(s)$ is inverting. The loop filter output signal $X'(s)$ is given by

$$X'(s) = \frac{H(s)}{1 - K(s)H(s)A}\Big(V_i(s)[AK(s) - bBK'(s)] + E(s)A\Big) \tag{7.7.1}$$

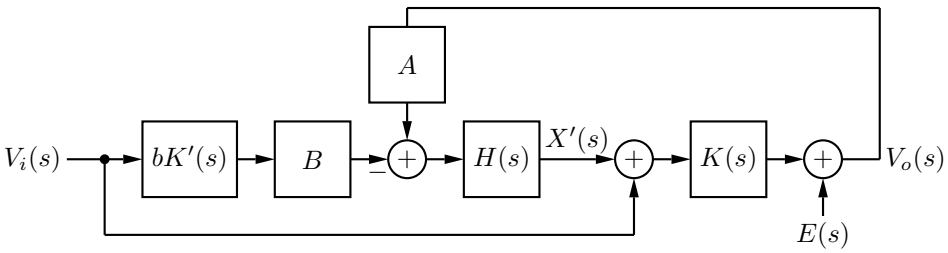


Figure 7.8: General control system with estimation filter.

If we choose $A = bB$, the loop is similar to the loop in Section 2.5 and if $K'(s) \approx K(s)$ the loop filter output signal will consist only of a component related to the output

stage error. Measurements showed that the output level of a typical loop filter will be around 50 mV or less under maximum modulation. The lowest saturation threshold of the saturation circuit introduced in Section 2.5 is around 550 mV, which is still significantly higher than the expected output of the loop filter. To improve the clipping behaviour of the amplifier we increase the input related component of the loop filter output signal such that the loop filter output signal is just below the saturation threshold at the onset of clipping.

The transfer function from input $V_i(s)$ to output $V_o(s)$ is given by

$$\frac{V_o(s)}{V_i(s)} = K(s)\frac{1 - bBH_2(s)K'(s)}{1 - AH_2(s)K(s)} \tag{7.7.2}$$

If we assume $K'(s) \approx K(s)$, $bBH_s(s)K'(s) \gg 1$, $AH_2(s)K(s) \gg 1$ and that the loop filter output signal is dominated by the $V_i(s)$ component, we can approximate (7.7.2) as

$$\frac{V_o(s)}{V_i(s)} \approx K(s)\frac{bB}{A} \tag{7.7.3}$$

and (7.7.1) as

$$X'(s) \approx \frac{V_o(s)}{K(s)}\left(1 - \frac{A}{bB}\right) \tag{7.7.4}$$

From (7.7.4) can be seen that the polarity of the loop filter output signal depends on the relationship between the gains A, b and B. Care should be taken to ensure that the loop filter output signal has the correct polarity. When the modulator is over-modulated, the loop filter output $X'(s)$ will saturate and be out of phase with the amplifier output signal $V_o(s)$. The loop filter output $X'(s)$ should therefore also be out of phase with the amplifier output $V_o(s)$ during normal operation. Hence it is required that $1 - \frac{A}{bB} > 0$. We can now calculate the value of the gain term B as

$$B = \frac{A}{b}.\frac{v_{o(max)}}{v_{o(max)} - v_{sat}|K(s=0)|}, \tag{7.7.5}$$

where $v_{o(max)}$ is the maximum amplifier output voltage, v_{sat} is the saturation limit of the loop filter and $K(s=0)$ is the DC gain of $K(s)$. For this specific design, $A = \frac{1}{R_1}$, $B = \frac{1}{R_2}$, $v_{o(max)} \approx V_s$ and $K(s=0) = STF_1(f=0)$, with R_1 and R_2 as in Figure 7.5. Thus the value of R_2 is given by

$$R_2 = bR_1\left(1 - \frac{v_{sat}|STF_1(f=0)|}{V_s}\right). \tag{7.7.6}$$

For $b = 0.206$, $R_1 = 18$ kΩ, $v_{sat} = 550$ mV, $|STF_1(f=0)| = 4.86$ and $V_s = 30$ V, we get $R_2 = 3.38$ kΩ. We choose $R_2 = 3.3$ kΩ. It should be noted that the value of R_2 directly affects the clipping behaviour of the amplifier. The value selected here for R_2 is only an initial value and the final value will be determined through measurement.

Also note that in (7.7.6) it is assumed that the maximum amplifier output voltage is equal to the supply rail V_s. However, in reality the maximum amplifier output voltage will be slightly lower, and load dependant, due to the equivalent output resistance of the power stage.

Another important point to note is that scaling the loop filter output by introducing a mismatch between bB and A will modify the closed-loop response of the entire amplifier. The approximate closed-loop transfer function given by (7.7.3) does not explain this. However, the change in frequency response becomes apparent when the exact transfer function, given by (6.4.6), is evaluated. This is shown in Section 7.8.

7.8 Analysis of the Control Loop Design

Figure 7.9 shows the root locus of the inner loop for an output load of $R_o = 100$ kΩ. The inner loop is unconditionally stable; a reduction in gain will not lead to instability. Note that there are two zeros in the z-domain, while the s-domain transfer function only had one zero. Figure 7.10 shows the root locus of the complete control loop, which is conditionally stable.

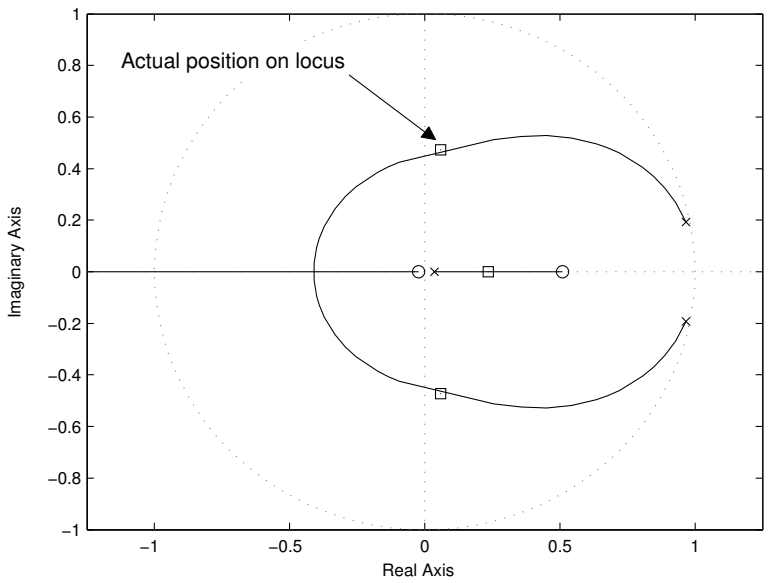


Figure 7.9: Root locus of the inner control loop with an output load of $R_o = 100$ kΩ.

Figure 7.11 shows a bode plot of $KG_1(z)$, from which the stability margins of the inner loop are determined. Figure 7.12 shows a bode plot of $K[G_1(z) + G_2(z)]$, from which the

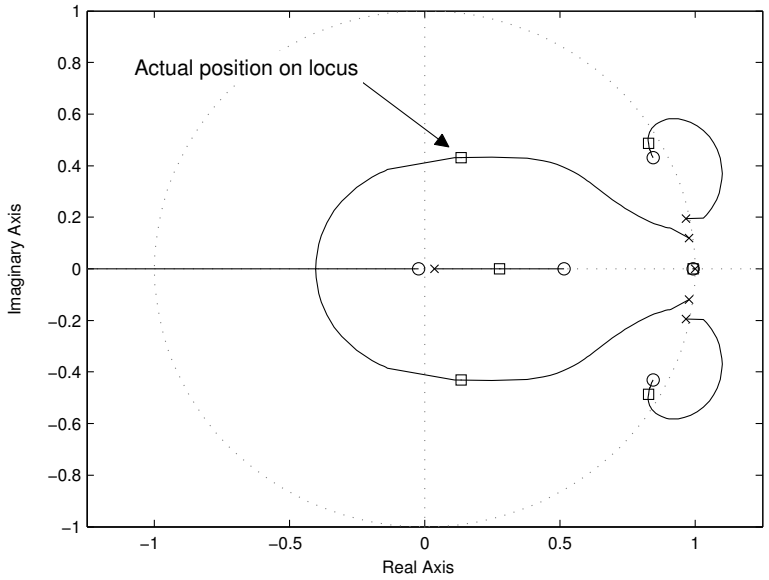


Figure 7.10: Root locus of complete control loop with an output load of $R_o = 100$ kΩ.

stability margins of the complete control system are determined. Both Figure 7.11 and Figure 7.12 are for a 100 kΩ load and a propagation delay of $t_d = 150$ ns.

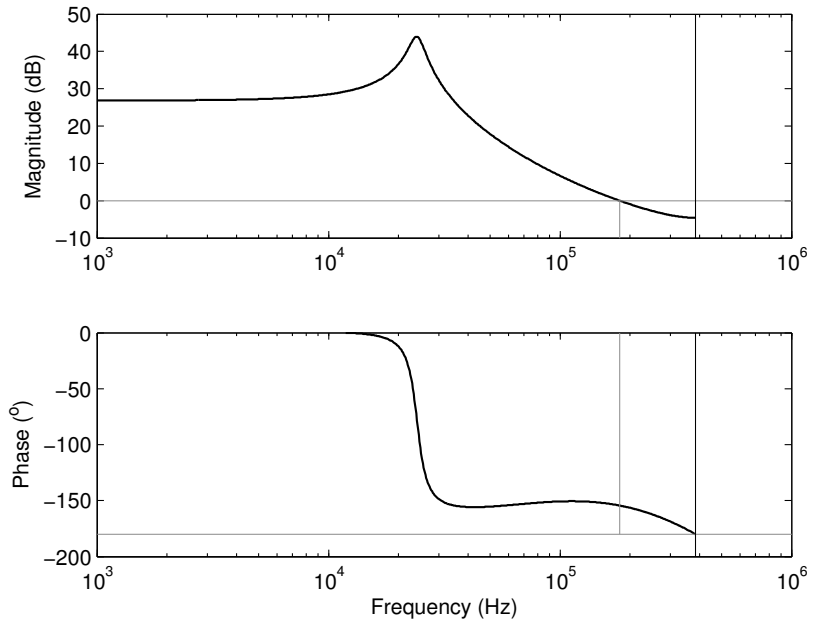


Figure 7.11: Bode plot of $KG_1(z)$ for a 100 kΩ load and a propagation delay of $t_d = 150$ ns. Gain margin is 4.59 dB and phase margin is 25.6°.

Figure 7.13 shows the stability margins of the complete loop as a function of the propagation delay t_d for different output loads. As expected, the absolute value of the

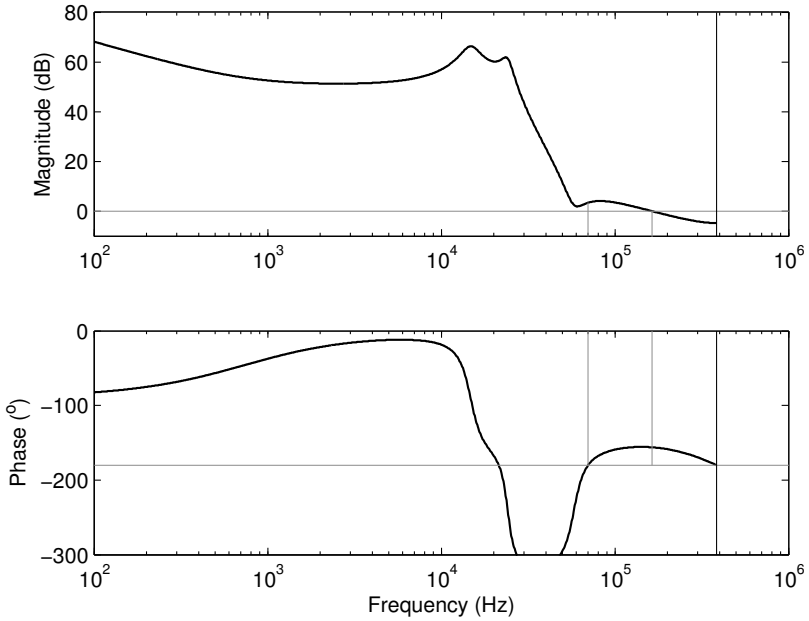
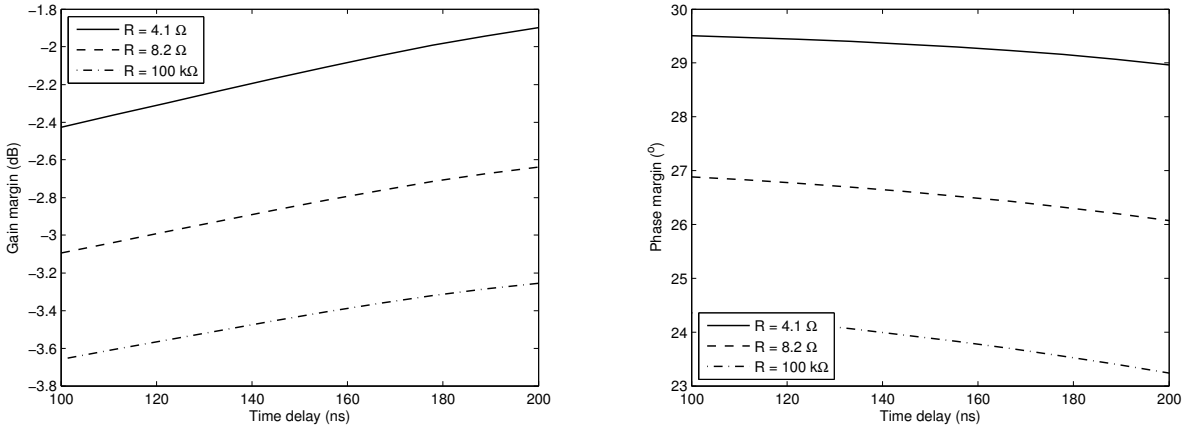


Figure 7.12: Bode plot of $K[G_1(z) + G_2(z)]$ for a 100 kΩ load and a propagation delay of $t_d = 150$ ns. Gain margin is −3.43 dB and phase margin is 23.9°.

gain margin increases and phase margin decreases for an increase in load resistance, and vice versa. Also, an increase in the propagation delay reduces the stability of the system. Although not shown in Figure 7.13, the system is unstable for a load resistance lower than $R_o = 1.84\ \Omega$ when $t_d = 200$ ns. It should be noted that the actual propagation delay is not constant, but is a function of the output current of the power stage. For $m_a = 0$, the longest propagation delay was measured as $t_d = 160$ ns (see Section 3.10).



(a) (b)

Figure 7.13: Gain margin (a), and phase margin (b), versus propagation delay for different loads.

Figure 7.14 shows the magnitudes of the error transfer functions $|ETF_1(f)|$ and

$|ETF_2(f)|$ versus frequency for an 8.2 Ω load. The inner loop error transfer function is fairly constant across the audio band with a value of -27.2 dB. Adding the outer loop improves this to a maximum value of -50.8 dB in the audio band.

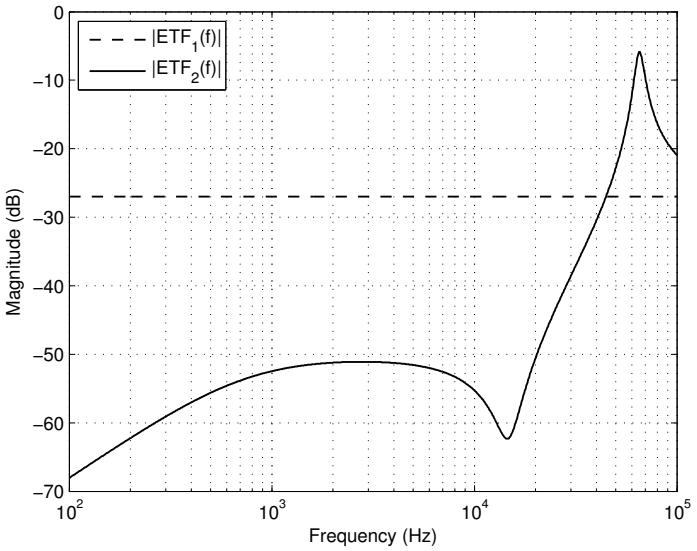


Figure 7.14: Calculated magnitude versus frequency of $ETF_1(f)$ and $ETF_2(f)$ for an 8.2 Ω load.

Figure 7.15 shows the frequency response of the complete control system for various resistive output loads, calculated from (6.4.6) using the component values as determined in this chapter. For reference, the frequency response of the approximate transfer function given by (7.7.3) is plotted in grey for an 8.2 Ω load. As expected, scaling the outer loop filter output level results in a frequency response that is different to that of the inner loop. However, despite this the frequency response is flat to within 0.08 dB and, due to the high loop gain, there is very little variation in magnitude with a variation in load.

The outer loop filter is implemented with an OPA1611 operational amplifier from Texas Instruments. It is important to verify that the op-amp is able to produce the desired closed-loop transfer function. The open-loop gain of the operational amplifier has to be significantly higher than its closed-loop gain, otherwise the closed-loop gain will not be accurate and the op-amp itself will start to add noise and distortion. Figure 7.16 shows that the op-amp does indeed have enough loop gain to accurately realise the closed-loop transfer functions $AH_2(s)$ and $BH_2(s)$. Only at frequencies close to DC will the op-amp run out of loop gain due to the integrator in the loop filter. However, in this case the closed-loop gain of the operational amplifier at very low frequencies is not critical, as long as it is very large.

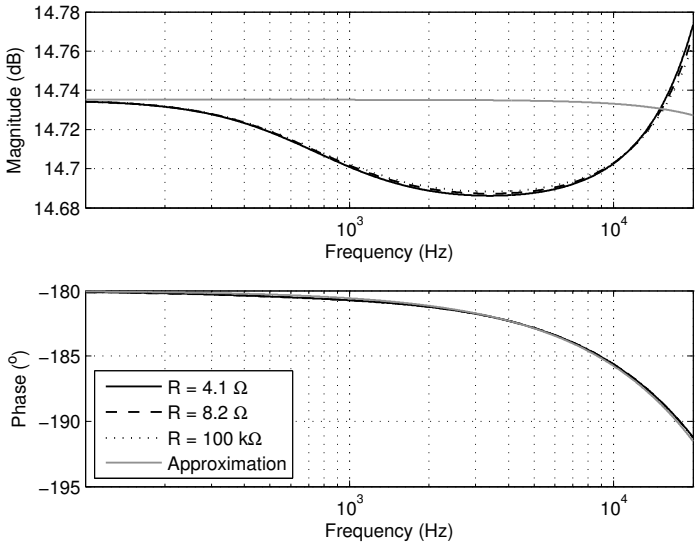


Figure 7.15: Calculated closed-loop transfer function $STF_2(f)$ of the complete loop for output loads $R = 4.1\ \Omega$, $R = 8.2\ \Omega$ and $R = 100\ \text{k}\Omega$. The grey line is an approximation.

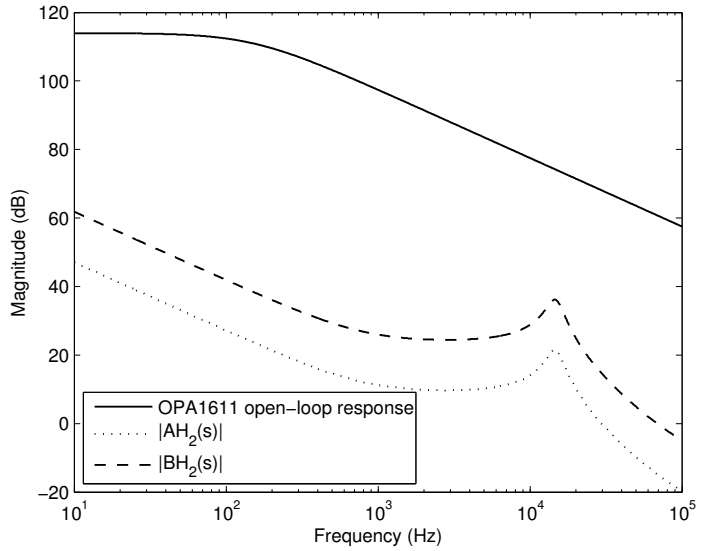


Figure 7.16: Open-loop frequency response of the OPA1611 op-amp, and transfer functions $|AH_2(s)|$ and $|BH_2(s)|$.

7.9 Carrier Pre-Filter Transfer Function

Referring to Section 2.4, one way to implement ripple compensation is to add a sawtooth carrier filtered by the transfer function through which the comparator output signal is filtered before reaching the comparator input to the original sawtooth carrier. In this design, the comparator output signal propagates through two different loops before reaching the comparator input. However, the outer loop filter has a low-pass characteristic with a cut-off frequency significantly lower than the carrier frequency. The inner loop filter does

not have a low-pass characteristic. Consequently, the contribution of the outer loop to the feedback ripple component is negligible compared to that of the inner loop. Thus, we ignore the outer loop when implementing ripple compensation.

In addition to ripple compensation, the carrier has to be pre-filtered to cancel the filtering of the passive summation network. The output of the carrier generator is a unity amplitude sawtooth filtered by the transfer function

$$Q(s) = \frac{A_s}{P(s)} + \frac{e^{-st_d} V_s F(s) H_1(s)}{A_p P(s)}. \tag{7.9.1}$$

The first term in (7.9.1) scales the unity amplitude sawtooth to have an amplitude of A_s. Also, the first term cancels the pole and zero of the passive summation pre-filter $A_p P(s)$. Note that the gain term A_p of the passive summation is not cancelled. This means that the effective amplitude of the sawtooth arriving at the input of the comparator is $A'_s = A_s A_p$. The second term in (7.9.1) is the ripple compensation term filtered by the inverse of the passive summation pre-filter.

7.10 Miscellaneous

This section discusses the implementation of hardware related to the control loop circuitry that was not discussed in the preceding sections.

7.10.1 Control Circuit Power Supply

A bipolar supply voltage of 12 V per rail is provided to the op-amps and the comparator of the control circuit through LM7812 and LM7912 linear regulators. The output of the comparator is pulled up to a 5 V supply, which is provided by an LM7805 linear regulator.

7.10.2 Comparator

Figure 7.17 shows the LM306 comparator circuit used in the control loop. The LM306 is powered from the same voltage supply as the op-amps in the control loop. The output of the comparator is pulled up to a 5 V supply through resistor R_1. The value of the pull-up resistor is $R_1 = 560\ \Omega$. Resistor R_2 helps to reduce the voltage undershoot caused by the high rate of change in output voltage when the current-sinking output transistor of the comparator switches on, and has a value of $R_2 = 22\ \Omega$.

7.10.3 Loop Filter Saturation Circuit

Figure 7.18 shows the loop filter saturation circuit that was described in Section 2.5. The transistor circuit is powered from the same voltage supply as the loop filter op-amps. The

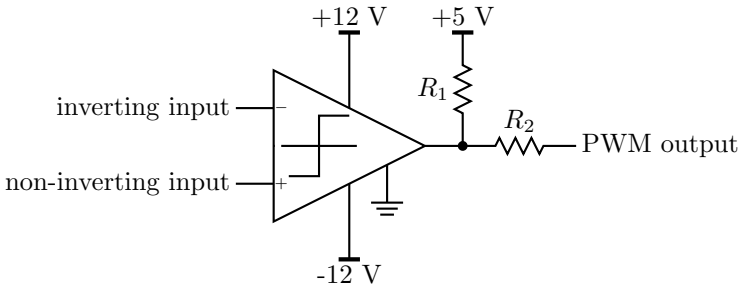


Figure 7.17: The LM306 comparator circuit.

zener diodes are omitted to reduce the saturation threshold. The Transistors Q_1 and Q_2 are integrated in a single BCV62C dual-transistor package. Transistors Q_5 and Q_6 are BCV61C transistors, and is also in a single package. Transistors Q_3 and Q_4 are BC849C and BC859C transistors, respectively. The choice of transistors for this circuit is not critical, as long as they have a high current gain and collector-emitter voltage ratings of greater than 24 V.

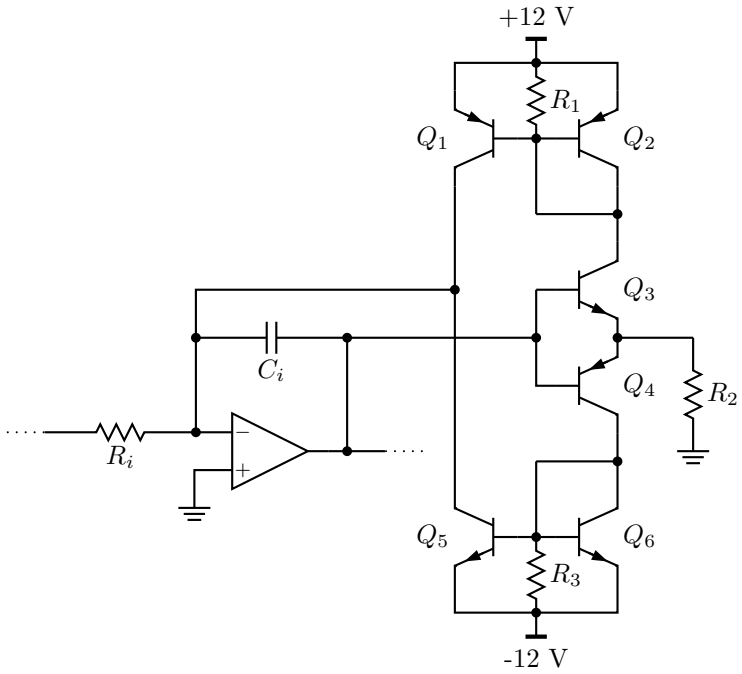


Figure 7.18: Transistor-based loop filter saturation circuit.

The values of R_1 and R_3 are not critical either. Resistors R_1 and R_3 have to be small enough to not turn on the current mirrors due to leakage currents when Q_3 and Q_4 are off, and large enough to properly turn on the current mirrors when Q_3 or Q_4 are turned on by the loop filter op-amp. They are chosen as $R_1 = R_3 = 10$ kΩ. Resistor R_2 limits the maximum transistor current. We choose $R_2 = 100\ \Omega$ to limit the maximum current to 120 mA.

7.11 Summary

In this chapter an optimal control loop was designed by means of an iterative optimisation algorithm. Component values of the analogue circuits were calculated. The complete control system is conditionally stable and provides at least 50 dB rejection of output stage errors. The estimation filter is realised with a second order multiple-feedback op-amp filter, and the outer loop filter output level is scaled to improve clipping behaviour.

Chapter 8

Simulations

8.1 Introduction

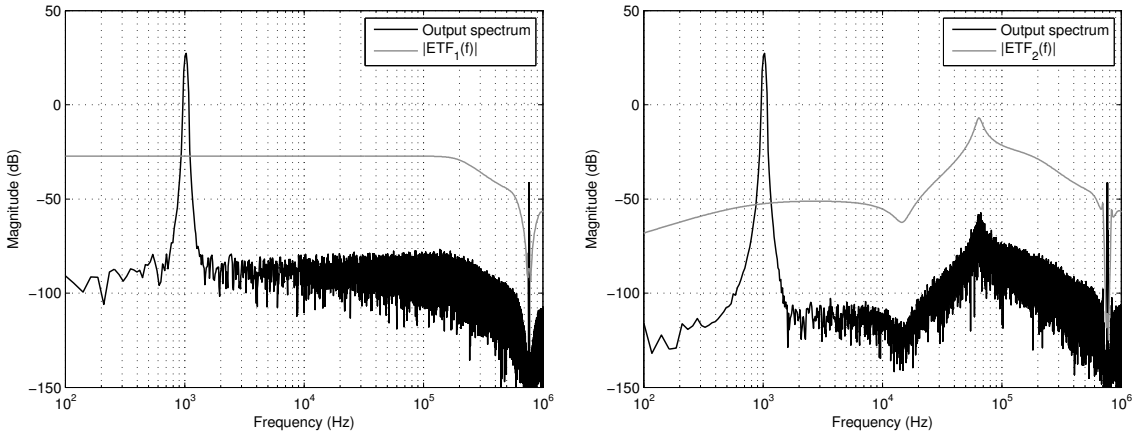
The designed control loop is simulated in both MATLAB Simulink and a SPICE-based simulator to verify its operation. All simulations are done with an 8.2 Ω load, unless stated otherwise. The first section primarily concerns the effect of ripple compensation on the performance of the control loop. The second section focusses on the behaviour of the control loop when over-modulation occurs.

8.2 Simulink

Figure 8.1 (a) shows a spectrum of the Simulink simulated amplifier output with only the passive inner loop active. The modulation index is $m_a = 0.8$ and the input frequency is 1 kHz. Note that the magnitude of the noise is not representative of the actual amplifier noise. The noise in the simulation is due to the finite simulation time-step and a small amount of Gaussian noise added as a timing error at the comparator output. The important observation here is that the shape of the noise approximately follows the shape of the error transfer function $|ETF_1(f)|$. Figure 8.1 (b) shows a spectrum of the simulated amplifier output under the same conditions with both loops active. Again, the shape of the noise matches that of the error transfer function $|ETF_2(f)|$.

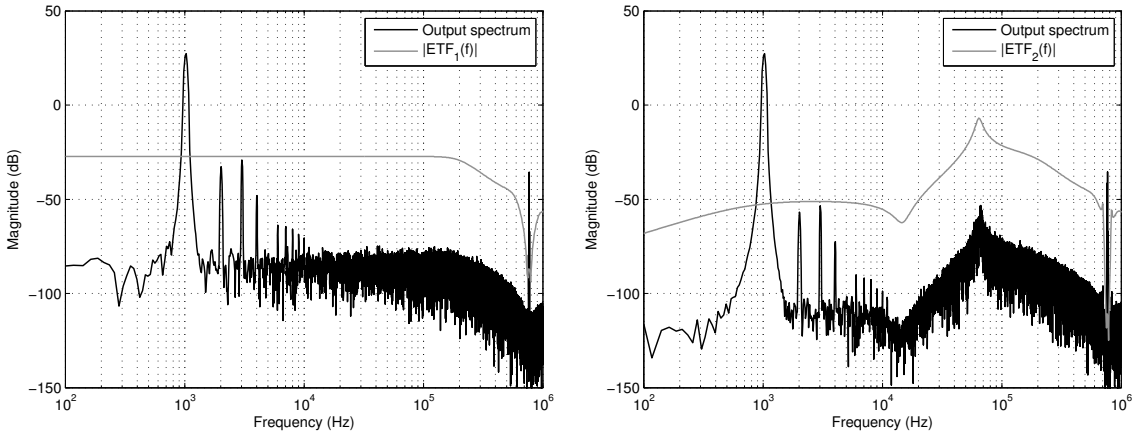
Figure 8.2 shows the data for the same simulation as Figure 8.1, but this time without ripple compensation. Although the shape of the noise still follows that of the error transfer functions, harmonics of the fundamental signal are now clearly visible. These harmonics are not present in the open loop system, and is a direct consequence of feedback ripple aliasing [1, 7].

Figure 8.3 shows the simulated comparator gain with and without ripple compensation for an amplifier input signal of 1 kHz and $m_a = 0.8$. The simulated gain is calculated



(a) (b)

Figure 8.1: Magnitude spectrum of simulated amplifier output with only the inner loop active (a) and with both loops active (b). The error transfer functions are shown in grey for comparison.



(a) (b)

Figure 8.2: Magnitude spectrum of simulated amplifier output without ripple compensation with only the inner loop active (a) and with both loops active (b). The error transfer functions are shown in grey for comparison.

using the derivative of the comparator input signal at a sampling instant. The dashed line indicates the theoretical value of the comparator gain K, and closely matches the simulation. Without ripple compensation there is a 4.2 dB variation in comparator gain, which is reduced to 0.04 dB when ripple compensation is implemented. Note the sudden changes in the gain when ripple compensation is not used. At these points the ripple component has shifted in phase relative to the sawtooth to such an extent that the slope of the ripple component at the sampling instant is reversed.

Figure 8.4 shows the reference input signal that the comparator compares to the sawtooth carrier. The top waveform is not ripple compensated and inspection of the

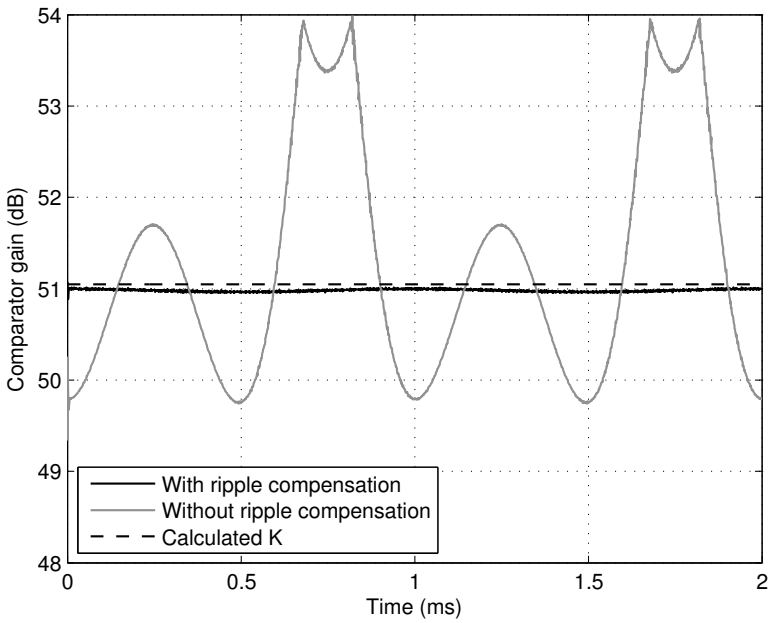


Figure 8.3: Simulated comparator gain with and without ripple compensation. The input signal frequency is 1 kHz and $m_a = 0.8$.

envelope of the signal clearly shows that the superimposed ripple component is duty cycle dependent. The bottom waveform is ripple compensated and the ripple component is virtually independent of duty cycle.

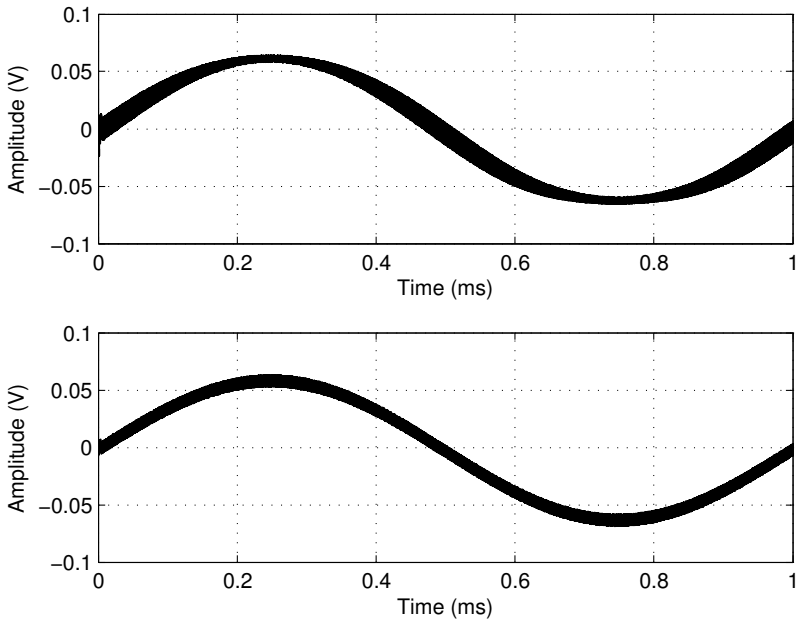
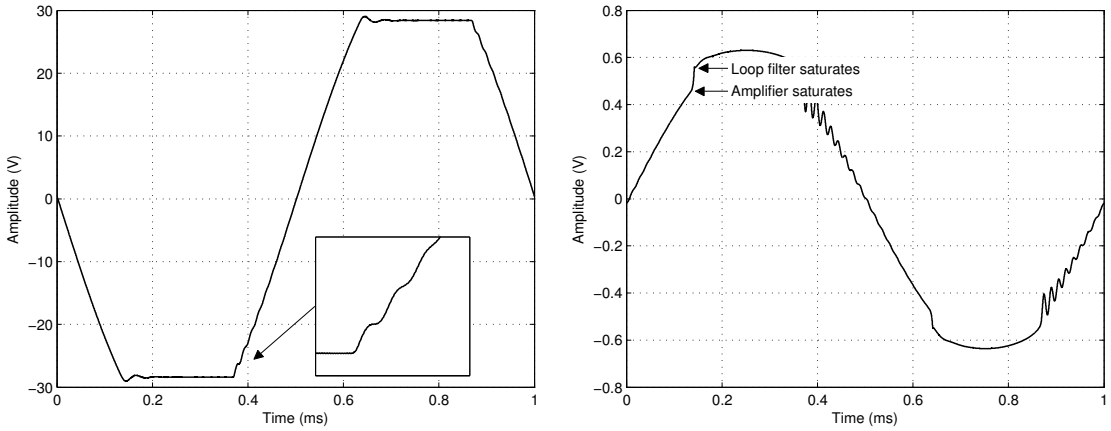


Figure 8.4: Simulated comparator input reference signal without ripple compensation (top) and with ripple compensation (bottom). The input signal frequency is 1 kHz and $m_a = 0.8$.

8.3 SPICE

Figure 8.5 shows SPICE simulation waveforms of when the modulator is over-modulated. The output signal of the amplifier, shown in Figure 8.5 (a), recovers from over-modulation with only a slight oscillation. The reason for this oscillation becomes apparent when the output signal of the outer loop filter, shown in Figure 8.5 (b), is considered. When the amplifier saturates, the output of the outer loop filter is not yet at the saturation threshold of the loop filter saturation circuit. This is because the equivalent series resistance of the power stage, which causes the amplifier to saturate to a voltage lower than the 30 V supply rails, was not taken into account in (7.7.6).

The slight recovery oscillation is unlikely to be audible, since at this point the outer loop filter is active and providing error rejection in the audio band. However, the clip-recovery can be improved by increasing the magnitude of the loop filter output signal. Figure 8.6 shows the waveforms when the loop filter output has been increased by decreasing the value of resistor R_2 (Figure 7.5) from 3.3 kΩ to 3.25 kΩ. The amplifier and loop filter now saturates almost simultaneously, and consequently the clip-recovery is almost perfect. Note that the control loop has no control over the output voltage when the modulator is in saturation and the overshoot of the output waveform at the start of clipping is the natural response of the demodulation filter.

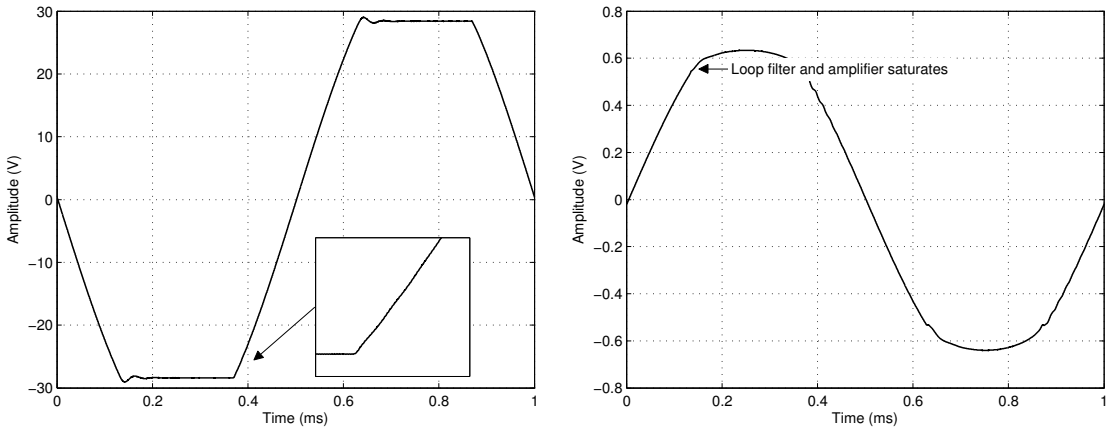


(a) (b)

Figure 8.5: Spice simulation of amplifier output (a) and outer loop filter output (b) during over-modulation for $R_2 = 3.3$ kΩ.

8.4 Summary

This chapter presented some simulation results that confirmed the correct operation of the control loop that was designed in the preceding chapters. The simulations correlated



(a) (b)

Figure 8.6: Spice simulation of amplifier output (a) and outer loop filter output (b) during over-modulation for $R_2 = 3.25$ kΩ.

well with theoretical expectations. Furthermore, the simulations illustrated the ability of the ripple compensation technique to minimise ripple aliasing and comparator gain fluctuations. It was also confirmed that the conditionally stable loop remains stable when loop gain collapses due to over-modulation.

Chapter 9

Measurements

9.1 Introduction

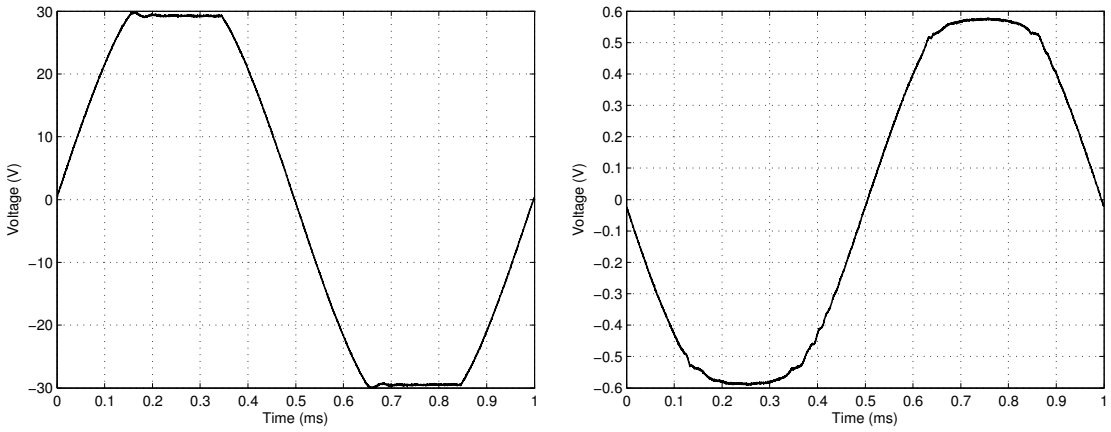
This chapter presents detailed measurements of the amplifier. Except for oscilloscope measurements, all measurements were performed with an Audio Precision SYS-2722 audio analyser. In earlier design iterations the power stage of a commercial class-D amplifier module was used. In most cases measurements of the amplifier with the commercial power stage will also be given for comparison. We will refer to the power stage that was designed in this thesis as power stage one (PS1) and the commercial power stage as power stage two (PS2). PS1 is assumed if no reference is made to a specific power stage. Unless stated otherwise, ripple compensation is implemented and the delay in the pre-filter transfer function $Q(s)$ is $t_d = 150$ ns.

9.2 Clipping Behaviour

Figure 9.1 shows the behaviour of the amplifier during clipping. The value of resistor R_2 is 3.3 kΩ (see Section 7.7). Loop filter saturation and modulator overload happens almost simultaneously. Hence, the clip-recovery is very good and no further adjustment is necessary.

9.3 Distortion

A measurement of total harmonic distortion and noise (THD+N) gives an indication of the linearity of the amplifier. All THD+N measurements are measured through an AUX-0025 switching amplifier measurement filter [50]. The measurement bandwidth is restricted to 20 kHz by enabling the 20 kHz AES17 filter of the analyser. This is required because a THD+N measurement does not differentiate between distortion and noise. The noise



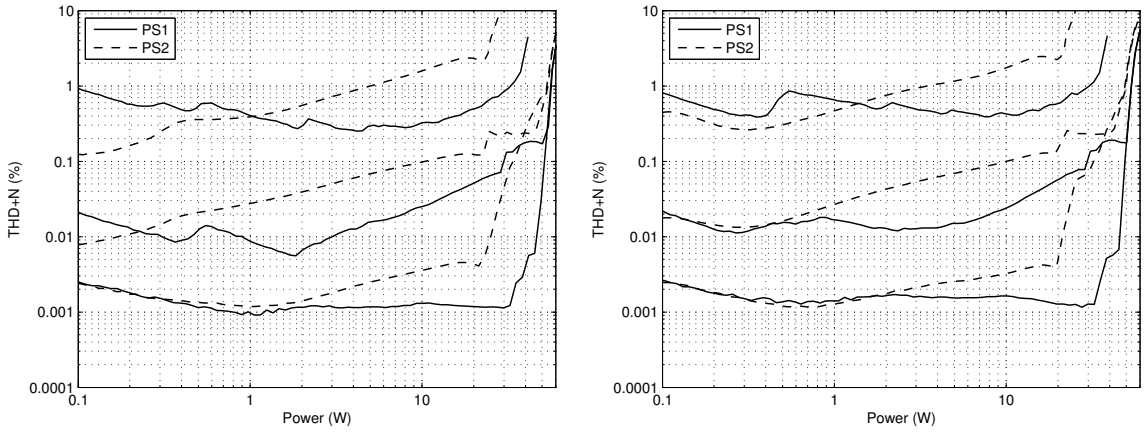
(a) (b)

Figure 9.1: Oscilloscope measurements of (a) the output of the amplifier and (b) the output of the outer loop filter for $m_a > 1$.

shaping characteristic of the control loop results in a rapid increase in noise just above 20 kHz (see Section 8.2), which will contaminate the measurement if the bandwidth is not restricted. Note that restricting the measurement bandwidth to 20 kHz means that any THD+N measurement above 10 kHz will consist of only noise. Unless indicated otherwise, power is measured relative to an 8.2 Ω load. This makes it easier to compare measurements with different output loads.

Figure 9.2 shows measurements of THD+N as a function of output power. Figure 9.2 (a) is for an 8.2 Ω output load and (b) for a 4.1 Ω load. The top trace is the THD+N of the open loop system, and the centre and bottom traces are with the inner control loop and the complete control loop active, respectively. Closing the inner loop around the output stage reduces THD+N at 10 W into 8.2 Ω from 0.324% to 0.025%. This is a reduction of 22.3 dB, which is less than we expect, because $|ETF_1(f)| \leq -27.2$ dB in the audio band. Closing the outer loop further reduces THD+N by 25.7 dB from 0.025% to 0.0013%. This is more in line with theoretical expectations, since the outer loop reduces the error transfer function by at least 23.6 dB. The total reduction in THD+N compared to open loop operation at 10 W into 8.2 Ω is 48 dB. We expected a reduction of at least 50.8 dB.

We can gain some insight into the discrepancy between the expected and measured values of THD+N by comparing the measurements of PS1 and PS2. From Figure 9.2 we see that the "shape" of the THD+N versus power measurement for PS2 does not change when the inner loop and outer loop is closed around the output stage, except at very low and very high power levels. In other words, the error rejection capability of the control loops do not depend on modulation index. This is correct, because with ripple compensation we do not expect the effectiveness of the control loops to depend on



(a) (b)

Figure 9.2: Measured THD+N versus output power at 1 kHz with (a) $R_o = 8.2\ \Omega$ and (b) $R_o = 4.1\ \Omega$. From top to bottom: open loop, with the inner control loop active, and with the complete control loop active.

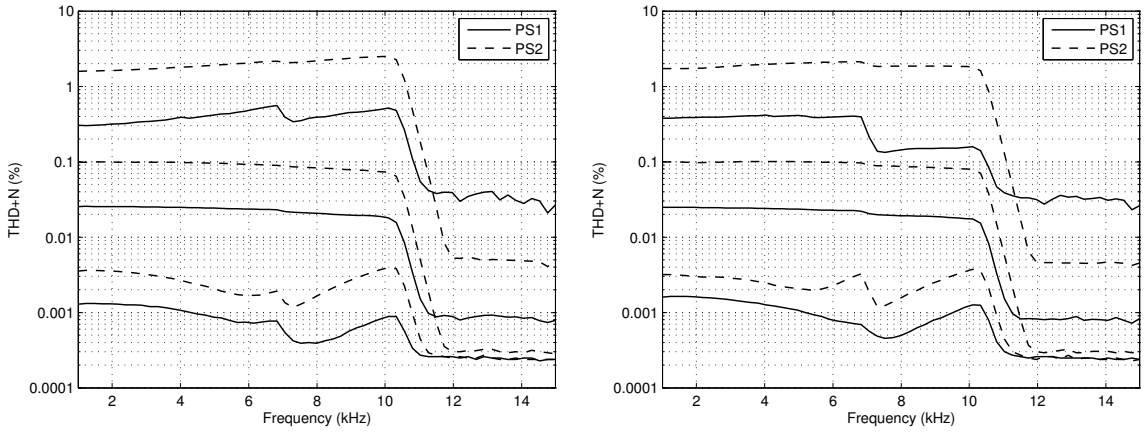
modulation index. In contrast, for PS1 the reduction in THD+N varies with modulation index. The inner loop reduces THD+N by 33 dB at 1 W into 8.2 Ω, which is more than the loop gain, and only by 22.3 dB at 10 W. Furthermore, the outer loop does the opposite: it reduces THD+N more effectively at higher values of m_a.

It should be understood that PS1 and PS2 are completely different power stage designs. PS2 has discrete comparator and gate drive circuitry that are not equivalent to the integrated circuits used in PS1. Furthermore, the EMI performance of PS2 is superior to that of PS1 [35]. It is believed that self-pollution is the main reason for the non-ideal behaviour of the control loop with regards to PS1.

It is noted that the measurements of THD+N versus power for PS2 is not entirely as expected either. Although the reduction in THD+N is largely independent of modulation index, the inner loop reduces THD+N by 24.4 dB and not 27.2 dB as expected. When both loops are active THD+N is reduced by 53.2 dB. The measurements for PS2 are more in line with theoretical expectations than those of PS1. In Section 9.8 it will be shown that the delay in the ripple compensation pre-filter transfer function also affects the performance of the control loop.

With reference to Figure 9.2, with both loops active THD+N for PS1 exceeds 0.1% at about 51 W into 8.2 Ω and 98.6 W (49.3 W on the graph) into 4.1 Ω. The sudden rise in distortion just above 30 W is due to the power stage reaching its minimum pulse width. At this point the outer loop filter is still active. At about 50 W over-modulation occurs, at which point the outer loop filter saturates due to the large output stage error. Note that the THD+N measurement with both loops active is dominated by noise for power levels below about 1 W.

Figure 9.3 shows measurements of THD+N as a function of frequency at 10 W into 8.2 Ω and 20 W into 4.1 Ω. The open loop THD+N changes with frequency in accordance with the frequency response of the demodulation filter. With an 8.2 Ω load the demodulation filter has a low damping ratio and distortion rises with frequency. With a 4.1 Ω load there is less of a rise in open loop THD+N with frequency due to the increased damping ratio.



(a) (b)

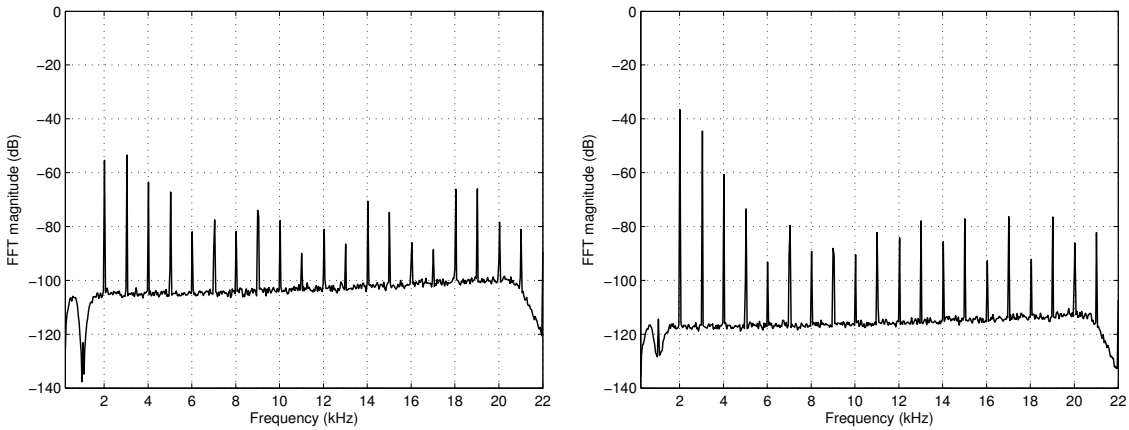
Figure 9.3: Measured THD+N versus frequency at 10 W with (a) $R_o = 8.2\ \Omega$ and (b) $R_o = 4.1\ \Omega$. From top to bottom: open loop, with the inner control loop active, and with the complete control loop active.

Closing the inner loop around the output stage makes the error transfer function independent of the transfer function of the demodulation filter, and constant in the audio band. Consequently, THD+N does not rise with frequency when the inner loop is active. Above 6.7 kHz the third harmonic falls outside the measurement bandwidth. However, this does not cause a significant reduction in THD+N, because with the inner loop active distortion is mainly second harmonic. THD+N only drops significantly above 10 kHz when the second harmonic falls outside the measurement bandwidth. With both control loops active the distortion varies with frequency as dictated by the total noise transfer function $ETF_2(f)$.

9.4 Spectral Analysis

Figure 9.4 (a) shows an FFT of the distortion residue when PS1 is operated open loop and delivering 10 W at 1 kHz into 8.2 Ω. THD+N is 0.295%. Figure 9.4 (b) shows the same measurement for PS2, and THD+N is 1.587%. The distortion residue of both PS1 and PS2 is dominated by the second and third harmonic, although significant higher order

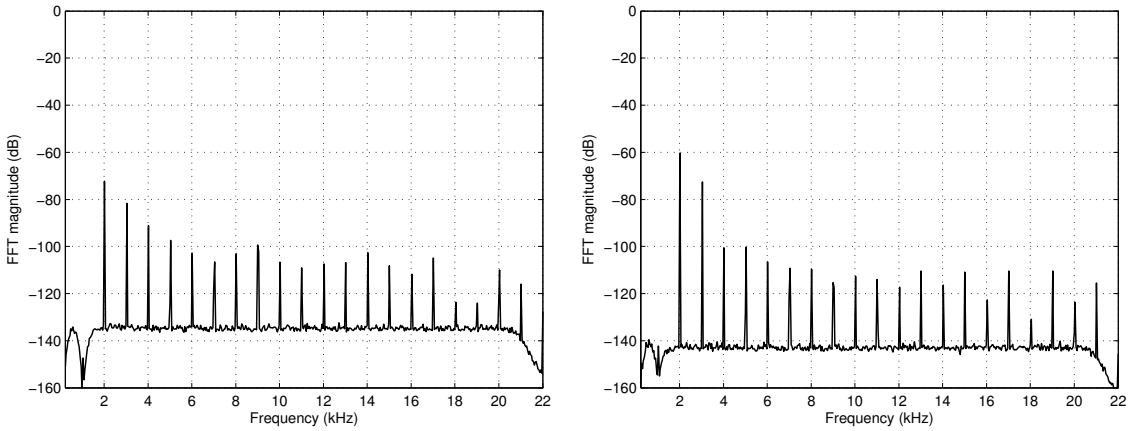
components are also present. Note that while the distortion of PS1 is lower than that of PS2, the noise floor of PS2 is about 13 dB lower than that of PS1.



(a) (b)

Figure 9.4: FFT of the open loop distortion residue with 10 W at 1 kHz into 8.2 Ω for (a) PS1 and (b) PS2. THD+N is (a) 0.295% and (b) 1.587%. The suppressed fundamental is at 0 dB.

Figure 9.5 shows FFT's of the distortion residues for the same conditions as in Figure 9.4 when the inner loop is active. Note that, as expected, the noise floor is now constant with frequency. The noise floor is reduced by roughly 30 dB for PS1 and 25 dB for PS2 compared to open loop operation.



(a) (b)

Figure 9.5: FFT of the distortion residue with the inner loop active with 10 W at 1 kHz into 8.2 Ω for (a) PS1 and (b) PS2. THD+N is (a) 0.0254% and (b) 0.0985%. The suppressed fundamental is at 0 dB.

Figure 9.6 shows FFT's of the distortion residues when both loops are active. The noise is still constant with frequency, despite the fact that the gain of the outer loop filter

is not constant with frequency. Ideally, we expect a dip in the noise floor at 15 kHz, which is the frequency of the complex pole pair of the outer loop filter. Furthermore, the noise floor is only down by 10 dB for PS1 and 3 dB for PS2 compared to the noise floor with the inner loop active. Also, the open loop noise floor of PS2 is 13 dB lower than that of PS1, while with both loops active the noise floor of PS1 and PS2 is the same. This suggests that with both loops active, the noise of the control circuitry itself and the noise of the analyser start to become significant. The measured unweighed noise of the amplifier is 21 μV_{rms} (22 Hz - 20 kHz bandwidth) when both loops are active.

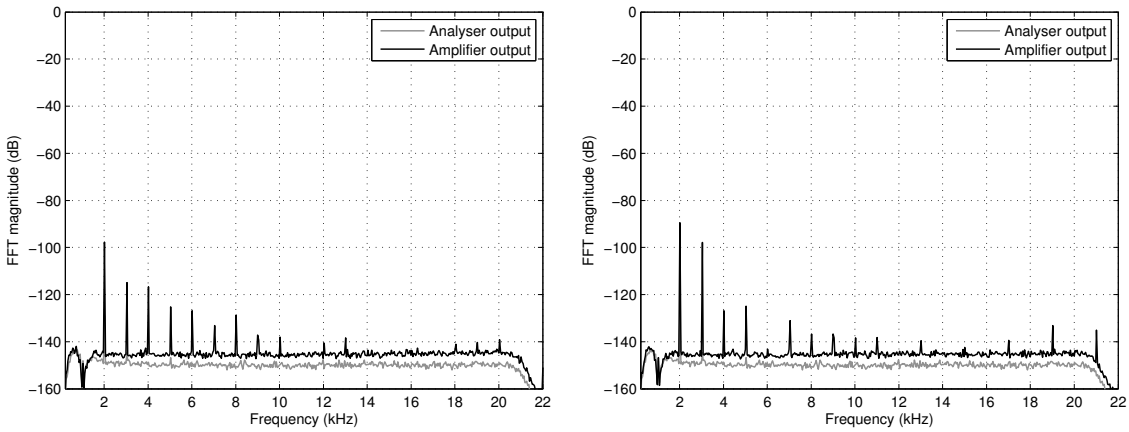
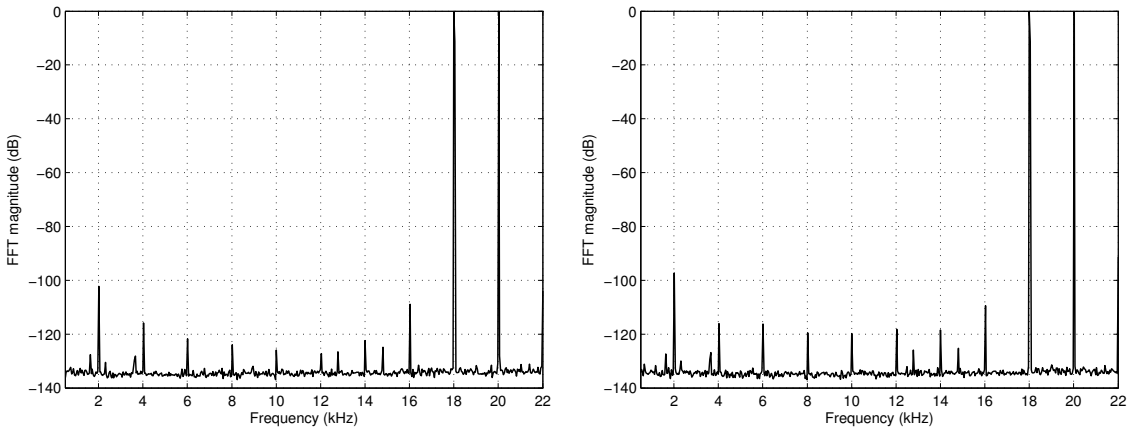


Figure 9.6: FFT of the distortion residue with both loops active with 10 W at 1 kHz into 8.2 Ω for (a) PS1 and (b) PS2. THD+N is (a) 0.00132% and (b) 0.00354%. The suppressed fundamental is at 0 dB.

Figure 9.7 shows FFT's of the amplifier output with both loops active for a twin-tone input. The frequencies of the input tones are 18 kHz and 20 kHz and the output power is 10 W into 8.2 Ω. A twin-tone test can assess the linearity of the amplifier at frequencies above half the measurement bandwidth, where standard THD+N or single tone FFT measurements are not meaningful. Figure 9.7 shows that there are no unexpected excessive intermodulation components. The intermodulation components that are present correspond reasonably well with the harmonic components of the distortion residuals in Figure 9.6. Note that the components that are not at integer multiples of 2 kHz are those of the DAC and ADC of the analyser.

9.5 Frequency Response

Figure 9.8 shows the measured frequency response when the inner loop is closed around the output stage. The measurement bandwidth is 80 kHz and the measurement was taken at an output power of 1 W into 8.2 Ω. There is only a 0.05 dB variation in magnitude



(a) (b)

Figure 9.7: Normalised FFT of the amplifier output with 18 kHz and 20 kHz input tones for (a) PS1 and (b) PS2. Output power is 10 W into 8.2 Ω.

when the output load is changed from $R_o = 100$ kΩ to $R_o = 4.1$ Ω. The dashed line is the calculated frequency response of the inner loop for an output load of 8.2 Ω and matches the measured response to within 0.01 dB and 0.27°.

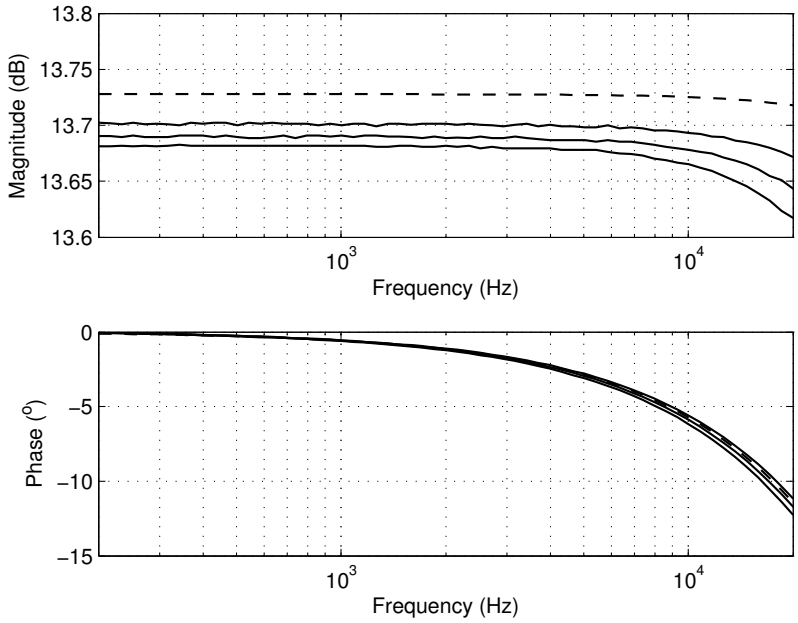


Figure 9.8: Measured closed loop frequency response of the inner loop for various output loads. From top to bottom: $R_o = 100$ kΩ, $R_o = 8.2$ Ω and $R_o = 4.1$ Ω. The dashed line is the theoretical frequency response for an 8.2 Ω load.

Figure 9.9 shows the measured frequency response when both loops are closed around the output stage. There is almost no distinguishable difference in frequency response with a variation in load. This indicates a very low output impedance. The measured frequency

response correlates very well with the theoretical calculation, except for a 0.39 dB difference in DC gain. This deviation is likely due to component tolerances. The frequency response of the amplifier is flat to within 0.08 dB in the audio band.

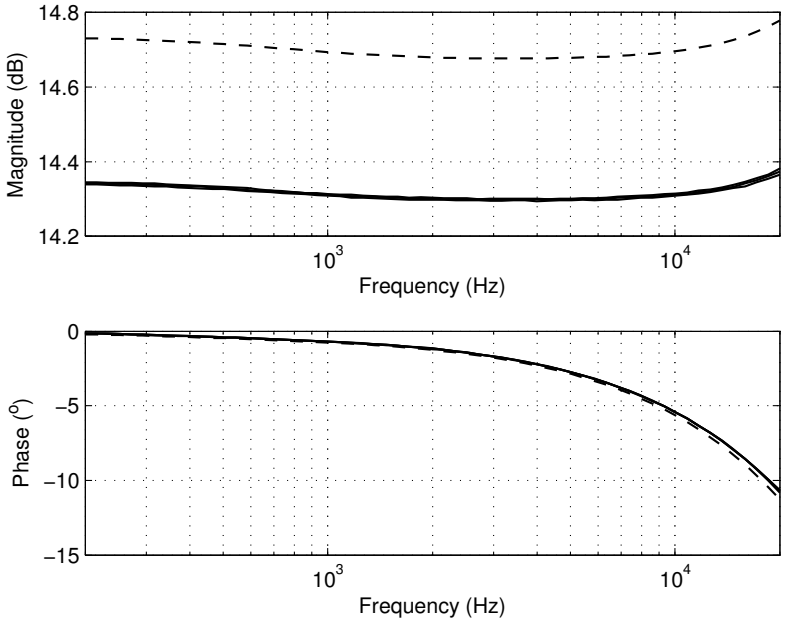


Figure 9.9: Measured closed loop frequency response of the complete control loop for various output loads. From top to bottom: $R_o = 100$ kΩ, $R_o = 8.2$ Ω and $R_o = 4.1$ Ω. The dashed line is the theoretical frequency response for an 8.2 Ω load.

9.6 Output Impedance

The output impedance of the amplifier is very low and cannot be accurately calculated by simply measuring the change in output voltage with a change in load. Instead we make use of Kelvin sensing to measure the output impedance of the amplifier. Figure 9.10 shows the measurement setup. Current is forced into the output impedance Z_o of the device-under-test (DUT) by the differential current source i_f. This generates a voltage v_o over the output impedance which is measured by the audio analyser. The magnitude of the output impedance is then given by $Z_o = \frac{v_o}{i_f}$. We can use the generator output of the analyser as a current source, because its output impedance of 40 Ω is significantly larger than the output impedance of the amplifier. The magnitude of the current forced into the output of the amplifier is $i_f = 50$ $\mathrm{mA_{rms}}$.

Figure 9.11 shows the measured magnitude of the output impedance as a function of frequency for both PS1 and PS2. The output impedance is exceptionally low and only exceeds 10 mΩ at 20 kHz for PS1.

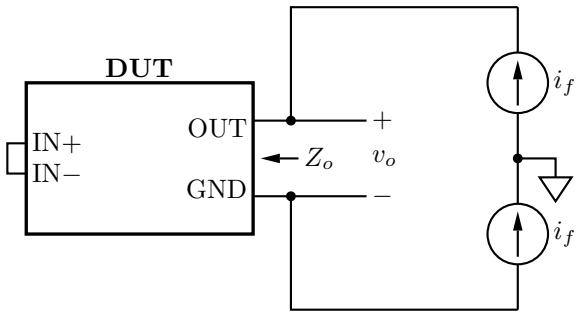


Figure 9.10: Output impedance measurement setup.

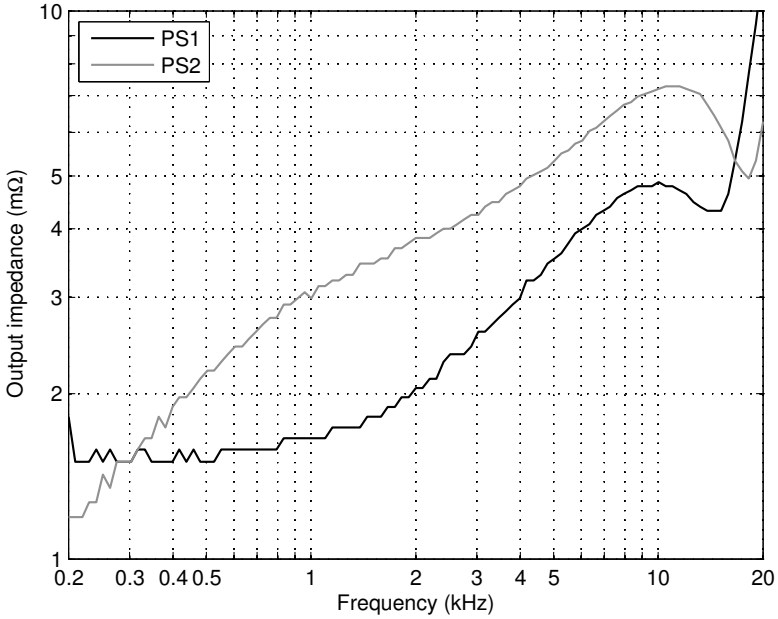


Figure 9.11: Measured output impedance for PS1 and PS2.

9.7 Power Supply Rejection Ratio

In a self-oscillating modulator the equivalent carrier scales proportionally to the supply rails. Consequently, a self-oscillating modulator has an inherent mechanism for rejecting supply voltage variations. A clocked modulator has no such mechanism and the control loop is solely responsible for rejecting supply voltage fluctuations. In most cases supply voltage fluctuations consist of components related to the AC mains frequency. The integrator in the outer loop filter will help to provide increased immunity against mains related power supply noise.

To measure the power supply rejection ratio (PSRR) we inject a signal into the supply rail of the amplifier and measure the magnitude of the signal that is present at the output of the amplifier. The PSRR is the ratio between the signal at the output of the amplifier and the signal injected into the supply rail.

There are several ways to inject a signal into the supply rail [51]. One method is to couple a signal into the supply rail through a transformer. Another method is to connect the floating generator output of the analyser in series with the power supply. However, this can potentially damage the analyser. It was decided to inject a signal into the supply rail through a buffer amplifier, thereby protecting the generator output of the analyser.

Figure 9.12 shows the measurement setup. The buffer amplifier is a commercial UcD180ST class-D amplifier module from Hypex Electronics [52]. The resistor R_{limit} in series with the output of the buffer amplifier limits the maximum inrush current into the decoupling capacitors of the DUT and has a value of 8.2 Ω. The signal injected into the supply rail is regulated to 200 mV_{rms}.

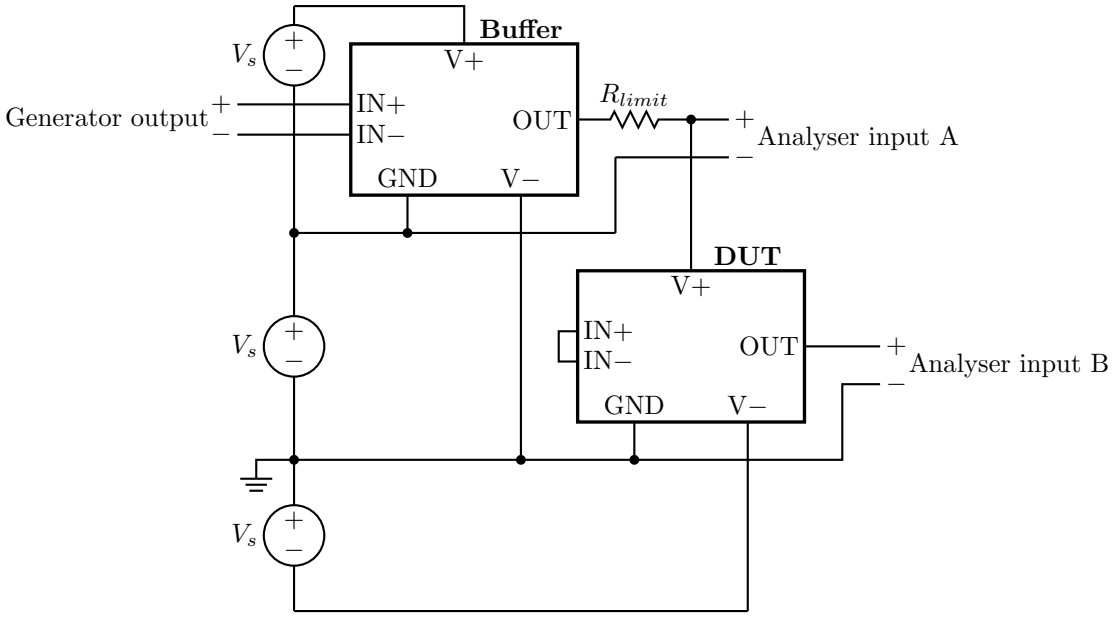


Figure 9.12: PSRR measurement setup.

Figure 9.13 shows the measured PSRR as a function of frequency. The effect of the integrator in the outer loop filter is clearly visible. At 50 Hz the PSRR is -78 dB, increasing to -62.5 dB at 1 kHz.

9.8 The Effect of Ripple Compensation

With reference to Section 7.9, the ripple compensation pre-filter $Q(s)$ contains a constant time delay t_d equal to the propagation delay of the loop. The actual propagation delay of the loop is, of course, not constant and is a function of the output current which varies with time. It was found that the pre-filter time delay t_d greatly affects the performance of the control loop. Figure 9.14 shows a measurement of THD+N versus output power

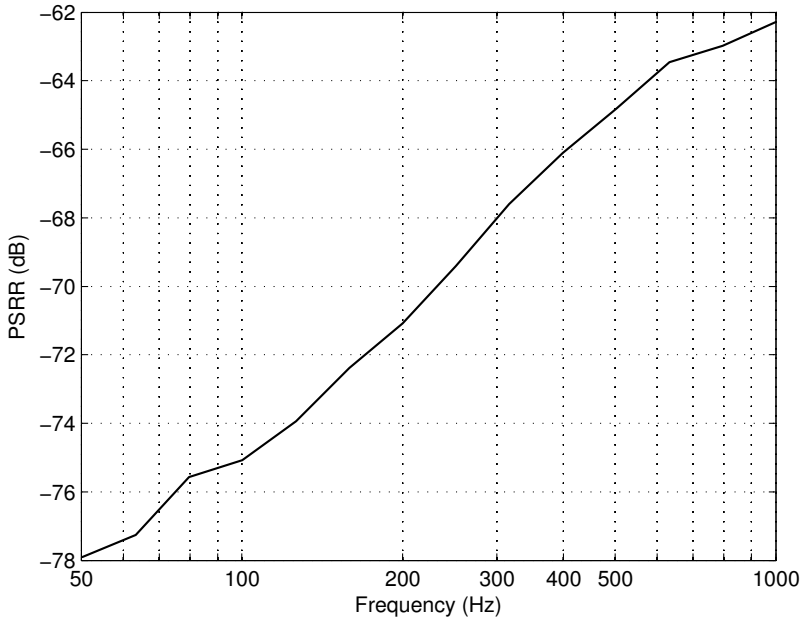


Figure 9.13: Measured PSRR as a function of frequency.

for PS1 with different values of t_d when both control loops are active. The load is 8.2 Ω and the frequency of the input signal is 1 kHz. Note the significant variation in the measurements between different values of t_d. When $t_d = 125$ ns there is a substantial improvement in THD+N below 20 W, with THD+N as low as 0.0004 % at 13 W. It was found that decreasing t_d below 125 ns resulted in reduced performance. Also note that, as expected, distortion is significantly higher when ripple compensation is absent.

Figure 9.15 shows a similar measurement for PS2. In this case there is an improvement in THD+N for increasing values of t_d. Increasing the value of t_d above 225 ns results in reduced performance.

The propagation delays for PS1 and PS2 were measured as 160 ns and 108 ns, respectively, when $m_a = 0$. It is at present unclear as to how exactly the actual, time-variant, propagation delay and the constant delay in the ripple compensation transfer function interacts to affect distortion in this way.

For completeness, Figure 9.16 shows a measurement of THD+N versus frequency for PS1 when $t_d = 125$ ns for 10 W into 8.2 Ω. Figure 9.17 shows an FFT of the distortion residue for 10 W into 8.2 Ω with a 1 kHz test tone. Comparing Figure 9.6 (a) and Figure 9.17, we see that the main difference between $t_d = 125$ ns and $t_d = 150$ ns is the magnitude of the second harmonic. With $t_d = 125$ ns the second harmonic is about 17 dB lower compared to when $t_d = 150$ ns.

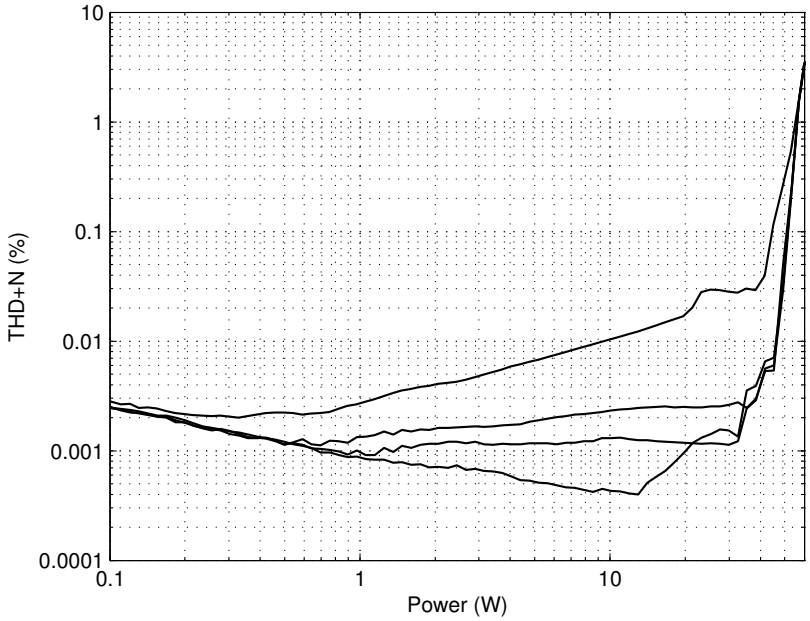


Figure 9.14: Measured THD+N versus frequency of PS1 with 1 kHz into 8.2 Ω for different values of t_d. From top to bottom: no ripple compensation, $t_d = 175$ ns, $t_d = 150$ ns, and $t_d = 125$ ns.

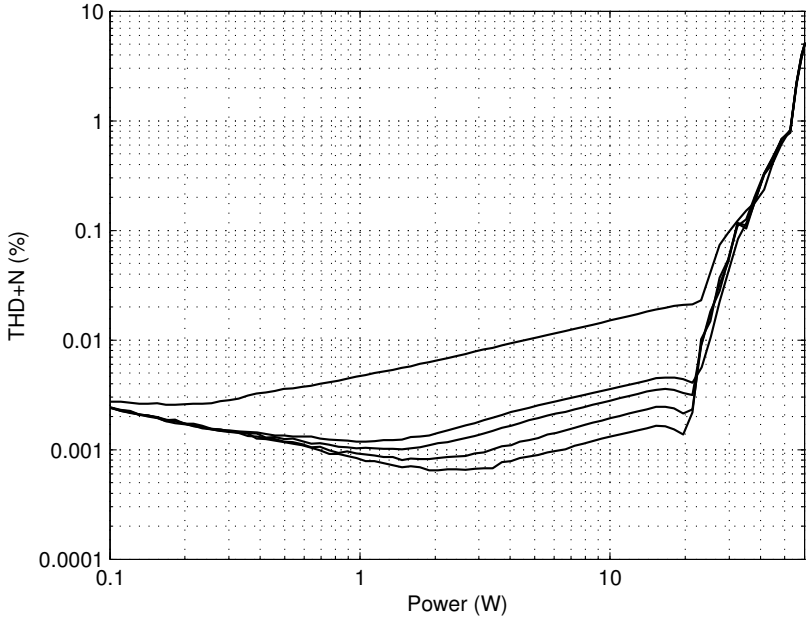


Figure 9.15: Measured THD+N versus frequency of PS2 with 1 kHz into 8.2 Ω for different values of t_d. From top to bottom: no ripple compensation, $t_d = 150$ ns, $t_d = 175$ ns, $t_d = 200$ ns, and $t_d = 225$ ns.

9.9 Efficiency

Optimising efficiency was not the focus of this thesis. Nevertheless, the efficiency of the amplifier is 87.3% with 100 W into 4.1 Ω. Total idle losses are 2.54 W, with power stage

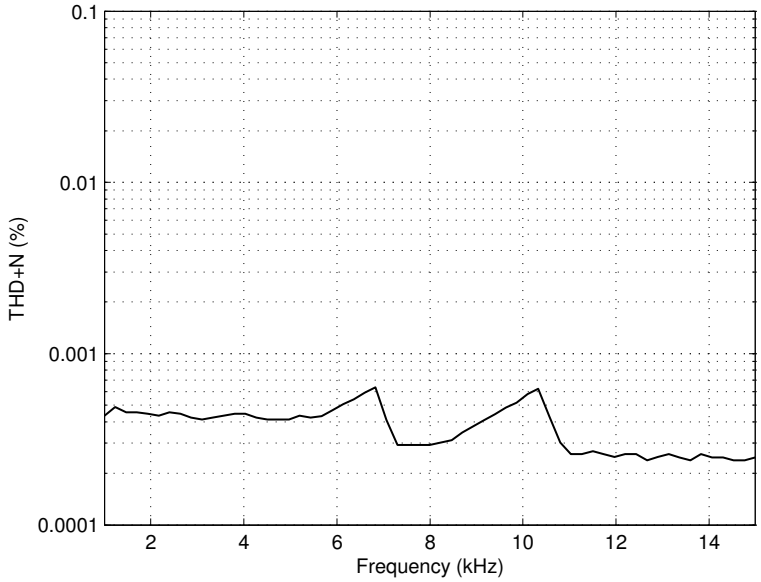


Figure 9.16: Measured THD+N versus frequency of PS1 at 10 W with $R_o = 8.2\ \Omega$ and $t_d = 125$ ns.

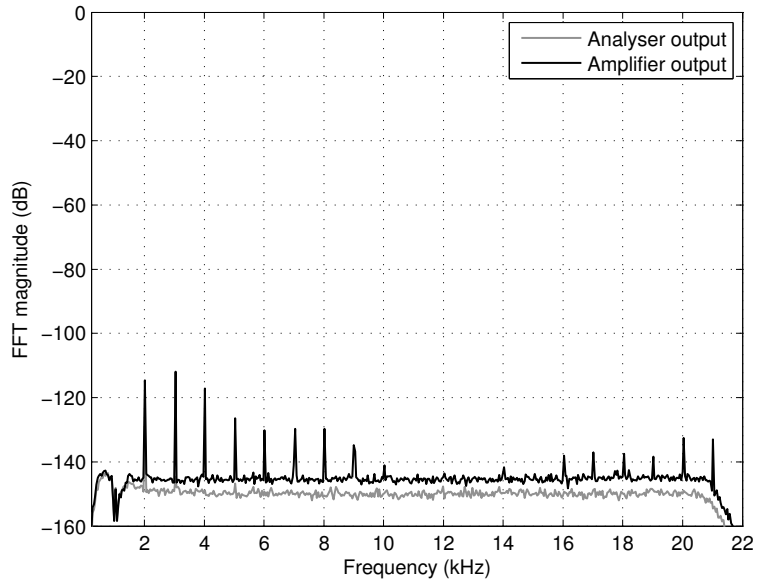


Figure 9.17: FFT of the distortion residue of PS1 with 10 W at 1 kHz into 8.2 Ω for $t_d = 125$ ns. THD+N is 0.00044%. The suppressed fundamental is at 0 dB.

shoot-through due to the small blanking time contributing 1.94 W.

9.10 Summary

This chapter presented measurements of the amplifier as designed in the previous chapters. Most measurements correlated well with theoretical expectations. It is shown that the

control loop is capable of improving the relatively poor open loop performance of the amplifier to state-of-the-art levels. THD+N levels as low as 0.0004% at 1 kHz with 13 W into 8.2 Ω is achievable. The frequency response is flat to within 0.08 dB in the audio band and output impedance does not exceed 10 mΩ. PSRR is lower than -62 dB for frequencies below 1 kHz.

Chapter 10

Conclusions

10.1 Overview

10.1.1 Hardware Design

Chapter 3 documented the design of a half-bridge class-D output stage. The output stage was designed with closed-loop operation in mind and specific attention was paid to EMI considerations. The output stage is capable of delivering 100 W into a 4 Ω load. Measured THD+N is 0.3% with 10 W into 8.2 Ω at 1 kHz.

In Chapter 4 the design of an FPGA-based carrier generator was discussed. The advantage of an FPGA carrier generator lies in the fact that an arbitrary carrier can be generated, which is very useful in a prototype design. Furthermore, it is very simple to implement the ripple compensation technique.

10.1.2 Control Design

Chapter 5 concerned the development of the control loop topology. The final control loop consists of two feedback loops: a passive, unconditionally stable inner loop and an active, conditionally stable outer loop. When over-modulation occurs, the outer loop is deactivated in order to maintain stability.

In Chapter 6 the control loop of Chapter 5 was modified by modelling the comparator as a sampling operation. The feedback loops were converted to the z-domain through the impulse invariant transform. Signal transfer functions and error transfer functions were derived.

Chapter 7 concerned the detail design of the control loop. The effect of the impedance of the loudspeaker on stability was investigated. It was found that the loudspeaker can be modelled as a resistor, but not necessarily a resistor with value equal to the nominal

impedance of the loudspeaker. The error transfer function was optimised and has a maximum value of -50.8 dB in the audio band.

10.1.3 Design Verification

Chapter 8 showed simulation results that confirmed the correct operation of the control loop. It was confirmed that the control loop scales the power stage error in accordance with the error transfer function and that the system remains stable during over-modulation.

Detailed measurements of the amplifier were presented in Chapter 9. Most measurements correlated well with theoretical expectations. It was found that the delay in the ripple compensation transfer function significantly affects the performance of the control loop. Measurements confirmed that excellent performance can be achieved with relatively high levels of open loop distortion. The performance goals listed in Section 1.2 were all surpassed. Efficiency was measured as 87.3% at 100 W, which is far greater than any linear amplifier of similar power and performance can achieve.

10.2 Improvements and Future Work

10.2.1 Switching Frequency

The switching frequency of 768 kHz is very high and leads to unnecessarily high switching losses. We needed a high switching frequency to obtain the necessary loop gain for the inner loop to make its frequency response insensitive to load variations. In hindsight, however, the author is of the opinion that a lower loop gain would have been sufficient for the inner loop. It should also be noted that a reduction in switching frequency lowers the total required loop gain, since open loop distortion scales approximately proportional to switching frequency.

10.2.2 Robustness

In Chapter 7 the system is designed for a phase margin of 24°. This is a fairly large phase margin considering the accuracy with which the system is modelled. Initial designs had smaller phase margins and, consequently, higher loop gains. However, these designs were not always stable into high impedance loads. It is believed that the modulator might be plagued by a problem that is also found in high-order continuous-time sigma-delta modulators. The noise transfer function of an ideal high-order sigma-delta modulator has significant out-of-band gain. The amplified out-of-band noise can cause instability by overloading the quantiser [45]. Further investigation is needed to improve robustness.

10.2.3 Carrier Generation

The FPGA-based carrier generator worked very well, but it is not feasible in a cost-optimised design. It is suggested that an analogue carrier generator be developed. Note that while this might seem simple in principle, the generation of a highly accurate saw-tooth waveform is not a trivial matter.

10.2.4 Design Optimisation

The optimisation algorithm that is used in Chapter 7 to optimise the control loop is very crude and computationally inefficient. It is suggested that other design optimisation methods are investigated. The possibility of designing directly in the z-domain, instead of continually transforming between the s- and z-domain, should also be investigated.

10.2.5 The Effect of a Non-Constant Propagation Delay on Ripple Compensation

The value of the constant delay in the ripple compensation transfer function, which should ideally match the propagation delay in the loop, has a significant impact on THD. The behaviour of ripple compensation in a loop with a non-constant propagation delay should therefore be investigated.

10.3 General Conclusions

The thesis objectives as set out in Section 1.2 have been reached. It has been shown that, if properly implemented, feedback error control can make high-fidelity clocked class-D amplification possible without necessarily sacrificing efficiency or EMI performance. Also, it should be understood that the work presented in this thesis is not limited to class-D audio power amplifiers. Many other PWM based power electronic converter applications can benefit from the same techniques.

As a closing remark, the author greatly enjoyed the research topic. The knowledge and experience gained is invaluable.

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Appendices

Appendix A

Complete Circuit Schematics

This appendix contains complete circuit schematics, as used in the PCB design.

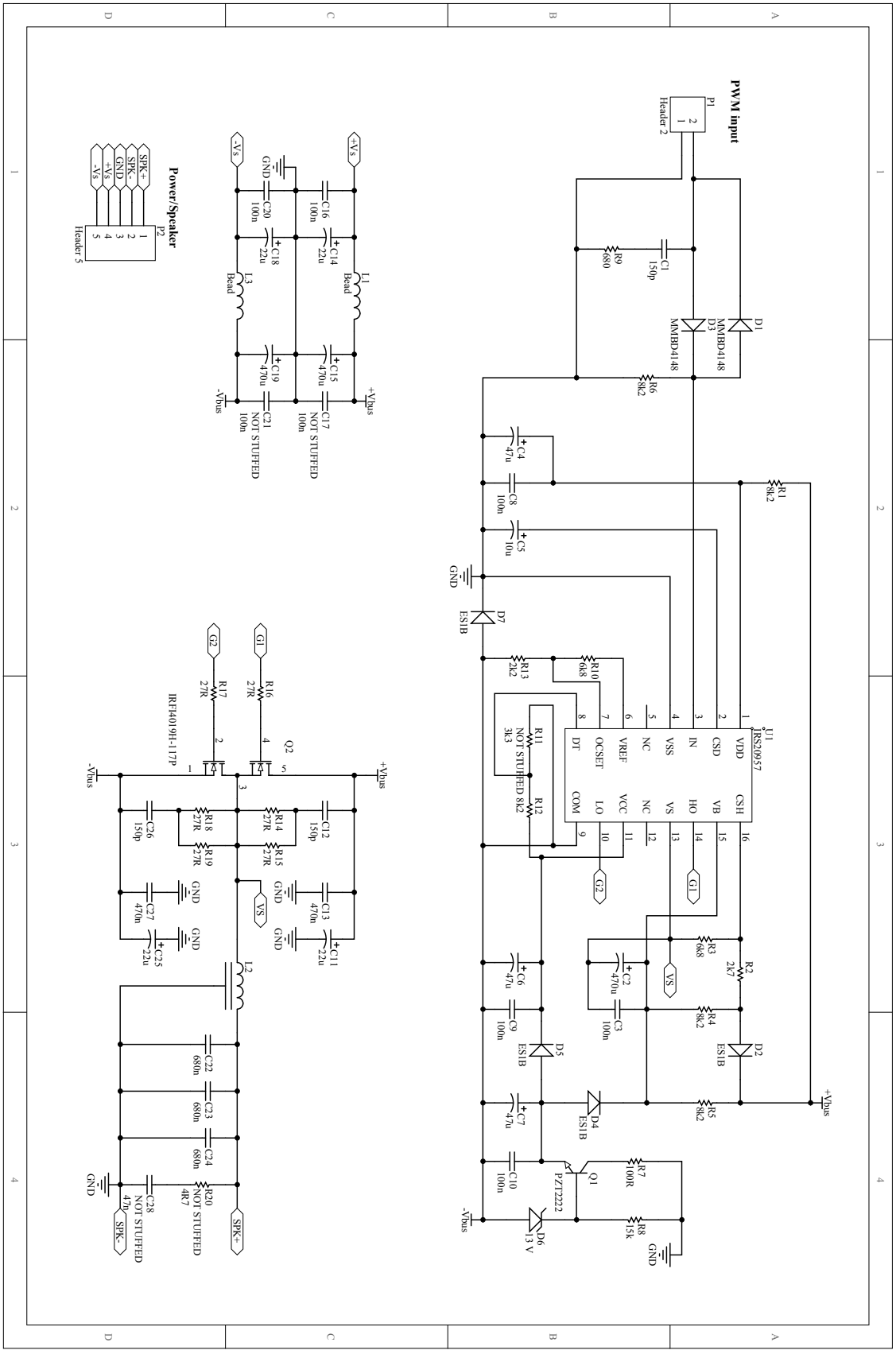

Figure A.1: Output stage schematic.

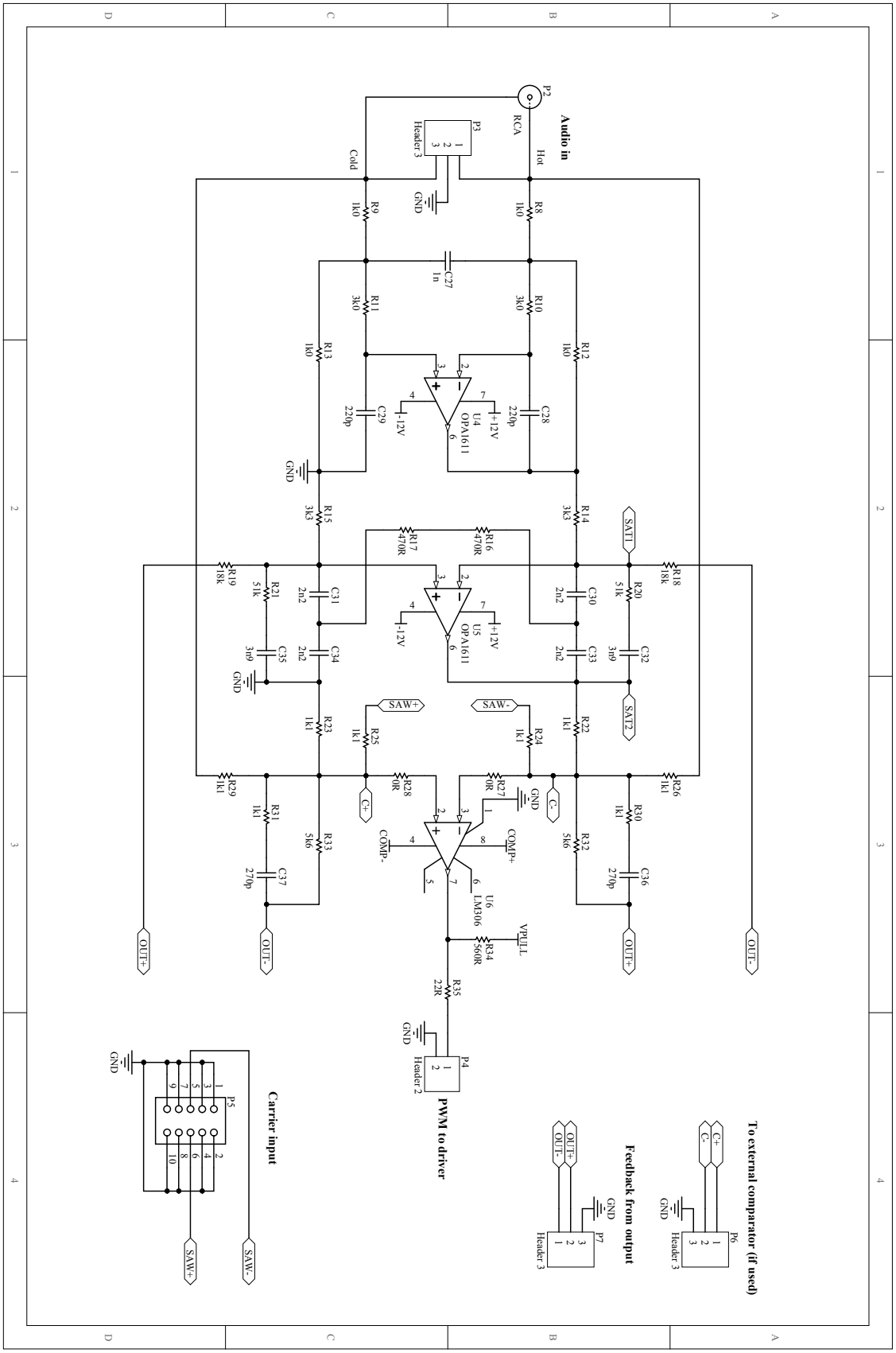

Figure A.2: Control stage schematic (part one).

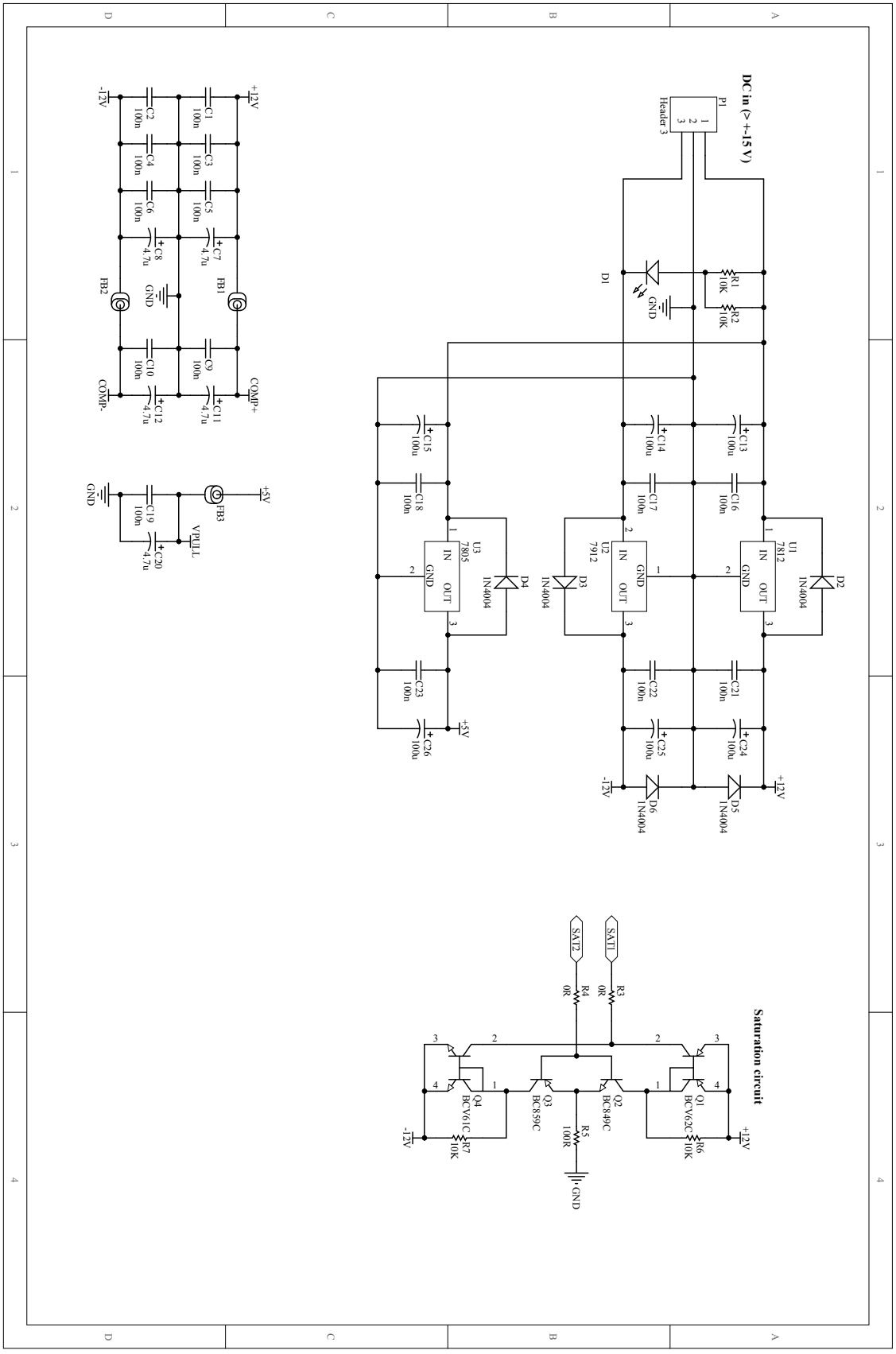

Figure A.3: Control stage schematic (part two).

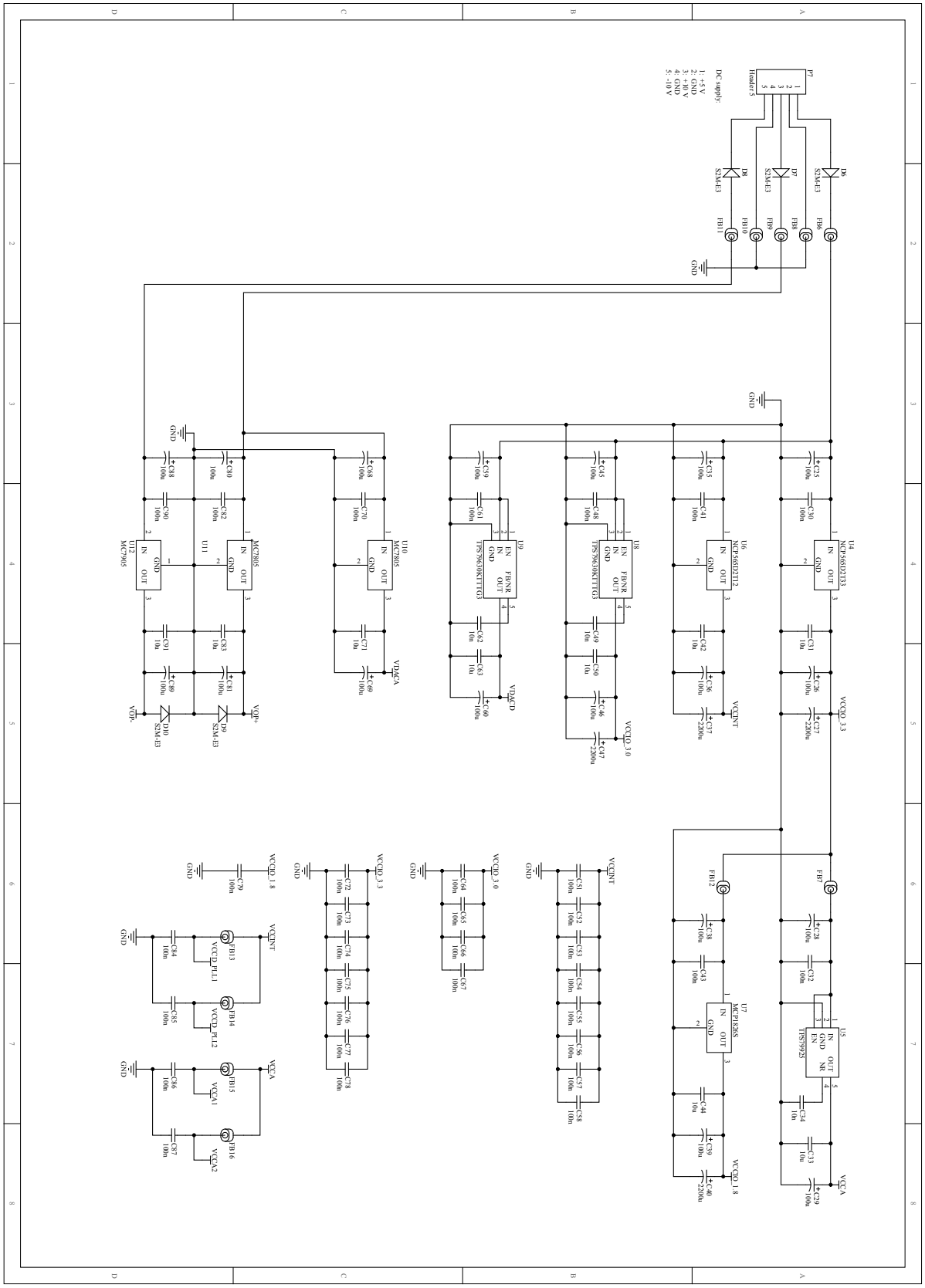

Figure A.4: FPGA carrier generator schematic (part one).

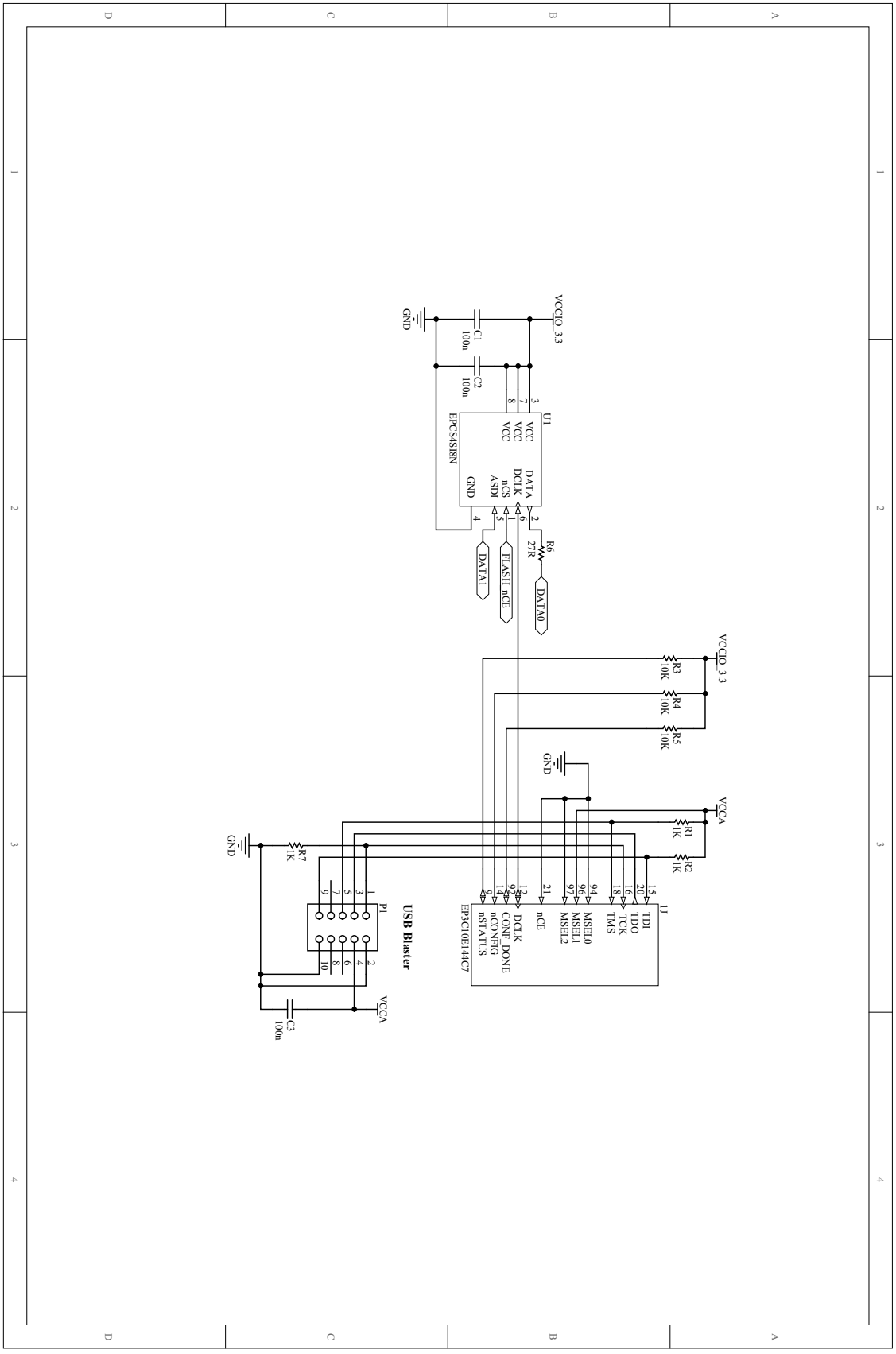

Figure A.5: FPGA carrier generator schematic (part two).

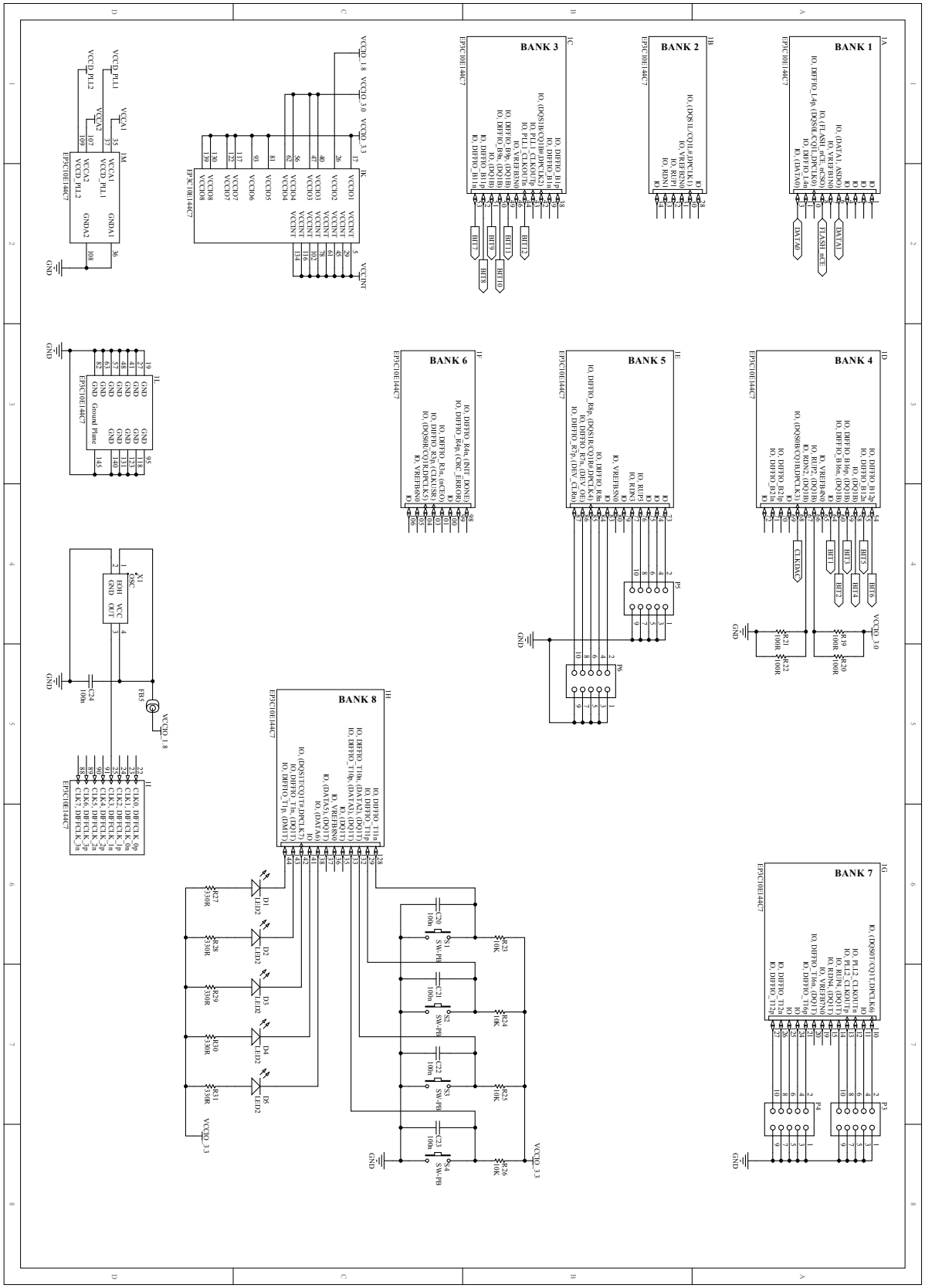

Figure A.6: FPGA carrier generator schematic (part three).

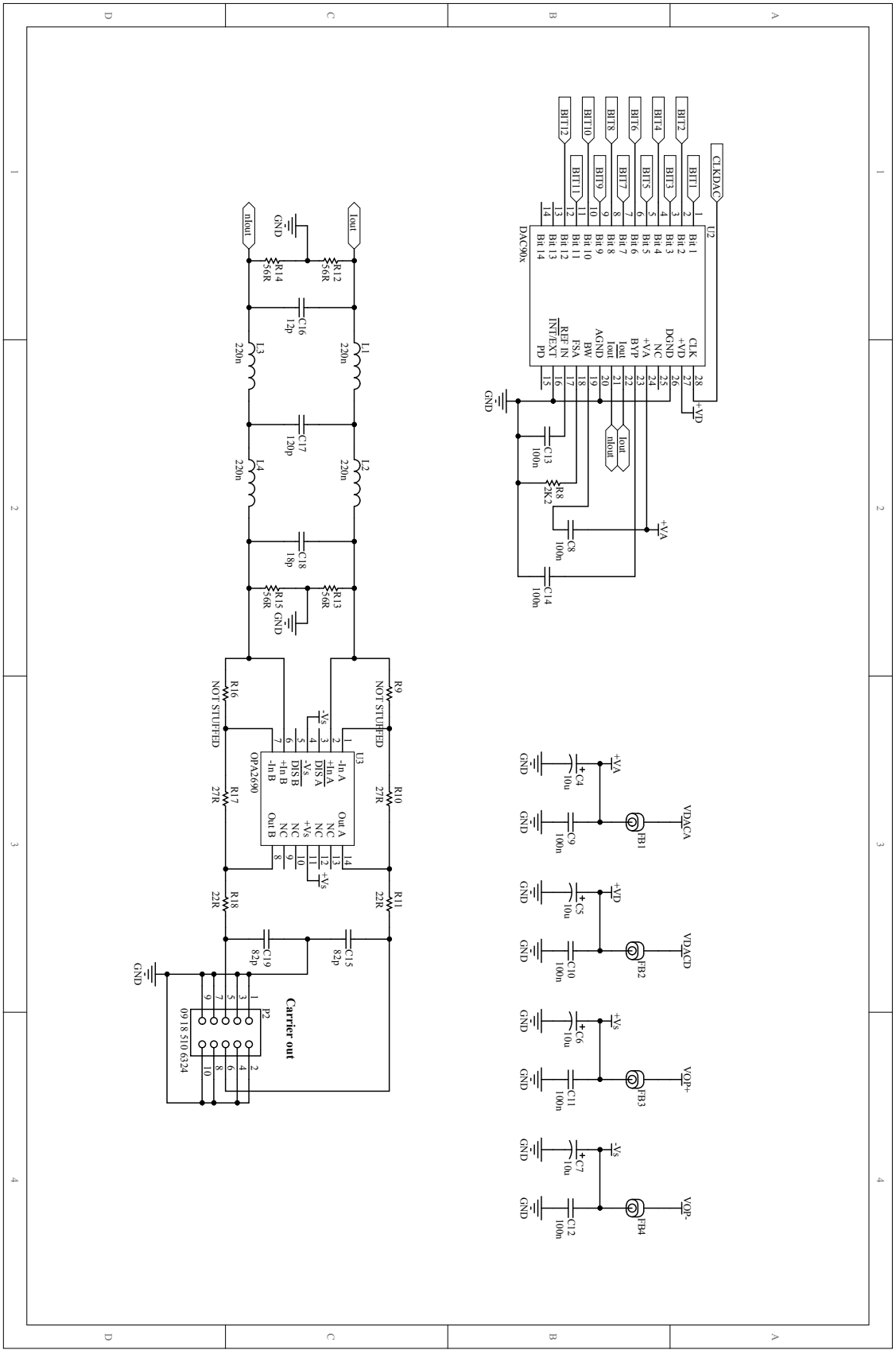

Figure A.7: FPGA carrier generator schematic (part four).