

11. IC DESCRIPTIONS

• SM5807FP (quadruple oversampling digital filter)

This LSI is equipped with a digital filter for two channels, permitting quadruple oversampling output for each channel, so that a simple analog filter is sufficient for post processing.

In addition, since input and output are serial, compact system design was made possible, and by setting the output switching terminal it can be used for both 1 D/A converter and 2 D/A converter systems.

(I : Input terminal, O : Output terminal, IP : Input terminal with pull-up)

Pin No.	Pin Name	I/O	Pin Function	
1	XT	I	Oscillation input terminal	
2	$\overline{\text{XT}}$	O	Oscillation output terminal	
3	$\overline{\text{CKSL}}$	IP	$\overline{\text{CKSL}}=\text{H}$: Crystal oscillation (384 fs=16.9344 MHz) or external input to XT. $\overline{\text{CKSL}}=\text{L}$: Crystal oscillation (192 fs=8.4672 MHz) or external input to XT. (See Note 1.)	
4	CKO	O	Clock output (See Note 1.)	
5	LRCI	IP	44.1 kHz sync clock input Operation starts at the rising edge of the sync clock LRCI.	
6	DIN	IP	Serial data input	Serial input data is input at the rising edge of the serial input bit clock BCKI. The serial data is latched at the internal register by the sync clock LRCI after 16 bits are entered.
7	BCKI	IP	Serial input bit clock	
8	Vss	/	GND terminal (0V)	
9	$\overline{\text{SOMD}}$	IP	$\overline{\text{SOMD}}=\text{H}$: 1 D/A converter output mode (Serial data of Lch and Rch is output alternately from DOUT, thus conversion can be performed by one D/A converter.) $\overline{\text{SOMD}}=\text{L}$: 2 D/A converter output mode (Lch bit clock pulse is output from the WDCO terminal, thus in-phase conversion using two D/A converters is possible.)	
10	DGR	O	Deglitched signal for Rch (176.4 kHz, 25% duty)	
11	DGL	O	Deglitched signal for Lch (176.4 kHz, 25% duty)	
12	DOUT	O	Serial data output Data is output by MSB first with two's complement format. The data varies synchronizing at the serial output bit clock (BCKO terminal output) falling edge.	
13	WDCO	O	$\overline{\text{SOMD}}=\text{H}$: Output control clock (352.8 kHz) $\overline{\text{SOMD}}=\text{L}$: Lch bit clock	
14	$\overline{\text{LRCO}}$	O	Output control clock (176.4 kHz)	
15	BCKO	O	Serial output bit clock (8.4672 MHz) output terminal	
16	VDD	/	+ power supply terminal (TYP=5V)	

Note 1 :
The system clock pulse is generated by crystal oscillation (X'tal) or external input (EXT) as shown in table 11.1.

$\overline{\text{CKSL}}$	H or open	L
Clock pulse generation method	Crystal oscillation or external input	Crystal oscillation or external input
XT input frequency	384 fs= 16.9344 MHz	192 fs= 8.4672 MHz
Clock output (CKO)	384 fs= 16.9344 MHz	192 fs= 8.4672 MHz
System clock	192 fs= 8.4672 MHz	192 fs= 8.4672 MHz

Table 11.1 Clock Pulse Generation Method