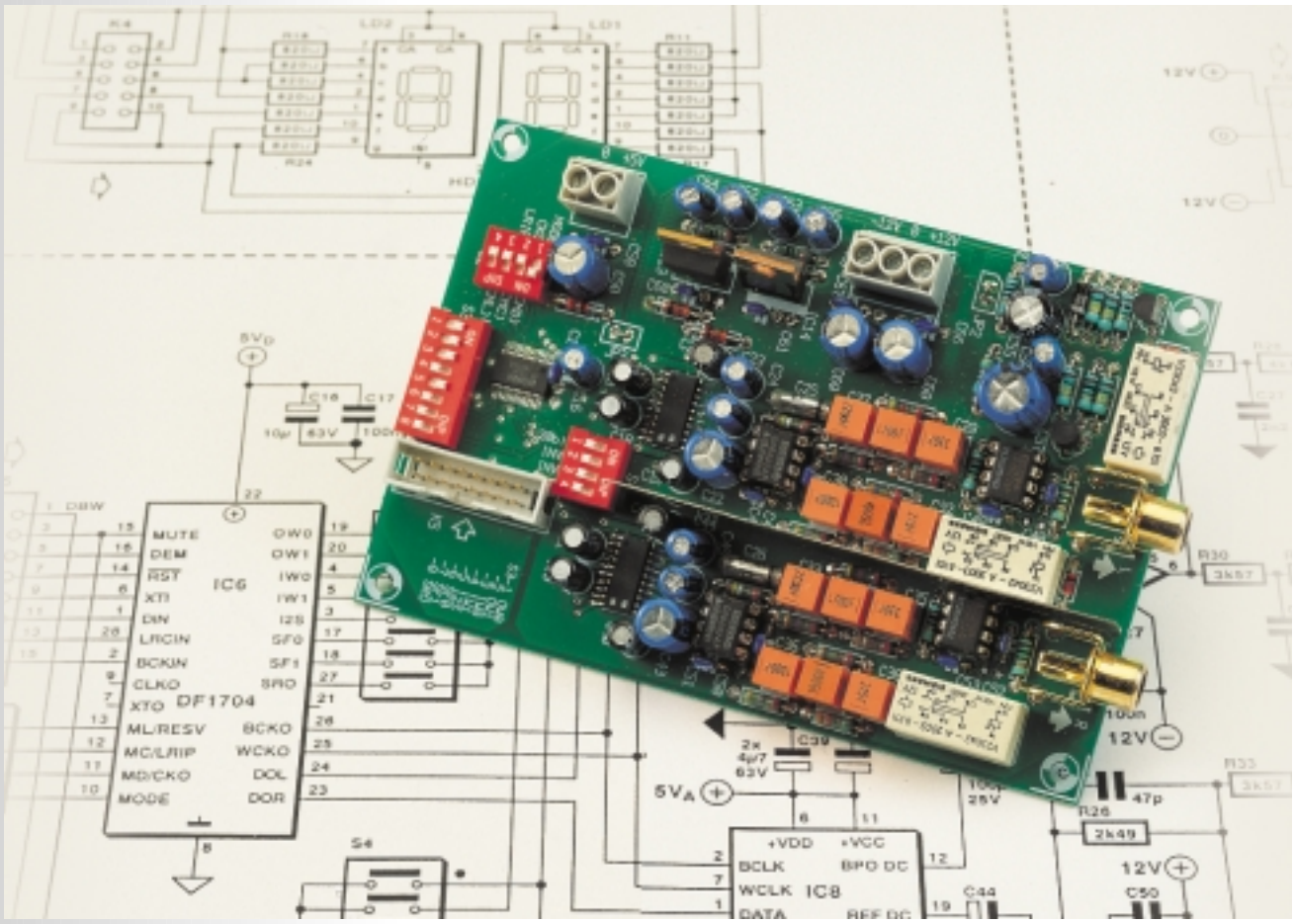
audio DAC 2000

Part 2

digital filter and DACs



Last month's Part 1 of this article dealt primarily with a general description of the new digital-to-analogue converter (DAC) 'Audio DAC 2000' and details of the input section. In this second and penultimate part the remainder of the circuit, more especially the digital interpolation filter and the actual DACs, is described.

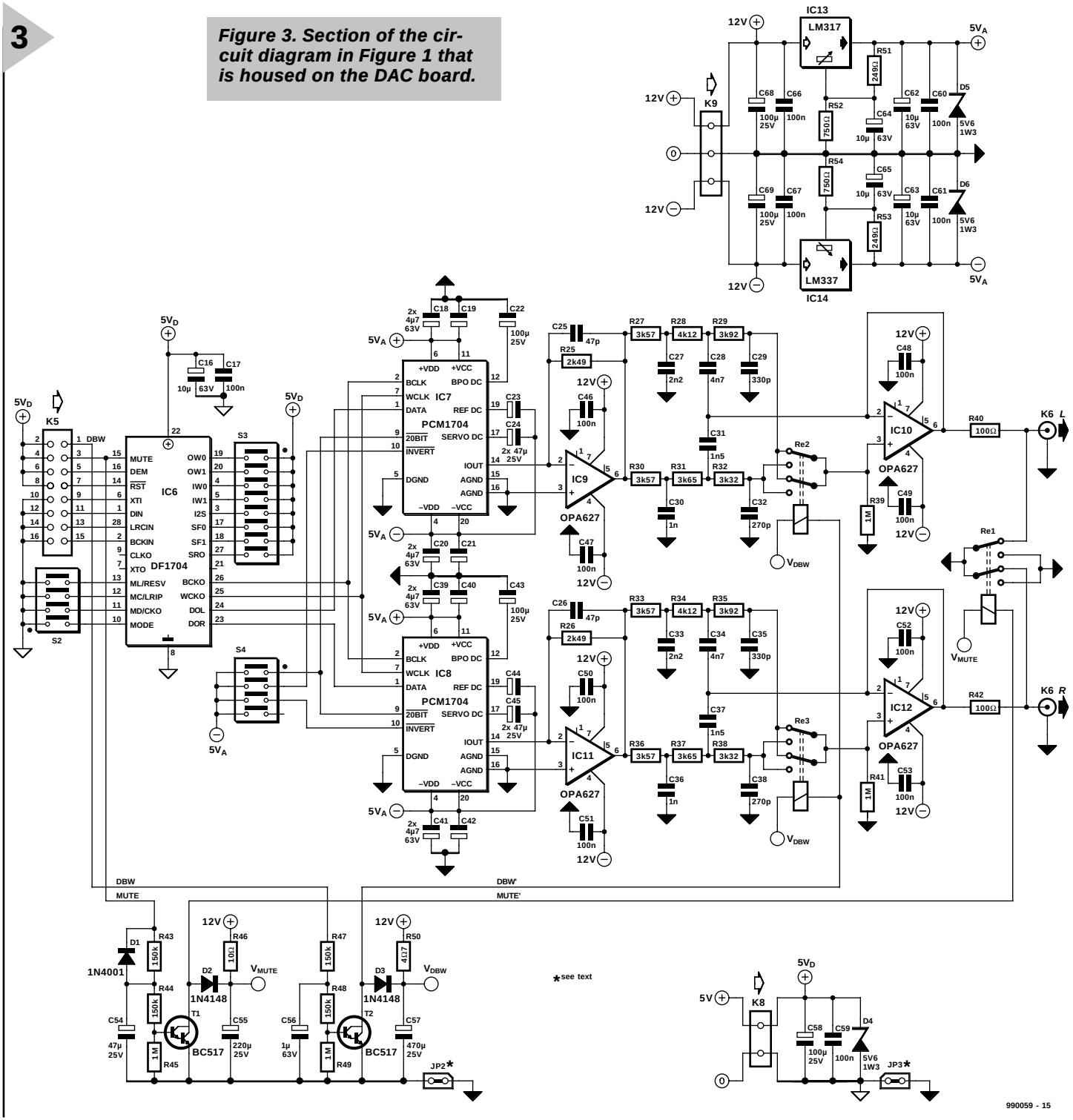
Design by T Giesberts

INTRODUCTION

It is clear from the description of the overall design in last month's instalment that the Audio DAC 2000 can be divided into four distinct sections: the power supply, the receiver and display driver, the LED display, and the DACs. These sections are identified in the circuit diagram in Figure 1 by dashed lines.

The DAC section includes the digital interpolation filter, the output filter, the various relays, and the DACs. For clarity's sake, these circuits are reproduced in **Figure 3**.

Figure 3. Section of the circuit diagram in Figure 1 that is housed on the DAC board.



DIGITAL FILTER

The integrated digital interpolation filter, IC_6 (Burr-Brown Type DF1704) is a multipurpose device, which

- is suitable for sampling rates of 32–96 kHz;
- can be used as a notch filter providing 115 dB attenuation;
- has an input suitable for 16/20/24 bits;
- has an output of 16/18/20/24 bits;
- provides automatic sensing of the ratios of the clock frequencies (system clock up to $768F_s$ – where F_s is the sampling rate);
- can be used as slow roll-off filter;
- provides a soft mute;
- provides digital emphasis;
- has a digital attenuator.

Various input and output formats can be set via hardware or software. In the Audio DAC, setting via hardware has been opted for, since in its standard application the unit will invariably have a fixed place in the audio system. This means that the various DIP switches normally need to be set only once. However, as in the receiver, there is space for experimentation, but note that the measurements given in this article refer to default settings of the DF1704.

The only difference between control via software and hardware is that with the former a digital attenuator can be used independently, providing 256 steps of 0.5 dB each both to the left and to the right.

One of the more important settings is the correct tuning to the format set at the receiver, that is, I^2S.

With reference to **Table 1**, the various possible settings are detailed below.

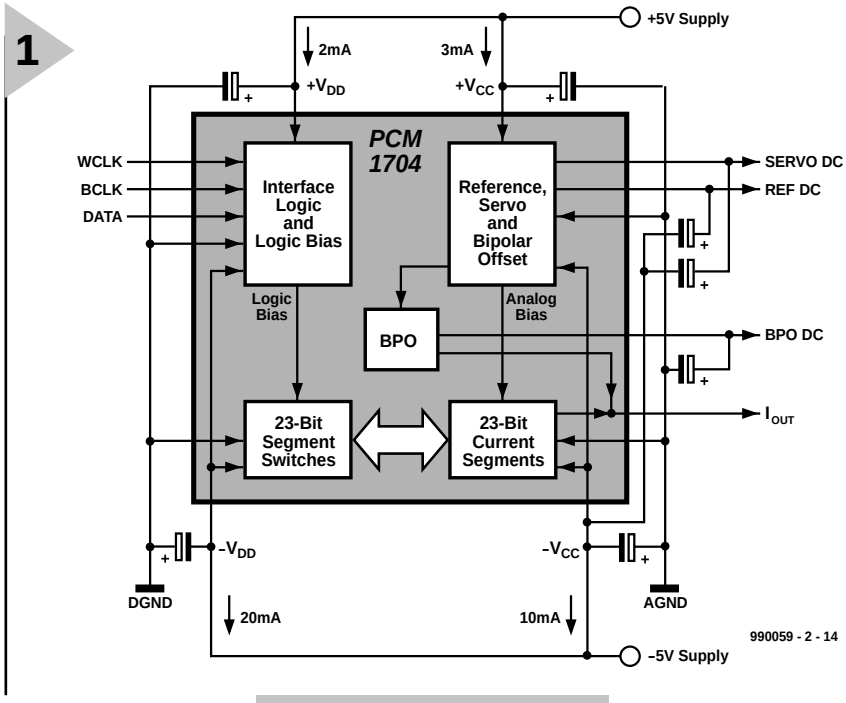


Figure 4. Internal block diagram of the integrated digital-to-analogue converter Type PCM1704.

DIP switch S2 is a quadruple device since pins 11–13 have dual functions. When mode pin 10 is high, these pins form a 3-wire software-control port and are then called MD, MC, and ML, respectively. These names are shown in brackets adjacent to the pin locations on the board. At the other side of the location the hardware mode functions are shown, just as the levels adjacent to ON and OFF. In the present application, this arrangement is not used, but S2 may, if desired, be replaced by an 8-pin board connector (to accept flatcable) to, say, link the digital filter to a microcontroller.

Pins 11–13 and mode pin 10 have internal pull-up resistors, so that a closed DIP switch (ON) results in a low level at S2. This means that for the hardware mode, section 1 of S2 must be closed (Mode = low). Pin 13 (RESV – section 4 of S2) is then not used.

Pin 12 (LRIP – section 3 of S_2) determines at which level of the L/R clock the data must be considered as belonging to the lefthand channel or to the righthand channel. When section 3 of S2 is off, LRIP is high, whereupon it is assumed that when clock signal LRCIN is high, the data are intended for a lefthand sample. In the I^2S mode, LRIP is not used.

Pin 11 (CKO – section 2 of S2) determines whether the CLKO output on pin 9 is equal to the clock at XTI or XTI/2. This pin has no specific function in the Audio DAC and is therefore not used.

It is possible to connect a crystal oscillator to pins XTI and XT0, but this is rather pointless since XTI is provided by the high-precision master clock (MCK) in IC_1. XTI may have a number of values: $256F_s$, $384F_s$, $512F_s$, and $768F_s$. Its maximum value at $512F_s$ and a sampling rate of 96 kHz is 49.152 MHz, but the maximum possible frequency of a crystal oscillator is 24.576 MHz. In fact, at $256F_s$ and a sampling rate of 96 kHz, the manufacturer advises against the use of a crystal oscillator and suggests the use of an external source for XTI. This is the reason that there is no space reserved for a crystal oscillator on the board.

Bit clock BCKIN may be $32F_s$, $48F_s$, or $64F_s$, while LRCIN is, of course, always equal to F_s. The input formats are self-evident and should be compared with the output format of IC_1. When both a CD player and a DVD player with a 24 bit/96 kHz are to be connected to the Audio Dac, the mode should always be 24 bit, which fixes the position of the MSB.

The various input formats are determined by inputs IW0 and IW1, and I^2S, that is, sections 3, 4, and 5, of S3 respectively. For clarity's sake, the function of the sections of S3 is shown in tabular form on the board adjacent to K5.

The output format is determined by inputs OW0 and OW1, that is, sections 1 and 2 of S2, XTI, and the 8-times oversampling. The format is always complement 2, MSB first and right justified. DOR contains samples for the righthand channel only, and DOL for the lefthand channel only. The inputs sense whether the data at the output contains 16, 18, 20, or 24 bits per sample.

Output word clock WCKO is, of course, always $8F_s$, irrespective of the system clock. Output bit clock BCKO is determined by the system clock and is $256F_s$ when XTI is $256F_s$ or $512F_s$, or $192F_s$ when XTI is $384F_s$ or $768F_s$. In the present application, BCKO is always equal to the master clock (MCK) of IC_1. The outputs are set to 24 bits by setting sections 1 and 2 of S3 to ON.

The slow rolloff filter function ensures reduced ringing in the pass band, but produces more aliasing products. The manufacturer recommends that the filter is not used above 96 kHz. Input SRO (pin 27) determines whether the filter is used; its level is set with section 8 of S3, which is normally OFF.

When the deemphasis control is actuated by the receiver, IC1, the two remaining inputs, SF0 and SF1 (pin 17 and 18) respectively determine for which sampling rate the deemphasis is valid. This is normally 44.1 kHz, on the assumption that deemphasis is usually required for certain CDs only. All inputs that are controlled via S3 have internal pull-down resistors, which is the reason that S3 is linked to the +5 V line.

Soft mute control input MUTE is switched directly by error output ERF of IC1 (which is inverted by the GAL). When the level at MUTE is low, the digital filter is in the mute position — the output relay is then deactuated.

The DF1704 has an internal power-on reset as well as a reset input. The internal reset lasts for 1024 system clock periods after the supply voltage has been switched on; all outputs are then low. This is true also after a low-to-high change at the RST pin.

DIGITAL-TO-ANALOGUE CONVERTERS (DAC)

The data from the digital filter is applied to two high-quality digital-to-analogue converters (DACs), IC7 and IC8, whose internal block schematic is shown in **Figure 4**.

These devices

- are suitable for sampling rates of 16–96 kHz;
- provide 8× oversampling;
- provide a choice of 20 or 24 bit data;
- have a dynamic range of 112 dB;
- provide a signal-to-noise ratio of 120 dB;
- have a glitch-free output;
- invert the data.

In contrast to oversampling data converters using, for instance, the delta-sigma architecture, the Burr-Brown devices use a different solution to the bipolar zero transition problem.

Delta-sigma converters have an inherent poor signal-to-noise ratio which makes the use of noise-shaping

circuits to improve that ratio within the audio band essential. Unfortunately, this creates an appreciable increase in noise outside the audio band. If the outputs of the DACs were not filtered correctly, an overall deterioration of performance would ensue.

The PCM1704 uses the traditional DAC structure (*R*–2*R*) in such a manner as to provide excellent low-frequency performance and yet not lose the outstanding properties of this structure: excellent full-scale performance; high signal-to-noise ratio, and simplicity of design. Burr-Brown designers term this architecture sign-magnitude. Briefly, this means that two 23-bit DACs are combined in a complementary setup which results in a highly linear output so that a 24-bit resolution is assured at the zero crossings.

The two DACs have a common reference and *R*–2*R* ladder network. The network uses dual-balanced current segments that ensure correct performance in all kinds of circumstance. Moreover, the discrete bits of the DACs are alternated so that, after laser trimming of the resistors, the DACs are identical for all purposes required by the present application.

The DAC is timed so that only the 24 bit before word clock WCLK goes low causes the data in the serial input register to be transferred to the parallel DAC register. If pin 9 (20-bit mode) is active (linked to the –5 V line), the foregoing also applies to the last 20 bit. Any other bits present will not be accepted, so that the data applied to the DAC must correspond to the mode to which the DAC is set. If this is not so, the data will become mutilated or the level is much too low.

The maximum bit clock is specified as 25 MHz, which is related to the 8× oversampling, a 32-bit frame for the data, and the maximum sampling rate, (8×32×96 kHz = 24.576 MHz). The data can be inverted by linking pin 10 (INVERT) of the PCM1704 to the negative supply line.

Pins 9 and 10 have internal pull-up resistors to digital ground (DGND) and are switched with DIP switch S4. Section 4 of this switch is not connected, so that a 3-section switch would suffice. However, 4-section switches are much more readily available.

The ICs are powered by a symmetrical ±5 V supply. This is derived via regulators IC13 and IC14 from the analogue ±12 V line and used only for the DACs. Potential dividers R51-R52 and R53-R54 set the regulators to exactly 5 V. Since there is some residual ripple on the ±12 V line (which does not affect the op amps), capacitors C64 and C65 provide additional ripple suppression. Zener diodes D5 and D6 protect the DACs against errors such as wrong resistors or defect regulators.

The manufacturer's specification stipulates that the supply lines to the digital and analogue sections must be linked as a single line to an analogue supply. There is no advantage in separating the digital and analogue supplies, but it is essential that they are decoupled to the ground plane as close to the relevant IC pins as possible. This, and that fact that internal voltages SERVO DC, REF DC, and BPO DC must be decoupled in a like manner, is the reason that the ICs are surrounded by decoupling capacitors.

The current output of the DAC is specified as 1.2 mA/200 ns (the full range is ±1.2 mA), which demands certain requirements from the I/U converter as described in the following section.

I/U CONVERTER

Op amps IC9 and IC11 on which the current-to-voltage converters are based must have:

- a very low bias current to obviate additional offset;
- a high slew rate to be able to follow the DAC accurately;
- excellent linearity.

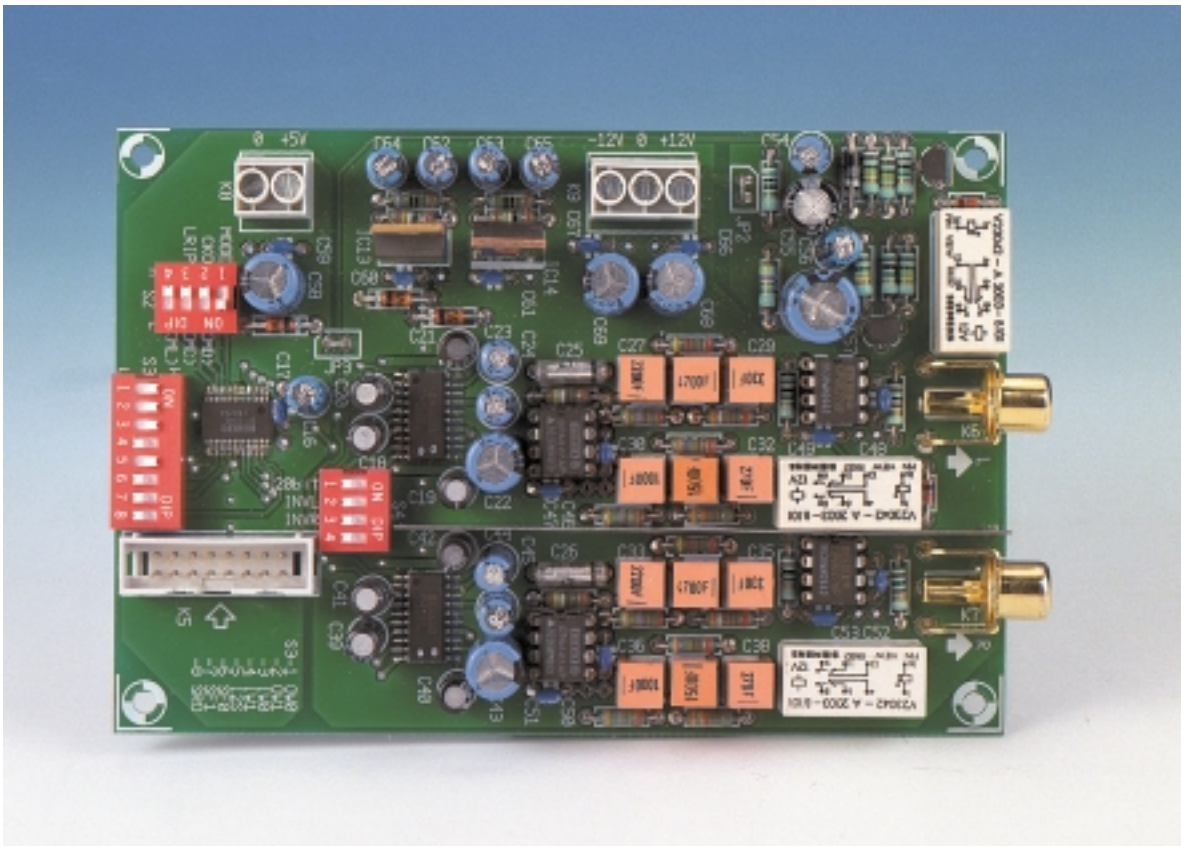
In the Audio DAC the OPA627 is used, which has a bias current of just 10 pA, a slew rate of 55 V μs^{-1}, and a distortion of only 3×10^{-7} (0.00003%).

The inherent input offset of the OPA627 ≤ 0.5 V, which results in overall offset voltages at the output of the prototype ≤ 10 mV and ≤ 20 mV respectively. This is low enough to prevent the use of an output capacitor, particularly since this would inevitably adversely affect the quality of the output signal. It is assumed in any case that there is invariably a coupling capacitor between preamplifier and output amplifier. If nevertheless an output capacitor is desired, a metallized polypropylene (MKP, Siemens) type of about 10 µF should be used. Resistors R40 and R42 may then be replaced by an external *RC* network. It should be borne in mind that a 10 µF MKP capacitor is fairly large.

The one disadvantage of the OPA627 is its low-frequency noise, which in any FET op amp is fairly high. Even so, the specified values of 20 nV/√Hz at 10 Hz and 5.6 nV/√Hz at 1 kHz are very good indeed.

Since the value of R25 and R26 is retained at 2.49 kΩ, the actual output voltage of 2.1 Vrms is slightly higher than the standard 2 Vrms.

Capacitors C25 and C26 are needed to filter r.f. components from the signal.



Because of quality considerations, these capacitors should be (axial) polystyrene types.

OUTPUT FILTER

Although the digital interpolation filter attenuates most aliasing frequencies by at least 115 dB, an analogue low-pass filter is still required to remove any residual components plus any spurious products caused by jitter of the system clock.

In fact there are two output filters, which are selected by a relay. The first, R27–R29-C27–C29 is a 3rd order Butterworth type for the more usual sampling rates of 32 kHz, 44.1 kHz, and 48 kHz. The cut-off frequency of this filter is about 27 kHz.

The second filter, R33–R35-C30–C32, is a 3rd order Bessel type for use with sampling rates of 88.2 kHz and 96 kHz. Its cut-off frequency is about 43.7 kHz.

The amplitude characteristics of the two filters are virtually identical over the audio range.

The filters are 3rd order types since the first passive section of this type of filter provides much better r.f. suppression than that of a 2nd order filter. In the latter, r.f. suppression depends on the ratio of the impedance of the filter network and the output impedance of the relevant buffer op amp.

Switching between the two filters is effected in each channel by a relay with parallel-connected double-pole change-over contacts (Re2 and Re3 respectively). The relays are 12 V types that are energized directly by the analogue +12 V line. The supply to the relays is separately filtered by R57-C57. The board layout is designed so that the return currents are separate up to the 0 terminal.

The relays switch the outputs of the two filters to the input of buffer IC10 (one channel) or IC12 (other channel). Although the non-selected filter loads the relevant I/U converter and output buffer, it does not affect the response of the selected filter.

The relays are energized indirectly by signal DBW from the GAL on the receiver board. Since this signal is a TTL signal (5 V) and the relays need 12 V, voltage conversion is needed, which is provided by darlington transistor T2. The base current of this transistor is low enough not to load the GAL to an unacceptable extent.

The only load is presented by potential divider R47–R49, which is decoupled by capacitor C56. Resistor R49 ensures that T2 is switched off at any residual voltage, which results in a much better defined switching signal for the transistor.

Diode D3 is a freewheeling diode that provides a leakage path for the energy in the circuit when the relay is deenergized.

Note that T2 switches both relays, since the coils of them are in parallel.

PIN NAME	PIN NUMBER	DESCRIPTION
RESV	13	Reserved, Not Used
LRIP	12	LRCIN Polarity LRIP = H: LRCIN= H = Left Channel, LRCIN= L = Right Channel LRIP = L: LRCIN= L = Left Channel, LRCIN = H = Right Channel
CKO	11	CLKO Output Frequency CKO = H: CLKO Frequency = XTI/2 CKO = L: CLKO Frequency = XTI
MUTE	15	Soft Mute Control: H = Mute Off, L = Mute On
I²S IW0 IW1	3 4 5	Input Data Format Controls I²S IW1 IW0 INPUT FORMAT L L L 16-Bit, Standard, MSB-First, Right-Justified L L H 20-Bit, Standard, MSB-First, Right-Justified L H L 24-Bit, Standard, MSB-First, Right-Justified L H H 24-Bit, MSB-First, Left-Justified H L L 16-Bit, I²S H L H 24-Bit, I²S
SRO	27	Digital Filter Roll-Off: H = Slow, L = Sharp
OW0 OW1	19 20	Output Data Word Length Controls OW1 OW0 OUTPUT FORMAT L L 16-Bit, MSB-First L H 18-Bit, MSB-First H L 20-Bit, MSB-First H H 24-Bit, MSB-First
SF0 SF1	17 18	Sample Rate Selection for the Digital De-Emphasis Control SF1 SF0 SAMPLING RATE L L 44.1kHz L H Reserved, Not Used H L 48kHz H H 32kHz
DEM	16	Digital De-Emphasis: H = On, L = Off

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Table 1. Hardware mode controls of the digital interpolation filter.

MUTE RELAY

The mute relay, Re1, at the output of the DAC circuit, obviates switch-on clicks and other irregular pulses on the supply lines. It is controlled by a signal from IC1 and switches the digital filter to the mute state when the receiver detects an error.

Since the impedance of both outputs is low, one relay suffices without any risk of deterioration of the channel separation at high frequencies. If there is a drawback, it is that the relay is not fast enough at switch-off, which may cause a loud click.

Like the output filters, the relay is switched by a darlington transistor, T1. When the relay is not energized, the outputs are in the mute state.

When the supply voltage is switched on, or when an error has been remedied, the relay is energized gradually to ensure that all stages have been reset correctly before the relay operates. The delay time is determined by network R43-R44-C54, the time constant of which is 3 seconds in case of a switch-on, but rather shorter after an error has been remedied.

Capacitor C1 is discharged via diode D1 so that the relay changes state immediately upon the receiver detecting an error, such as the absence of an input signal.

Network R46-C55 decouples the 12 V supply lines to ensure that the switching of the relay contacts does not create pulses on these lines.

Diode D2 is a freewheeling diode that provides a leakage path for the energy in the circuit when the relay is deenergized.

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The third and last part of this article will deal primarily with the printed circuit boards, the construction, and the test results.