audio DAC 2000
Part 1
for perfectionists

This brand-new digital-to-analogue converter (DAC) is intended especially for those audio enthusiasts who wish to have their audio system fully up to date at the beginning of the new millennium. The 24-bit resolution and the top sampling rate of 96 kHz ensure that full advantage can be taken of the qualities of the latest compact discs (CDs) and digital video discs (DVDs).

Design by T Giesberts

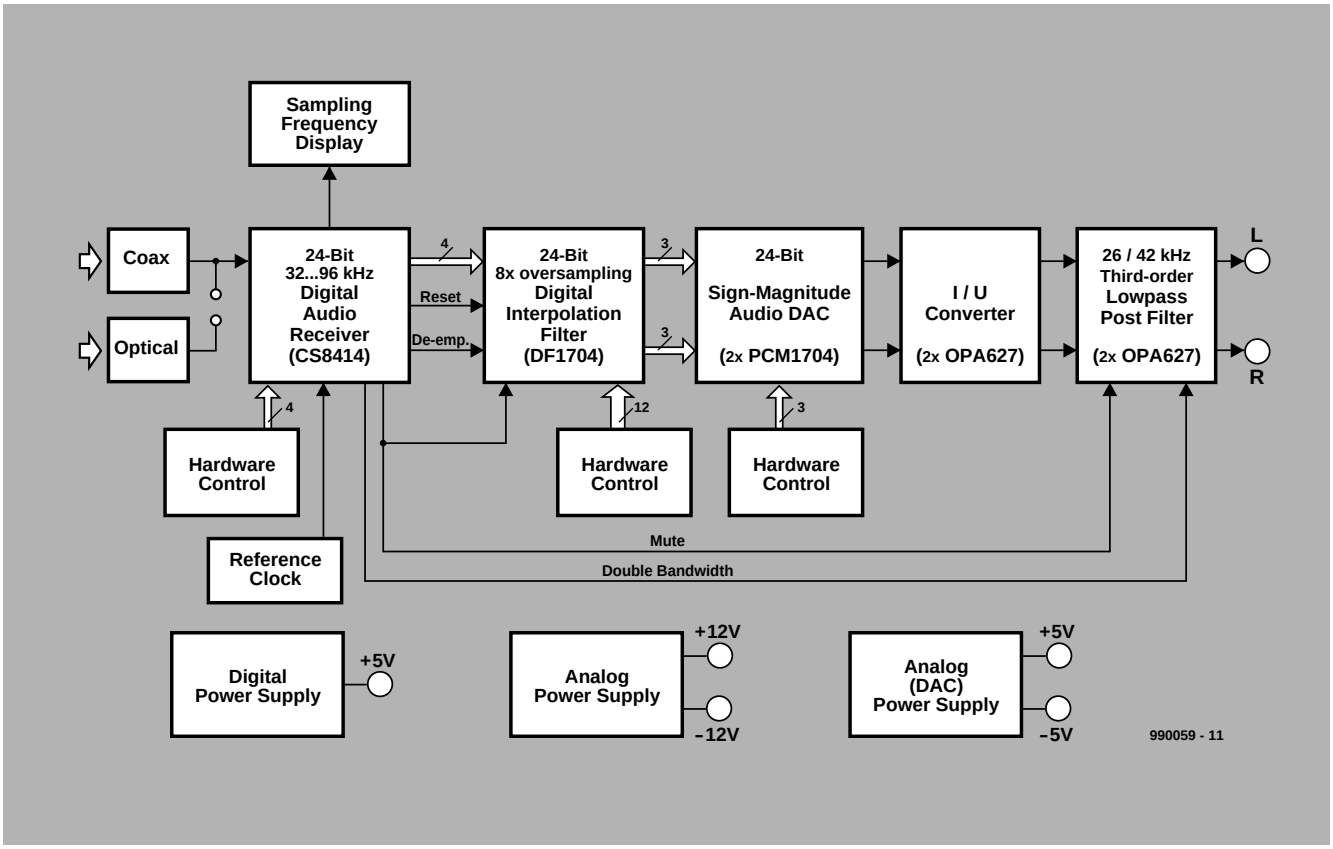


Figure 1. The block diagram of the Audio DAC 2000 clearly shows the design and what are the most important parts of the unit.

INTRODUCTION

Over the past few years there have been quite a few developments in digital audio engineering. Although quality-conscious audio enthusiasts generally welcome these developments, many of them wonder if there will ever be an end to their having to update and adapt their systems. It is, therefore, perfectly understandable that the quality DACs published in this magazine over the past seven years or so have proved very popular. After all, when it comes to re-evaluating a digital audio source, it is much simpler to update just the DAC and not the entire system. Moreover, a stand-alone DAC has the advantage that it is universal and can be combined with any CD/DVD player or digital tape recorder.

The Audio DAC 2000 is intended for the new millennium: it has a 24-bit resolution and is suitable for sampling rates of 32–96 kHz. These properties make it state of the art as far as technology is concerned, while the design of the practical circuit is aimed at quality without compromise.

Some enthusiasts may wonder why higher sampling rates have not been catered for. The answer to this is that it is questionable whether higher rates will ever be implemented. Although the new 192 kHz standard is written, pundits reckon that it will take quite a few years before the hardware and software will become commercially available.

DESIGN

The circuit is contained on four individual printed-circuit boards: one for the ±12 V and +5 V power supplies; one for the digital audio receiver with display driver; one for a 2-digit LED display; and one for the digital/analogue circuits, the digital filter, the DACs and the analogue output stage. Its block diagram is shown in **Figure 1**.

The power supplies comprise a +5 V section for the digital circuits (receiver and digital filter) and a ±12 V section for the analogue output section, including the associated relays. There is also a ±5 V supply, derived from the ±12 V supply for the DACs.

The digital audio receiver is associated with a sampling rate display, hardware control, and reference clock.

The display consists of two 7-segment LED modules for indicating the sampling rates: 32 kHz, 44 kHz (in reality 44.1 kHz), 48 kHz, 88 kHz (in reality 88.2 kHz), or 96 kHz.

The hardware control is primarily a circuit for setting the receive mode via a 4-pole dual-in-line (DIP) switch.

The reference clock is an accurate crystal oscillator operating at 6.144 MHz which is used by a comparator in the receiver to determine the frequency of the received clock – a phase-locked loop, PLL.

The data that indicate the sampling rate, and the most important received channel-status bits (strictly speaking only the emphasis bit) are multiplexed by the receiver.

The data are demultiplexed by a Generic Array Logic – GAL™ – which also drives the display. As far as the multiplexed data is concerned, they are translated and passed to the outputs of the registers. This prevents additional switching lines coming into being: a multiplexed display would demand quite a high current.

In normal operation, the outputs of the GAL are static. A number of links needed for the display are already interconnected so as to keep the number of requisite outputs to a minimum.

The link between the digital audio receiver and the display is made by a length of 10-core flatcable, and that between the receiver and DAC board by 16-core flatcable. The 16-core cable also carries the +5 V supply and various signals to and from the digital filter: serial audio data, power on reset, de-emphasis, mute, and switching. The

™ GAL is a trademark of National Semiconductor Corporation.
* Sony/Philips Digital Interface Format

switching signals almost double the bandwidth of the filter when sampling rates of 88.2 kHz or 96 kHz are detected.

The mute signal is actuated when there is no signal at the receiver input or when the PLL cannot lock. It is taken from the error output (pin 5 – ERF) of IC_1 and used to de-energize the output relay and to switch the digital filter to the mute mode.

The reset pulse for the receiver and digital filter is generated by network R_6-C_{13} and inverted by the GAL.

The de-emphasis signal is used by the digital filter to correct the pre-emphasis in the source signal. Twelve DIP switches determine the various settings of the filter as regards the input and output formats, the number of bits, the filter characteristic, and others.

The digital filter drives two DAC chips: one for the lefthand and one for the righthand channel. These chips can be set by hardware which will be reverted to later.

The output of each of the DACs is a pure current source. The type specified was chosen in view of its well-defined voltage, good linearity, low noise, low offset voltage and high slew rate. It is not cheap, but ideally suited to the present application.

The analogue filter at the output is needed to remove the residue of the oversampling products and the r.f. noise. It can be switched between two cut-off frequencies to allow the use of the two highest sampling rates.

Each filter section uses a double-pole relay, since a single-pole type for both channels would not give the requisite channel separation at high frequencies. This is because the *RC* sections of the filters have too high an impedance.

Since the output impedance per channel is only 100 Ω, a single double-pole relay is used at the output to switch the mute function on/off and to obviate switch-on noises.

CIRCUIT DESCRIPTION

The circuit diagram of the Audio DAC 2000 is shown in **Figure 2**.

An important task of the circuit is the decoding of the S/PDIF* data flow into a serial data format that can be used by the DACs, which is carried out by IC_1. The circuit associated with this chip is housed on a discrete board so that the coaxial and optical input connectors can be placed in the most convenient position on the enclosure.

The input impedance, which has the traditional value of 75 Ω as far as the coaxial input is concerned, is determined by resistor R_1.

The optical input is provided by IC_2, which is a standard chip used for this purpose in consumer equipment.

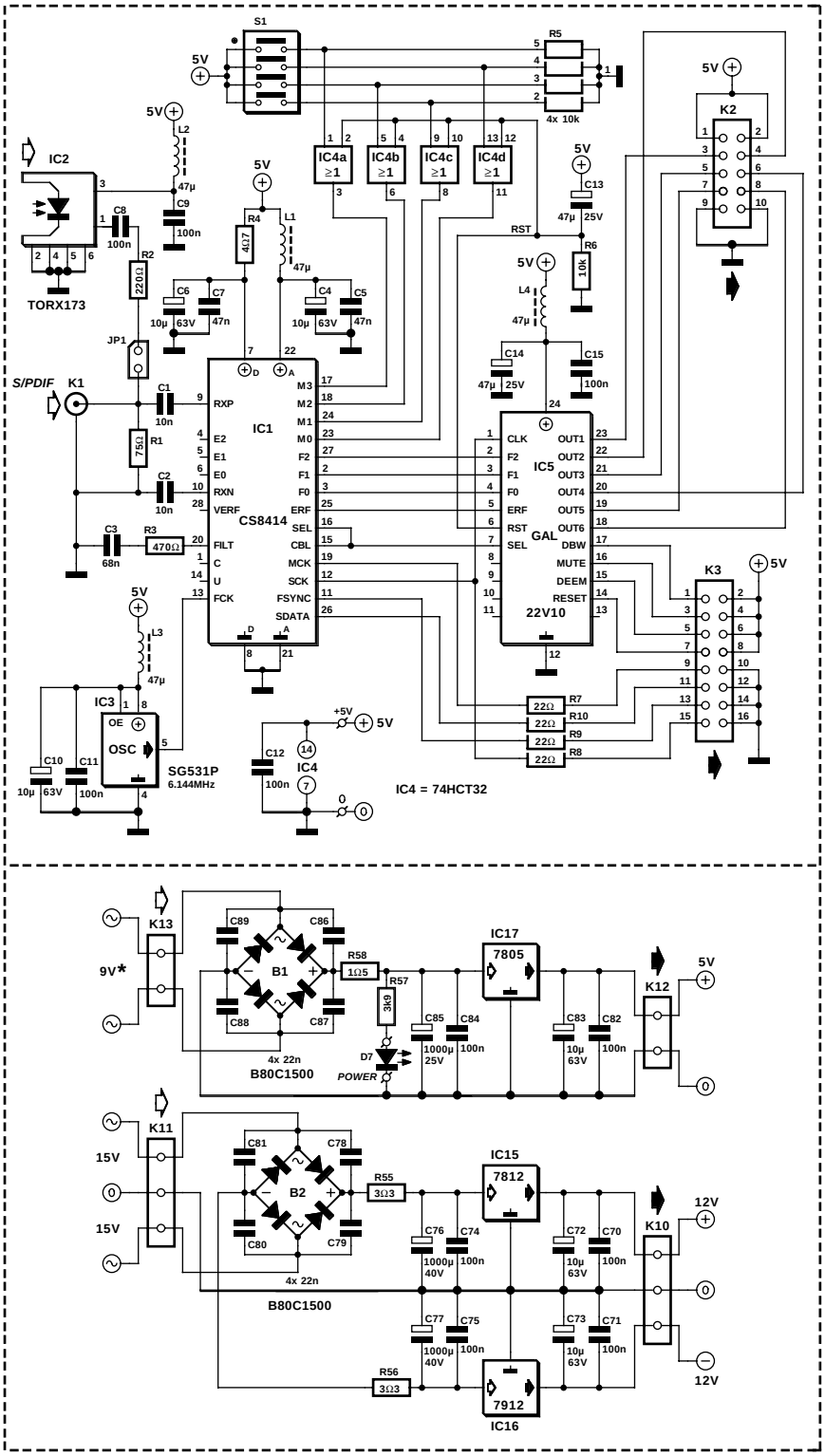
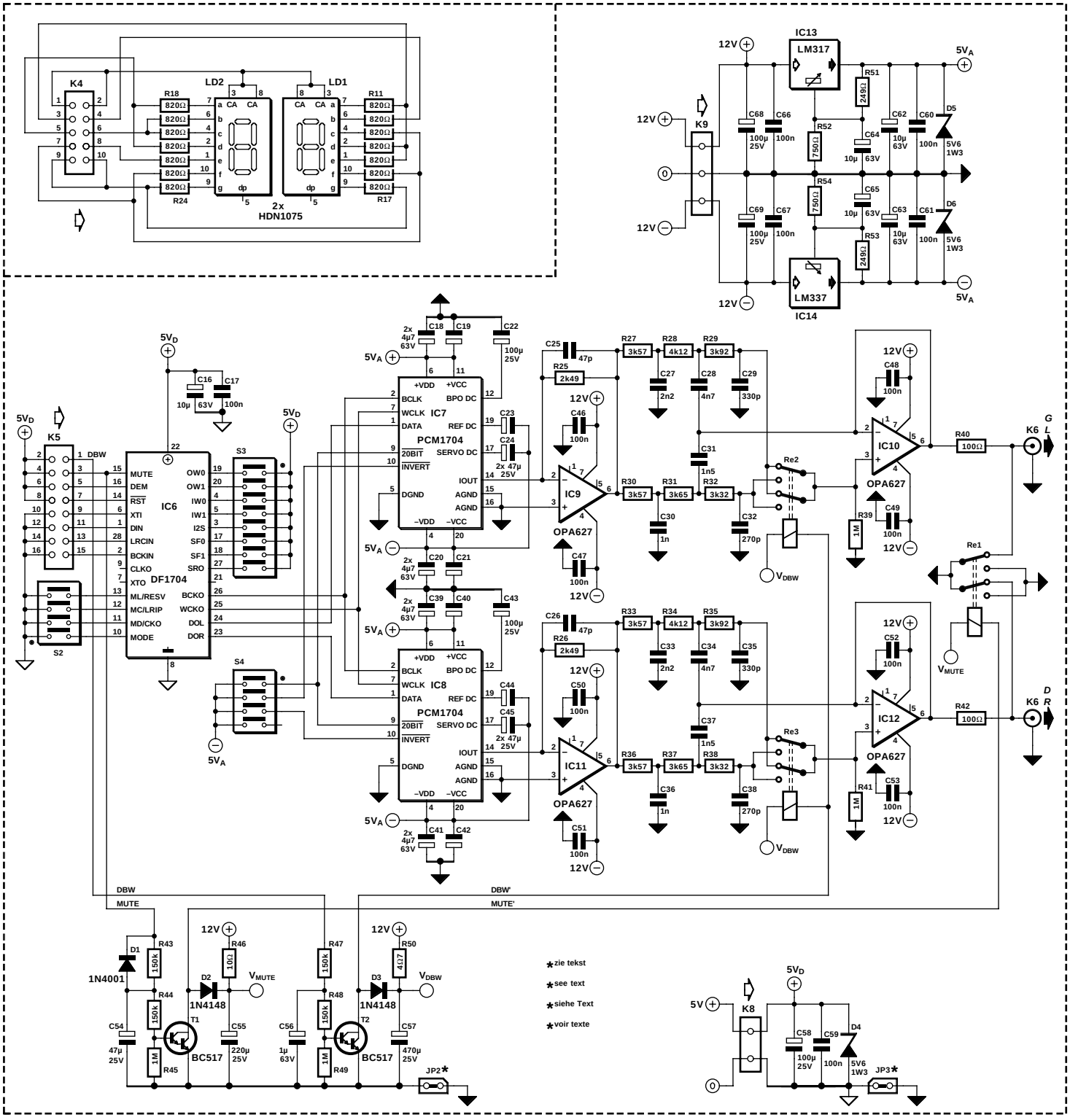


Figure 2. Circuit diagram of the Audio DAC 2000. The dashed lines show how the circuit is divided on to the four boards.

The output of the IC is applied to the input of IC_1 via potential divider R_1-R_2, whose values are chosen such that the signal across R_1 is slightly larger (0.6 V) than the standard one from the coaxial input (0.5 V). The 0.1 µF coupling capacitor prevents any d.c. on the input from reaching the receiver.

When the optical input is used, jumper JP_1 must be shorted, and the coaxial input cannot be used. It is then, however, possible to use the coaxial input as S/PDIF* output. In this case, the output impedance and signal levels are no longer standard, but the latter may be increased by slightly reducing the value of resistor R_2. In fact, the level of the input signal across R_1 may be as high as 1 $V_{p\text{-}p}$ without any problems.

The IC uses a number of frequency sensors to ensure that the PLL locks as rapidly as possible to the incoming



data flow. In the absence of an input signal, the frequency of the voltage-controlled oscillator (VCO) is low.

The digital filter on the DAC board needs four signals, all derived from the incoming S/PDIF data by the receiver chip:

SDATA contains the serial data of both channels.

PSYNC is the lefthand/righthand clock to separate the samples for the two channels. Depending on the mode of operation, it is equal to the sampling rate, F_s, or twice that rate.

Serial clock SCK is needed for clocking the individual bits and is equal to $64F_s$.

MCK, a clock equal to $256F_s$, which is needed for oversampling and interpolation. Resistors R_7–R_{10} limit any ringing caused by the capacitive loads formed by the flatcable and the digital filter.

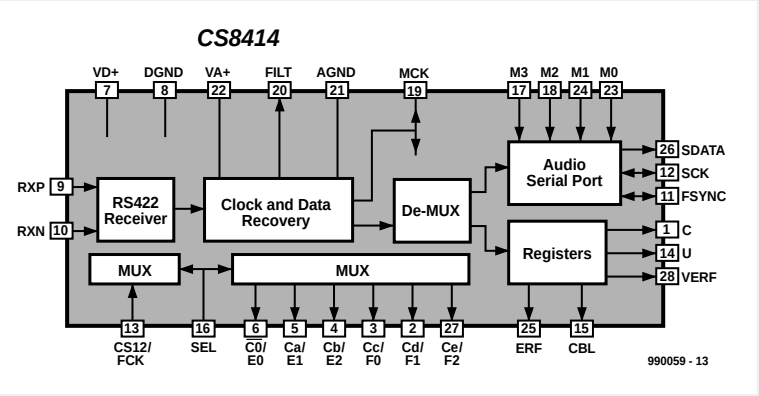
These four signals can be provided by the receiver in various standard formats: which one is determined by mode pins M_0–M_3. Details of this can be found in the CS8414 data sheets elsewhere in this issue.

The recommended mode is the I²S mode, since in this the number of bits is basically not fixed: it may be 16-bit data or 24-bit. Because of this, the preferred setting of DIP switch S_1 is $S_{1–4}$ ON ($M_1 = 1$) and the remainder OFF ($M_0 = M_2 = M_3 = 0$). Note that on the switch M_0–M_3 are mixed up but on the board the relevant names are adjacent to them (as is the level at ON or OFF).

Other formats are often just as they

96 kHz Digital Audio Receiver Type CS8414

The Type CS8414 is an upgraded version of Digital Audio Receiver Type CS8412, which has been used in several past articles published in this magazine. It is pin-compatible with its predecessor, but is available in a 28-pin SOIC (standard SMD) case only. A data sheet of it can be found elsewhere in this issue.



The most notable difference between the two devices is that the range of sampling rates available with the CS8414 has been extended to 96 kHz. The frequency indication with 400 ppm accuracy of the CS8412 has been sacrificed in favour of the 88.2 kHz and 96 kHz rates in the new device.

Clock detection is carried out by a 2nd-order loop filter via a phase-locked loop (PLL). In the CS8414 the design of the external RO-filter is slightly different than with the CS8412.

The input of the CS8414 is an RS422 receiver that can handle differential (symmetric) as well as asymmetric (single-ended) signals. In the Audio DAC2000 the input is configured for decoding single-ended signals only: input RXN is therefore bypassed to earth.

To ensure optimum operation of the phase detector in the internal PLL, the input is based on a 50 mV Schmitt trigger.

are named, for instance, 'MSB first right justified', whereby the location of the least significant bit (LSB) is fixed with respect to the L/R clock. The result of this is that some most significant bits (MSBs) may be missing. In the I^2S mode, the location of the MSB is fixed, so that, assuming there are more bits, only some LSBs may be 0. Some of the other formats are fully compatible with the Burr Brown digital filter, but that is left to the reader to sort out if he/she so wishes.

The various modes have been made presettable on purpose in view of future extension/expansion/upgrade or other applications. It also enables the receiver board to be used with other audio DACs. This board therefore has an extra +5 V terminal: the 5 V line is linked to it from the DAC board via K_3.

The manufacturers recommend resetting the IC immediately after a power up, for which purpose a circuit with four OR gates contained in IC_4 is used. This circuit cannot be provided in the GAL used, since this would require four additional inputs and four outputs.

The IC is reset when all mode pins are made high, which is the reason that the DIP switch is linked to the mode input via the OR gates. The reset proper, which is also applied to the digital filter on the DAC board via the GAL, is provided by network R_6-C_{13}.

The reference frequency of 6.144 MHz which the receiver needs to determine the sampling rate is provided by crystal oscillator IC_3. The output pin of this IC is located very close to the relevant input (FCK) of IC_1 to minimize the noise level of the clock signal. The supply lines are well decoupled by network L_3-C_{10}-C_{11}.

The supply lines to all ICs are decoupled effectively: those to the analogue and digital sections of IC_1 separately.

Channel status output C, User bit output U, and Validity and ERror Flag VERF are not used.

The Channel status BLock (CBL) start is used to demultiplex the channel status output bits (pins 2–6 and 27) by linking these to select pin SEL. When SEL is low, the Error Condition (not used) and Frequency Reporting Bits are applied to the outputs, which are then called E_0–E_2 and F_0–F_2 respectively. When SEL is high, the Channel Status is applied to the relevant outputs in the shape of some status channel bits, whereupon the outputs are called C_0 and C_a–C_e. Of these, only C_c (F_0) is used, which is channel status bit C_3. In fact, this is the emphasis bit of the channel status. It is inverted by the GAL and retained via a register output, which therefore retains the actual level and does not follow SEL. The CBL output is therefore linked to an input of the GAL to demultiplex the data.

When SEL is low, bits F_0–F_2 are recoded to six register outputs to drive a 2-digit LED display. Various segments of the display are already combined so that, without the need of multiplexing, only six outputs are needed to display the five sampling frequencies on two 7-segment displays (7 mm types). The only compromise is that any value after the decimal point (rate in kHz) is omitted.

The six outputs, +5 V, and earth, are linked to the display board via K_2, a 10-core flatcable, and a 10-pin connector. Owing to its height and location behind the front panel, a box header cannot be used on this board.

When ERF is active, all display outputs are high and only two dashes (hyphens) light. Both g-segment LEDs are permanently linked to earth via R_{17} and R_{24} respectively and therefore light permanently as long as there is supply voltage.

The SCK clock (pin 1 of the GAL) is used to clock all register outputs.

The information on the actual sampling rate is used not only for driving the frequency display, but also for switching the cut-off frequency of the analogue output filter to a higher value. That is, output DBW (double bandwidth) goes high when a rate of 88.2 kHz or 96 kHz is detected.

De-emphasis output DEEM is applied to the digital filter only. An indication of this is purposely not provided since CDs with pre-emphasis are very rare indeed. However, since the facility is there, it is used in the Audio DAC 2000 for correcting any pre-emphasis, particularly so since there is now no need for an additional *RC* network in the analogue output output filter (both channels).

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Next month's instalment describes the DAC board with particular emphasis on the digital filter and the DACs.