Built-in Adaptive Test and Calibration of DAC

Wei Jiang and Vishwani D. Agrawal
Electrical and Computer Engineering, Auburn University, Auburn, AL 36849
{weijiang,agrawvd}@auburn.edu

***Abstract*—Linearity is a critical measurement for overall performance of digital-to-analog converters (DAC) in mixed-signal system-on-chips (SoCs). Device parameters become more difficult to control due to variations from fabrication process with deep sub-micron technology. Such parameters also continue to degrade after fabrication as time elapses. Process variations of DACs are major source of non-linearity errors and will seriously keep degrading performance of SoCs. In this paper, we propose a novel digital post-fabrication variation-tolerant solution to reduce non-linearity error of on-chip high-resolution DAC by digital signal processor which is generally available on the SoC. The non-linearity error will be measured by a high-linear sigma-delta ADC and the DAC will be adaptively characterized to obtain a best matching polynomial. Then the non-linearity error can be corrected using the polynomial through a low-resolution dithering DAC. Simulation results show that a sigma-delta modulator with effective number of bits (ENOB) equivalent to a 17-bit ADC. A 6-bit dithering DAC is sufficient to calibrate a 14-bit high-resolution on-chip DAC and reduce the maximum non-linearity error from 3 LSB to 0.5 LSB. The proposed solution is technology independent and can be applied to any digitally controllable mixed-signal device for various process variation-tolerant applications.**

***Index Terms*—BIST, adaptive non-linearity compensation, self-calibration, mixed-Signal, DAC, SoC**

I. Introduction

With rapid advances in the integrated circuit (IC) technology, feature size in modern semiconductor devices has been shrinking into nanoscale (65nm and smaller) dimensions. The underlining motivations are higher performance, reduced power consumption, and lower overall system cost. However, nanoscale technologies have given rise to new problems of increased parameter variation [2], higher leakage, and time-dependent degradation, all of which are active research areas.

The above issues have influenced testing as well. Advancing the built-in self-test methods, a recent paper [4] proposes self-calibration of mixed signal components (DAC and ADC) on a system-on-chip (SoC) devices. In that particular design, nonlinearity is corrected by a built-in by self-calibration scheme before the device is put in the operational mode. Nonlinearity error was estimated as a third-degree polynomial with coefficients stored on chip for run time correction.

In nanoscale devices, parameters may change (degrade) with time and with operating conditions. One such phenomenon that has received attention is the *negative bias temperature instability* (NBTI) [7]. The parameter changes will require that any calibration and compensation procedure should be able to adopt. In this paper, we propose a polynomial error fitting type of non-linearity compensation where the degree of the polynomial is self-adaptable. Thus, the system can recalibrate the the compensation parameters either the idle times or the restart of the system.

In mixed-signal SoCs, the challenges of nanoscale technologies [2] more difficult to deal with. Digital components may require built-in redundancy and reconfiguration, but analog and mixed-signal components may be correctable through measurement, calibration and correction schemes. Typical mixed-signal components of a modern SoC include digital-to-analog (DAC) and analog-to-digital (ADC) converters. In this paper we discuss the DAC. Similar techniques can be developed for ADC [4] and are the subject of our ongoing research.

One of the most critical parameters of DAC is output linearity, which determines the input signal quality for the analog subsystem on a mixed-signal SoC and may be a decisive factor for the overall performance. With increasing demand to integrate high-resolution on-chip DAC with high-speed digital signal processor (DSP), it becomes more expensive and challenging to test and diagnose such DAC by an external automatic test equipment (ATE). Several papers [3], [5], [10] have described histogram-based test architectures for testing of DAC using low-cost low-resolution converters. Such approaches require large amount of memory to save intermediate data and reference values, especially for high-resolution DACs. Hence, an external ATE is used.

Built-in self-test (BIST) for digital devices has been widely studied for testing and guaranteeing correctness of digital components. A similar design-for-test (DFT) methodology can also be applied to test mixed-signal components [9], which can test and diagnose them using fault-free digital signal processor (DSP) circuitry often assumed available on the SoC.

A recent paper [4] presents a self-calibration BIST approach to measure and fit the on-chip DAC output non-linearity error with a third-order polynomial. When the third-order polynomial is found insufficient the device fails the test.

II. Proposed BIST Scheme for DAC

In this paper, we propose a novel DSP-based post-fabrication BIST and self-calibration scheme shown in Figure 1. The non-linearity error of DAC is estimates as a polynomial whose degree is dynamically selected. A measuring ADC (m-ADC), consisting of a sigma-delta modulator and a digital low-pass filter, and a low-resolution dithering DAC (d-DAC) are added. Testing procedure would run every time the SoC powers up, or during idle periods, or on special interrupts. The first step is the conventional BIST of all digital circuitry including the DSP. The second step is the self-test and self-calibration of mixed-signal components using the fault-free

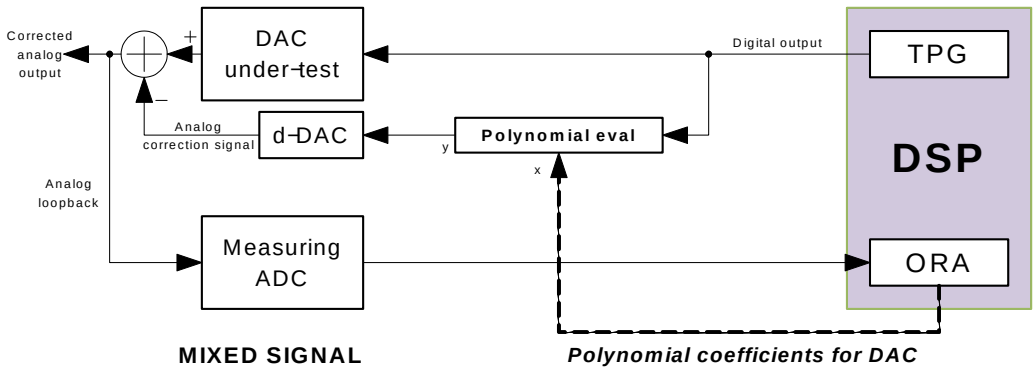

Fig. 1. Proposed BIST and self-calibration scheme of DAC.

digital components. A analog loopback is established between DAC and ADC/m-ADC and the on-chip DAC is tested with ramp codes generated as test patterns by the DSP. The m-ADC measures non-linearity errors, which are analyzed using an adaptive polynomial algorithm fitting a series of polynomials to select the minimum degree for a good fit. The coefficients of the selected polynomial are used by d-DAC to generate analog correction signals for the DAC output. The coefficients can also be considered as characteristics of the DAC and used to determine if DAC is faulty by comparing them with pre-defined reference values. After the correction, non-linearity errors are removed from DAC outputs. Meanwhile, m-ADC and d-DAC conduct a self-test procedure to diagnose any potential catastrophic fault by the same test patterns. Finally, the calibrated outputs are again examined by m-ADC using same ramp codes to verify the correctness of the DAC outputs.

After the testing phase, m-ADC and analog loopback are disabled while d-DAC continues to generate correction signal for each input code to maintain linear outputs from the on-chip DAC during the normal operation. The calibrated DAC can also be used in an extended test mode to generate a highly linear analog test signal to diagnose other mixed-signal devices like on-chip ADC and mixer.

The proposed self-calibration technique runs before normal operation every time the system starts up. In case the characteristics of the on-chip DAC vary as a function of time and render the previous calibration inadequate, the adaptive degree of polynomial algorithm can be reapplied. This would typically require an interrupt or restart of the system. Alternatively, recalibration can be automatically scheduled during idle periods.

Similar techniques may be developed for various mixed-signal devices with digital controls.

III. Adaptive Self-Calibration Test of DAC

We assume that the DSP and other digital circuitry has been tested and is fault-free. Before actual testing of on-chip DAC under test, a loopback as shown in Figure 1 is established. The DSP sends a series of random numbers through its output port and checks the input port for response. This step will detect any interconnect faults at DSP input/output.

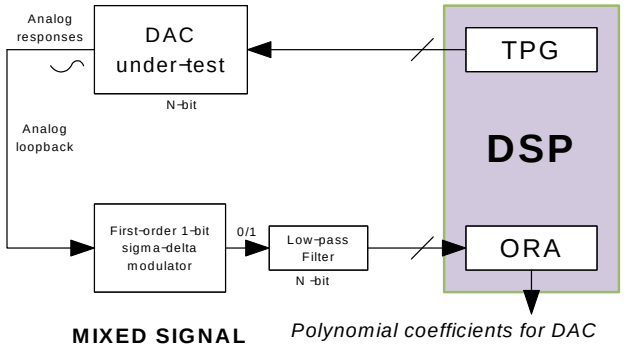

Fig. 2. Testing and characterization of DAC.

A. Test of Measuring ADC

Next, an analog loopback, shown in 1, between DAC output and ADC/m-ADC input port is established, as is also shown in Figure 2, to transmit DAC outputs back to ADC/m-ADC for measurement. Now, a series of consecutive ramp codes are generated and sent to DAC as both on-chip ADC and m-ADC measure DAC outputs. We chose a first-order 1-bit sigma-delta modulator based ADC as m-ADC because of its flexibility and highly linear outputs. A sigma-delta modulator can have very high resolution and linearity with high oversampling ratio (OSR). A suitable OSR can be selected to obtain the effective number of bits (ENOB) for various requirements and applications, of course, at the cost of sampling time. The digital outputs from two ADCs are collected and compared against digital test codes by DSP. Because among DAC, ADC and m-ADC any could be faulty, any serious inconsistency or significant difference among these three digital numbers would indicate fault in any of the components, barring some highly improbable cases of identical errors in all three. On a mismatch, the chip is marked as faulty. A predefined fault-tolerance factor (α) is specified to determine the inconsistency. The factor α also defines the maximum correction capability of the proposed self-calibration test scheme for DAC.

B. Best Matching Polynomial Fitting Algorithm

If the inconsistency among test code and ADC responses is smaller than the fault-tolerance factor, the on-chip DAC-

under-test (DUT) is considered fixable. Such inconsistencies between test code (k) and m-DAC response ($\hat{k}$) is actually the digitized and combined integral non-linearity (INL) errors of both DUT and m-DAC.

$$INL_k = \frac{v_k - v_0}{LSB} - k = \hat{k} - k \tag{1}$$

where v_k is N-bit DUT output and the least significant bit (LSB) is the minimal unit voltage value for the DUT. For example, given reference voltage V_{ref}, LSB of 14-bit DAC is

$$V_{LSB} = \frac{V_{ref}}{2^{14}} \tag{2}$$

Because m-ADC is based on sigma-delta modulator and has high linearity with large OSR, the INL error of m-ADC can be ignored and thus $\hat{k} - k$ can be considered as the INL error of sole DUT for given code k. An adaptive polynomial fitting algorithm is employed to fit the non-linearity errors (INL_k for each code k) of DUT to obtain the best-matching minimum degree polynomial for non-linearity characteristics of DUT outputs.

Consider an order-p fitting polynomial:

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 + \cdots + (p-1) \cdot x^{p-1} + p \cdot x^p \tag{3}$$

where b_0, b_1, b_2, ..., b_{p-1}, b_p are polynomial coefficients. Best-matching polynomial gives minimum mean-square error. To obtain the best-matching polynomial, we apply fitting to data for successively increasing degrees of polynomials. Although a higher order polynomial may have better fitting and lower error, it takes more time to calculate the coefficients, will require more memory to store and will need more complex digital circuitry for calculation. Thus, a higher order polynomial will require more gates and delay than a lower order one. Too high an order also brings metastability to system and negatively affects product reliability. Therefore, make trade-off between fitting accuracy and fitting time/hardware overhead. To make at-speed DAC correction possible, the maximum path delay of digital polynomial calculation circuitry must not exceed DAC conversion delay. So for given process and DAC design, maximum available order of polynomial shall be specified as well as fault-tolerance factor.

Accuracy of matching polynomial can be determined as the root mean square (RMS) error between measured INL errors and the polynomial values:

$$\Delta v_k = v_k - (v_0 + k \cdot LSB) \tag{4}$$

$$y_{rms} = \sqrt{\frac{1}{2^N} \sum_{k=0}^{2^N-1} (\Delta v_k - y(k))^2} \tag{5}$$

for N-bit DAC-under-test. In the proposed BIST procedure, a low-order polynomial fitting algorithm is used at first and then high-order ones, until the RMS errors drops below a specified threshold. For each polynomial, two steps are executed: coefficients extraction and polynomial evaluation. In coefficients extraction step, a series of consecutive ramp codes are generated as test patterns to DUT, then the sigma-delta modulator will measure DUT responses and DSP will collect both test patterns and DUT responses to calculate current polynomial coefficients for INL errors. In polynomial evaluation step, another series of consecutive ramp codes will be generated to evaluate the polynomial with calculated coefficients and obtain its RMS value for ramp codes. Thus the fitting accuracy of current polynomial to INL errors of DUT outputs can be defined as the RMS value. In real implementation, polynomial evaluation step of previous polynomial may be combined with coefficients extraction of next polynomial because these two steps will be using different hardware at the same time with possible race issue. The coefficients may also indicate if DUT is correctable by comparing to pre-defined values.

1) Zero-order polynomial: First of all, Zero-order polynomial will be tried, which is just mean value of all non-linearity errors of N-bit DAC in fact.

$$y = b_0 \tag{6}$$

$$b_0 = \frac{1}{2^N} \int_{-2^{N-1}}^{2^{N-1}} v_k dk = \frac{1}{n} \int_{-n/2}^{n/2} v_k dk \tag{7}$$

where $n = 2^N$ is the total number of input codes for N-bit DAC-under-test.

This polynomial is actually a constant value fitting for every input code. It has the least hardware overhead and delay for polynomial evaluation but may have the most fitting error.

2) First-order polynomial: The responses for input ramp codes is divided into two equal-length sections and two sums of these two sections can be obtained by

$$S_0 = \int_{-2^{N-1}}^{0} v_k dk = \int_{-n/2}^{0} v_k dk = \frac{n}{2} b_0 - \frac{n^2}{8} b_1 \tag{8}$$

$$S_1 = \int_{0}^{2^{N-1}} v_k dk = \int_{0}^{n/2} v_k dk = \frac{n}{2} b_0 + \frac{n^2}{8} b_1 \tag{9}$$

Then we define two syndromes for the first-order polynomial

$$B_0 = S_1 + S_0 = n b_0 \tag{10}$$

$$B_1 = S_1 - S_0 = \frac{n^2}{4} b_1 \tag{11}$$

Therefore the first-order polynomial and two coefficients can be obtained by

$$y = b_0 + b_1 \cdot x \tag{12}$$

$$b_0 = \frac{1}{n} B_0 \tag{13}$$

$$b_1 = \frac{4}{n^2} B_1 \tag{14}$$

3) Second-order polynomial: The responses is divided into three equal-length sections for second-order polynomial. Each of three sections are accumulated up to obtain three sums

$$S_0 = \int_{-n/2}^{-n/6} v_k dk = \frac{n}{3} b_0 - \frac{n^2}{9} b_1 + \frac{13n^3}{324} b_2 \tag{15}$$

$$S_1 = \int_{-n/6}^{n/6} v_k dk = \frac{n}{3} b_0 + \frac{n^3}{324} b_2 \tag{16}$$

$$S_2 = \int_{n/6}^{n/2} v_k dk = \frac{n}{3} b_0 + \frac{n^2}{9} b_1 + \frac{13n^3}{324} b_2 \tag{17}$$

Then we define three syndromes for the second-order polynomial

$$B_0 = S_2 - 26S_1 + S_0 = -8nb_0 \tag{18}$$

$$B_1 = S_2 - S_0 = \frac{2n^2}{9}b_1 \tag{19}$$

$$B_2 = S_2 - 2S_1 + S_0 = \frac{2n^3}{27}b_2 \tag{20}$$

Therefore the second-order polynomial and three coefficients can be obtained by

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 \tag{21}$$

$$b_0 = -\frac{1}{8n}B_0 \tag{22}$$

$$b_1 = \frac{9}{2n^2}B_1 \tag{23}$$

$$b_2 = \frac{27}{2n^3}B_2 \tag{24}$$

4) Third-order polynomial: The response is divided into four equal-length sections for third-order polynomial, as discussed in [8], [6]. The sum of each section is

$$S_0 = \int_{-n/2}^{-n/4} v_k dk = \frac{n}{4}b_0 - \frac{3n^2}{32}b_1 + \frac{7n^3}{192}b_2 - \frac{15n^4}{1024}b_3 \tag{25}$$

$$S_1 = \int_{-n/4}^{0} v_k dk = \frac{n}{4}b_0 - \frac{n^2}{32}b_1 + \frac{n^3}{192}b_2 - \frac{n^4}{1024}b_3 \tag{26}$$

$$S_2 = \int_{0}^{n/4} v_k dk = \frac{n}{4}b_0 + \frac{n^2}{32}b_1 + \frac{n^3}{192}b_2 + \frac{n^4}{1024}b_3 \tag{27}$$

$$S_2 = \int_{n/4}^{n/2} v_k dk = \frac{n}{4}b_0 + \frac{3n^2}{32}b_1 + \frac{7n^3}{192}b_2 + \frac{15n^4}{1024}b_3 \tag{28}$$

Then we can define four syndromes as below (also same as in [8])

$$B_0 = S_3 + S_2 + S_1 + S_0 = nb_0 + \frac{n^3}{12}b_2 \tag{29}$$

$$B_1 = S_3 + S_2 - S_1 - S_0 = \frac{n^2}{4}b_1 + \frac{n^4}{32}b_3 \tag{30}$$

$$B_2 = S_3 - S_2 - S_1 + S_0 = \frac{n^3}{16}b_2 \tag{31}$$

$$B_3 = S_3 - 3S_2 + 3S_1 - S_0 = \frac{3n^4}{128}b_3 \tag{32}$$

Therefor the third-order polynomial and four coefficients can be obtained by

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 + b_3 \cdot x^3 \tag{33}$$

$$b_0 = \frac{1}{n}(B_0 - \frac{4}{3}B_2) \tag{34}$$

$$b_1 = \frac{4}{n^2}(B_1 - \frac{4}{3}B_3) \tag{35}$$

$$b_2 = \frac{16}{n^3}B_2 \tag{36}$$

$$b_3 = \frac{128}{3n^4}B_3 \tag{37}$$

5) N^{th}-order polynomial: Repeat the procedure above and we can obtain $N+1$ syndromes by dividing output responses into $N+1$ equal-length sections. And then $N+1$ coefficients for N^{th}-order polynomial can be calculated from these syndromes. In theory high-order polynomial may result in better fitting results. However, higher-order polynomial may have much greater penalty upon hardware overhead and delay, especially for high-order multiply computation. We observed that N=3 is sufficient in most cases so there is no need to explore higher-order polynomial fitting equations.

C. DUT Calibration by Dithering DAC

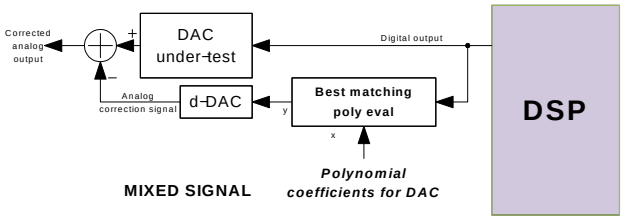

Fig. 3. DUT calibration by dithering DAC (d-DAC) and best matching polynomial.

After the order and polynomials of best matching fitting polynomial are determined, they will be compared to predefined values. INL errors of DUT is correctable only if the polynomial coefficients are within the specified range; otherwise DUT will be marked as faulty by DSP. For correctable DUT, the fitting polynomial and its coefficients will be saved into memory cells and retrieved by polynomial evaluation circuit to generate correcting codes.

A low-resolution low-cost dithering DAC (d-DAC) will convert such correcting codes into correcting analog signals to remove non-linearity errors from DUT output, as shown in Figure. 3. Low-resolution d-DAC is simple to design and manufacture cost if low while converting speed is high. Higher-resolution d-DAC may generate more accurate correcting signals if total delay of polynomial evaluation circuit and d-DAC is less than converting time of DUT and such hardware overhead is acceptable. The reference voltage of d-DAC is defined by the resolution of DUT and fault-tolerant factor.

$$\begin{aligned} V_{ref,d-DAC} &= \pm\frac{2^\alpha}{2} \cdot LSB \\ &= \pm\frac{2^\alpha}{2} \cdot \frac{2V_{ref}}{2^N} = \pm 2^{\alpha-N} \cdot V_{ref} \end{aligned} \tag{38}$$

$$\begin{aligned} LSB_{d-DAC} &= \frac{2V_{ref,d-DAC}}{2^{N'}} \\ &= 2^{1+\alpha-N-N'} \cdot V_{ref} \end{aligned} \tag{39}$$

for N-bit DAC-under-test with reference voltage V_{ref},N'-bit d-DAC, and fault-tolerant factor α.

In most case, it is sufficient to choose α equal to 3 and to use 6-bit d-DAC for DUT correction. Thus for given 14-bit

DAC-under-test, the reference voltage and LSB of d-DAC are

$$V_{ref,d-DAC} = \pm\frac{V_{ref}}{2^{11}} \tag{40}$$

$$LSB_{d-DAC} = \frac{V_{ref}}{2^{16}} \tag{41}$$

D. Resolution of Measuring ADC

A sigma-delta modulator-based measuring ADC (m-ADC) is employed to measure DUT outputs, as shown in Figure. 2. This m-ADC consists of a first-order 1-bit sigma-delta modulator and a digital low-pass filter (LPF). The measurements will compare to corresponding ramp test codes to obtain nonlinearity errors for polynomial fitting. So required minimal resolution of the sigma-delta modulator depends on the resolution of DUT and d-DAC as well as fault-tolerant factor.

The minimal effective number of bits (ENOB) of sigma-delta modulator can be obtained by

$$\begin{aligned}\hat{N} &= \log_2 \frac{V_{ref}}{LSB_{d-DAC}} \\ &= N + N' - \alpha - 1\end{aligned} \tag{42}$$

And signal-to-noise ratio (SNR) of m-ADC can be estimated as

$$\begin{aligned}SNR_{dB} &= 10\log\left(\frac{RMS_{signal}}{RMS_{noise}}\right) \\ &= 6.02\hat{N} + 1.76\end{aligned} \tag{43}$$

The relationship between SNR and oversampling ratio (OSR) of first-order sigma-delta modulator is [1]

$$OSR = \frac{f_s/2}{f_0} = \frac{f_s}{2f_0} \tag{44}$$

$$SNR = \frac{3}{8\pi^2}OSR^3 \tag{45}$$

$$\begin{aligned}SNR_{dB} &= 10\log_{10} SNR \\ &= 30\log_{10} OSR - 14.2\end{aligned} \tag{46}$$

where f_0 is maximum frequency of measured analog signals and f_s is sampling clock frequency of sigma-delta modulator.

Thus OSR of sigma-delta modulator can also be determined from (42) (43) and (46)

$$OSR = 10^{\frac{SNR_{dB}+14.2}{30}} \tag{47}$$

$$= 10^{\frac{6.02N+N'-\alpha+10}{30}} \tag{48}$$

For a given 14-bit on-chip DAC and 6-bit d-DAC, assuming fault-tolerant factor is 3, minimal OSR can be calculated using (48)

$$OSR = 10^{\frac{6.0214+6-3+10}{30}} = 5555$$

IV. Simulation Results

We use Matlab to simulate the proposed adaptive self-calibration approach. INL errors of a 14-bit DAC-under-test is shown in Figure.4 and we try various order polynomials to fit the INL errors, as shown in Table I,II,III and IV.

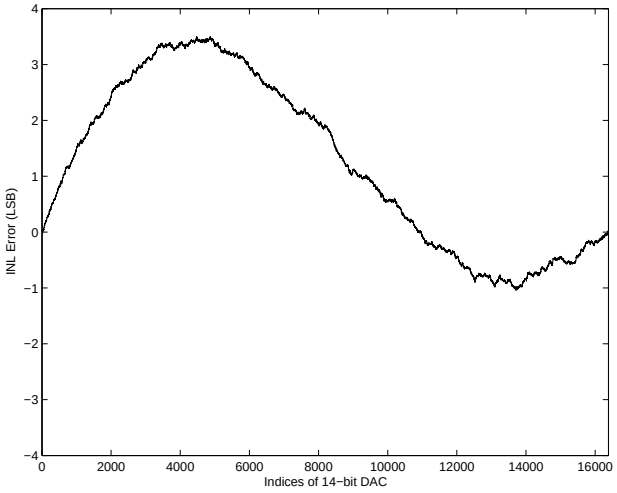

Fig. 4. INL errors of a 14-bit on-chip DAC-under-test.

TABLE I
ZERO-ORDER POLYNOMIAL FIT FOR *INL* OF FIGURE 4.

Sums	Syndromes	Coefficients
$S_0 = 1.9901 \times 10^4$	N/A	$b_0 = 1.2147$

TABLE II
FIRST-ORDER POLYNOMIAL FIT FOR *INL* OF FIGURE 4.

Sums	Syndromes	Coefficients
$S_0 = 2.054 \times 10^4$	$B_0 = 1.9901 \times 10^4$	$b_0 = 1.2147$
$S_1 = -645.4238$	$B_1 = -2.1192 \times 10^4$	$b_1 = -3.1578 \times 10^{-4}$

TABLE III
SECOND-ORDER POLYNOMIAL FIT FOR *INL* OF FIGURE 4.

Sums	Syndromes	Coefficients
$S_0 = 1.3676 \times 10^4$	$B_0 = -2.2853 \times 10^5$	$b_0 = 1.7435$
$S_1 = 9.2011 \times 10^3$	$B_1 = -1.6649 \times 10^4$	$b_1 = -2.7910 \times 10^{-4}$
$S_2 = -2.9731 \times 10^3$	$B_2 = -7.6993 \times 10^3$	$b_2 = -2.3633 \times 10^{-8}$

TABLE IV
THIRD-ORDER POLYNOMIAL FIT FOR *INL* OF FIGURE 4.

Sums	Syndromes	Coefficients
$S_0 = 9.0857 \times 10^3$	$B_0 = 1.9901 \times 10^4$	$b_0 = 1.7672$
$S_1 = 1.1461 \times 10^4$	$B_1 = -2.1192 \times 10^4$	$b_1 = -6.5577 \times 10^{-4}$
$S_2 = 1.8845 \times 10^3$	$B_2 = -6.7893 \times 10^3$	$b_2 = -2.4699 \times 10^{-8}$
$S_3 = -2.5300 \times 10^3$	$B_3 = 1.7112 \times 10^3$	$b_3 = 1.0132 \times 10^{-11}$

Figure 5 compares fitting curves of those three polynomials and RMS errors of each order polynomials can also be calculated: 1.5188 for zero-order, 0.9643 for first-order, 0.8407 for second-order, and 0.0907 for third-order. It can be observed that third-order polynomial is the best match polynomial to fitting on-chip DAC in this case. It is possible that fourth-order polynomial may have better matching results but due to significant increase on hardware overhead and delay, fourth-order polynomial is not suitable in this case.

The d-DAC correcting outputs is shown in Figure 6 and final corrected INL error is shown in Figure 7. INL error is significantly reduced by our adaptive self-calibration technique, from $\pm 4LSB$ down to only $\pm 0.4LSB$.

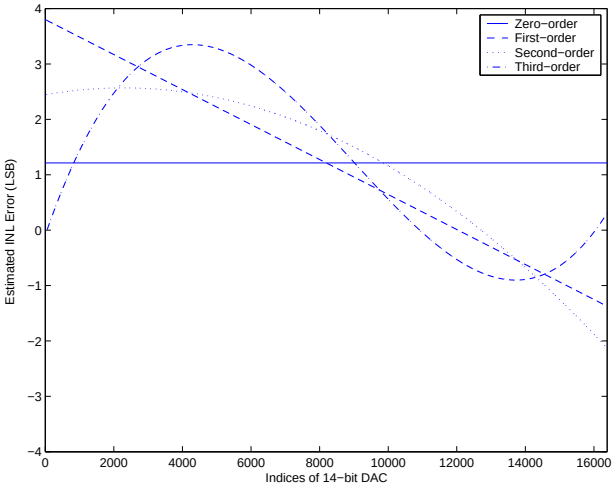

Fig. 5. Fitting results from different order polynomials.

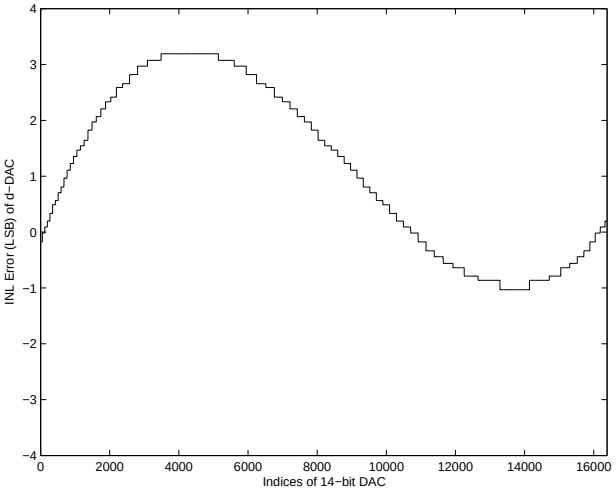

Fig. 6. Correcting signals converted by a 6-bit d-DAC using third-order fitting polynomial.

V. Conclusion

A DSP-based adaptive self-calibration BIST scheme is proposed in this paper to test and diagnose on-chip DAC with best-matching polynomial fitting algorithm. A sigma-delta modulator-based measuring ADC is used to measure on-chip DAC outputs. The native non-linearity error of sigma-delta modulator are ignored by selecting sufficient oversampling ratio (OSR). The order and coefficients of best-matching polynomial can be calculated to retrieve non-linearity errors as output correcting code. A low-resolution dither DAC is employed to convert digital correcting code to analog correcting signals for DAC output. This BIST scheme will be executed every time when SoC starts up to get up-to-date characteristics of on-chip DAC. The adaptive self-calibration approach has been verified by simulation and shows significant improvements of linearity to noisy on-chip DAC outputs.

Acknowledgment: This research was supported in part by the National Science Foundation Grant CNS-0708962.

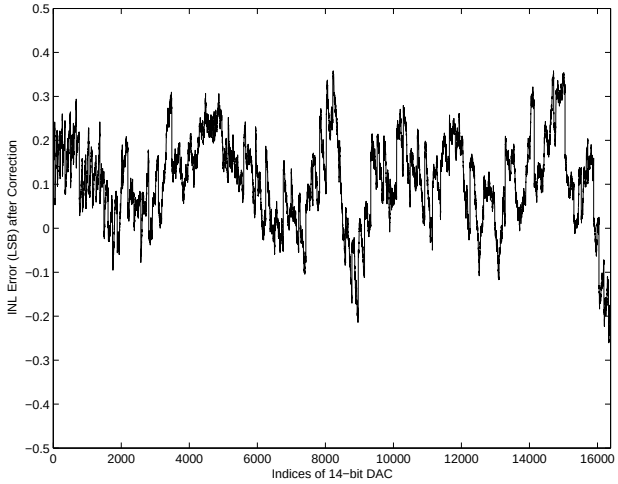

Fig. 7. INL errors of 14-bit on-chip DAC corrected usng 6-bit d-DAC.

References

[1] F. F. Dai and C. E. Stroud, *Analog and Mixed-Signal Test Architectures*, chapter 15. Morgan Kaufmann, 2008.

[2] http://www.itrs.net/Links/2007ITRS/Home2007.htm, "International technology roadmap for semiconductors," 2007.

[3] H. Jiang, D. Chen, and R. L. Geiger, "Dither Incorporated Deterministic Dynamic Element Matching for High Resolution ADC Test Using Extremely Low Resolution DACs," in *IEEE International Symp. Circuits and Systems*, May 2005, pp. 4285–4288.

[4] W. Jiang and V. D. Agrawal, "Built-in Self-Calibration of On-Chip DAC and ADC," in *IEEE Proc. International Test Conference*, Oct. 2008. Paper No. 32.2.

[5] K.-J. Lee, S.-J. Chang, and R.-S.Tzeng, "A Sigma-Delta Modulation Based BIST Scheme for A/D Converters," in *Proc. 12th Asian Test Symp.*, 2003, pp. 124–127.

[6] A. Roy, S. Sunter, A. Fudoli, and D. Appelo, "High Accuracy Stimulus Generation for A/D Converter BIST," in *IEEE Proc. International Test Conference*, 2002, pp. 1031–1039.

[7] D. K. Schroder, "Negative Bias Temperature Instability: What Do We Understand?," *Microeletronics Reliability*, vol. 47, pp. 841–852, June 2007.

[8] S. Sunter and N. Nagi, "A Simplified Polynomial Fitting Algorithm for DAC and ADC BIST," in *IEEE Proc. International Test Conference*, 1997, pp. 389–395.

[9] B. Vinnakota, editor, *Analog and Mixed-Signal Test*. Prentice-Hall PTR, 1998.

[10] Y.-S. Wang, J.-X. Wang, F.-C. Lai, and Y.-Z. Ye, "A Low-Cost BIST Scheme for ADC Testing," in *Proc. 6th International Conf. on ASIC*, volume 2, Oct. 2005, pp. 694–698.