Sample-and-Hold Amplifiers

INTRODUCTION AND HISTORICAL PERSPECTIVE

The *sample-and-hold amplifier*, or SHA, is a critical part of most data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

When the SHA is used with an ADC (either externally or internally), the SHA performance is critical to the overall dynamic performance of the combination, and plays a major role in determining the SFDR, SNR, etc., of the system.

Although today the SHA function has become an integral part of the *sampling* ADC, understanding the fundamental concepts governing its operation is essential to understanding ADC dynamic performance.

When the sample-and-hold is in the sample (or track) mode, the output follows the input with only a small voltage offset. There do exist SHAs where the output during the *sample* mode does not follow the input accurately, and the output is only accurate during the *hold* period (such as the AD684, AD781, and AD783). These will not be considered here. Strictly speaking, a sample-and-hold with good tracking performance should be referred to as a *track-and-hold* circuit, but in practice the terms are used interchangeably.

The most common application of a SHA is to maintain the input to an ADC at a constant value during conversion. With many, but not all, types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted—this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion.

From a historial perspective, it is interesting that the ADC described by A. H. Reeves in his famous PCM patent of 1939 (Reference 1) was a 5-bit 6-kSPS counting ADC where the analog input signal drove a vacuum tube pulse-width-modulator (PWM) directly—the sampling function was incorporated into the PWM. Subsequent work on PCM at Bell Labs led to the use of electron-beam encoder tubes and successive approximation ADCs; and Reference 2 (1948) describes a companion 50-kSPS vacuum tube sample-and-hold circuit based on a pulse transformer drive circuit.

There was increased interest in sample-and-hold circuits for ADCs during the period of the late 1950s and early 1960s as transistors replaced vacuum tubes. One of the first analytical treatments of the errors produced by a solid-state sample-and-hold was published in 1964 by Gray and Kitsopolos of Bell Labs (Reference 3). Edson and Henning of Bell Labs describe the results of experimental work done on a 224-Mbps PCM system, including the 9-bit ADC and a companion 12-MSPS sample-and-hold. References 4, 5 , and 6 are representative of work done on sample-and-hold circuits during the 1960s and early 1970s.

In 1969, the newly acquired Pastoriza division of Analog Devices offered one of the first commercial sample-and-holds, the SHA1 and SHA2. The circuits were offered on PC boards, and the SHA1 had an acquisition time of 2 µs to 0.01%, dissipated 0.9 W, and cost approximately $225. The faster SHA2 had an acquisition time of 200 ns to 0.01%, dissipated 1.7 W, and cost approximately $400. They were designed to operate with 12-bit successive approximation ADCs also offered on PC boards.

Modular and hybrid technology quickly made the PC board sample-and-holds obsolete, and the demand for sample-and-holds increased as IC ADCs, such as the industry-standard AD574, came on the market. In the 1970s and into the 1980s, it was quite common for system designers to purchase separate sample-and-holds to drive such ADCs, because process technology did not allow integrating them together onto the same chip. IC SHAs such as the AD582 (4-µs acquisition time to 0.01%), AD583 (6-µs acquisition time to 0.01%), and the AD585 (3-µs acquisition time to 14-bit accuracy) served the lower speed markets of the 1970s and 1980s.

Hybrid SHAs such as the HTS-0025 (25-ns acquisition time to 0.1%), HTC-0300 (200-ns acquisition time to 0.01%), and the AD386 (25-µs acquisition time to 16-bits) served the high-speed, high-end markets. By 1995, Analog Devices offered approximately 20 sample-and-hold products for various applications, including the following high-speed ICs: AD9100/AD9101 (10-ns acquisition time to 0.01%), AD684 (quad 1-µs acquisition time to 0.01%) and the AD783 (250-ns acquisition time to 0.01%).

However, ADC technology was rapidly expanding during the same period, and many ADCs were being offered with internal SHAs (i.e., *sampling* ADCs). This made them easier to specify and certainly easier to use. Integration of the SHA function was made possible by new process developments including high-speed complementary bipolar processes and advanced CMOS processes. In fact, the proliferation and popularity of sampling ADCs has been so great that today (2003), one rarely has the need for a separate SHA.

The advantage of a sampling ADC, apart from the obvious ones of smaller size, lower cost, and fewer external components, is that the overall dc and ac performance is fully specified, and the designer need not spend time ensuring that there are no specification, interface, or timing issues involved in combining a discrete ADC and a discrete SHA. This is especially important when one considers dynamic specifications such as SFDR and SNR.

Although the largest applications of SHAs are with ADCs, they are also occasionally used in DAC deglitchers, peak detectors, analog delay circuits, simultaneous sampling systems, and data distribution systems.

BASIC SHA OPERATION

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all SHAs as shown in the typical configuration of Figure 1.

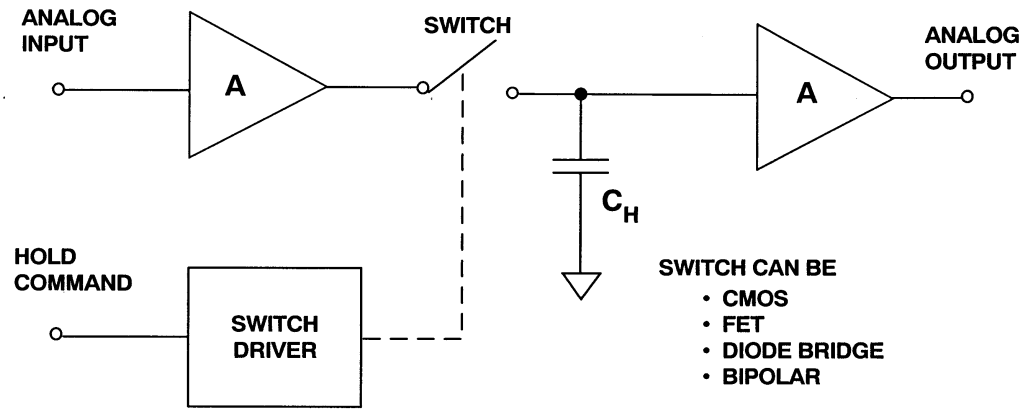


Figure 1: Basic Sample-and-Hold Circuit

The energy-storage device, the heart of the SHA, is a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the *track* mode, the voltage on the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the SHA is alternately switched between track and hold.

There are four groups of specifications that describe basic SHA operation: track mode, track-to-hold transition, hold mode, hold-to-track transition. These specifications are summarized in Figure 2, and some of the SHA error sources are shown graphically in Figure 3. Because there are both dc and ac performance implications for each of the four modes, properly specifying a SHA and understanding its operation in a system is a complex matter.

SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
STATIC: ◆ Offset ◆ Gain Error ◆ Nonlinearity	STATIC: ◆ Pedestal ◆ Pedestal Nonlinearity	STATIC: ◆ Droop ◆ Dielectric ◆ Absorption	
DYNAMIC: ◆ Settling Time ◆ Bandwidth ◆ Slew Rate ◆ Distortion ◆ Noise	DYNAMIC: ◆ Aperture Delay Time ◆ Aperture Jitter ◆ Switching Transient ◆ Settling Time	DYNAMIC: ◆ Feedthrough ◆ Distortion ◆ Noise	DYNAMIC: ◆ Acquisition Time ◆ Switching Transient

Figure 2: Sample-and-Hold Specifications

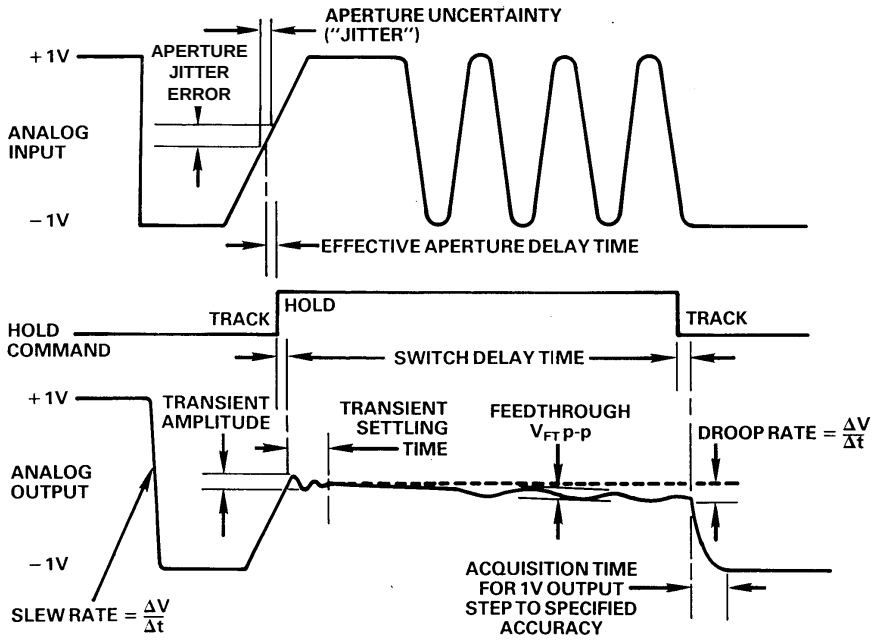


Figure 3: Some Sources of Sample-and-Hold Errors

TRACK MODE SPECIFICATIONS

Since a SHA in the sample (or track) mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. (SHAs which have degraded performance in the track mode are generally only specified in the hold mode.) The principle track mode specifications are *offset*, *gain*, *nonlinearity*, *bandwidth*, *slew rate*, *settling time*, *distortion*, and *noise*. However, distortion and noise in the track mode are often of less interest than in the hold mode.

TRACK-TO-HOLD MODE SPECIFICATIONS

When the SHA switches from track to hold, there is generally a small amount of charge dumped on the hold capacitor because of non-ideal switches. This results in a hold mode dc offset voltage which is called *pedestal* error as shown in Figure 4. If the SHA is driving an ADC, the pedestal error appears as a dc offset voltage which may be removed by performing a system calibration. If the pedestal error is a function of input signal level, the resulting nonlinearity contributes to hold-mode distortion.

Pedestal errors may be reduced by increasing the value of the hold capacitor with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

Switching from track to hold produces a transient, and the time required for the SHA output to settle to within a specified error band is called *hold mode settling time*. Occasionally, the peak amplitude of the switching transient is also specified.

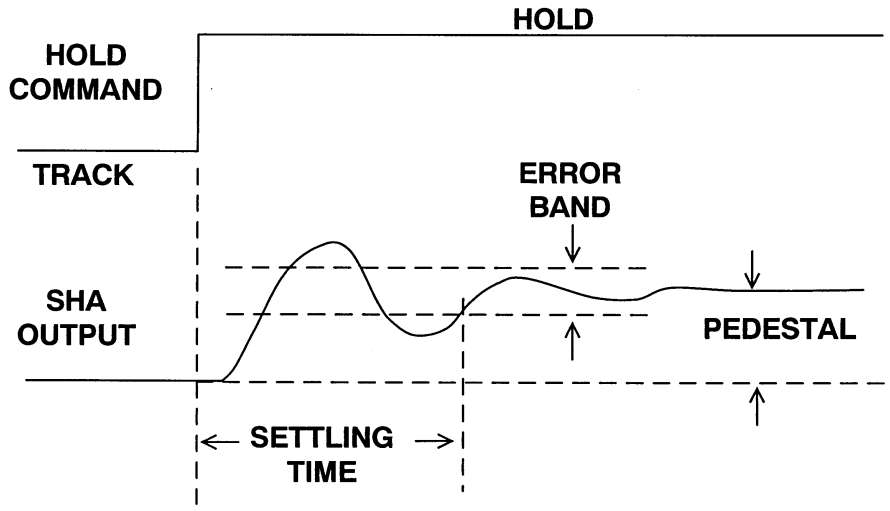


Figure 4: Track-to-Hold Mode Pedestal, Transient, and Settling Time Errors

Perhaps the most misunderstood and misused SHA specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called *aperture time*. The various quantities associated with the internal SHA timing are shown in the Figure 5.

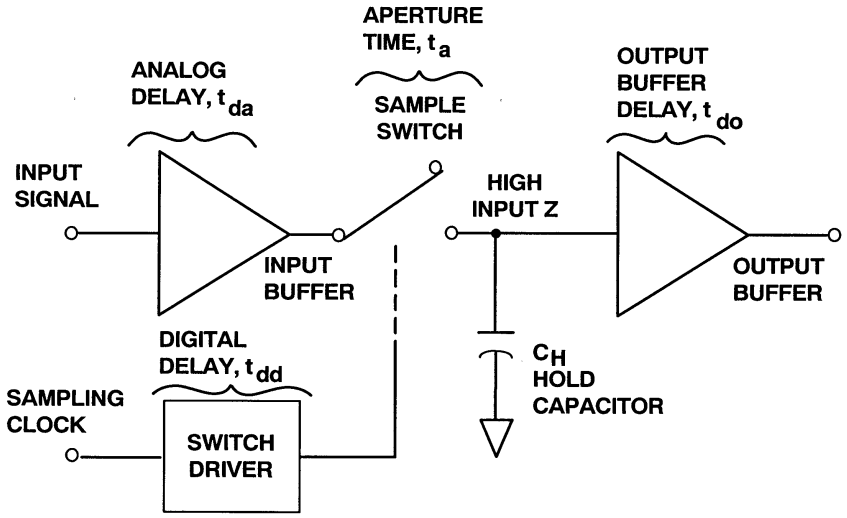


Figure 5: SHA Circuit Showing Internal Timing

The actual value of the voltage that is held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself. Figure 6 shows what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold pedestal and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch as shown in Figure 6. The first-order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (t_a).

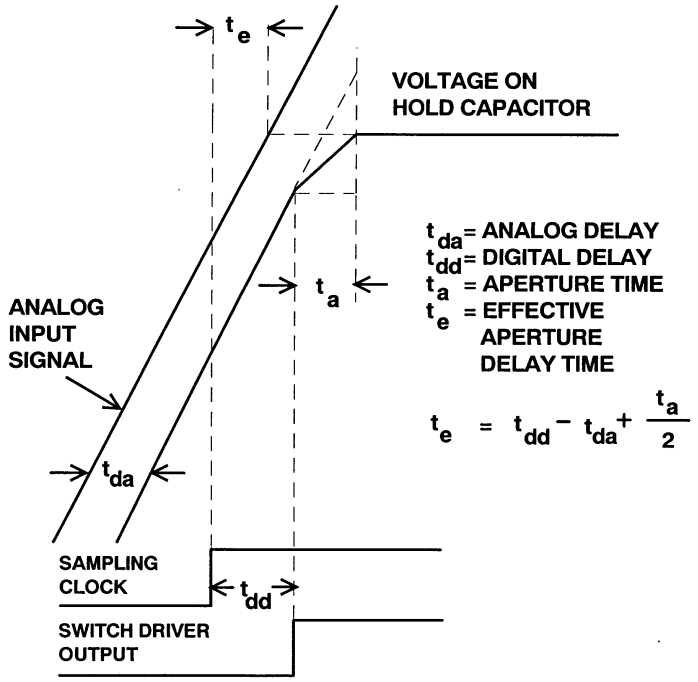


Figure 6: SHA Waveforms

The model shows that the finite time required for the switch to open (t_a) is equivalent to introducing a small delay in the sampling clock driving the SHA. This delay is constant and may either be positive or negative. It is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, (t_e) and is defined as the time difference between the analog propagation delay of the front-end buffer (t_{da}) and the switch digital delay (t_{dd}) plus one-half the aperture time ($t_a/2$). The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time ($t_a/2$) and the switch digital delay (t_{dd}) is less than the propagation delay through the input buffer (t_{da}). The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sinewave signal to the SHA and adjusting the synchronous sampling clock delay such that the output of the SHA is zero during the hold time. The relative delay between the input sampling clock edge and the actual zero-crossing of the input sinewave is the aperture delay time as shown in Figure 7.

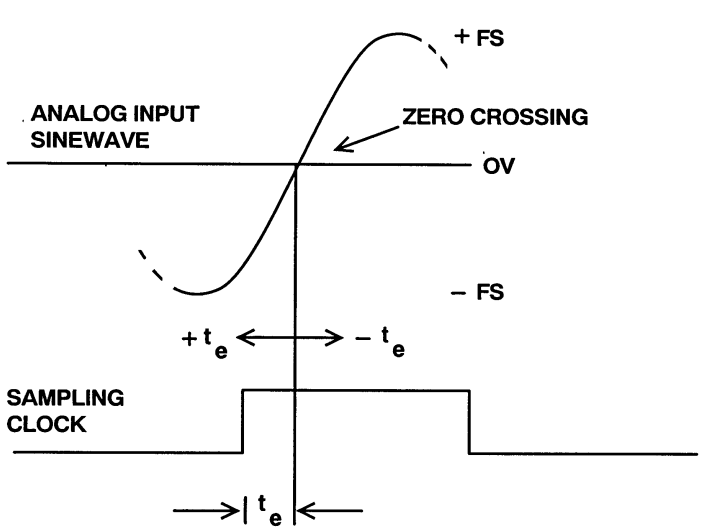


Figure 7: Effective Aperture Delay Time

Aperture delay produces no errors, but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). If there is sample-to-sample variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 8. This sample-to-sample variation in the instant the switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in picoseconds rms. The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input dv/dt increases.

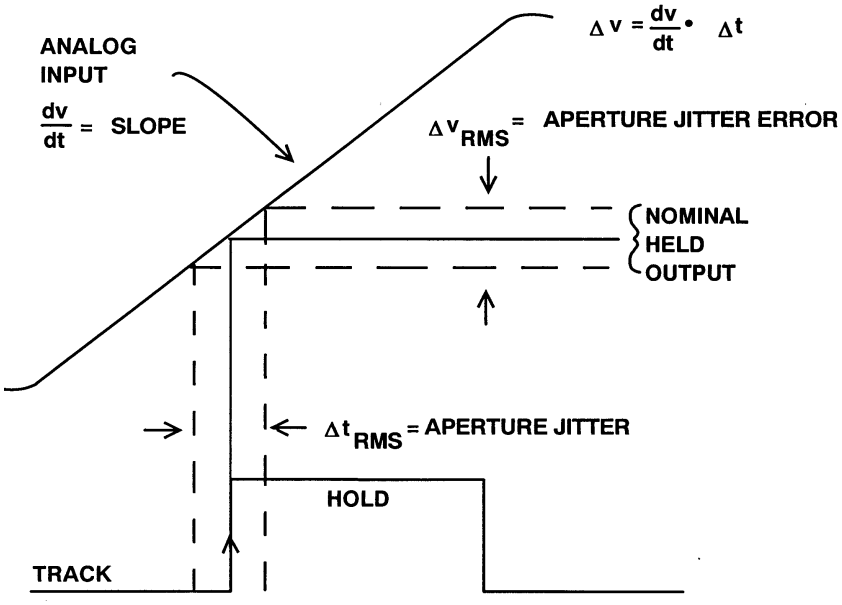


Figure 8: Effects of Aperture or Sampling Clock Jitter on SHA Output

Measuring aperture jitter error in a SHA requires a jitter-free sampling clock and analog input signal source, because jitter (or phase noise) on either signal cannot be distinguished from the SHA aperture jitter itself—the effects are the same. In fact, the largest source of timing jitter errors in a system is most often external to the SHA (or the ADC if it is a sampling one) and is caused by noisy or unstable clocks, improper signal routing, and lack of attention to good grounding and decoupling techniques. SHA aperture jitter is generally less than 50-ps rms, and less than 5-ps rms in high speed devices. Details of measuring aperture jitter of an ADC can be found in Chapter 5 of Reference 11.

Figure 9 shows the effects of total sampling clock jitter on the signal-to-noise ratio (SNR) of a sampled data system. The total rms jitter will be composed of a number of components, the actual SHA aperture jitter often being the least of them.

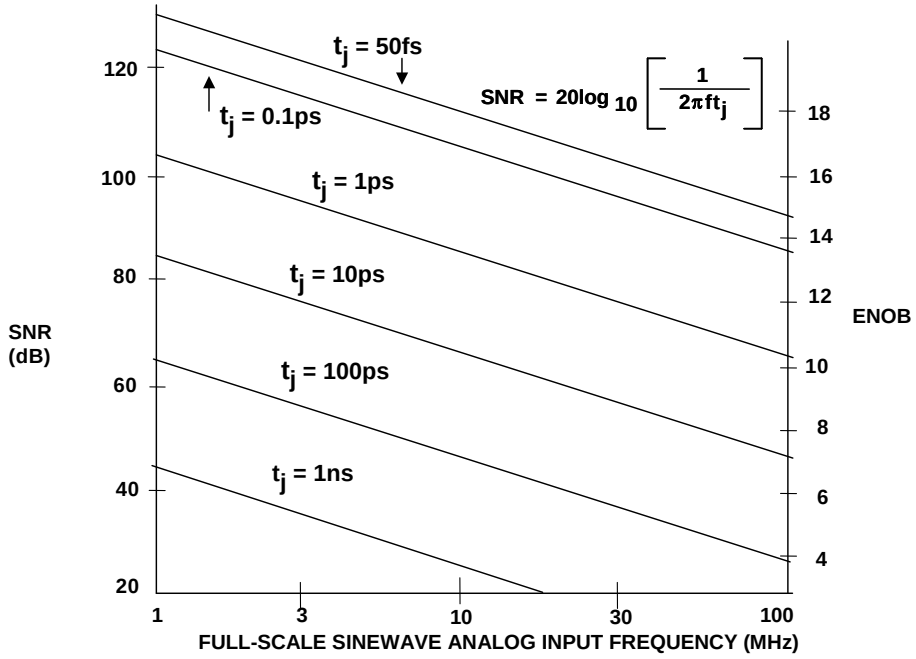


Figure 9: Effects of Sampling Clock Jitter on SNR

HOLD MODE SPECIFICATIONS

During the hold mode there are errors due to imperfections in the hold capacitor, switch, and output amplifier. If a leakage current flows in or out of the hold capacitor, it will slowly charge or discharge, and its voltage will change as shown in Figure 10. This effect is known as *droop* in the SHA output and is expressed in V/µs. Droop can be caused by leakage across a dirty PC board if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of the output buffer amplifier. An acceptable value of droop is where the output of a SHA does not change by more than ½ LSB during the conversion time of the ADC it is driving, although this value is highly dependent on the ADC architecture. Where droop is due to leakage current in reversed biased junctions (CMOS switches or FET amplifier gates), it will double for every 10°C increase in chip temperature—which means that it will increase a thousand fold between +25°C and +125°C.

Droop can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in the track mode. Differential techniques are often used to reduce the effects of droop in modern IC sample-and-hold circuits that are part of the ADC.

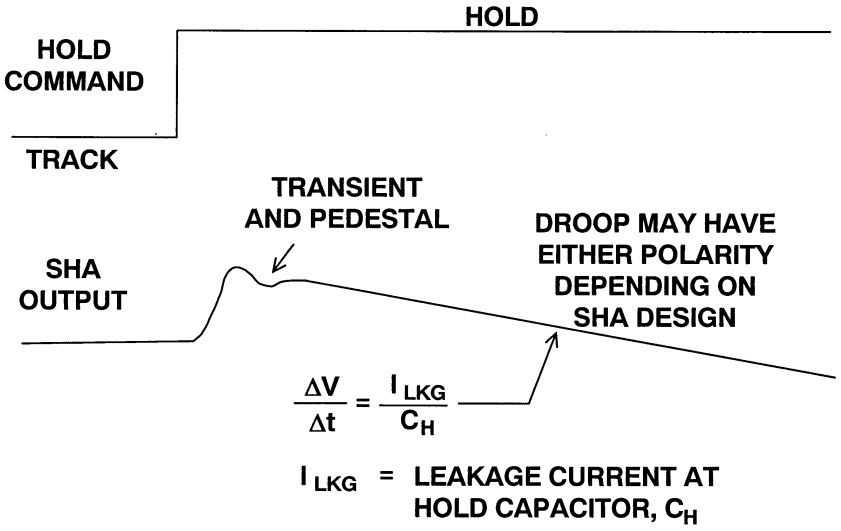
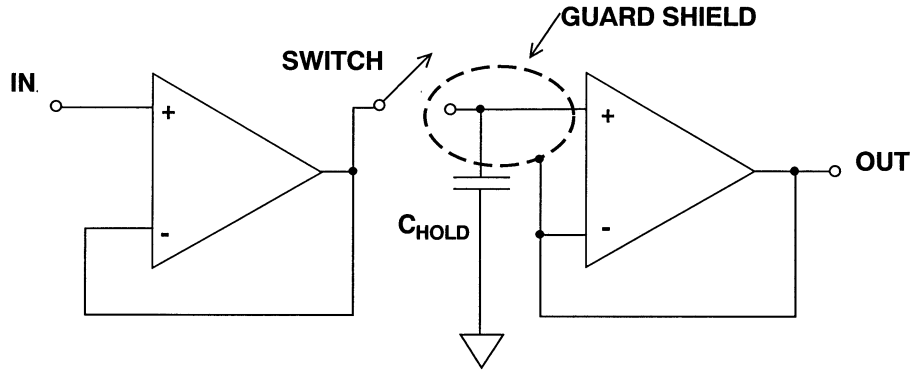


Figure 10: Hold Mode Droop

Even quite small leakage currents can cause troublesome droop when SHAs use small hold capacitors. Leakage currents in PCBs may be minimized by the intelligent use of guard rings. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential. Since there is no voltage between them, there can be no leakage current flow. In a non-inverting application, such as is shown in Figure 11, the guard ring must be driven to the correct potential, whereas the guard ring on a virtual ground can be at actual ground potential (Figure 12). The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB—and on multi-layer boards, guard rings should be present in all layers.



Note: Be Sure a Guard Shield is in Each Layer of the PCB

Figure 11: Drive the Guard Shield with the Same Voltage as the Hold Capacitor to Reduce Board Leakage

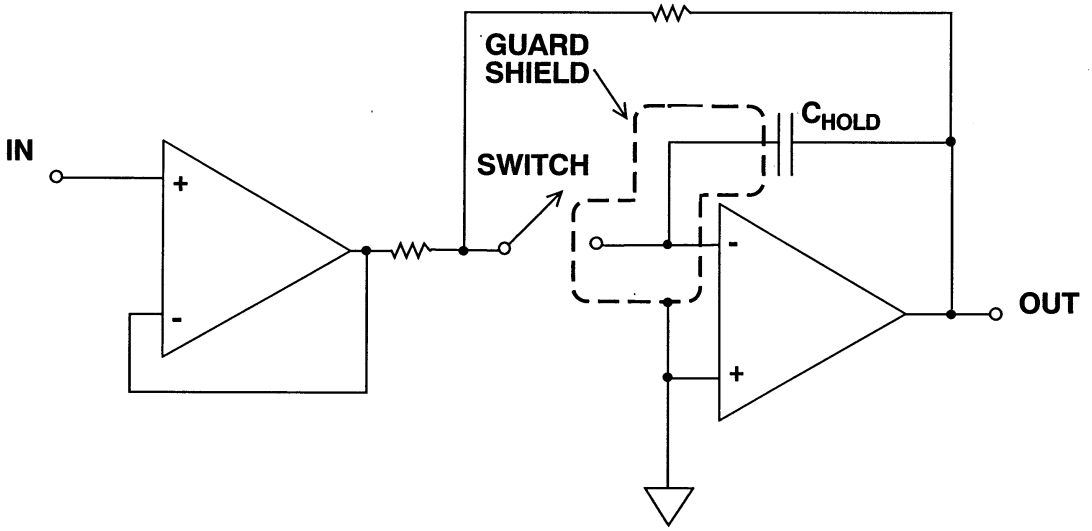


Figure 12: Using a Guard Shield on a Virtual Ground SHA Design

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit, it will recover some of its charge as shown in Figure 13. The phenomenon is known as *dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

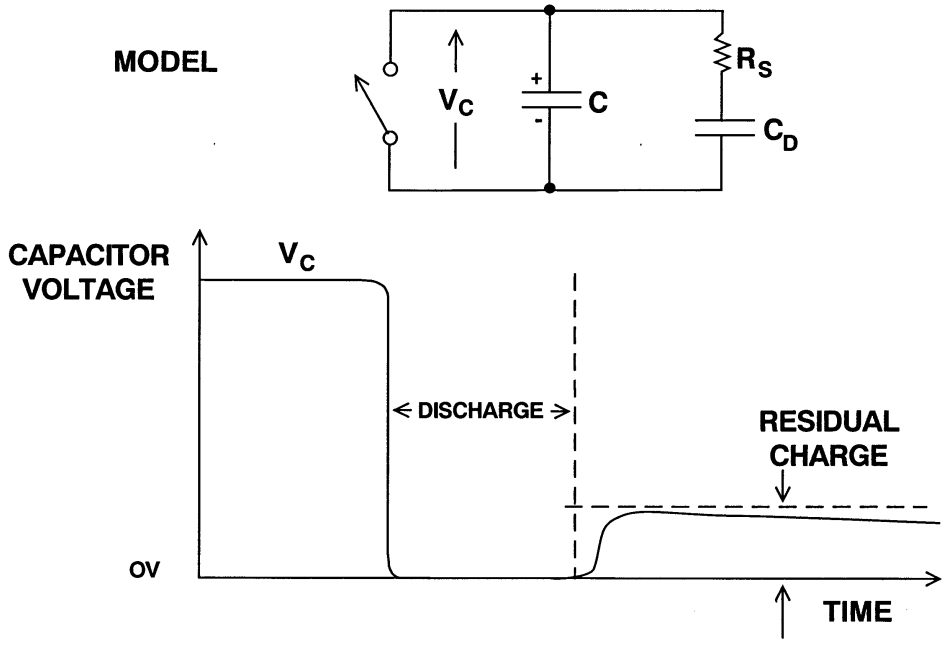


Figure 13: Dielectric Absorption

Different capacitor materials have differing amounts of dielectric absorption—electrolytic capacitors are dreadful (their leakage is also high), and some high-K ceramic types are bad, while mica, polystyrene and polypropylene are generally good. Unfortunately, dielectric absorption varies from batch to batch, and even occasional batches of polystyrene and polypropylene capacitors may be affected. It is therefore wise to pay 30-50% extra when buying capacitors for SHA applications and buy devices which are guaranteed by their manufacturers to have low dielectric absorption, rather than types which might generally be expected to have it.

Stray capacity in a SHA may allow a small amount of the ac input to be coupled to the output during hold. This effect is known as *feedthrough* and is dependent on input frequency and amplitude. If the amplitude of the feedthrough to the output of the SHA is more than ½ LSB, then the ADC is subject to conversion errors.

In many SHAs, distortion is specified only in the track mode. The *track mode distortion* is often much better than *hold mode distortion*. Track mode distortion does not include nonlinearities due to the switch network, and may not be indicative of the SHA performance when driving an ADC. Modern SHAs, especially high speed ones, specify distortion in both modes. While track mode distortion can be measured using an analog spectrum analyzer, hold mode distortion measurements should be performed using digital techniques as shown in Figure 14. A spectrally pure sinewave is applied to the SHA, and a low distortion high speed ADC digitizes the SHA output near the end of the hold time. An FFT analysis is performed on the ADC output, and the distortion components computed.

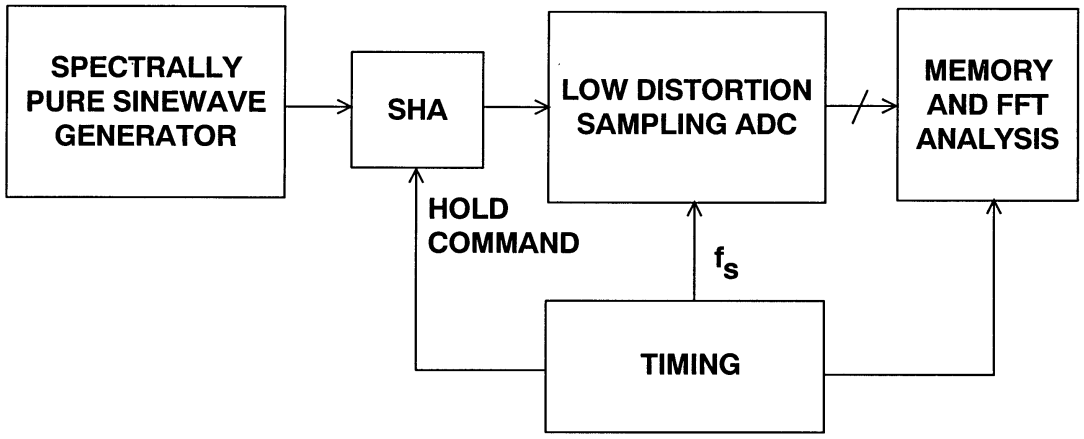


Figure 14: Measuring Hold Mode Distortion

SHA *noise* in the track mode is specified and measured like that of an amplifier. Peak-to-peak *hold mode noise* is measured with an oscilloscope and converted to an rms value by dividing by 6.6. Hold mode noise may be given as a spectral density in nV/√Hz, or as an rms value over a specified bandwidth. Unless otherwise indicated, the hold mode noise must be combined with the track mode noise to yield the total output noise. Some SHAs specify the total output hold mode noise, in which case the track mode noise is included.

HOLD-TO-TRACK TRANSITION SPECIFICATIONS

When the SHA switches from hold to track, it must reacquire the input signal (which may have made a full scale transition during the hold mode). *Acquisition time* is the interval of time required for the SHA to reacquire the signal to the desired accuracy when switching from hold to track. The interval starts at the 50% point of the sampling clock edge, and ends when the SHA output voltage falls within the specified error band (usually 0.1% and 0.01% times are given). Some SHAs also specify acquisition time with respect to the voltage on the hold capacitor, neglecting the delay and settling time of the output buffer. The hold capacitor acquisition time specification is applicable in high speed applications, where the maximum possible time must be allocated for the hold mode. The output buffer settling time must of course be significantly smaller than the hold time.

Acquisition time can be measured directly using modern digital sampling scopes (DSOs) or digital phosphor scopes (DPOs) which are insensitive to large overdrives.

SHA ARCHITECTURES

As with op amps, there are numerous SHA architectures, and we will examine a few of the most popular ones. The simplest SHA structure is shown in Figure 15. The input signal is buffered by an amplifier and applied to the switch. The input buffer may either be open- or closed-loop and may or may not provide gain. The switch can be CMOS, FET, or bipolar (using diodes or transistors) and is controlled by the switch driver circuit. The signal on the hold capacitor is buffered by an output amplifier. This architecture is sometimes referred to as *open-loop* because the switch is not inside a feedback loop. Notice that the entire signal voltage is applied to the switch, therefore it must have excellent common-mode characteristics.

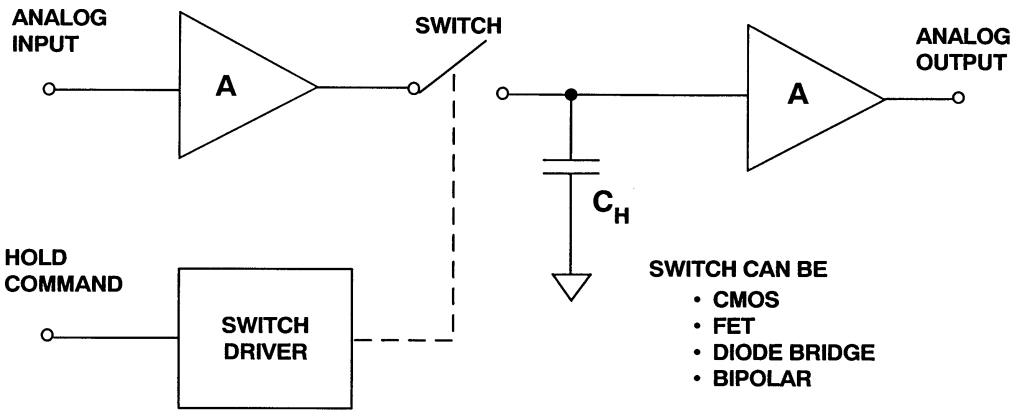


Figure 15: Open-Loop SHA Architecture

An implementation of this architecture is shown in Figure 16, where a simple diode bridge is used for the switch. In the track mode, current flows through the bridge diodes D1, D2, D3, and D4. For fast slewing input signals, the hold capacitor is charged and discharged with the current, I. Therefore, the maximum slew rate on the hold capacitor is equal to I/C_H. Reversing the bridge

drive currents reverse biases the bridge and places the circuit in the hold mode. Bootstrapping the turn-off pulses with the held output signal minimizes common-mode distortion errors and is key to the circuit. The reverse bias bridge voltage is equal to the forward drops of D5 and D6 plus the voltage drops across the series resistors R1 and R2. This circuit is extremely fast, especially if the input and output buffers are open-loop followers, and the diodes are Schottky ones. The turn-off pulses can be generated with high frequency pulse transformers or with current switches as shown in Figure 17. This circuit can be used at any sampling rate, because the diode switching pulses are direct-coupled to the bridge. Variations of this circuit have been used since the mid 1960s in high speed PC board, modular, hybrid, and IC SHAs.

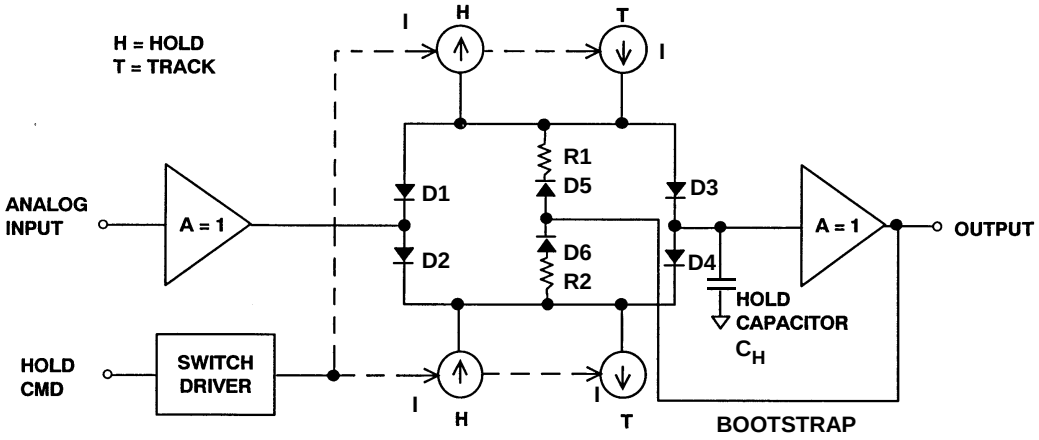


Figure 16: Open-Loop SHA Using Diode Bridge Switch

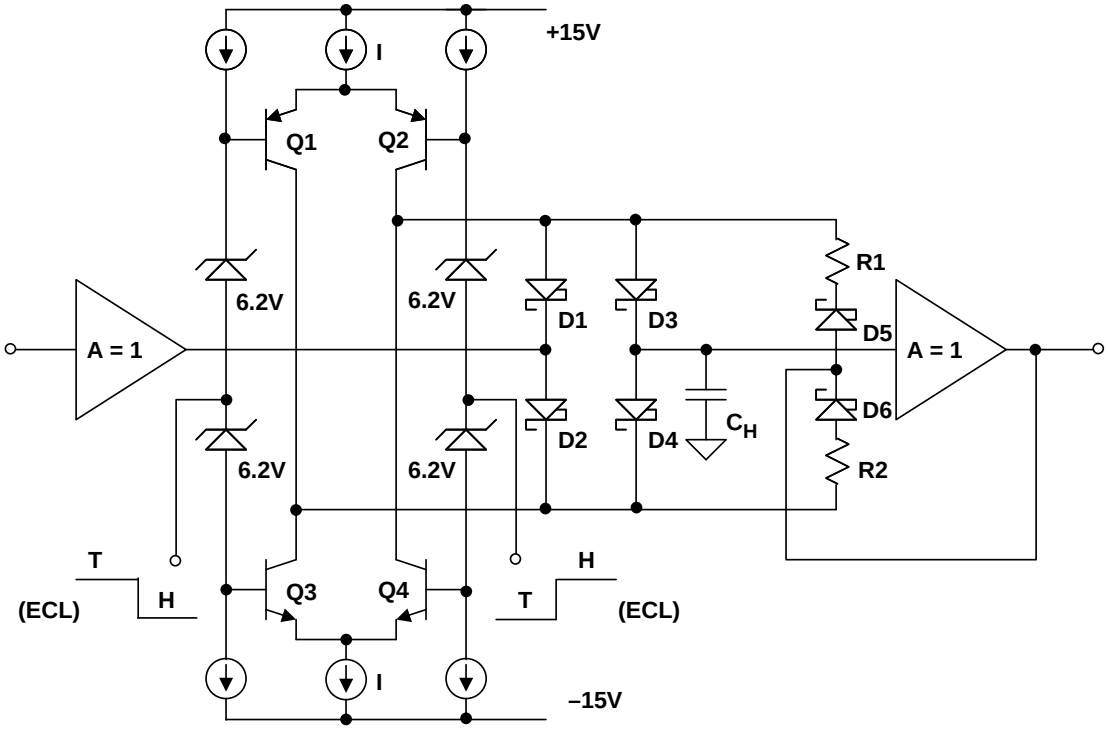


Figure 17: Open-Loop SHA Implementation

The SHA circuit shown in Figure 18 represents a classical *closed-loop* design and is used in many CMOS sampling ADCs. Since the switches always operate at virtual ground, there is no common-mode signal across them.

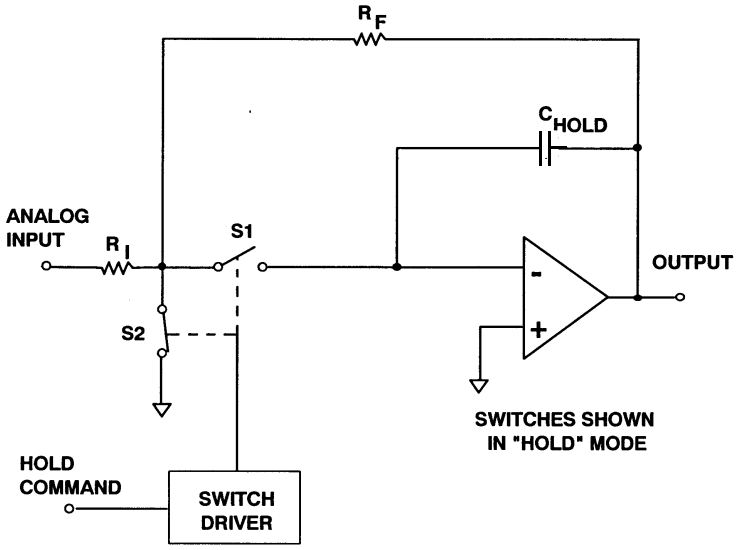


Figure 18: Closed-Loop SHA Based on Inverting Integrator Switched at the Summing Point

Switch S2 is required in order to maintain a constant input impedance and prevent the input signal from coupling to the output during the hold time. In the track mode, the transfer characteristic of the SHA is determined by the op amp, and the switches do not introduce dc errors because they are inside the feedback loop. The effects of charge injection can be minimized by using the differential switching techniques shown in Figure 19.

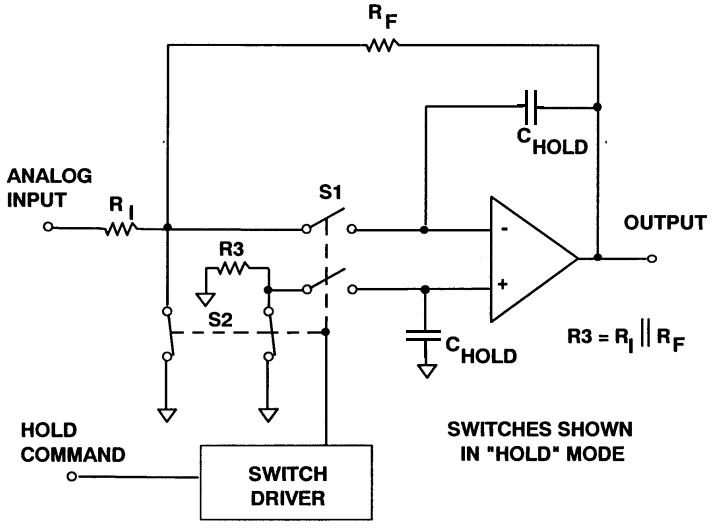
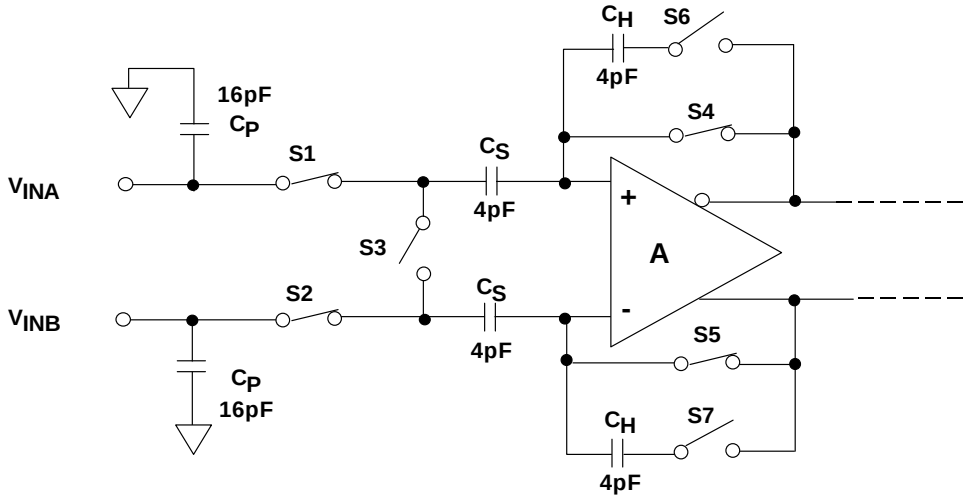


Figure 19: Differential Switching Reduces Charge Injection

INTERNAL SHA CIRCUITS FOR IC ADCS

CMOS ADCs are quite popular because of their low power and low cost. The equivalent input circuit of a typical CMOS ADC using a differential sample-and-hold is shown in Figure 20. While the switches are shown in the *track* mode, note that they open/close at the sampling frequency. The 16-pF capacitors represent the effective capacitance of switches S1 and S2, plus the stray input capacitance. The C_S capacitors (4 pF) are the sampling capacitors, and the C_H capacitors are the hold capacitors. Although the input circuit is completely differential, this ADC structure can be driven either single-ended or differentially. Optimum performance, however, is generally obtained using a differential transformer or differential op amp drive.



SWITCHES SHOWN IN TRACK MODE

Figure 20: Simplified Input Circuit for a Typical Switched Capacitor CMOS Sample-and-Hold

In the *track* mode, the differential input voltage is applied to the C_S capacitors. When the circuit enters the *hold* mode, the voltage across the sampling capacitors is transferred to the C_H hold capacitors and buffered by the amplifier A (the switches are controlled by the appropriate sampling clock phases). When the SHA returns to the *track* mode, the input source must charge or discharge the voltage stored on C_S to a new input voltage. This action of charging and discharging C_S, averaged over a period of time and for a given sampling frequency f_S, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ($1/f_S$), the input impedance is dynamic, and certain input drive source precautions should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that is drawn by C_H from the input drive source. It can be shown that if C_S is allowed to fully charge to the input voltage before switches S1 and S2 are opened that the average current into the input is the same as if there were a resistor equal to $1/(C_S f_S)$ connected between the inputs. Since C_S is only a few picofarads, this resistive component is typically greater than several kΩ for an f_S = 10 MSPS.

Figure 21 shows a simplified circuit of the input SHA used in the AD9042 12-bit,41-MSPS ADC introduced in 1995 (Reference 7). The AD9042 is fabricated on a high speed complementary bipolar process, XFCB. The circuit comprises two independent SHAs in parallel for fully differential operation—only one-half the circuit is shown in the figure. Fully differential operation reduces the error due to droop rate and also reduces second-order distortion. In the track mode, transistors Q1 and Q2 provide unity-gain buffering. When the circuit is placed in the hold mode, the base voltage of Q2 is pulled negative until it is clamped by the diode, D1. The on-chip hold capacitor, C_H, is nominally 6 pF. Q3 along with C_F provide output current bootstrapping and reduce the V_{BE} variations of Q2. This reduces third-order signal distortion. Track mode THD is typically –93 dB at 20 MHz. In the time domain, full-scale acquisition time to 12-bit accuracy is 8 ns. In the hold mode, signal-dependent pedestal variations are minimized by the voltage bootstrapping action of Q3 and the A = 1 buffer along with the low feedthrough parasitics of Q2. Hold mode settling time is 5 ns to 12-bit accuracy. Hold-mode THD at a clock rate of 50 MSPS and a 20-MHz input signal is –90 dB.

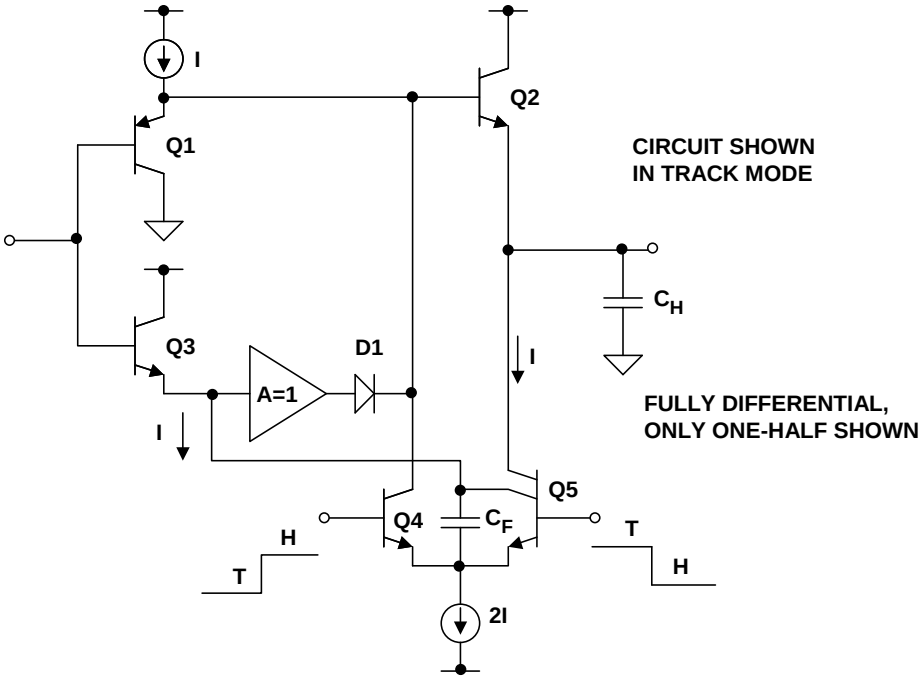


Figure 21: SHA Used in AD9042 12-Bit, 41 MSPS ADC Introduced in 1995

Figure 22 shows a simplified schematic of one-half of the differential SHA used in the AD6645 14-bit, 105-MSPS ADC recently introduced (Reference 9) gives a complete description of the ADC including the SHA). In the track mode, Q1, Q2, Q3, and Q4 form a complementary emitter follower buffer which drives the hold capacitor, C_H. In the hold mode, the polarity of the bases of Q3 and Q4 is reversed and clamped to a low impedance. This turns off Q1, Q2, Q3, and Q4, and results in double isolation between the signal at the input and the hold capacitor. As previously discussed, the clamping voltages are bootstrapped by the held output voltage, thereby minimizing nonlinear effects.

Track mode linearity is largely determined by the V_{BE} modulation of Q3 and Q4 when charging C_H. Hold mode linearity depends on track mode linearity plus nonlinear errors in the track-to-hold transitions caused by imbalances in the switching of the base voltages of Q3 and Q4 and the resulting imbalance in charge injection through their base-emitter junctions as they turn off.

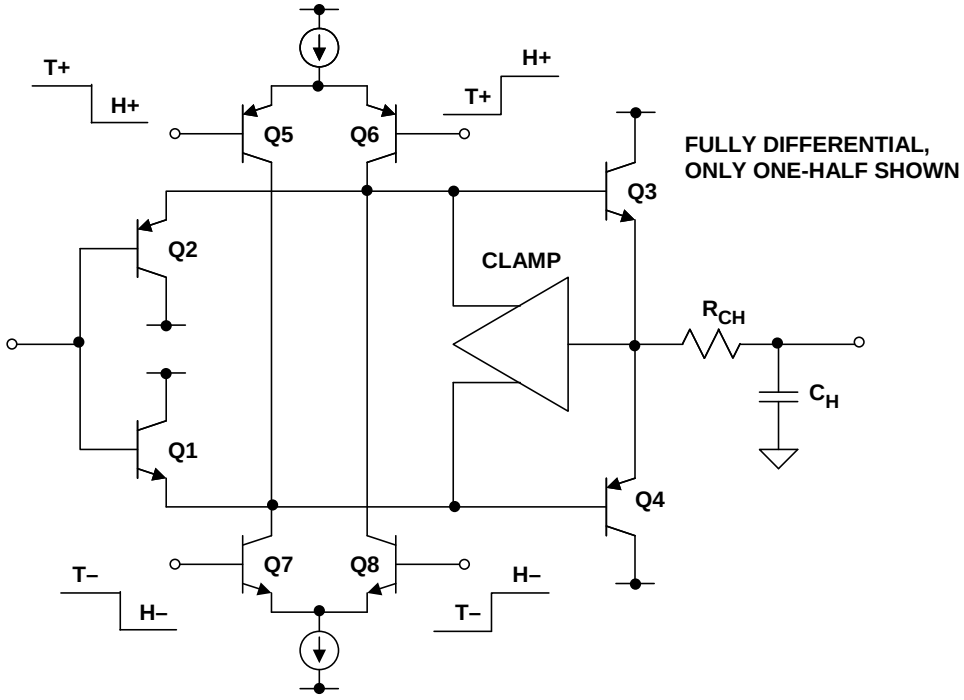


Figure 22: SHA Used in AD6645 14-Bit, 105 MSPS ADC Introduced in 2000

SHA APPLICATIONS

By far the largest application of SHAs is driving ADCs. Most modern ADCs designed for signal processing are sampling ones and contain an internal SHA optimized for the converter design. Sampling ADCs are completely specified for both dc and ac performance and should be used in lieu of discrete SHA/ADC combinations wherever possible. In a very few selected cases, especially those requiring wide dynamic range and low distortion, there may be advantages to using a discrete combination.

A similar application uses a low distortion SHA to minimize the effects of code-dependent DAC glitches as shown in Figure 23. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are not code-dependent, occur at the update frequency, and are easily filterable. This technique may be useful at low frequencies to improve the distortion performance of DACs, but has little value when using high speed low-glitch low distortion DACs designed especially for DDS applications where the update rate is several hundred MHz.

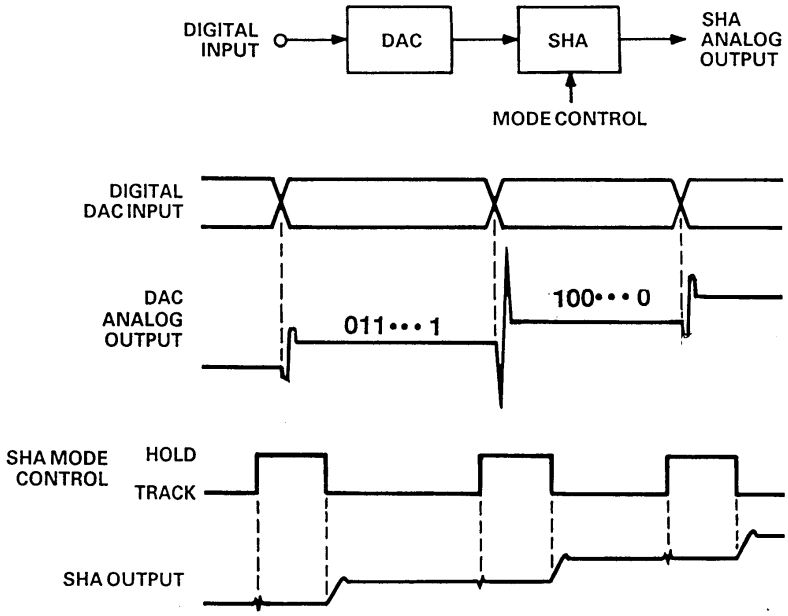


Figure 23: Using a SHA as a DAC Deglitcher

Rather than use a single ADC per channel in a simultaneous sampled system, it is often more economical to use multiple SHAs followed by an analog multiplexer and a single ADC (Figure 24). Similarly, in data distribution systems multiple SHAs can be used to route the sequential outputs of a single DAC to multiple channels as shown in Figure 25; although this is not as common, as multiple DACs usually offer a better solution.

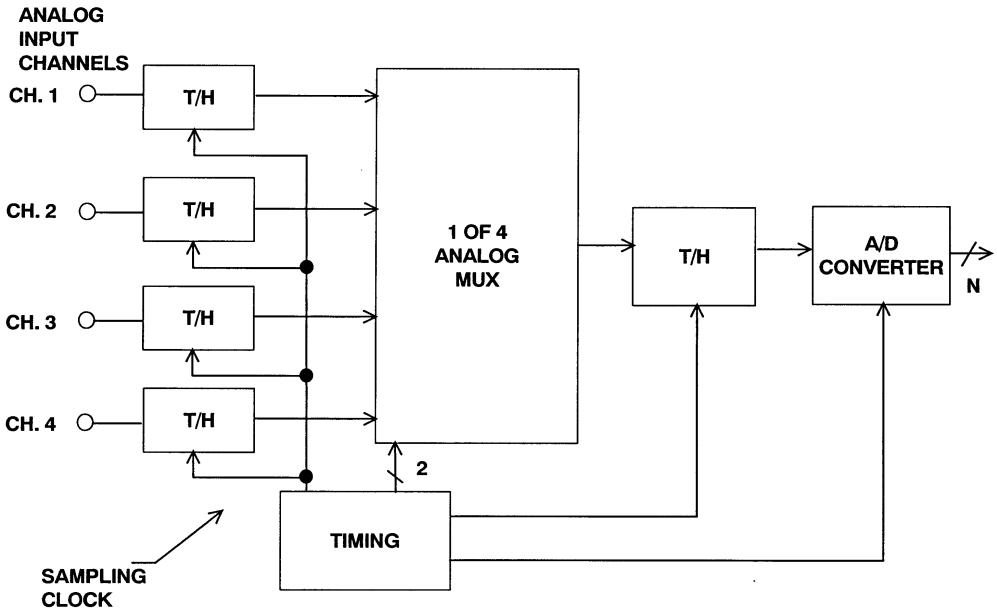


Figure 24: Simultaneous Sampling Using Multiple SHAs and a Single ADC

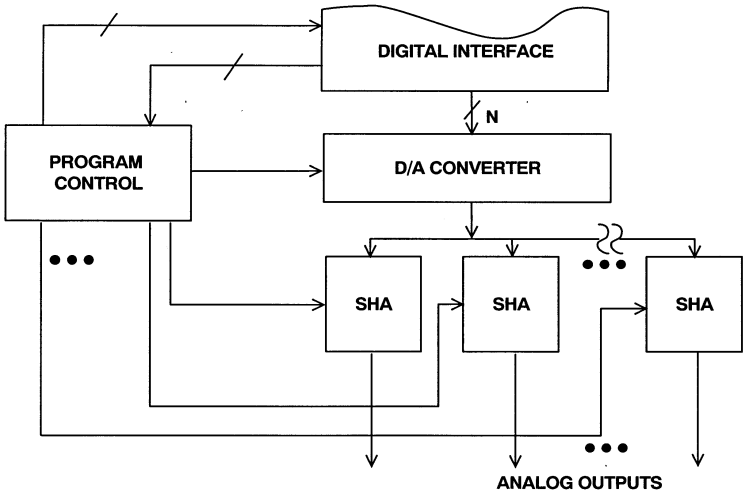


Figure 25: Data Distribution System Using Multiple SHAs and a Single DAC

A final application for SHAs is shown in Figure 26, where SHAs are cascaded to produce analog delay in a sampled data system. SHA 2 is placed in hold just prior to the end of the hold interval for SHA 1. This results in a total pipeline delay greater than the sampling period T. This technique is often used in multi-stage pipelined subranging ADCs to allow for the conversion delays of successive stages. In pipelined ADCs, a 50% duty cycle sampling clock is common, thereby allowing alternating clock phases to drive each SHA in the pipeline (see tutorial MT-024 for details on pipelined ADCs).

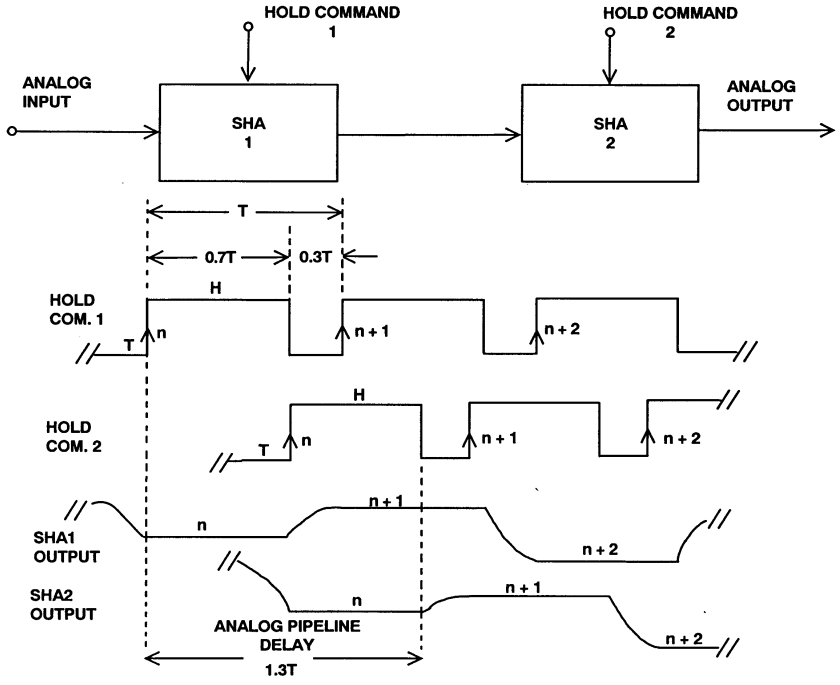


Figure 26: SHAs Used for Analog Pipelined Delay

REFERENCES:

1. Alec Harley Reeves, "Electric Signaling System," *U.S. Patent 2,272,070*, filed November 22, 1939, issued February 3, 1942. Also *French Patent 852,183* issued 1938, and *British Patent 538,860* issued 1939. *(the classic patents on PCM including descriptions of a 5-bit, 6-kSPS vacuum tube ADC and DAC).*

2. L. A. Meacham and E. Peterson, "An Experimental Multichannel Pulse Code Modulation System of Toll Quality," *Bell System Technical Journal*, Vol 27, No. 1, January 1948, pp. 1-43. *(describes the culmination of much work leading to this 24-channel experimental PCM system. In addition, the article describes a 50-kSPS vacuum tube sample-and-hold based on a pulse transformer driver).*

3. J. R. Gray and S. C. Kitsopoulos, "A Precision Sample-and-Hold Circuit with Subnanosecond Switching," *IEEE Transactions on Circuit Theory*, CT11, September 1964, pp. 389-396. *(an excellent description of a solid-state transformer-driven diode bridge SHA, along with a detailed mathematical analysis of the circuit and associated errors).*

4. J. O. Edson and H. H. Henning, "Broadband Codecs for an Experimental 224Mb/s PCM Terminal," *Bell System Technical Journal*, Vol. 44, pp. 1887-1940, Nov. 1965. *(summarizes experiments on ADCs based on the electron tube coder as well as a bit-per-stage Gray code 9-bit solid state ADC. The electron beam coder was 9-bits at 12MSPS, and represented the fastest of its type).*

5. D. J. Kinniment, D. Aspinall, and D.B.G. Edwards, "High-Speed Analogue-Digital Converter," *IEE Proceedings*, Vol. 113, pp. 2061-2069, Dec. 1966. *(a 7-bit 9MSPS three-stage pipelined error corrected converter is described based on recircuilating through a 3-bit stage three times. Tunnel (Esaki) diodes are used for the individual comparators. The article also shows a proposed faster pipelined 7-bit architecture using three individual 3-bit stages with error correction. The article also describes a fast bootstrapped transformer-driven diode-bridge sample-and-hold circuit).*

6. A. Horna, "A 150Mbps A/D and D/A Conversion System," *Comsat Technical Review*, Vol. 2, No. 1, pp. 39-72, 1972. *(a description of a subranging ADC including a detailed analysis of the sample-and-hold circuit).*

7. Roy Gosser and Frank Murden, "A 12-bit 50MSPS Two-Stage A/D Converter," *1995 ISSCC Digest of Technical Papers*, p. 278. *(a description of the AD9042 error corrected subranging ADC using MagAMP stages for the internal ADCs).*

8. Carl Moreland, "An 8-bit 150 MSPS Serial ADC," *1995 ISSCC Digest of Technical Papers*, Vol. 38, p. 272. *(a description of an 8-bit ADC with 5 folding stages followed by a 3-bit flash converter, including a discussion of the sample-and-hold circuit).*

9. Carl Moreland, Frank Murden, Michael Elliott, Joe Young, Mike Hensley, and Russell Stop, "A 14-bit 100-Msample/s Subranging ADC," *IEEE Journal of Solid State Circuits*, Vol. 35, No. 12, December 2000, pp. 1791-1798. *(describes the architecture used in the 14-bit, 105MSPS AD6645 ADC and also the sample-and-hold circuit).*

10. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 7.

11. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 7. Also available as *The Data Conversion Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 7.