General description

The AX5689 is an 8 channel data converter- and controller IC with PWM outputs for digital audio amplifiers.

On-chip high-performance low latency sigma-delta data converters measure the analog signal directly at the speaker terminals and provide feedback to the digital controller.

A total of 8 ADCs enables flexible configurations, not only for control loop feedback, but also for analog audio input, supply and temperature sensing, etc.

A sophisticated and versatile digital controller enables feedback after the output filter such that it corrects for distortions caused by the supply, power stage and analog output filter. The digital implementation of the loop filter allows aggressive filtering with up to 5 orders per channel, instead of the traditional 2nd order.

The already high performance per channel becomes exceptional when multiple slices are used in parallel. The linear ADCs and high loop gain enables distortion lower than 0.003% and damping factors in excess of 1000.

This product is still in development and all information in this datasheet is preliminary and subject to change. Information is confidential and should not be distributed

Features

- Digital class-D controller with feedback after filter
- 8 controller slices and 8 ADCs enable 8 single-ended channels, 4BTL, combinations and other uses
- 105 dB dynamic range,
  Up to 114dB with parallel ADCs
- 0.003% THD
- Serial audio interface with 44.1kHz-192kHz sample rates
- Configurable interconnections between slices and ADCs for versatility and MIMO control.
- Volume control and soft mute

Applications

- High-end audio amplifiers and entertainment systems
- Active loudspeaker systems
- Active noise reduction systems
- High-resolution low latency data-conversion
- High-speed closed loop controller

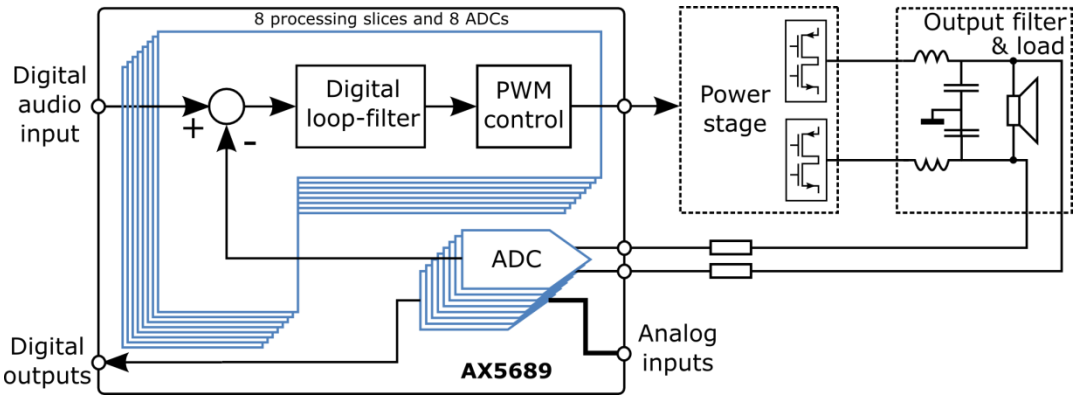

Figure 1 Application of the AX5689

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2 Block diagram

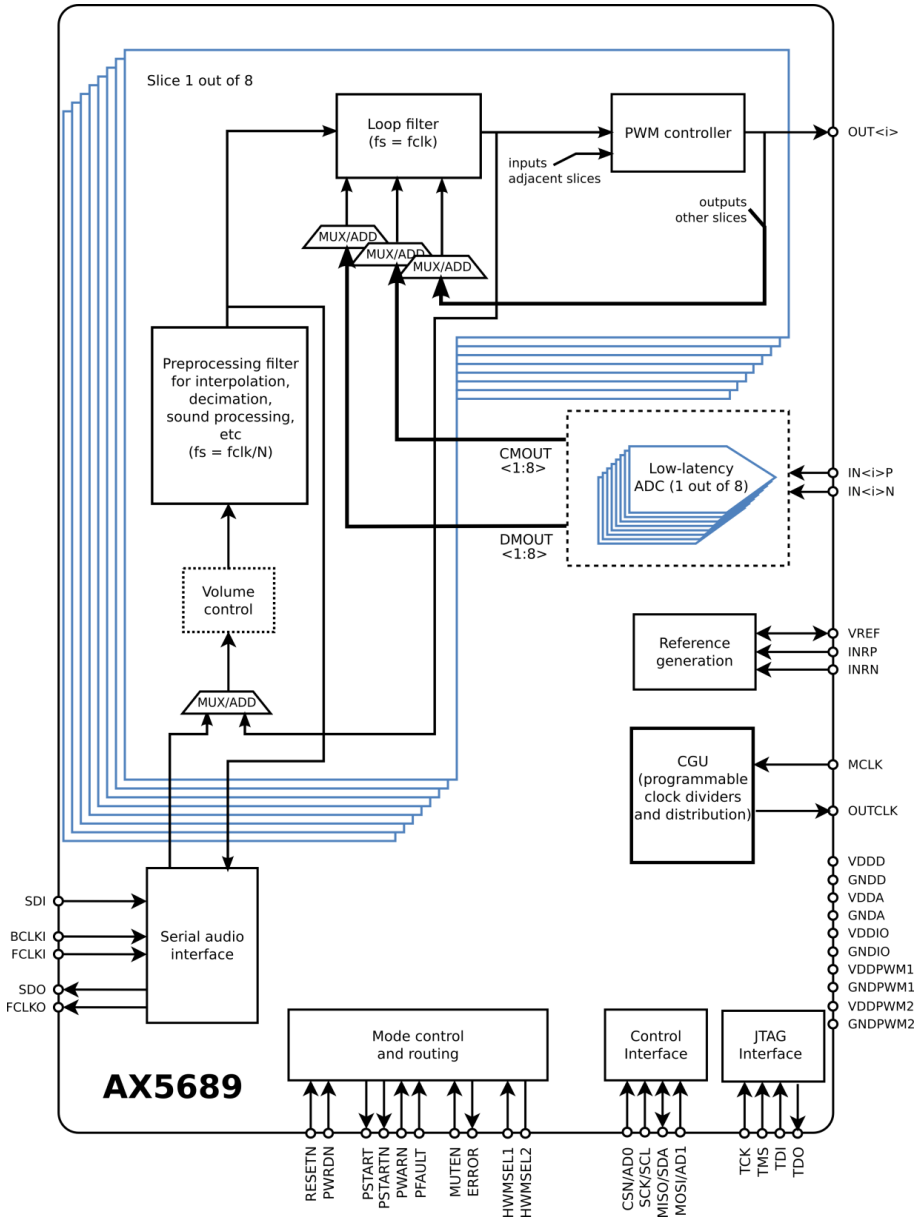

Figure 2: Functional block-diagram of the AX5689

2.1 Package

The exact package is to be determined. The most likely candidate is a QFP, preferably a QFP64.

3 Features

- High dynamic range
  - 105B A-weighted with one ADC per channel
  - >114dB A-weighted with 8ADCs per channel
- HD audio compatible
  - <0.03% THD to 40kHz
- Class-D with feedback after filter with high loop-gain
  - Flattens LC transfer
    - Enables lower $f_{corners}$
    - Enables under damped filters with small L
  - Suppresses nonlinearities in L and C
- High-loop gain also gives high suppression of:
  - Supply disturbance
  - Power stage artifacts such as dead-zone or crossover distortion
- Reduction of external components and BOM costs:
  - No separate DACs or ADCs required
  - No external filtering needed for on-board ADCs
  - For class-D:
    - Can optimize L/C values for cost while maintaining flat transfer
    - Non-linear L and C are possible
    - Boucherot cells (a.k.a. Zobel networks) can be omitted as LC response is damped by feedback
- Low latency ADCs (8 instances)
  - Primary functions:
    - Load voltage conversion
    - High-performance analog inputs
  - Other functions:
    - Power stage supply sensing
    - Current sensing
    - Auxiliary audio inputs
    - Analog volume control input
    - Multi-purpose (temperature sensing, etc)
- Integrated high-quality ADC reference with bandgap noise rejection
- Flexible PWM controllers:
  - Single-ended (SE) or bridge-tied-load (BTL) output channels
    - Single-ended outputs can either be capacitively coupled, have a symmetric supply or use one channel as common return.
  - Differential (AD) or tri-level (BD and BD+) modulation
    - BD+ modulation has low common-mode and low differential mode radiation
  - PWM frequencies programmable from *300kHz* up to $1/3*f_{clk}$
  - Also supports PDM output
  - PWM phases selectable per channel (for staggered phases)
- Flexible routing and configurations from 1-8 channels:
  - Digital audio inputs can be routed to one or more control loop slices

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    - Analog inputs can be routed to one or more control loop slices and ADCs can be combined for lower noise
- PWM outputs usable for:
    - Interface to class-D power stage
    - Line-level DAC outputs (with passive RCRC or LC filter network)
    - Class-AB amplifier input signals to enable class-AB with digital feedback
        - With output filter either before or inside the class-AB amp.
        - *TBD for future/special versions? feedback can be taken from after the line transformer in e.g. tube amplifiers.*
    - Headphone PWM output *(It is to be determined whether the outputs themselves have low output impedance or whether an intermediate headphone driver is needed)*
- Digital serial audio interface:
    - 16 – 32 bit.
    - 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz Sampling Rates
- Soft volume control and mute.
    - Supports different programmable rates for volume, soft-mute and fast-mute transitions.
    - Analog volume control possible with one of the on-board ADCs
- 3.3V inputs *(5V tolerant inputs T.B.D)*
- *1.8*-3.3V digital outputs *with separate supply for easy swing control*
- Hardware mode, to enable operation without microcontroller
    - Two dedicated inputs can select between 4 common use-case
    - Easy to use

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4 Functional description

4.1 General

The AX5689 is a controller IC for digital audio reproduction. It contains specialized low-latency ADCs that can sense output signals directly at the load and sophisticated digital control algorithms that enable a mixed-signal closed-loop system with high bandwidth, high loop-gain and compensation for external output filters.

An amplifier that uses the AX5689 can achieve high performance at low cost, as all backend error sources are highly suppressed by the loop gain. This results in relaxed requirements for the power supply and the power stage. For class-D amplifiers with feedback after the output filter this also results in relaxed requirements for the filter components and their associated costs.

The AX5689 is usable with many different amplifier configurations. The loads can be connected either in a bridge-tied-load or single-ended fashion, including AC-coupled loads or power stages with symmetric supply. For BTL operation, two slices can be configured such that one process the differential mode signal and the other controls the common-mode. The common-mode controller ensures that the outputs are biased properly in any of the configurations and ensures low-pop startup and shutdown.

A flexible PWM controller converts the signal to 1-bit form with a wide selection of pulse frequencies and modulation methods. The PWM outputs can be fed directly to a switching power stage that is followed by an output reconstruction filter. For other uses or other types of amplifiers, the PWM outputs can also be fed first to a (passive) reconstruction filter that removes the high-frequency switching components. The filter compensation on the AX5689 can correct for a wide range of external filters, provided that their order is not higher than two at frequencies close to the audio band.

For best performance, the ADC inputs that feedback the signal should be connected directly at the load-point (regardless of whether the load is a speaker, a line-level output or something else). If however the external filters have an overall roll-off with a higher order than two, then an intermediate point should be chosen for the feedback.

The AX5689 has a modular structure with flexible routing. The overall signal processing path consists of a digital input interface, volume control, an interpolation stage , the digital loop-filter and PWM controller. Eight copies (slices) of this signal path are available to enable operation with up to eight channels per chip. Each of the slices is separately configurable and cross connections between the slices enable MIMO control. Next to the 8 signal processing slices, 8 ADCs are included on the AX5689. Selectable routing between the ADCs and the slices not only simplifies PCB layout, but also enables different signal configurations. ADCs can be used either for the feedback, or can be used to convert analog input signals. Outputs of multiple ADCs can also be combined. When the inputs of these combined ADCs are also connected to the same signal, then they can achieve higher performance (as the noise of multiple ADCs scales down compared to their combined signal). ADCs can also be selected for auxiliary functions such as analog volume inputs or supply sensing. The outputs of a selection of the ADCs can be decimated and made available through a serial digital output interface.

5 Application example

The example application diagram in Figure 3 shows the application of the AX5689 as amplifier controller for an integrated stereo class-D power stage in BTL configuration. The audio inputs can be chosen to be either digital or analog. The digital audio inputs are connected via the serial audio interface. The analog audio inputs can be connected via the analog inputs of the ADC's, which can then be routed to the input of digital control loop. The analog input data can also be made available as digital output data through the serial audio interface.

As this example assumes usage without a microcontroller, operation modes are selected with hardware mode settings. Depending on the type of input (analog or digital), the AX5689 can be chosen to start-up in different hardware modes (HWMSEL1 = 1; HWMSEL2 toggles between 0 and 1 for analog or digital input). Note that in both modes AX5689 is enabled for 4 channels. It is therefore also possible to connect a second power stage for 4 channel operation.

In this example application the PWM outputs from slice 1 and 2 (OUT1P/OUT1N and OUT2P/OUT2N) of AX5689 are connected to inputs IN1A through IN2B of the power stage.

The outputs OUT1A through OUT2B (differential output terminals) are fed back to the input of the analog inputs of the AX5689. The AX5689 will process the signal through the ADC back to the input of the digital loop filter. This way the feedback loop is closed including the power stage and its filter section. By including the filter section inside the loop, it is possible to correct for non-linearity introduced by this section. Next to improved linearity, the feedback loop also dampens the LC filter by creating a low output impedance. This way the Zobel/Boucherot networks that are usually incorporated inside the filter section can be omitted.

The example application diagram is work in progress. Full connection diagram which includes for example supply connections, decoupling, etc. will be added in future versions.

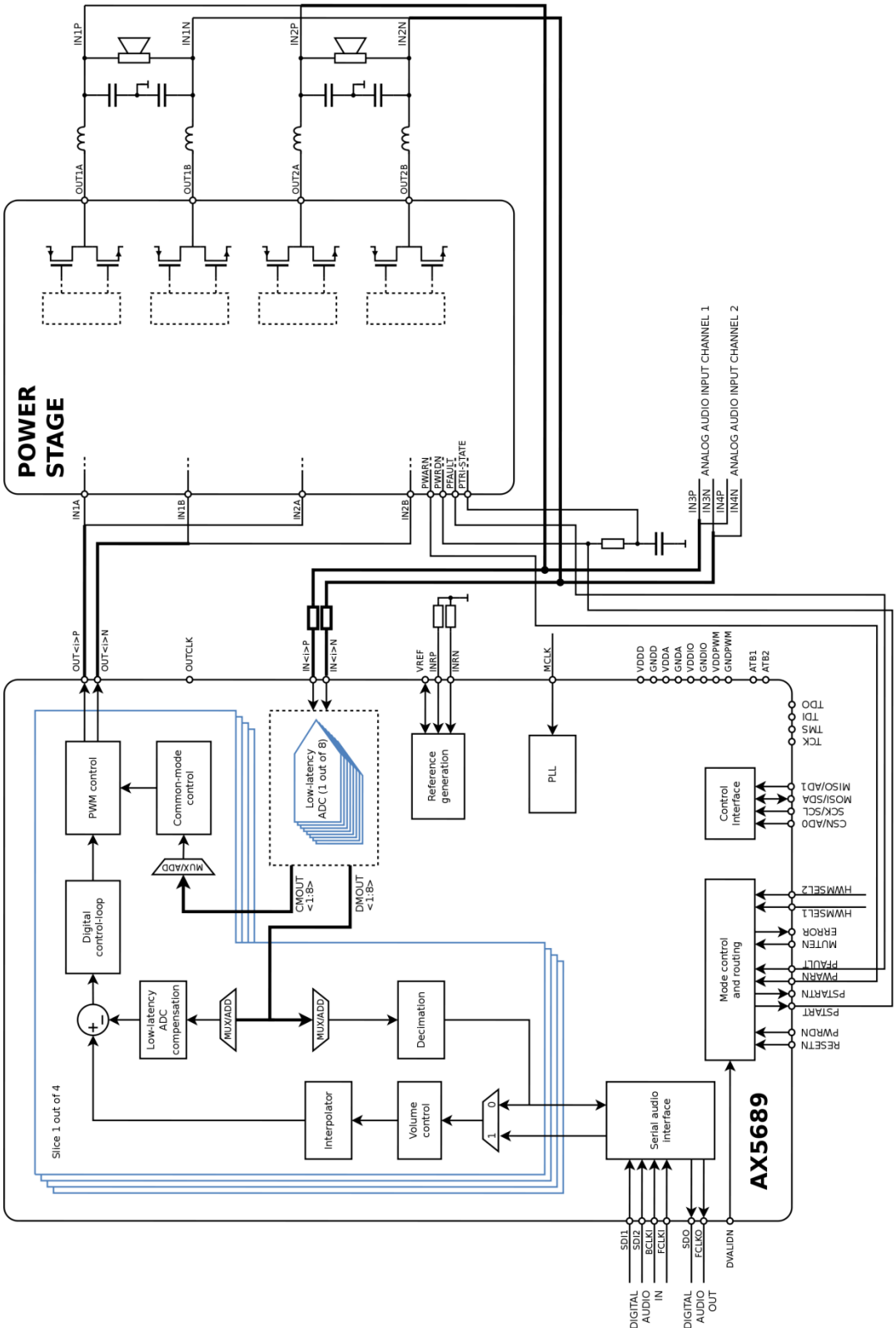

Figure 3 Application diagram

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6 Specifications

6.1.1 Electrical specifications

Table 1

Parameter	Description	min	typ	max	units
	DC characteristics				
I_{DDD}	Digital supply current - Operating, all slices active - Power down			~50 0.01	mA
I_{DDA}	Analog supply current - all ADCs active - Power down			~100 0.01	mA
V_{REF}	Reference voltage	0.85	0.9	0.95	V
V_{OS}	Input-equivalent (ADC) offset			~100	µV
ΔG	Gain mismatch	-1	0	1	dB
ADC / Mixed signal performance characteristics					
THD+N	Total harmonic distortion and noise 100Hz, Vin = ½*Vin-peak 1kHz, Vin = ½*Vin-peak 6kHz, Vin = ½*Vin-peak	 -80 -80 -80	 -90 -90 -90		dB
SNR_{peak}	Peak signal to noise ratio		90		dB
DR_{DM}	Dynamic Range		105		dB Awtd
X_{talk}	Inter channel crosstalk	~60			dB
PSR	Power supply rejection	~60			dB
	TBD: More specs to be added:				

6.1.2 Typical characteristics

As the integrated product is not yet available, the concept of digitally controlling a class-D power stage with feedback after the filter has been verified using a multi-chip bench demonstrator. Results of this multi-chip bench demonstrator are given in this section.

The multi-chip bench demonstrator includes:

- PCB containing low-latency ADC
- Spartan-3 FPGA
- TFA9810 class-D power stage

The TFA9810 uses 14.4 V supply rail and is connected in BTL configuration to a 8 ohm load. Feedback is taken at the speaker terminals to include the LC filter section and fed back to the inputs of the low-latency ADC. The complete digital control loop (including filter compensation and PWM controller) is implemented on a Xilinx Spartan-3 FPGA. A digital input is connected using I2S.

The following graphs show the results of the digital amplifier connected to the measurement equipment (APx526 by Audio Precision).

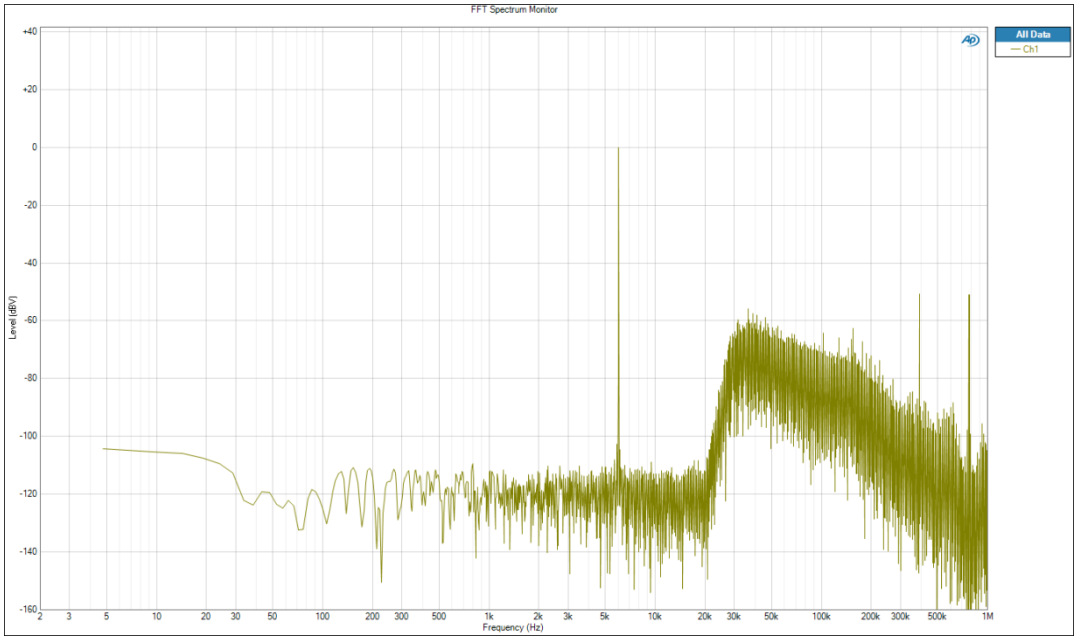

Figure 4: Spectrum of the output signal with 6kHz - 0dBV input. Harmonic distortion ratio >100dB.

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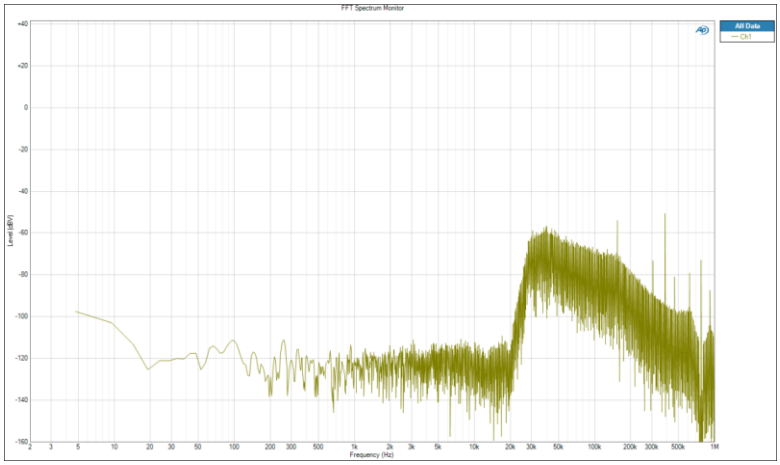

Figure 5: Spectrum of the output signal without input. Noise floor (integrated noise in audio band) <50uVrms (A-weighted).

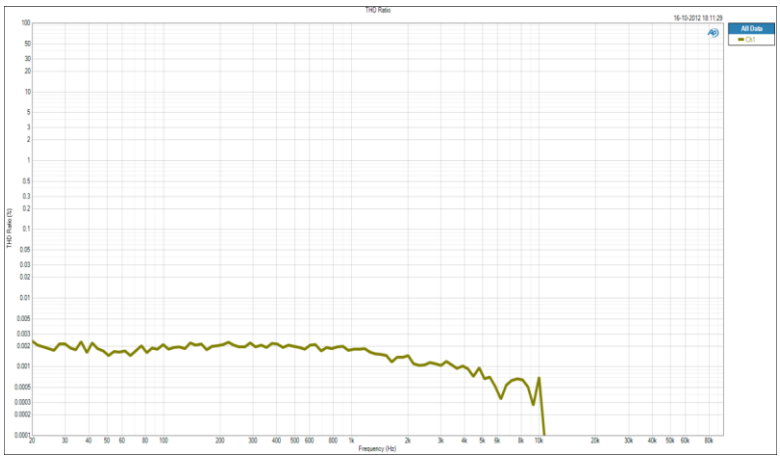

Figure 6 THD ratio vs. Frequency. Measured with 0 dBV output signal. THD ratio approximately 0.002% across audio band.

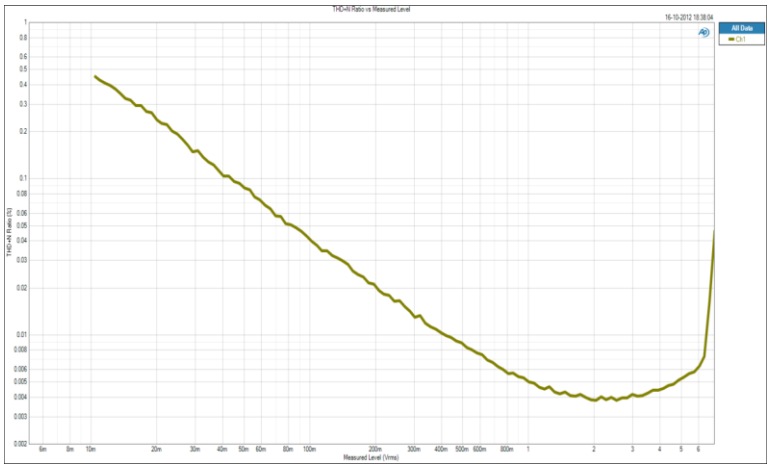

Figure 7 THD+N ratio vs. measured output level (Vrms). Measured with input frequency of 1 kHz. THD+N decreases to 0.004% for 0dBV output signal.

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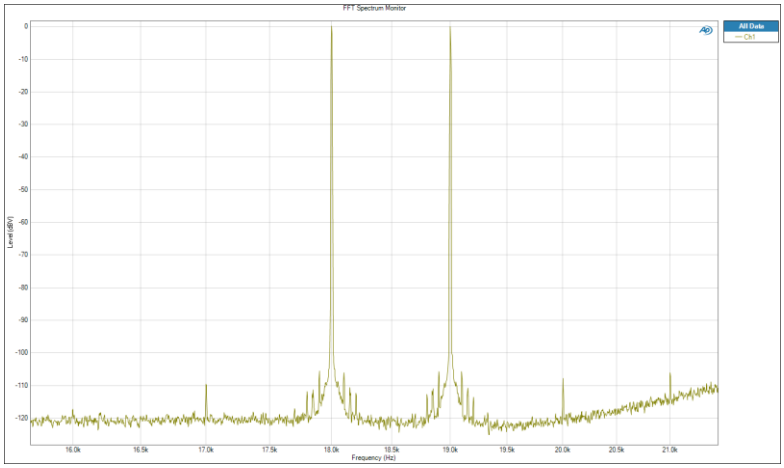

Figure 8 Output spectrum with 18 and 19 kHz input signal. Third order intermodulation distortion -110 dB

7 Revision history

Revision	Date	Reason for revision
D2g	20150216	Derived from version AX5689_amplifier_controller_datasheet_D2g

Table 2: Document revision history

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