Multiplexer U610 selects between the eight available hardware trigger signals. The selected signal is routed to the trigger comparator U840 on schematic <5> through buffer U641. The sync signal from the analog generator arrives via P34 and appears as a status bit as well as a trigger source. To match the threshold of the trigger comparator, the generator sync signal is attenuated by resistors R3401 and R5103 and centered around ground by R5102.

Antialias Filters <9>

The antialiasing filters are analog lowpass filters used to eliminate signals above the Nyquist rate from the A/D converter input. It is a "FDNR" (Frequency Dependent Negative Resistance) ladder filter as is the D/A reconstruction filter. A conventional LC ladder filter consists of series arms which are inductors and shunt arms which are capacitors. As the signal frequency increases, the series inductor impedance increases and the shunt capacitor impedance decreases. Above the corner frequency of the filter the attenuation rises rapidly, reducing out of band signals at the filter output. A FDNR ladder filter may be thought of as an LC lowpass ladder filter in which each inductor has been replaced by a resistor and each capacitor has been replaced by a FDNR element. Using this transformation, resistors in the original filter become capacitors in the transformed filter. Its impedance decreases with frequency twice as fast as a conventional capacitor. This doubly sharp shunt impedance, in combination with the fixed impedance in the series arms of the filter produces the same rolloff as the original LC filter.

Since the two filters are nominally identical, only one will be described here. The input signal is applied to the filter at C7103 and R8103. R8103 and R8101 provide a dc bias current path for U712, U720, U721, and U731. C7103 and C8302 are the source and load capacitances respectively. They are ratio matched to within 0.1% because their ratio directly determines the passband gain of the filter. R8102, R8202, R8211, and R8304 are the series elements of the ladder. R8104, U712, C7204, R8109, R8201, R8110 and C7205 comprise the first FDNR element, shunting the node between R8102 and R8202 to ground. Similarly, R8203, U720, C7207, R8204, C7208, R8206, R8205 and C7206 form the second FDNR element shunting the next node of the ladder. R8210, U721, C7301, R8209, R8212, R8208, C7302, R8207 comprise the third and final FDNR. R8301 and R8302 are the main gain setting resistors for buffer U731, providing a gain of 2 to compensate for the loss in the ladder network. R8303 and C8304 provide mid-band flatness compensation. C7303 and R8111 provide a dc signal path to exclude dc offsets from the filter.

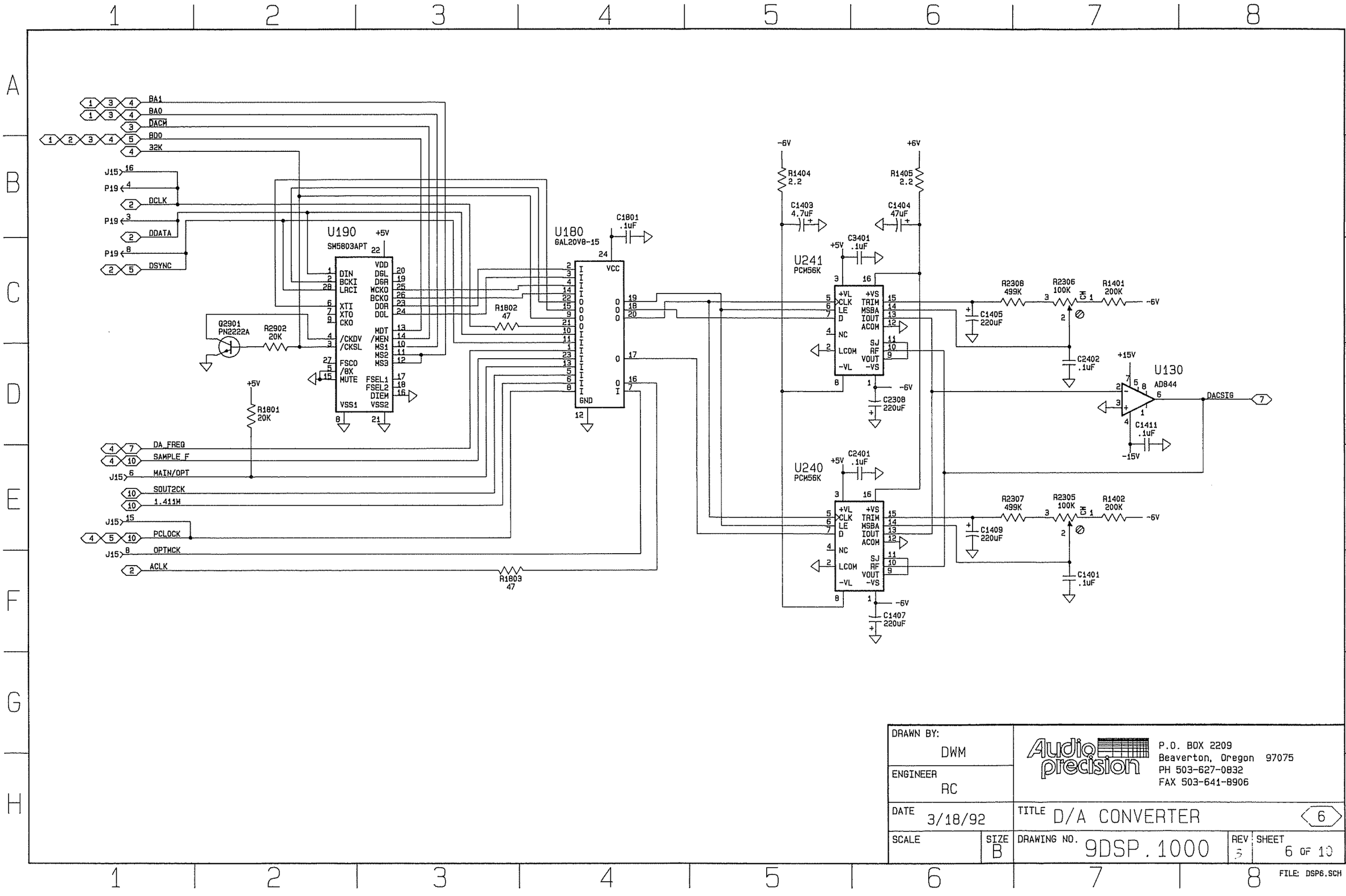
A/D Converters <10>

Analog signals are converted to digital signals for later processing by two 16-bit A/D converters and their associated sample-and-hold amplifiers. There are two nominally identical channels of A/D conversion. Only channel A will be described. The input signals from the antialiasing filters are applied to sample-and-hold amplifier U620. It operates in an inverting configuration with gain set by R7201 and R7101. The R7203-C7202 network peaks the response of the sample and hold U620, reducing the error signal during hold mode with fast slewing signals. Narrowband dither is added from U641 into the summing junction through R7202 to reduce quantization distortion. The sample and hold mode is controlled by the conversion complete signal out of the A/D converter.

The output of the sample and hold drives the analog input of the A/D converter. The full scale signal at this point is approximately ±3 Volts peak. The conversion clock applied to pin 16 is a divide-by-6 version of the master clock. When operating at the 192 kHz sample rate this is 4.096 MHz, at 176.4 kHz this is 3.7627 MHz. The conversion clock is stopped momentarily by U740 during the start conversion pulse to insure proper operation of the converter. The data is clocked out of the converter by a higher frequency clock applied to pin 21. This is a divide-by-4 signal from the master clock. Data output from the converter on pin 13 is routed through U740 to the serial input of the decimator dsp. Part of U740 acts as a dual input data selector, switching between data from the two A/D converters.

The converter MSB is adjusted by potentiometer R7204. The converter is heavily decoupled from the power supplies by sip network R6204 and capacitors C6304, C7203, C6302, and C6303 to reduce noise pickup. Resistor network R5301 shuts down the internal conversion clock. Capacitors C6301 and C6202 filter the internal reference voltage circuits.

8-bit counter U841 and programmable logic chip U740 generate the A/D converter clock signals. Crystal oscillator Y64 supplies a 22.5792 MHz clock to the pal for use in generating 44.1 kHz and 176.4 kHz sample rate signals. All other sample rates are derived from the 24.576 MHz clock. The SAMPLEF line from U640 routes the 24.576 MHz clock to U740 pin 22 when high and the 22.5792 MHz clock when low. Counter U841 derives binary sub-multiples of the selected clock which are combined in U740 to obtain the gated clocks required by the A/D converters and by the dsp's serial input port.



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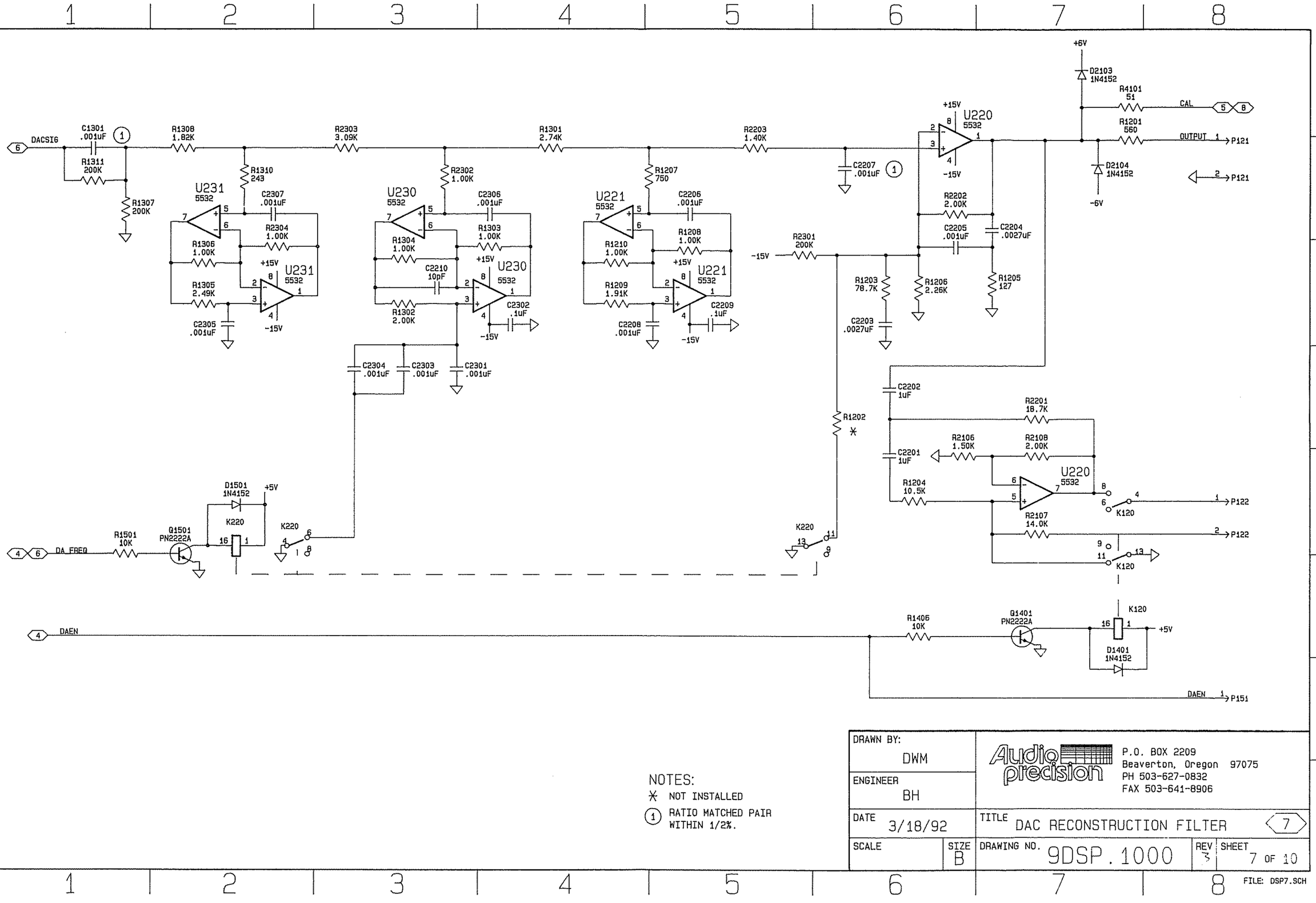
ENGINEER RC			
DATE 3/18/92	TITLE D/A CONVERTER		6
SCALE	SIZE B	DRAWING NO. 9DSP.1000	REV 3 / SHEET 6 OF 10

FILE: DSP6.SCH



NOTES:

* NOT INSTALLED

(1) RATIO MATCHED PAIR WITHIN 1/2%.

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ENGINEER BH		
DATE 3/18/92	TITLE DAC RECONSTRUCTION FILTER	7
SCALE	SIZE B	DRAWING NO. 9DSP.1000 · REV 3 · SHEET 7 OF 10

FILE: DSP7.SCH