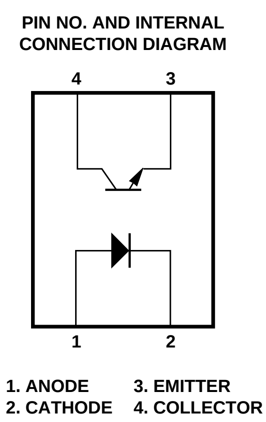
Agilent HCPL-817 Phototransistor Optocoupler High Density Mounting Type

Data Sheet

Description

The HCPL-817 contains a light emitting diode optically coupled to a phototransistor. It is packaged in a 4-pin DIP package and available in wide-lead spacing option and lead bend SMD option. Input-output isolation voltage is 5000 Vrms. Response time, t_r, is typically 4 µs and minimum CTR is 50% at input current of 5 mA.

Functional Diagram



Ordering Information

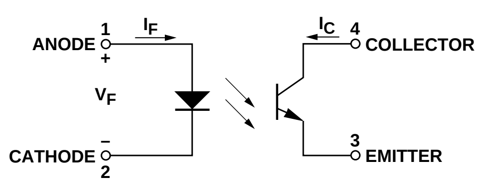
Specify part number followed by Option Number (if desired).

HCPL-817-XXX

└ Option Number

060	=	VDE0884 Option
W00	=	0.4" Lead Spacing Option
300	=	Lead Bend SMD Option
500	=	Tape and Reel Packaging Option
00A	=	Rank Mark A
00B	=	Rank Mark B
00C	=	Rank Mark C
00D	=	Rank Mark D
00L	=	Rank Mark L

Schematic



Features

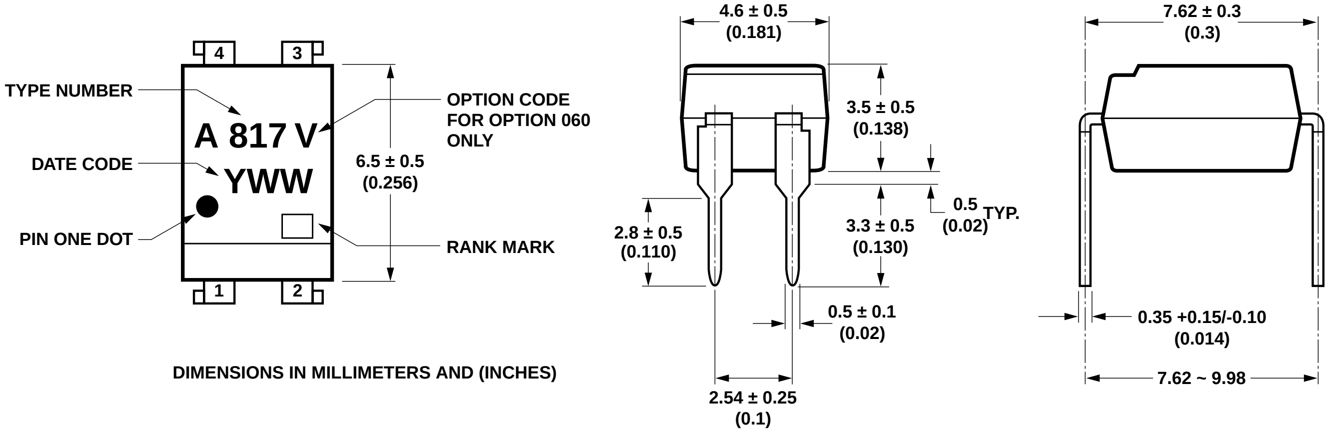
- **Current Transfer Ratio (CTR: min. 50% at I_F = 5 mA, V_{CE} = 5 V)**
- **High input-output isolation voltage (V_{iso} = 5000 Vrms)**
- **Response time (t_r: typ., 4 µs at V_{CE} = 2 V, I_C = 2 mA, R_L = 100 Ω)**
- **Compact dual-in-line package**
- **UL approved**
- **CSA approved**
- **VDE approved**
- **Options available:**
  - **Leads with 0.4" (10.16 mm) spacing (W00)**
  - **Leads bends for surface mounting (300)**
  - **Tape and reel for SMD (500)**
  - **VDE 0884 approvals (060)**

Applications

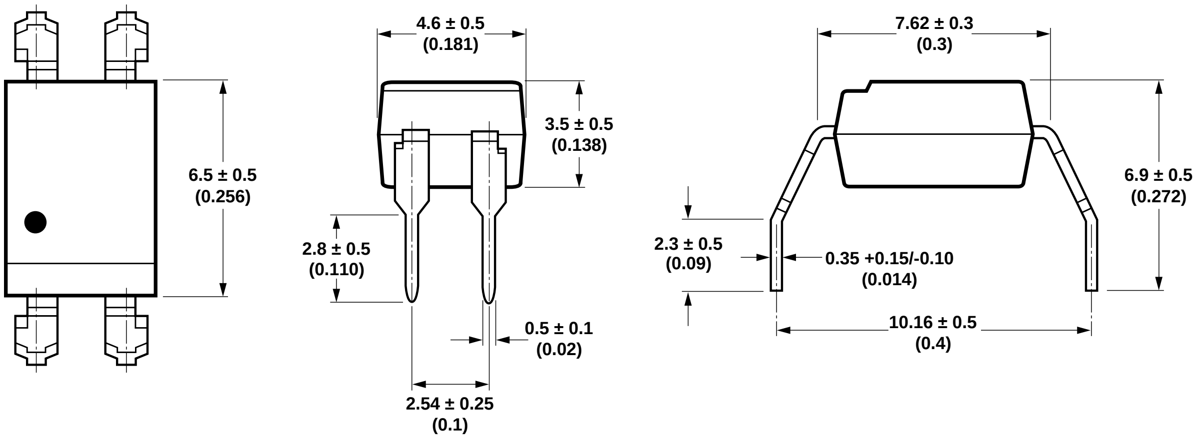
- **Signal transmission between circuits of different potentials and impedances**
- **I/O interfaces for computers**
- **Feedback circuit in power supply**

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Package Outline Drawings

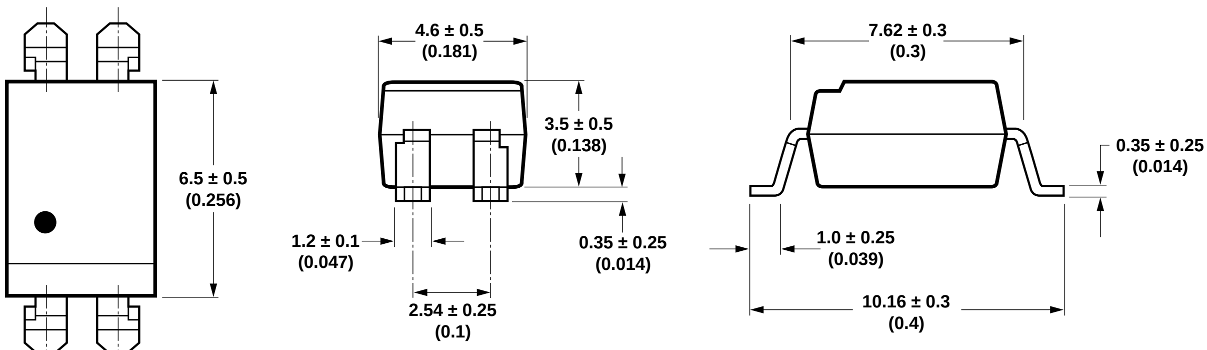


Package Outline – Option W00



DIMENSIONS IN MILLIMETERS AND (INCHES)

Package Outline – Option 300



DIMENSIONS IN MILLIMETERS AND (INCHES)

Absolute Maximum Ratings (T_A = 25°C)

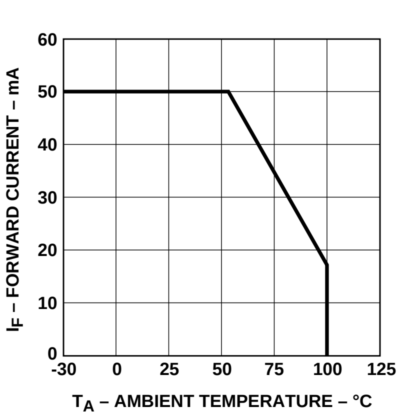
Storage Temperature, T_S	–55°C to +125°C
Operating Temperature, T_A	–30°C to +100°C
Lead Solder Temperature, max. (1.6 mm below seating plane)	260°C for 10 s
Average Forward Current, I_F	50 mA
Reverse Input Voltage, V_R	6 V
Input Power Dissipation, P_I	70 mW
Collector Current, I_C	50 mA
Collector-Emitter Voltage, V_{CEO}	35 V
Emitter-Collector Voltage, V_{ECO}	6 V
Collector Power Dissipation	150 mW
Total Power Dissipation	200 mW
Isolation Voltage, V_{iso} (AC for 1 minute, R.H. = 40 ~ 60%)	5000 Vrms

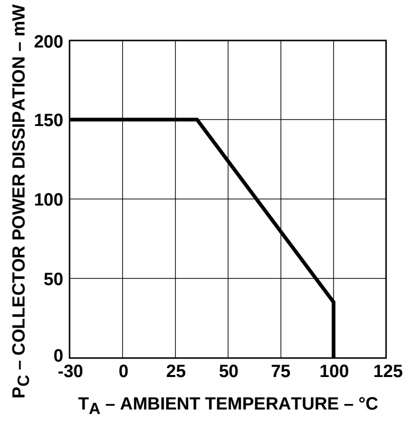
Electrical Specifications (T_A = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Forward Voltage	V_F	–	1.2	1.4	V	I_F = 20 mA
Reverse Current	I_R	–	–	10	µA	V_R = 4 V
Terminal Capacitance	C_t	–	30	250	pF	V = 0, f = 1 KHz
Collector Dark Current	I_{CEO}	–	–	100	nA	V_{CE} = 20 V
Collector-Emitter Breakdown Voltage	BV_{CEO}	35	–	–	V	I_C = 0.1 mA
Emitter-Collector Breakdown Voltage	BV_{ECO}	6	–	–	V	I_E = 10 µA
Collector Current	I_C	2.5	–	30	mA	I_F = 5 mA, V_{CE} = 5 V, $R_{BE} = \infty$
*Current Transfer Ratio	CTR	50	–	600	%	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	–	0.1	0.2	V	I_F = 20 mA, I_C = 1 mA
Response Time (Rise)	t_r	–	4	18	µs	V_{CC} = 2 V, I_C = 2 mA, R_L = 100 Ω
Response Time (Fall)	t_f	–	3	18	µs	
Cut-off Frequency	f_c	–	80	–	KHz	V_{CC} = 5 V, I_C = 2 mA R_L = 100 Ω, –3 dB
Isolation Resistance	R_{iso}	5×10^{10}	1×10^{11}	–	Ω	DC 500 V 40 ~ 60% R.H.
Floating Capacitance	C_f	–	0.6	1.0	pF	V = 0, f = 1 MHz

$$* \text{CTR} = \frac{I_C}{I_F} \times 100\%$$

Rank Mark	CTR (%)	Conditions
L	50 ~ 100	I_F = 5 mA, V_{CE} = 5 V, T_A = 25°C
A	80 ~ 160	
B	130 ~ 260	
C	200 ~ 400	
D	300 ~ 600	





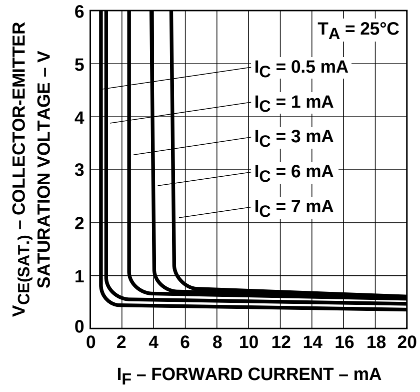
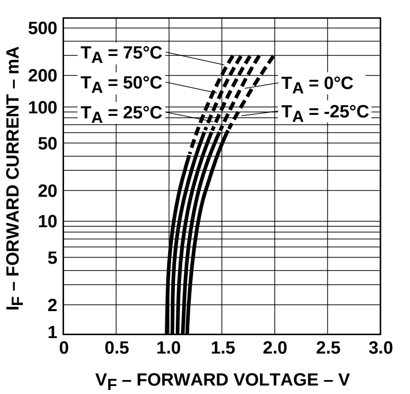
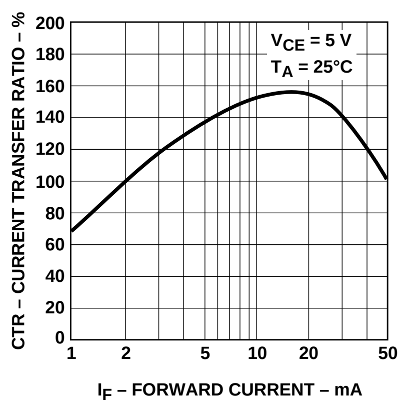


Figure 1. Forward current vs. temperature.

Figure 2. Collector power dissipation vs. temperature.

Figure 3. Collector-emitter saturation voltage vs. forward current.





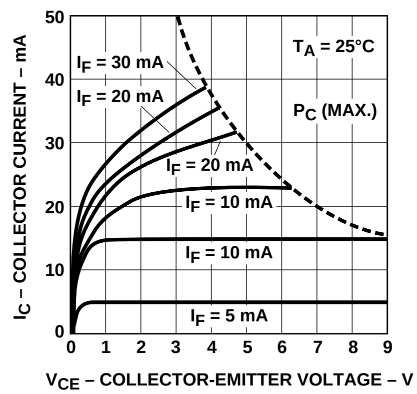
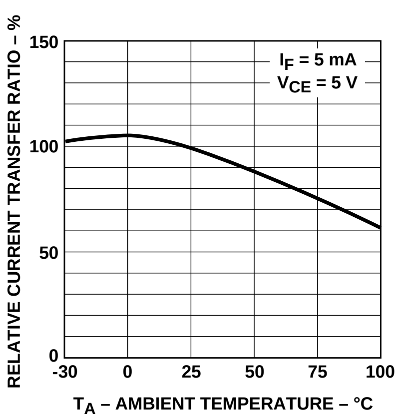
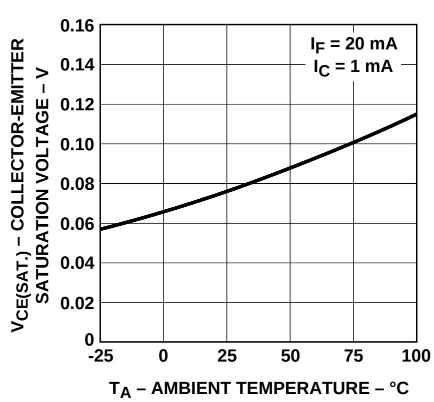


Figure 4. Forward current vs. forward voltage.

Figure 5. Current transfer ratio vs. forward current.

Figure 6. Collector current vs. collector-emitter voltage.





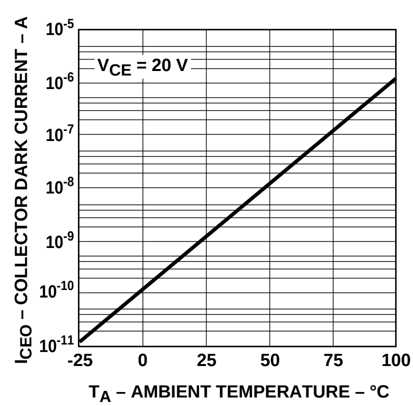


Figure 7. Relative current transfer ratio vs. temperature.

Figure 8. Collector-emitter saturation voltage vs. temperature.

Figure 9. Collector dark current vs. temperature.

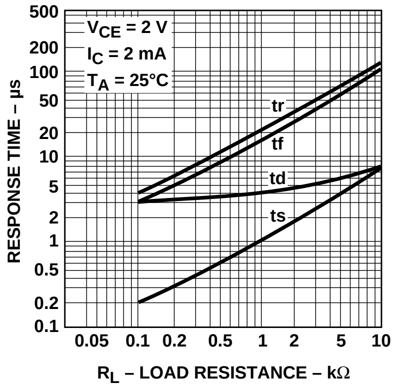


Figure 10. Response time vs. load resistance.

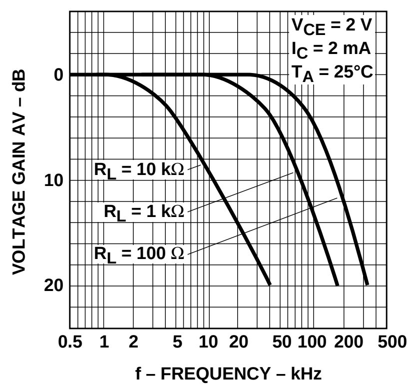
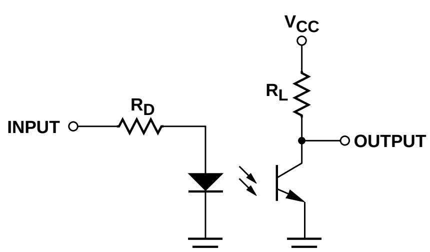
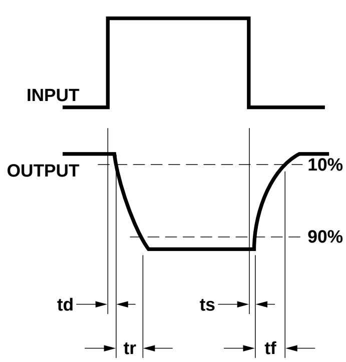


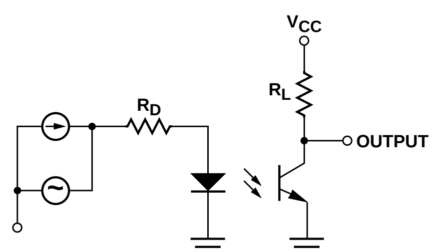
Figure 11. Frequency response.

Test Circuit for Response Time





Test Circuit for Frequency Response



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Data subject to change.

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