AN 18-BIT DAC FOR CONSUMER APPLICATIONS

By F.J. Highton and K. Ito

Burr-Brown Corporation
6730 South Tucson Boulevard
Tucson, Arizona 85706

ABSTRACT

PCM58 represents a significant advance in monolithic data conversion, being a self-contained 18-bit bipolar DAC which responds to serial input data. Designed for digital audio applications, it provides 16-bit accuracy at low cost.

INTRODUCTION

Consumers have now become accustomed to the sound quality associated with 16-bit pulse code modulated digital recording, and CD player manufacturers are trying to stimulate demand by offering further performance advantages. These include increased resolution and higher oversampling frequencies. Although only 16-bit words are available from a compact disc, most systems now employ digital filters and oversampling techniques which produce extra bits. These extra bits are essentially the result of interpolation between samples. If it is assumed that these extra bits are a fair representation of the original signal, the quantization noise can be reduced. An 18-bit system has a theorectical signal/noise limit of -110 dB compared to -98 dB for a 16-bit system. Oversampling is employed to reduce the need for multipole analog filtering. Presently 4 times oversampling is common but manufacturers are planning for 8 and even 16 times oversampling. These trends place stringent demands on the DAC design. 16-bit converters are available from several manufacturers with 14-bit accuracy and 4 times oversampling capability. An 18-bit converter was introduced last year and was readily accepted, being employed in several high quality players. To achieve the extremely low noise and distortion specifications it was decided not to incorporate a voltage reference, output amplifier or serial-to-parallel converter.[1] The challenge of the new design was to approach this performance yet add the customer convenience afforded by a self-contained reference and serial data input.

THE DESIGN

The converter is built on a 20V junction isolated bipolar process which offers thin film NiCr resistors and a buried zener. This process has been used for many monolithic DACs over the past five years and is well characterized. The chosen architecture, which uses conventional binary weighted current sources, has previously demonstrated its potential for high accuracy. The converter chip photograph is shown in Figure 1. An output amplifier is not included because customer response indicated a preference for a current output model. In the "high-end" market the ability to specify the analog components using listening tests is considered to be extremely important. This also dictates the need for operation with an external feedback resistor and mandates the specification for absolute output current to ±1%. An internal feedback resistor is included for customer flexibility and is designed to minimize the effects of self-heating on converter linearity.

The internal voltage reference employs the buried zener diode which has a well characterized positive temperature coefficient, and good long and short term stability. A Vbe multiplier is used to compensate the zener and an overall TC of ±25 ppm/°C is easily achievable without trimming. Zener bias current is derived from the zener reference voltage to improve stability and therefore a start up circuit is required. An epitaxial FET, which is subsequently pinched off the by "building" reference voltage is used for this purpose. This circuit provides all the bias voltages for the converter and is the source of the reference current, which, via the servo amplifier, determines the final output current.

A servo amplifier is necessary to provide an absolute bit current value independent of lot to lot variations of NiCr sheet resistance and zener breakdown voltage. The amplifier, shown in Figure 2, takes the temperature compensated reference current as an input and forces the output current to an absolute value, determined by a trimmed resistor ratio. In order to provide the necessary tracking accuracy an open loop gain in excess of 80 dB is provided. Compensation of the amplifier is achieved with the application of an external capacitor to the "reference decouple pin". This capacitor also ensures that the VREF line presents a low impedance to the DAC circuit over a wide frequency range. A low impedance is necessary to reduce the effect of glitches, coupled to the line when bit switches are activated. Simulations indicated that the impedance was sufficiently low that cascoding of the bit current source transistors was not needed.[1]

Noise from the reference and servo amplifier is reduced by the reference decoupling capacitor, and an external capacitor allows customers the flexibility to trade component size and cost for noise decoupling. Laser trimming of resistors R303 or R307 determines the absolute value of the output current. The current

generator employed in the servo loop is a close replica of the actual bit current generators in order to ensure accuracy. An anti-saturation clamp, Q316, prevents possible lock up of the servo amplifier in the event of uneven application of the supply voltages.

The DAC architecture is conventional and well proven. Binary weighted current sources are employed for the three most significant bits. An R-2R ladder is employed for bits 4 through 18 with binary current division of bits 14 and down. Bit switches are driven differentially to minimize glitching and digital feedthrough. Since the DAC is placed between ground and the negative supply rail, the serial-to-parallel converter that drives it is similarly placed. In this way, level shifting is required only between the digital inputs and the serial-to-parallel converter and not between every bit input. The serial-to-parallel converter consists of an 18-stage shift register and latch. The serial data is fed into the shift register MSB first and when all bits are in place a latch enable command, LEC, transfers the data to the latches. Bit currents are controlled by the output of the latches and thus the analog output remains steady while the shift register is updated. The serial-to-parallel converter employs differential current mode logic, DCML, which is very economical in terms of number of devices and current per gate. With a gate current of 100 μA the shift register will clock at frequencies up to 35 MHz. In order to minimize chip area a simple latch is used in place of an edge triggered type. This requires on chip generation of a LEC pulse which is achieved with minimal complexity by gating together the word clock and the clock pulse. Amplifier/drivers are used to drive the internal clock and control lines.

Digital input translators accept TTL input signals, level shift them below ground and convert them to DCML levels. In addition, hysteresis is applied to provide a Schmitt triggered input. This is an important feature for those many applications where system clocks and control signals may not be entirely clean and may otherwise cause false inputs. An input circuit is illustrated in Figure 3. The input circuit consists of a differential lateral PNP pair, Q1/Q2, which provides a very robust input, having breakdown voltages in excess of 20V in either direction. Using the PNPs the input signal is both level shifted and level translated. A second NPN differential amplifier stage, Q3/Q4, connected to the output of the PNP stage produces the fast feedback signal to control the input threshold. To ensure that the threshold will respond fast enough in either direction a push-pull arrangement, Q9/Q10, is employed.

A bipolar offset current is generated on chip to minimize the external circuitry required for the most common applications. This current is derived from the bit current reference line and therefore tracks the bit currents. Its polarity is changed by means of a reference amplifier, connected as a current to voltage converter and a reference resistor which is externally connected to the summing node of the output amplifier.

Adjustment of the four most significant bits, for those applications where 16-bit linearity is insufficient, may be achieved externally by connecting potentiometers from the bit resistors to VPOT. VPOT is connected to a voltage within the internal reference which tracks the bits and thus allows adjustments, once made, to hold over temperature. Since bit adjustment nodes are buffered from the sensitive bit current transistors, these pins may be safely ignored if not used.

LAYOUT CONSIDERATIONS

With an LSB of less that 23 μV, even minute changes i voltages dropped along bias lines can be problematic. Even though the effect of these drops may be trimmed out at one temperature, the combination of different temperature coefficients will ensure a mismatch over the operating temperature range. The only solution is to ensure matching of all drops. For a complex circuit with only a single metal layer available the task is difficult. In this design, matching of the 12 MSBs is achieved while drops associated with the 6 LSBs are minimized by using wide aluminum runs.

Thermal concerns are paramount since a temperature change of 0.1°C at a current source transistor will cause an output courrent change of more than one LSB. Self-heating of the bit switch transistors becomes significant and these must be placed symmetrically with respect to the current source transistor. Similarly, the digital circuitry must be placed to equalize the thermal contour at the bit current transistors. Since the digital circuitry is associated with the bit circuitry, the two can be placed together thereby evenly distributing the heat. The reference circuit is concentrated in one place and the only way to minimize its thermal contribution is to place it as far away as possible from the critical areas.

Glitching of the circuit is virtually eliminated by utilizing differential switching and by ensuring low impedance at all common nodes. In this way 16-bit performance can be achieved without deglitching.

CIRCUIT PERFORMANCE

The resulting DAC chip is 170 x 186 mils and is packaged in a 28 pin plastic double wide D.I.P. Figure 4 is an abbreviated specification table. Total harmonic distortion plus noise levels of 0.001% have been achieved at F.S.R. and a plot of full scale, THD + noise versus temperature is shown in Figure 5. This plot represents the data from five initial production units. With adjustment for the four MSBs a full scale, THD + n of less than 0.0007% has been achieved which is equivalent to 17-bit performance. Al the above measurements were made at 4 times oversampling frequency, at 8 times a very small $\simeq$ 0.0001% degradation was observed. This may well be due to digital signals coupling to the external amplifier at the higher frequency. Idle channel noise measured at bipolar zero with an OPA27 output amplifier and using an "A weight" filter is -122 dB compared to full scale.

Summarizing, an 18-bit DAC with true 16-bit performance, on board reference, and serial-to-parallel converter has been produced for the consumer marketplace.

[1] "An 18-bit D/A Converter for High Performance Digital Audio Applications" by Joel M. Halbert and Mark A. Shill, 83rd Convention Audio Engineering Society

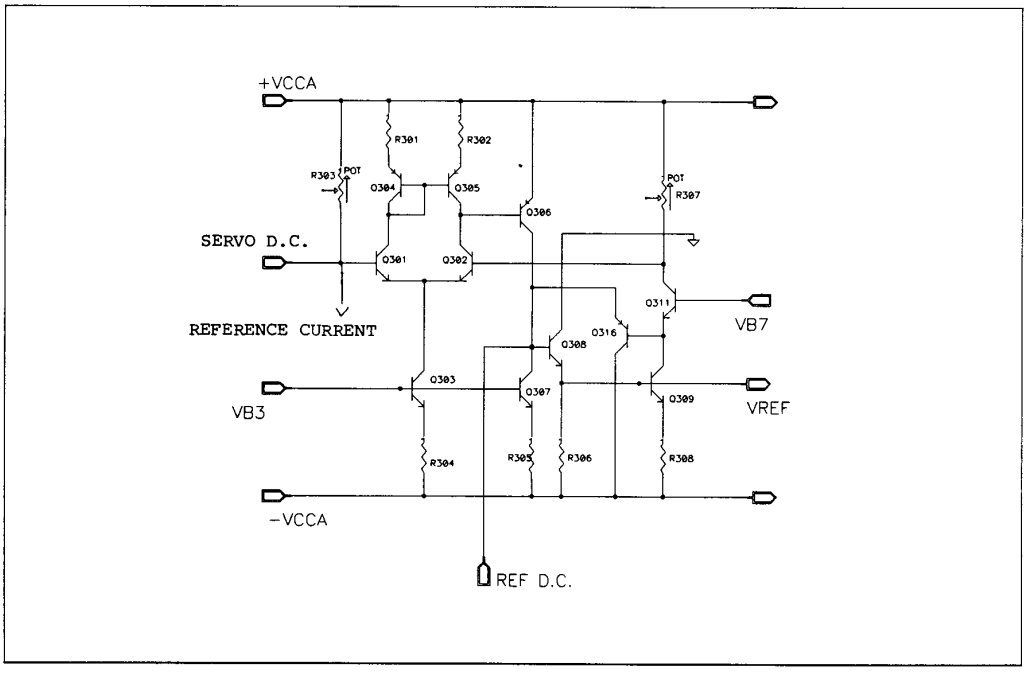

FIGURE 2

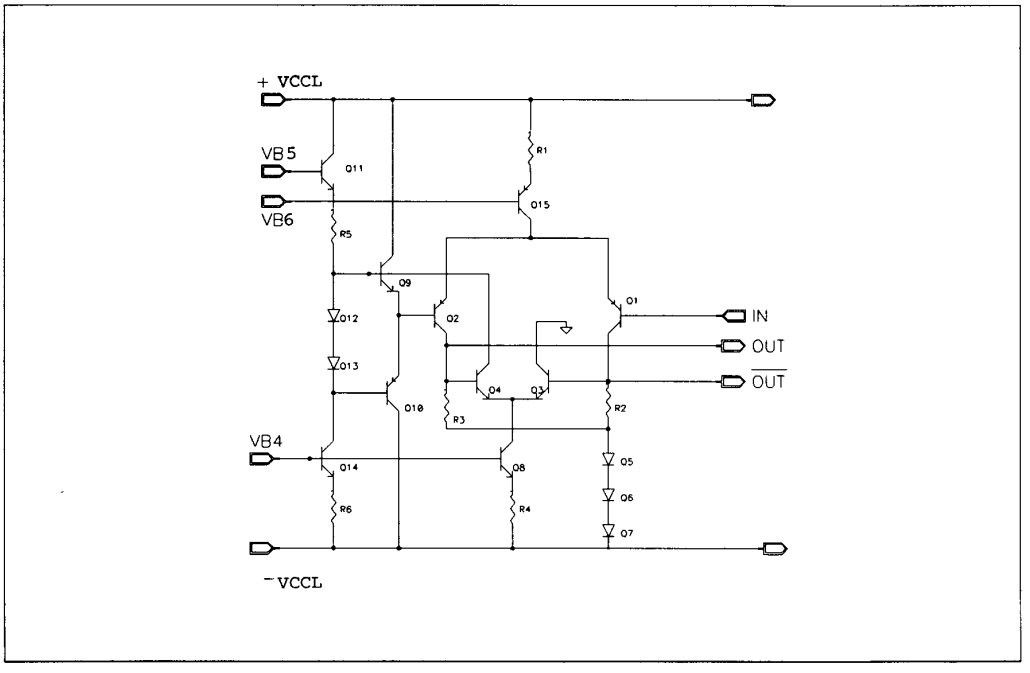

FIGURE 3

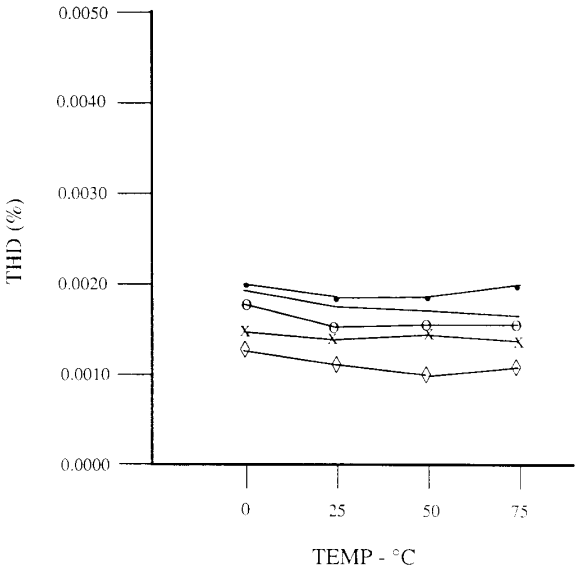

FIGURE 5

SPECIFICATION	MIN	TYP	MAX	UNITS
INPUT CLOCK FREQ	20			MHz
GAIN ERROR		±1		%
BIPOLAR ZERO ERROR		±10		µA
SIGNAL/NOISE		-120		dB
FS THD+n (K GRADE)			0.0015	%
-20 dB "			0.01	%
-60 dB "			1.0	%
POWER SUPPLY	-4.75		+5.5	V
POWER SUPPLY	-10.8		-13.2	V
POWER DISSIPATION		400		mW

FIGURE 4

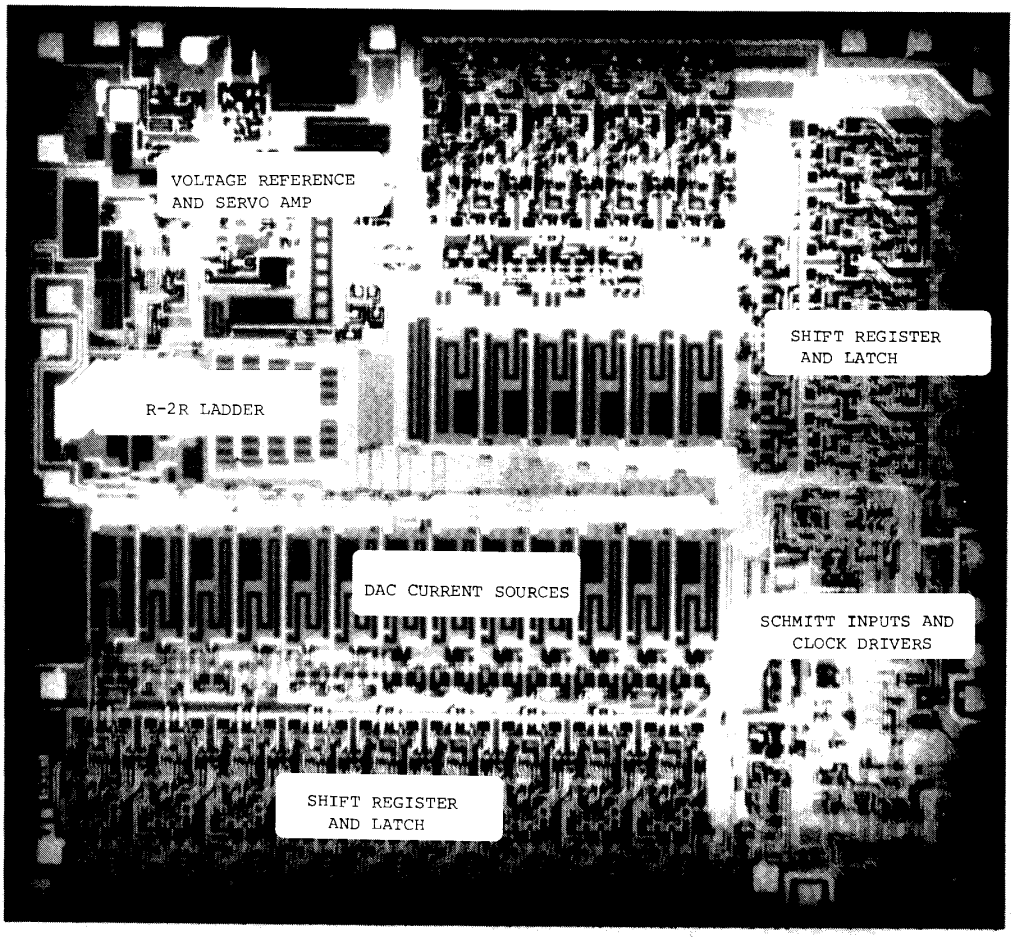

FIGURE 1