**Comments on**

# Audio Power Amplifier Design Handbook

**by Douglas Self**

Samuel Groner
February 24, 2011

## 1 Introduction

Douglas Self's writing on audio power amplifiers provides the reader with invaluable information. Not only does he teach the fundamentals (and details) of power amplifier design per se but also discloses a systematic approach to analyse the distortion performance of typical amplifier topologies. The latter is particularly important as systematics does not appear to be a natural thing in audio circuit design—at least if we consider many other publications which shall remain unnamed here. Two years ago the $5^{\text{th}}$ edition of the *Audio Power Amplifier Design Handbook* has been published as the latest book by Self on this topic, and that's the text I'm referring to below.

In recent years I've done considerable research in high performance (and in particular low distortion) amplifier topologies. This paper will highlight a couple of results from this research which complement or contrast with Self's writing. I hope that this information will be found helpful for audio circuit designers and that it will contribute to the art of power amplifier design.

For consistency with the *Audio Power Amplifier Design Handbook* I've largely adopted Self's terminology even if I've used a different nomenclature in other publications. The order of the topics discussed roughly follows the structure of Self's book. For ease of understanding, references to figures in the *Audio Power Amplifier Design Handbook* are noted as such by the addition of the corresponding page number in brackets.

At this point of writing I'd like to acknowledge the invaluable help received from Walt Jung, Bruno Putzeys, Brad Wood, and Scott Wurcer. The contributions ranged from literature suggestions, notes with regards to content, providing transistor samples to proof reading. This all is very much appreciated!

## 2 Nomenclature for Stage Counting

It should be noted that most of the opamp literature does refer to the topology shown in figure 2.1 (Self page 26) as two-stage—and not three-stage—amplifier. This is because the output stage is not thought to be fundamental for the basic operation of the amplifier, although it surely is difficult to omit in most practical circumstances. The difference in nomenclature might confuse some readers and should be mentioned. I might also add that the amplifier depicted in figure 5.10 (Self page 130) has been erroneously classified as three-stage amplifier; in fact it rather classifies as two-stage amplifier, as the folded cascode (Q4 and Q5) provides no current gain as noted by Self; it is a mere extension of the input stage rather than an independent second amplifier stage.

## 3 Improved Current Mirrors

When discussing DC acurracy of current mirrors it is important to not lose context; a crucial point is that the VAS also requires some bias current which upsets the collector current balance of the input pair. As it happens this error partially cancels with the base current errors of the basic Widlar mirror when using the standard topology considered in Self's book. Pretty accurate cancellation (which in the context of discrete design means: largely limited by transistor mismatch) can be achieved by biasing the emitter follower within the VAS at a collector current equivalent to the tail current of the input pair.

Better cancellation and more freedom for VAS biasing is achieved with the EFA mirror (figure 1). If R5 is chosen such that Q1 and Q2 are operated at equal collector voltage and R3 and R4 have equal value the error introduced by the base current of Q5 is cancelled with the base current of Q6. Overall this topology leads to very good input stage balance and offers low drift (see e.g. [1]). The use of a Wilson or improved Wilson mirror will lead to worse collector current balance for the input stage, as the VAS base current error is not cancelled. However as noted by Self on page 85 these mirrors might contribute less distortion.

Another performance aspect of current mirrors is their noise contribution. Self invariably uses 68 Ω emitter resistors for the current mirror. As detailed in [2] this value is well below the minimum value required for good noise performance. Indeed if the equivalent input noise of a model amplifier (as depicted in figure 2) is measured for various values it is seen that higher resistor values provide more than 5 dB improvement over the 68 Ω resistors. Figure 3 shows results for seven values from 10 Ω to 620 Ω as well as interpolated data. The measurements were done with a 98 Ω source impedance

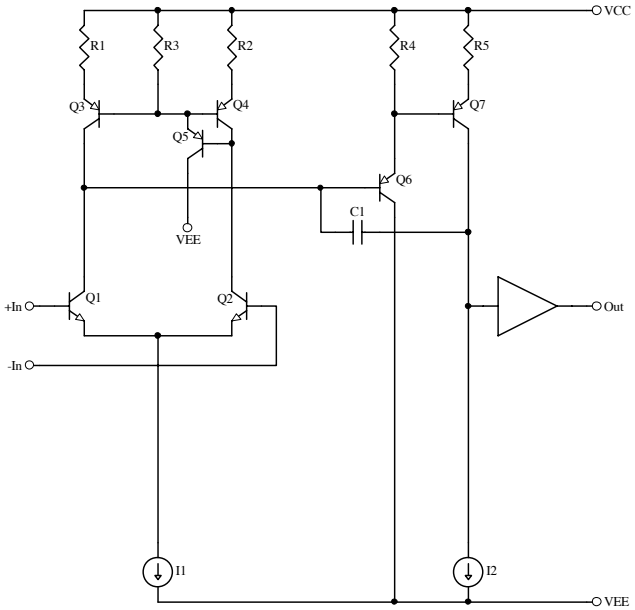


Figure 1: Amplifier with EFA current mirror.

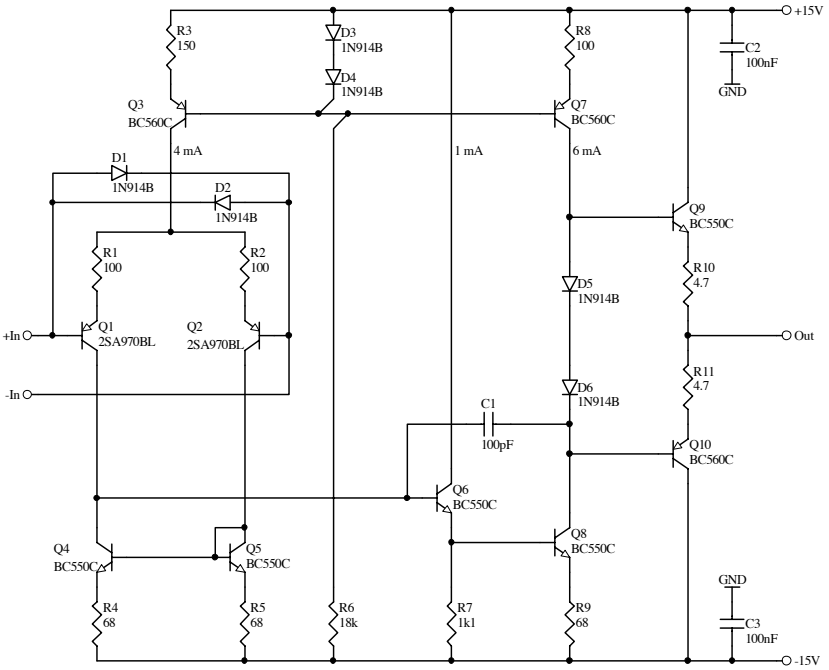


Figure 2: Model amplifier used to measure input-referred noise.

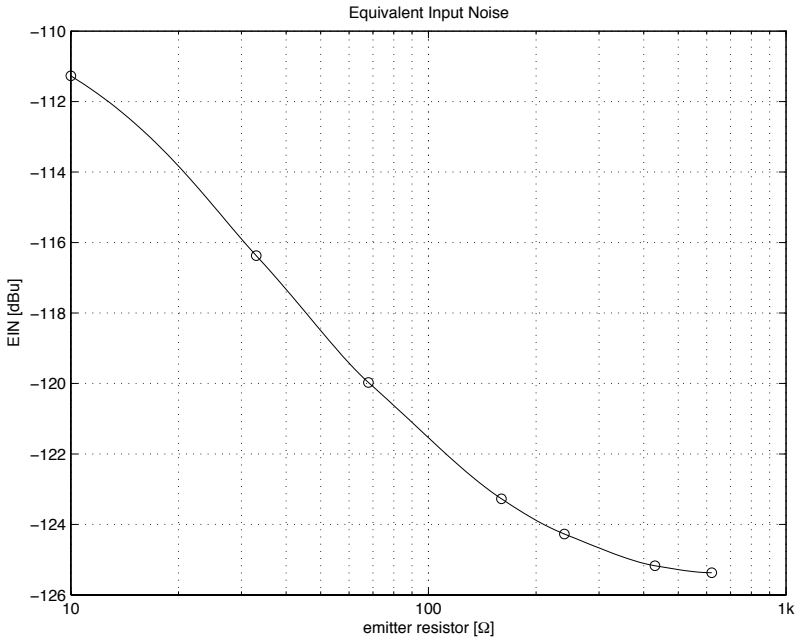


Figure 3: Equivalent input noise for a range of current mirror emitter resistor values. 22 Hz–22 kHz measurement bandwidth.

(which roughly emulates the noise contribution of the feedback network) and a measurement bandwidth of 22 Hz–22 kHz. At first it is counterintuitive that higher resistance values give lower noise, as for feedback networks and the emitter degeneration resistors of the input pair the opposite holds; however the noise contribution of the current mirror is in the form of a current, whereas the usual concern is voltage noise [3].

Figure 3 shows that even the highest resistor value of 620 Ω gives a slight advantage over the second largest (430 Ω). Higher values are not easily accomodated without further circuit changes, as already with 620 Ω the current mirror is dangerously close to saturation. However the slope of the interpolated data suggests that we can't expect further drastic reductions in noise anyway. Fortunately a value of about 300 Ω is easily implemented and gives a useful noise reduction of more than 4 dB at zero cost. A pleasing result. As often there is however a caveat: on page 263 Self notes that low current mirror emitter resistor values might be needed for best slew-rate performance, limiting the possible current mirror noise reduction. Indeed with 300 Ω emitter resistors positive slew-rate can be compromised. One possible fix for this is to add shunt capacitors in parallel with the emitter degeneration resistors; a value of 1 nF seems to be more than enough and does not compromise noise performance within the audio frequency range.

To conclude this section I'd like to add that the high sensitivity to current mirror noise contribution is a result of the heavily degenerated input stage. The reduction in transconductance which the degeneration resistors cause is accompanied by a proportional increase in sensitivity to current mirror noise. For an undegenerated bipolar input stage the detectable differences for the various emitter resistor values would be much lower.

# 4 Voltage Feedback vs. Current Feedback

High-speed circuit designers will be very familiar with the concept of current feedback operational amplifiers. In contrast to the ubiquituous voltage feedback amplifiers (which are the main focus of the book by Self) the current feedback amplifier class has the property of a closed-loop bandwidth which is to a good extent independent of closed-loop gain. Additionally typical topologies have either strongly reduced or entirely absent first-order slew-rate limits. This is achieved by making the inverting input low impedance, hence sensitive to current rather than voltage; as a result the current available to charge the compensation capacitor may be proportional to the input signal (which removes first-order slew-rate limitations) and the compensation becomes proportional to the total feedback network resistance (which achieves the constant bandwidth property). More precisely, the closed-loop bandwidth $f$ is given by:

$$f \approx \frac{1}{2\pi \cdot R_F C_C} \tag{1}$$

where $R_F$ denotes the feedback resistor and $C_C$ the compensation capacitor value. More details on the theoretical fundamentals of current feedback amplifiers may be found in [4].

I noted that the *Audio Power Amplifier Design Handbook* doesn't consider the special properties of this amplifier class. In particular for the amplifier shown in figure 4.3a (Self page 78) this results in misleading measurements. According to equation 1 the closed-loop bandwidth of this amplifier is a meagre 72 kHz[1], which is easily confirmed by simulation. It is hardly surprising that such an amplifier performs very poorly with respect to high-frequency distortion. To make a meaningful comparison to the standard voltage feedback architecture the compensation capacitor must be reduced to 10 pF or the feedback resistor scaled to 2.2 kΩ. It is clear that this change will greatly improve the linearity of the amplifier, and it is no longer obvious if a differential pair (with its even-order distortion product cancellation) offers lower distortion.

[1] This assumes a value of 100 pF for the compensation capacitor.

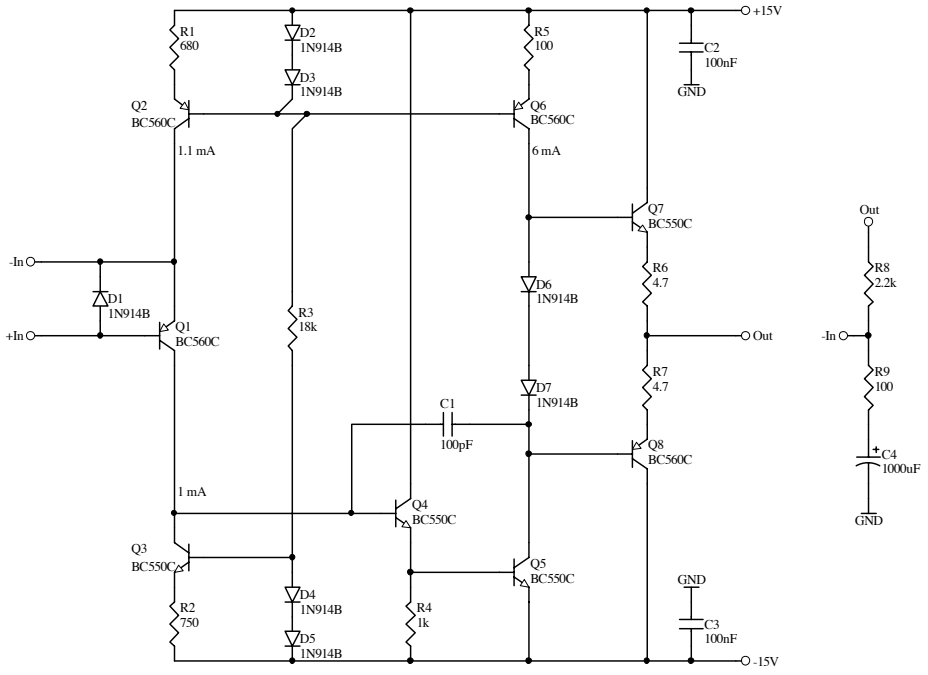


Figure 4: Model amplifier with single-ended input stage.

The amplifier shown in figure 4 implements the current feedback principle with correct compensation. Also the resistive collector load of the input pair has been replaced with an active current source and a second current source has been added to reduce DC offset. From the measurements shown in figure 5 it is clear that this amplifier still has appreciable high-frequency distortion which will be relevant for a power amplifier. However distortion is almost two orders of magnitude lower than what Self measured for the single-ended input stage (see figure 4.2, page 77). A tenfold reduction in distortion is explained by the increased loop gain; the additional distortion reduction is probably attributed to the increased input stage quiescent current and the use of an active load for the input stage.

More elaborate current feedback amplifiers use complementary input stages; one such is depicted in figure 5.14 (Self page 134). Deeper study of this amplifier reveals that Q1–Q4 effectively form a complementary emitter follower buffer and R2/R6 are used to sense the output current of this buffer. Linearity of such an input stage is not easily compared to the more traditional differential pair because of its fundamentally different operation. However it has been shown to be superior in [5] because of its absence of first-order large-signal limitations—slew-rates in excess of $500\,\mathrm{V}/\mu\mathrm{s}$ are easily achieved. Also equation 1 shows that the bias conditions of the input stage have no first-order influence on loop gain; this implies that large-signal

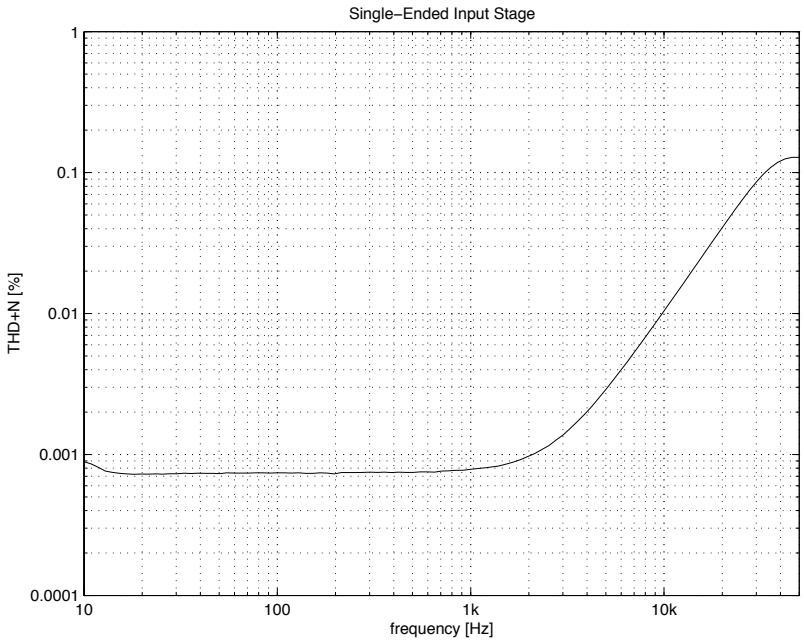


Figure 5: Distortion performance of the amplifier shown in figure 4. +20 dBu output level, 80 kHz bandwidth. The rise at frequencies below 20 Hz is due to the increasing oscillator residual contribution and not actual amplifier distortion.

conditions do not modulate open-loop gain. This is different for voltage feedback amplifiers because their loop gain is proportional to input stage transconductance. Hence appreciable lower high-frequency distortion for current feedback amplifiers is expected.

Reservations with respect to DC precision, noise, PSRR and CMRR apply to current feedback topologies but may be partially improved with more elaborate topologies [6]. A final conclusion whether voltage or current feedback topologies are more suitable for audio power amplifier design cannot be given here, as reasonably accurate discussion of the various possible current feedback architectures would probably require several weeks of research and another twenty pages of writing.

# 5 VAS Distortion

On page 64 Self correctly states that Miller compensation transfers global feedback to local VAS feedback towards higher frequencies. By the very amount that global feedback is reduced by the compensation capacitor the local VAS feedback is increased. This in turn means that the total feedback applied to the VAS remains constant. Page 120 suggests that VAS nonlinearity is a result of the basic exponential voltage-current transfer characteristics of bipolar transistors; as this characteristic can be expected to be largely independent of frequency (as is the total feedback applied to reduce it as stated above) we should expect the VAS distortion to be independent of frequency. However figure 5.2 (Self page 118) clearly shows distortion increasing with frequency.

It is obvious that we have a contradiction here, and I'd like to suggest that the exponential voltage-current transfer characteristic is not the main VAS distortion source. Page 118 correctly states that the common-emitter VAS transistor is (usually) operated in a current-driven fashion.[2] This means that the output collector current (and hence also the output voltage) is basically defined as base current (or input stage output current) times $h_{FE}$; there is no first-order distortion mechanism in this form of signal gain as long as $h_{FE}$ remains constant with collector current and collector voltage. The exponential transfer characteristic of the VAS transistor surely sets the output voltage of the input stage current mirror as function of collector current. This however has no first-order effect on the amplifier linearity (at least as long as we ignore the action of the compensation capacitor—more on this later).

[2]This also makes clear that the term *VAS* is rather inaccurate as the second amplifier stage is a transimpedance, not voltage amplifier stage.

To verify that the VAS is indeed not a standard voltage-driven common-emitter stage we may also contemplate the effect of adding an emitter resistor. If it were a voltage-driven common-emitter stage this would reduce its gain and hence total amplifier open-loop gain below the dominant pole in proportion to the resistor value. Simulation quickly reveals that the amplifier open-loop gain remains more or less constant even with large emitter resistor values.[3] Also the equation for open-loop gain below the dominant pole (as given by Self on page 62) indicates that the VAS transistor is current driven—otherwise its transconductance would be relevant and not its $h_{FE}$.

This is further supported by measurements of the amplifier shown in figure 6. Distortion has been measured with two different devices (2N4401 and MJE181) for Q7 as shown in figure 7. If the basic exponential voltage-current relationship of the bipolar transistor were the dominant distortion mechanism then both transistors should give very much identical distortion performance. Minor differences might appear due to saturation current differences or log conformance deviations. However the 6 times difference observed at 10 kHz in the measurement appears to be well beyond the expected order of magnitude of these effects. Also the exponential voltage-current relationship gives no reason why one transistor should be superior at low frequencies while the other outperforms at high frequencies.

Different $h_{FE}$ or Early voltage of the transistors used might be a reason for the distortion deviations observed; higher $h_{FE}$ or Early voltage leads to higher open-loop gain below the dominant pole and more local VAS feedback. To confirm that this does not explain the distortion difference the DC open-loop gain was measured. The observed figures were 95.6 dB for the 2N4401 and 96.2 dB for the MJE181. The tiny difference of 0.6 dB does neither explain the performance difference at low frequencies nor that at high frequencies—an unexpected result.

It's probably most easy if I proceed by just stating the three main distortion mechanisms I've been able to separate with the use of extensive simulation and measurement:

- Collector voltage dependent collector-base junction capacitance.
- Early effect.
- Nonlinear modulation of compensation capacitor reference voltage.

In the following I'll briefly discuss these three distortion mechanisms.

It is well known that the collector-base junction capacitance of a transistor shows a dependence on collector voltage [10] and that this can cause

[3] A detailed analysis [7] shows that a VAS emitter resistor reduces Early effect in the VAS transistor under certain conditions and hence can even increase open-loop gain.

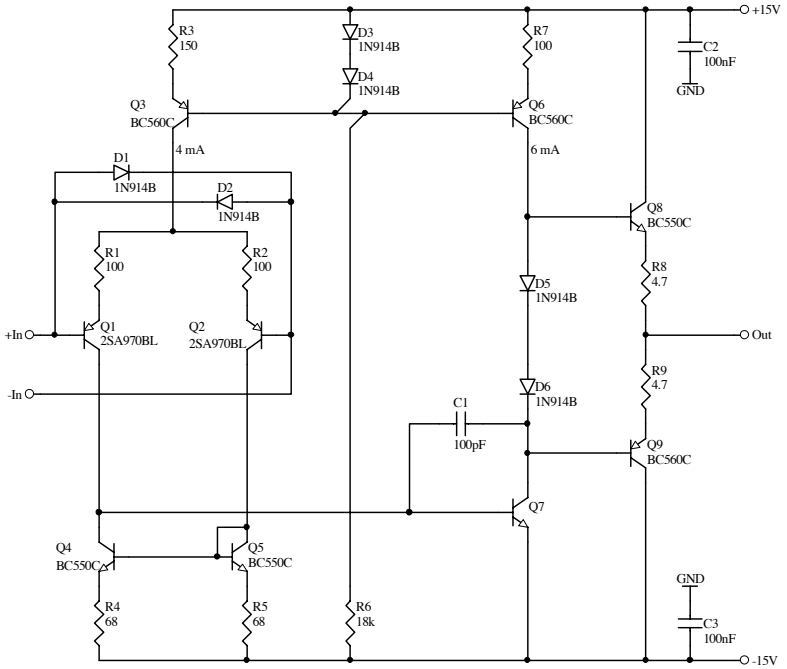


Figure 6: Model amplifier used to measure VAS distortion.

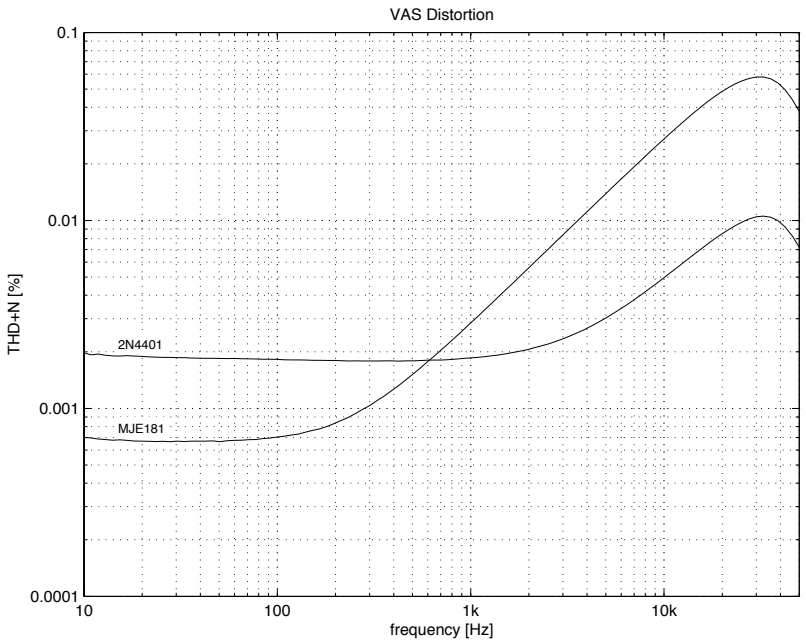


Figure 7: Distortion of the amplifier depicted in figure 6 at +20 dBu output level, 80 kHz measurement bandwidth and a noise gain of 22. Two different transistor types for Q7 were used.

distortion [11]; more precisely, the capacitance decreases at higher collector voltage. As the collector-base junction capacitance appears in parallel with the compensation capacitor it is clear that the open-loop gain above the dominant pole of the amplifier is modulated with output voltage. This necessarily modulates the closed-loop gain of the amplifier too, which is then observed as distortion. The asymmetric modulation of the junction capacitance suggests that the observed distortion must be mainly $2^{\text{nd}}$ harmonic—which is found to be true for the circuit shown in figure 6. Also as the capacitance modulation can be expected to be to a large extent independent of frequency, distortion should rise at 6 dB/octave because of falling loop gain. Again this is found to be true as shown in figure 7. Note that this distortion source is not linearised by local feedback of the compensation capacitor. Rather this distortion mechanism distorts the feedback action itself by making the feedback network component (i.e. the compensation capacitor) voltage dependent. It can hence only be linearised by global feedback.

In my experience collector voltage dependent collector-base junction capacitance is typically the dominant distortion source for frequencies above 1 kHz if a basic one-transistor VAS is used. Clearly its magnitude is proportional to the collector-base junction capacitance value; the datasheets available at the time of writing [8][9] quote a maximum value of 6.5 pF (2N4401) and 60 pF (MJE181) for collector-base junction capacitance. It is reasonable to assume that typical values will have a ratio which is roughly similar to that of the maximum values, so 9 times higher distortion for the MJE181 is expected. The measurements are in reasonable agreement with this figure.

Finally it is worth considering the effect of increased supply voltages. As stated above, the collector-base capacitance is reduced at higher collector voltages. Also for a given output level the modulation of the collector-base capacitance (i.e. the peak-to-peak capacitance value) is reduced as the greatest change in capacitance occurs at the lowest collector voltages. Hence it is reasonable to assume that distortion is reduced as well. This explains the improvement which has been observed with increased supply voltages in figure 5.2 (Self page 118).

The measurements depicted in figure 7 show frequency-independent low-frequency distortion floors which consist of a mixture of second and third harmonic distortion. This distortion is not explained by collector voltage dependent collector-base junction capacitance. However as the collector of the VAS transistor experiences large voltage swings Early effect is a strong candidate for the distortion source. For typical small-signal models Early effect is accounted for by the addition of a collector-emitter resistance $r_o$ and a collector-base resistance $r_\mu$ [10]. Their values are roughly proportional to Early voltage $V_A$ and inversely proportional to collector current $I_C$:

$$r_o = \frac{V_A + V_{CE}}{I_C} \quad (2)$$

$$r_\mu = \beta \cdot r_o \quad (3)$$

As may be seen from these equations both $r_o$ and $r_\mu$ show some dependence on collector voltage $V_{CE}$. At low frequencies we can expect $I_C$ to stay almost constant with output voltage as the impedance of the compensation capacitor, the constant current source collector load and the output stage is rather high. However the dependence on $V_{CE}$ will cause gain modulation with output voltage because $r_\mu$ appears as a local feedback element to the VAS transistor. Furthermore $r_o$ affects the effective resistance present at the VAS output node and hence again open-loop gain. As we know open-loop gain modulation will also cause some closed-loop gain modulation and hence distortion.

The distortion mechanism from $r_\mu$ is very similar to collector voltage dependent collector-base junction capacitance; the collector voltage dependent collector-base resistance $r_\mu$ appears as local VAS feedback network which modulates open-loop gain. Because of the resistive nature of this feedback network, distortion manifests itself as independent of frequency; the dominant pole compensation transfers global feedback to local VAS feedback with rising frequency but this does not affect the influence of the collector voltage dependent collector-base resistance. While the decreasing impedance of the compensation capacitor shunts the collector voltage dependent collector-base resistance and hence reduces its modulation effect, global feedback is also proportionally reduced, which brings the resulting distortion up again. As result distortion independent of frequency is observed.

Now we need to appreciate that equations 2 and 3 are substantial simplifications from the real world; $r_o$ and $r_\mu$ are in fact far stronger functions of collector voltage. At low collector voltages quasi-saturation effects (the so-called *Kirk effect*) occur and at high voltages weak breakdown effects start to affect transistor operation [12]. Both lead to reduced effective values of $r_o$ and $r_\mu$ and substantial additional distortion which is not considered in the basic Gummel-Poon model and hence not accurately reproduced in standard SPICE implementations. Detailed insight into these mechanisms is not easily found in the available literature. [13][14] at least give data for low collector voltages up to 6 V, although these are high speed transistors with presumably quite different characteristics from discrete high voltage transistors used in power amplifiers.

In any case it is very instructive to measure the DC open-loop gain of the amplifier shown in figure 6 as function of output voltage (figure 8 and 9) as well as the resulting low-frequency distortion spectrum (figure 10 and

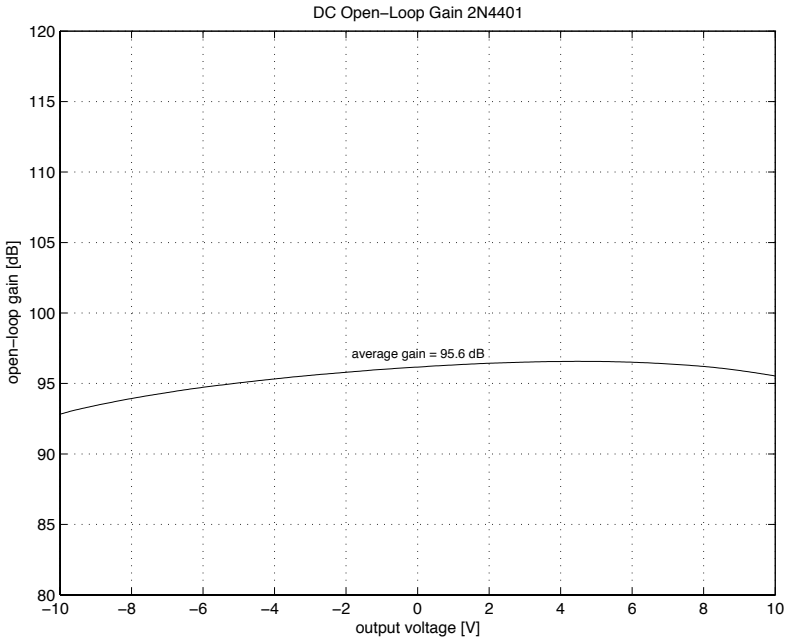


Figure 8: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a 2N4401 transistor type.

11). As noted before and depicted in figures 8 and 9 both the 2N4401 and MJE181 transistor give near-identical average open-loop gain. However the 2N4401 transistor type shows more variation with output voltage which explains the higher low-frequency distortion. As the MJE181 has a higher breakdown voltage rating as the 2N4401 (40 V vs. 60 V) it seems reasonable to assume that weak breakdown will occur much later (i.e. at higher collector voltages) and hence affect circuit operation less; also quasi-saturation is an effect which becomes more pronounced at collector currents which are high relative to the collector current rating—in other words transistors with low maximum collector current typically show the onset of quasi-saturation at lower collector currents than transistors with high maximum collector current. As the MJE181 is rated for much higher collector currents than the 2N4401 (600 mA vs. 3 A) quasi-saturation effects are expected to have comparably less effect at the given collector current of 6 mA. These explanations are in agreement with the low-frequency distortion differences observed between the two transistors; however they must remain speculative to some extent as the exact details of the collector voltage dependence of $r_o$ and $r_\mu$ is unknown.

As shown in equations 2 and 3 both $r_o$ and $r_\mu$ are inversely proportional to collector current; hence low-frequency distortion inversely proportional to collector current is expected. Figure 12 shows distortion measurements of the

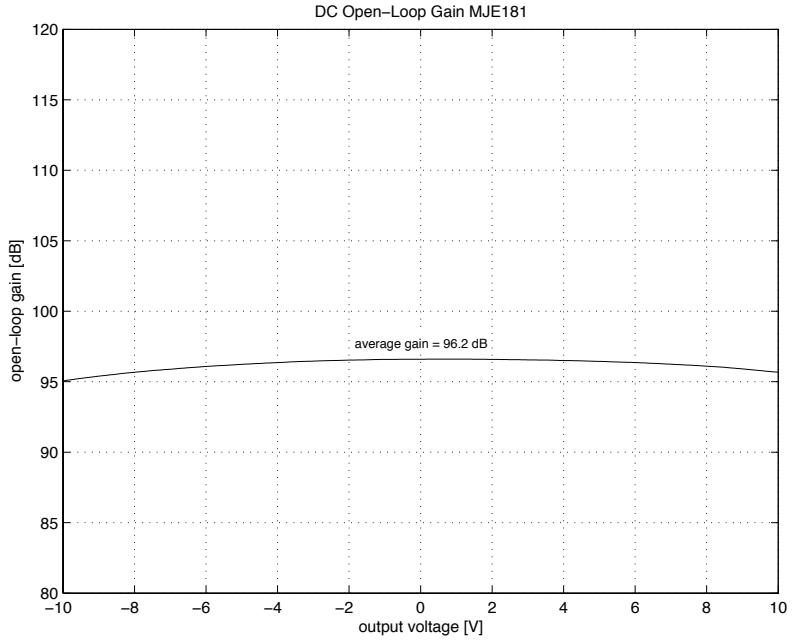


Figure 9: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a MJE181 transistor type.

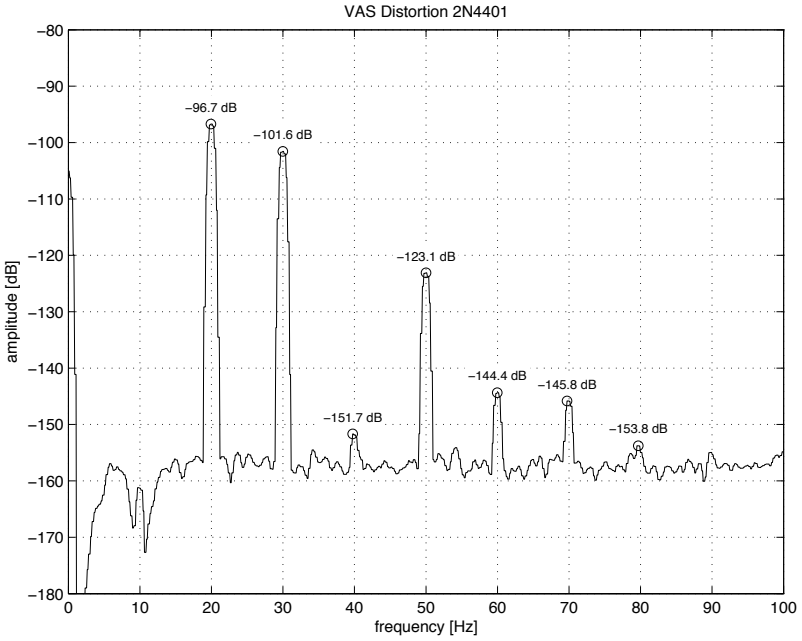


Figure 10: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a 2N4401 transistor type.

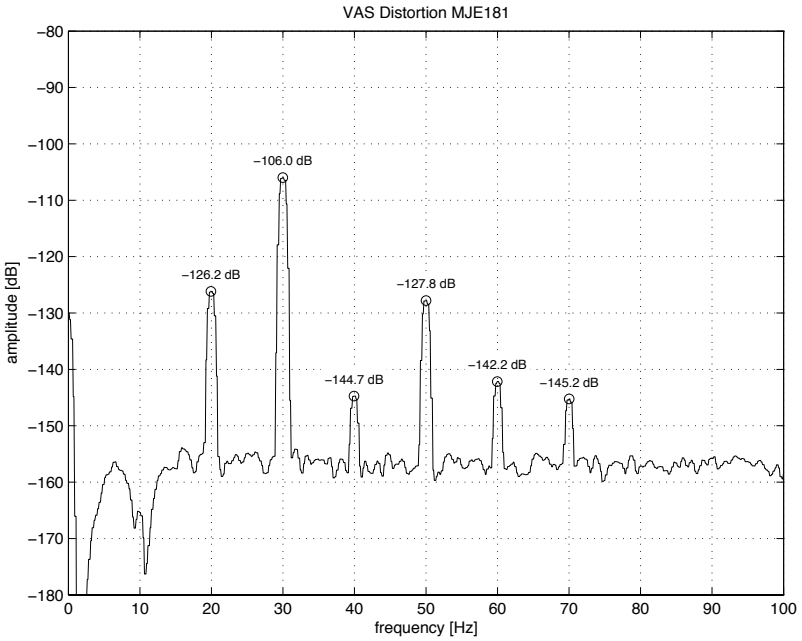


Figure 11: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a MJE181 transistor type.

amplifier shown in figure 6 with the VAS collector current varied from 3 mA to 12 mA. As predicted, low-frequency distortion approximately doubles for every doubling of collector current, indicating that the attribution of this distortion to Early effect is correct. High-frequency distortion is hardly affected as the junction capacitances are determined mainly by transistor geometry and are only a weak function of collector current; the lower distortion above 15 kHz and the dip at 1 kHz which is observed for the 12 mA collector current measurement can probably be attributed to cancellation effects between Early effect and collector-base junction capacitance modulation.

To further investigate distortion from voltage-dependent collector-base capacitance and Early effect several other transistor types were measured. These measurements are depicted in figures 13–33.

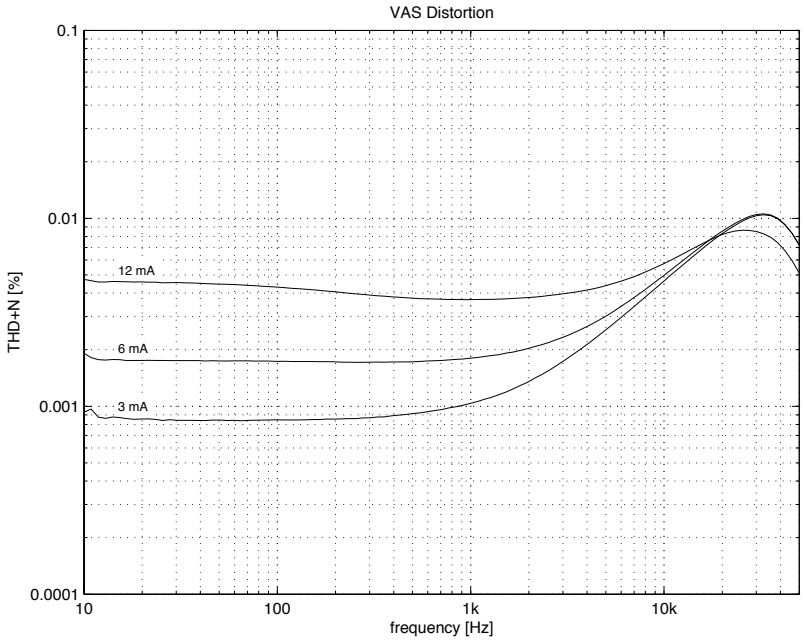


Figure 12: Distortion of the amplifier depicted in figure 6 at three different VAS collector currents. Measured at +20 dBu output level and with a 80 kHz measurement bandwidth. Q7 was a 2N4401 transistor type.

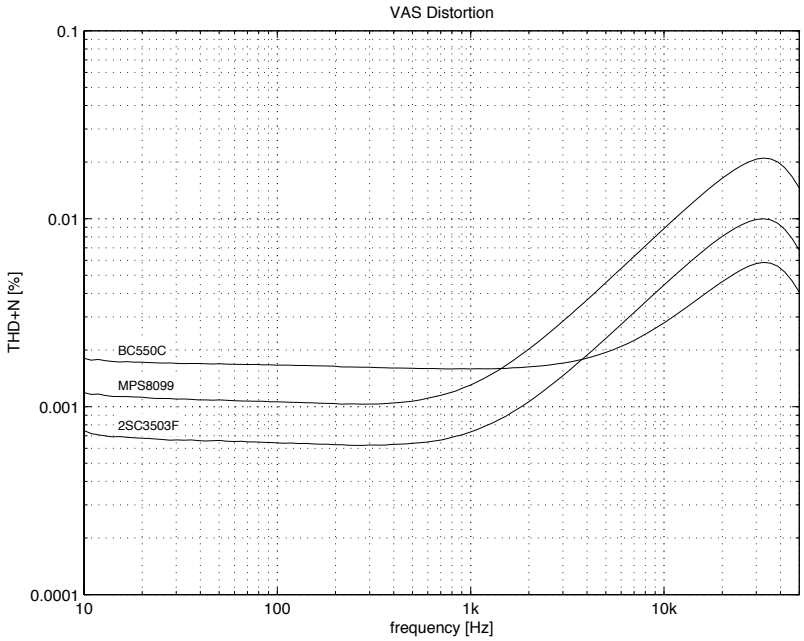


Figure 13: Distortion of the amplifier depicted in figure 6. Three different transistor types for Q7 were used.

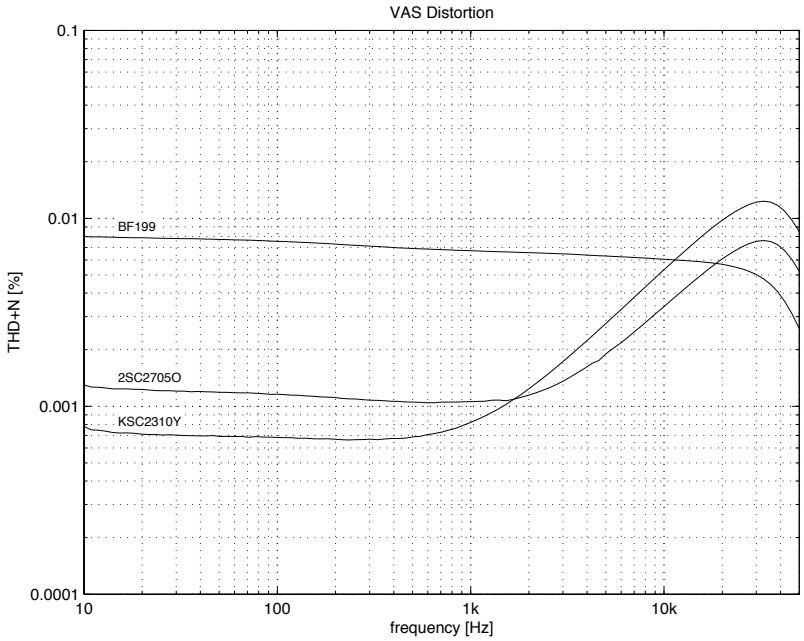


Figure 14: Distortion of the amplifier depicted in figure 6. Three different transistor types for Q7 were used.

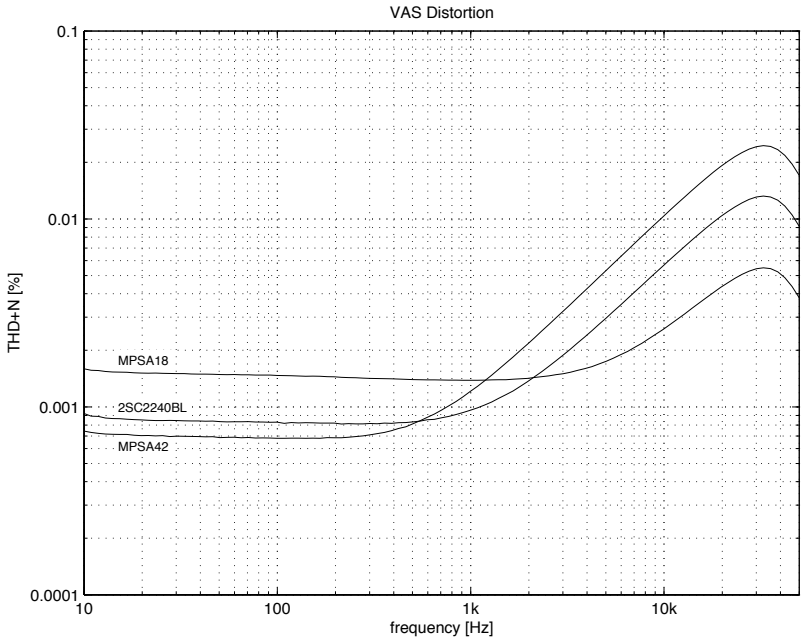


Figure 15: Distortion of the amplifier depicted in figure 6 at +20 dBu output level and 80 kHz measurement bandwidth. Three different transistor types for Q7 were used.

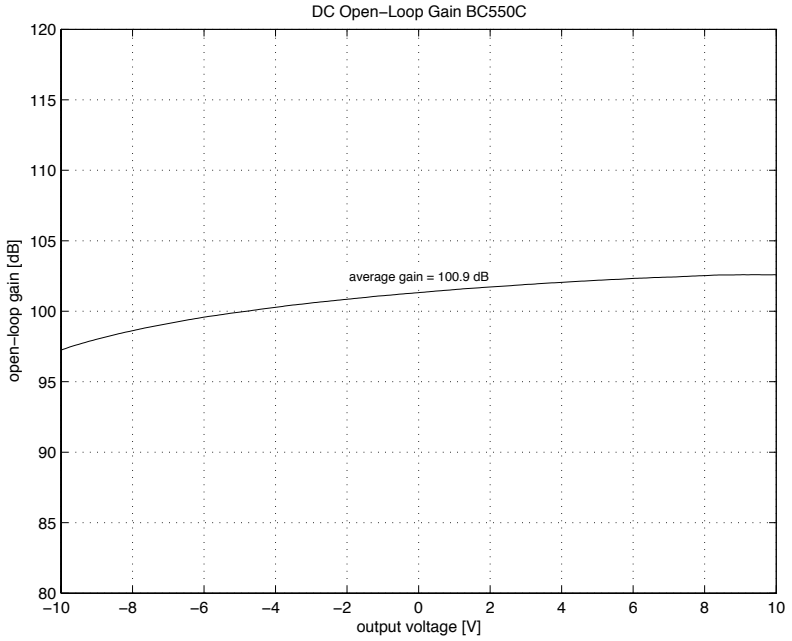


Figure 16: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a BC550C transistor type.

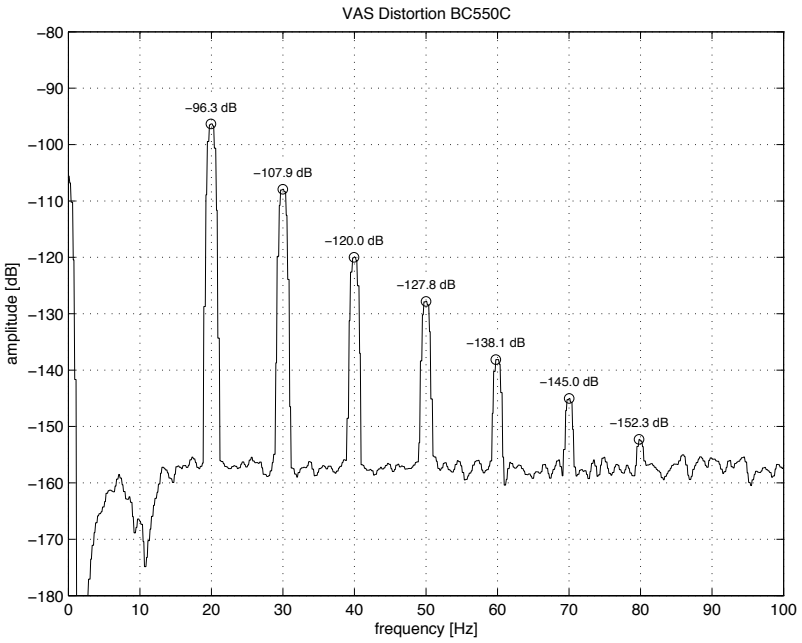


Figure 17: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a BC550C transistor type.

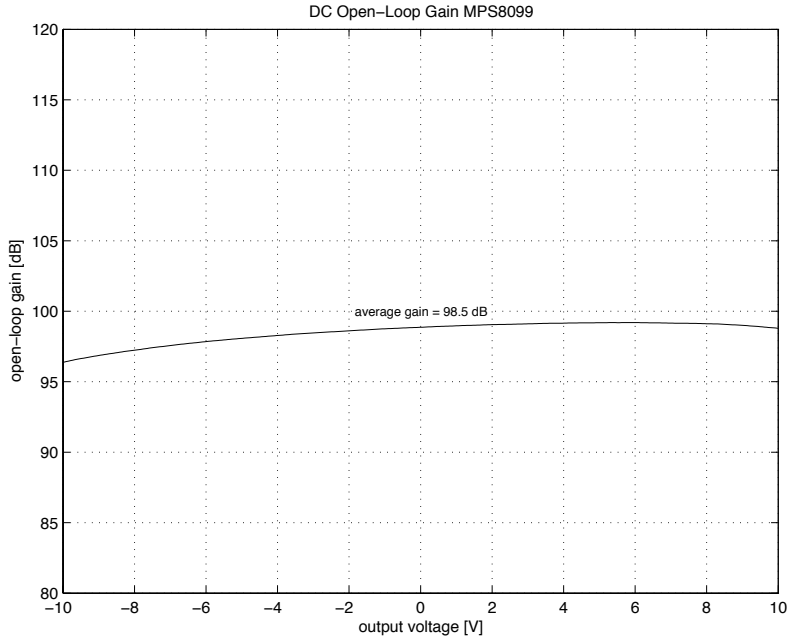


Figure 18: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a MPS8099 transistor type.

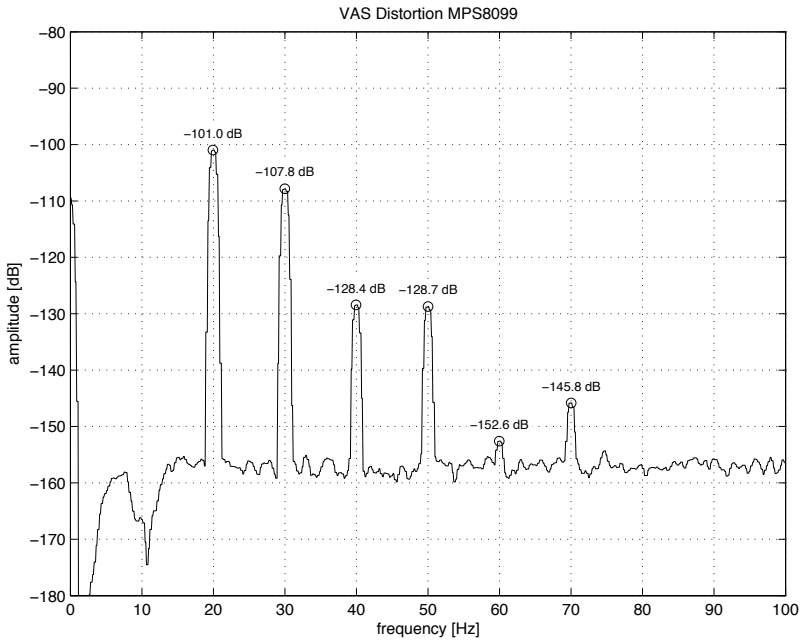


Figure 19: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a MPS8099 transistor type.

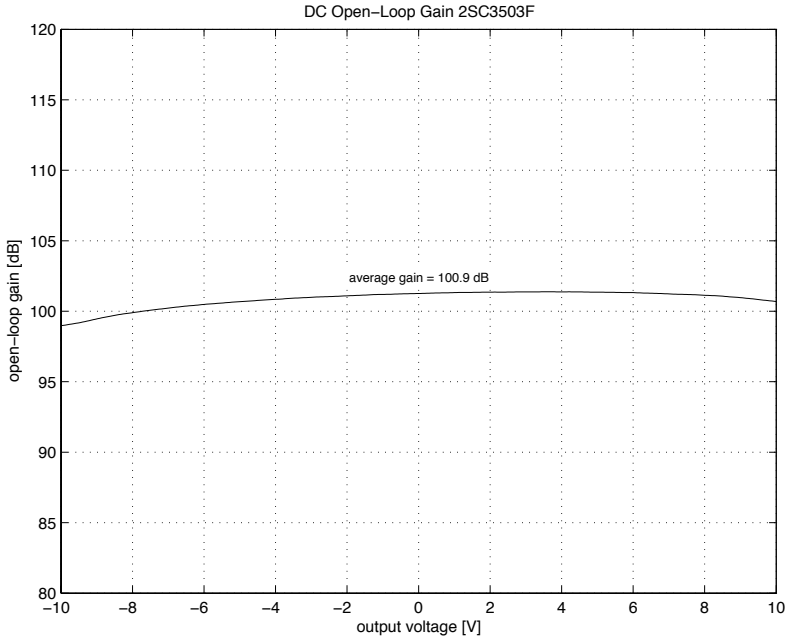


Figure 20: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a 2SC3503F transistor type.

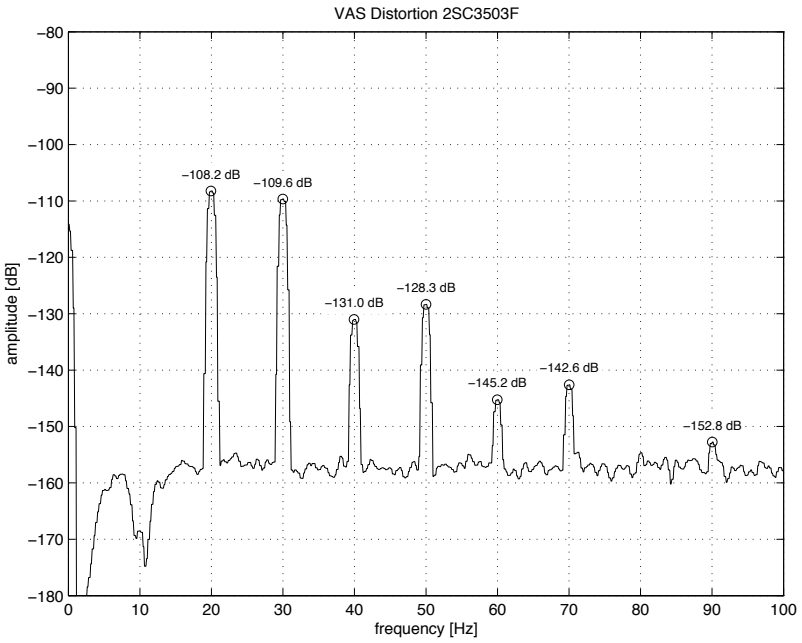


Figure 21: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a 2SC3503F transistor type.

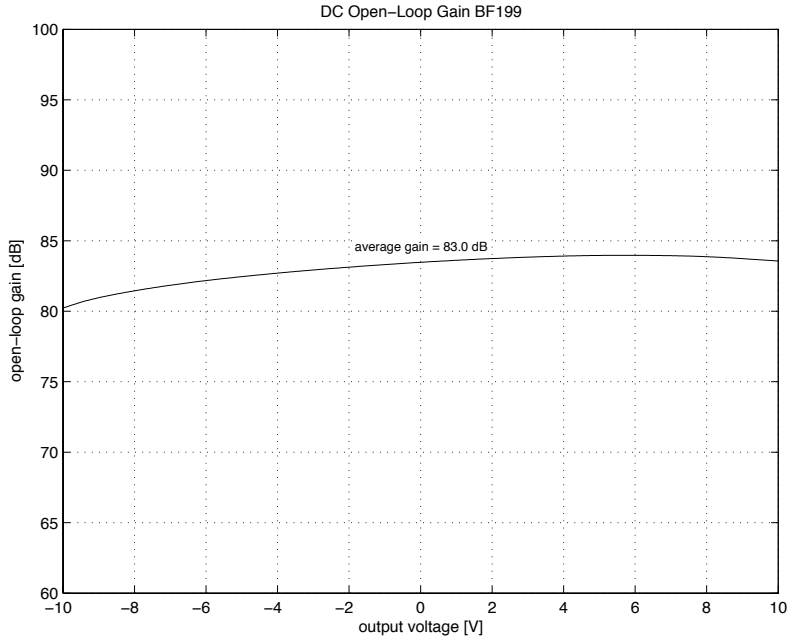


Figure 22: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a BF199 transistor type.

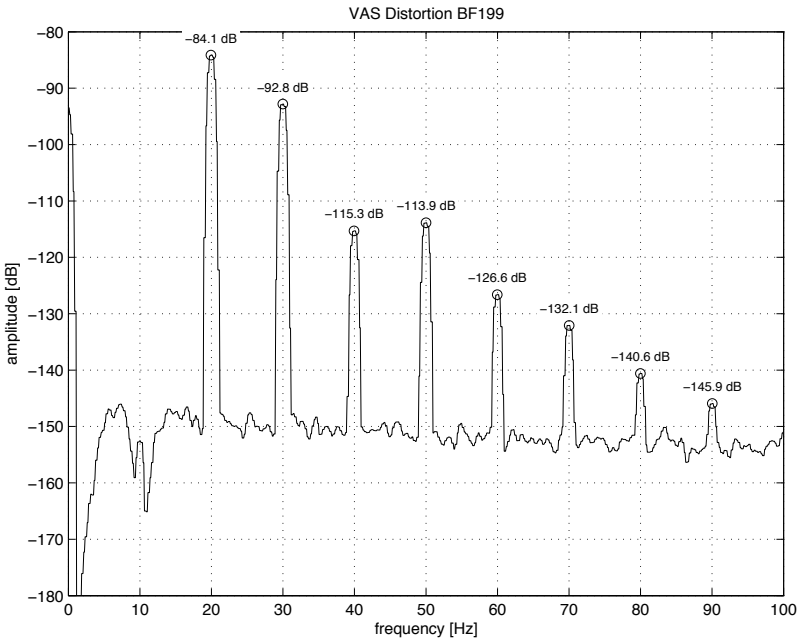


Figure 23: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a BF199 transistor type.

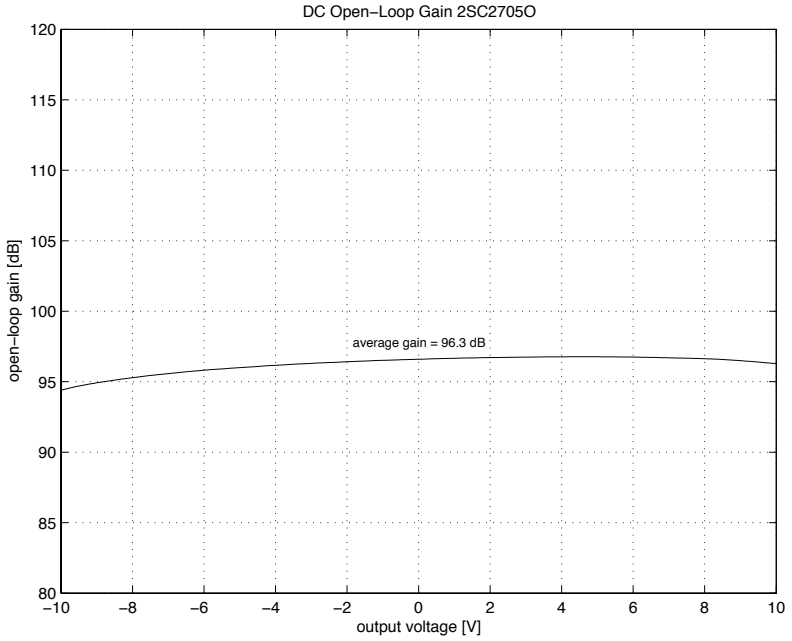


Figure 24: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a 2SC2705O transistor type.

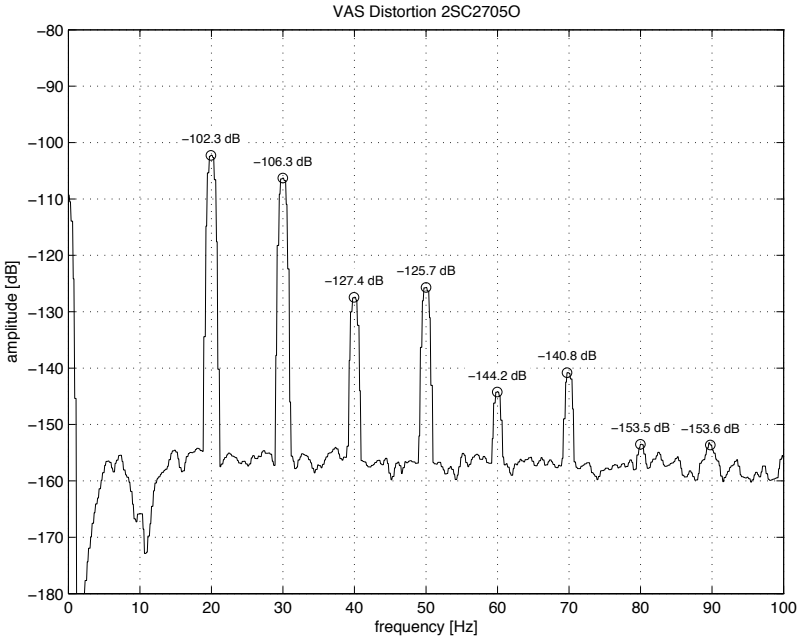


Figure 25: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a 2SC2705O transistor type.

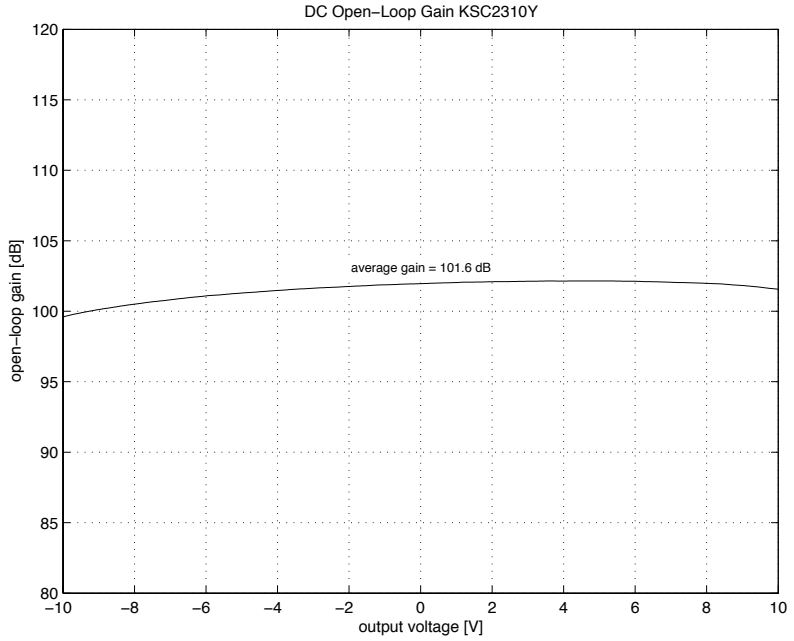


Figure 26: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a KSC2310Y transistor type.

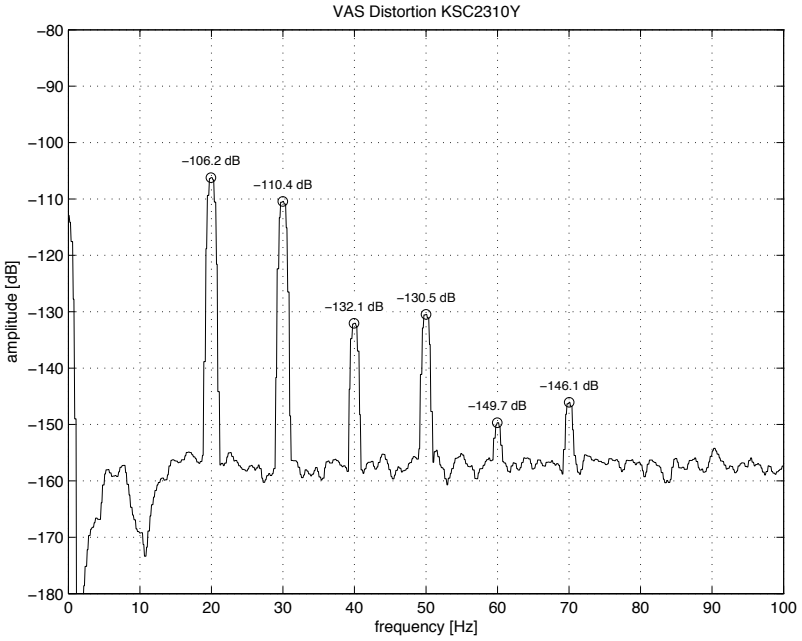


Figure 27: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a KSC2310Y transistor type.

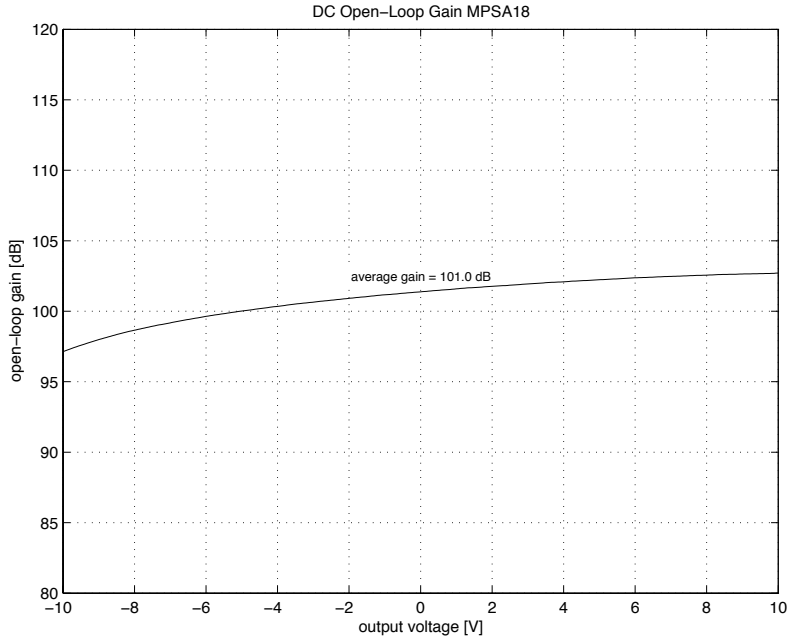


Figure 28: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a MPSA18 transistor type.

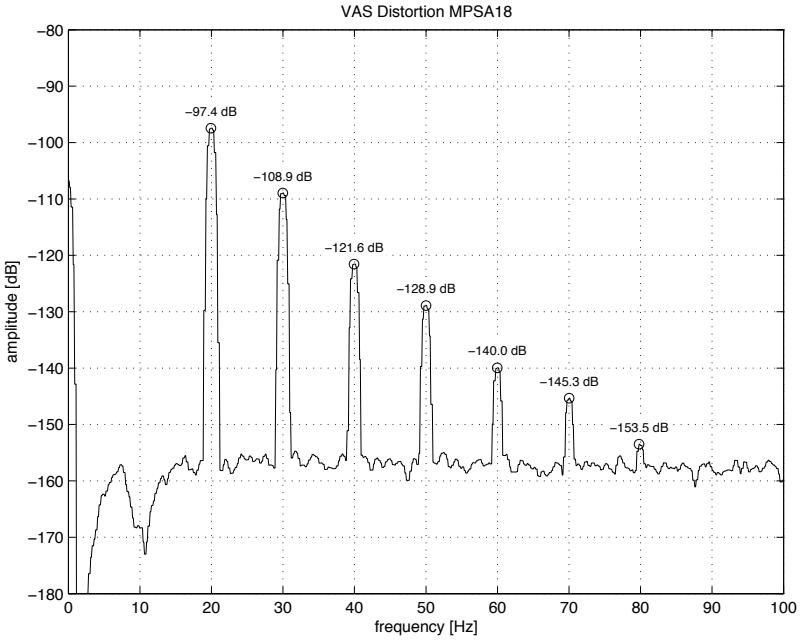


Figure 29: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a MPSA18 transistor type.

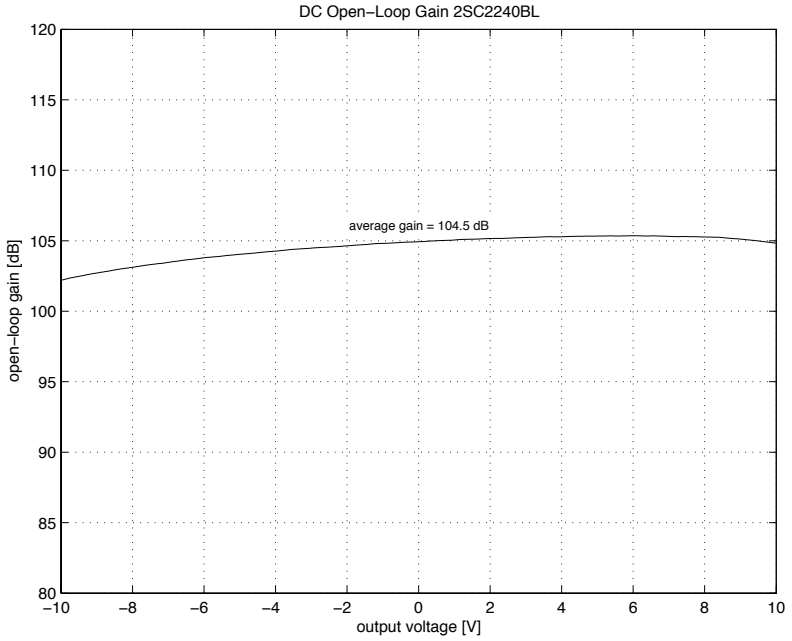


Figure 30: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a 2SC2240BL transistor type.

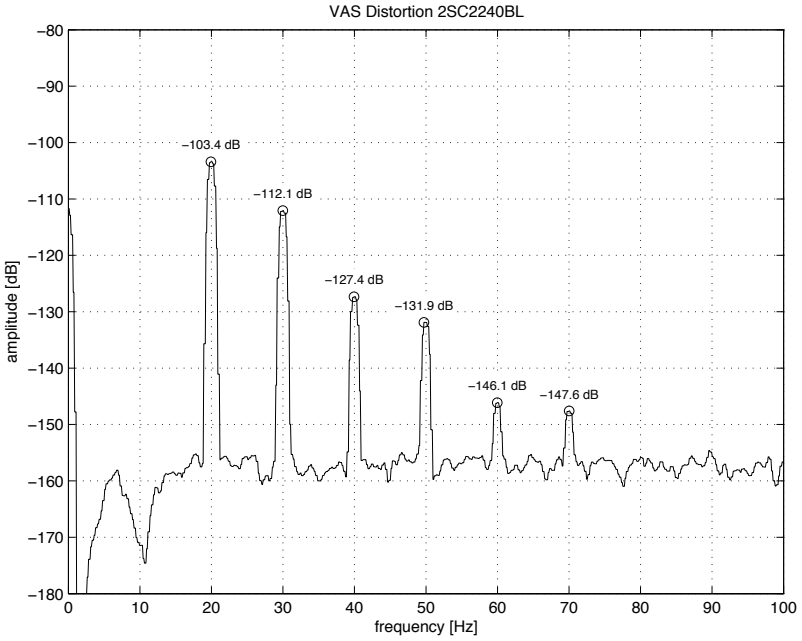


Figure 31: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a 2SC2240BL transistor type.

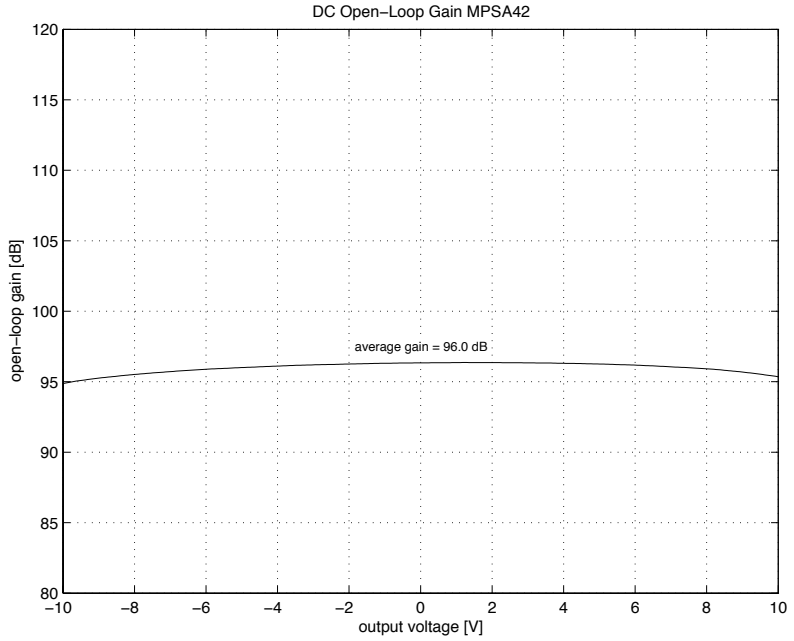


Figure 32: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a MPSA42 transistor type.

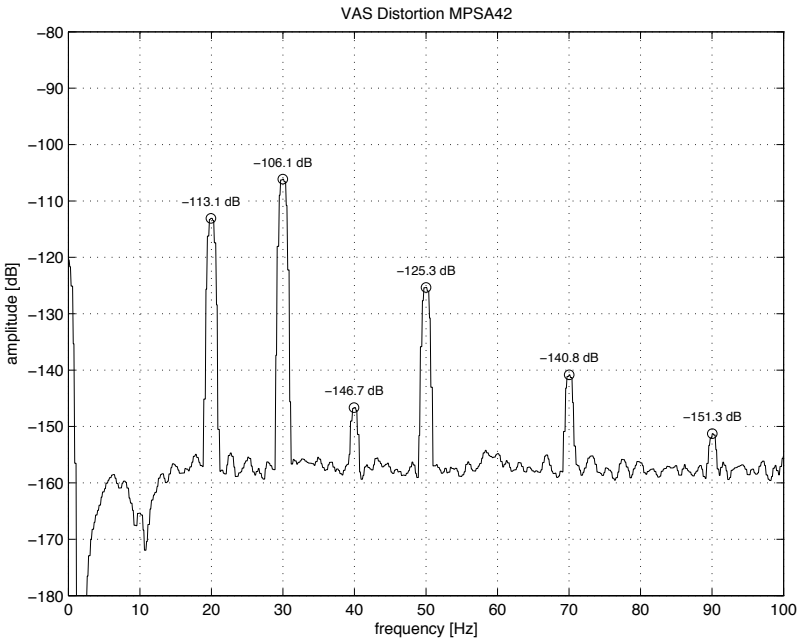


Figure 33: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a MPSA42 transistor type.

Each of these transistors shows a quite unique distortion characteristic and we may wonder about the procedure to select an optimum VAS transistor. To minimise distortion at high frequencies things are clear—the VAS transistor should have as low as possible collector-base junction capacitance. At low frequencies optimum choice is less easy; to maximise $r_o$ the transistor should have high Early voltage. Maximisation of $r_\mu$ additionally asks for high $h_{FE}$ and it is not entirely clear which parameter is more important. Furthermore we don't just want $r_o$ and $r_\mu$ to show high values but also a low dependence on collector voltage; understanding of the exact transistor physics which affects this is surely beyond a typical audio power amplifier design job.

To derive a practical design guideline I was looking for a parameter with good correlation to low-frequency distortion; Early voltage is an obvious candidate. However Early voltage is not usually stated in datasheets. Hence I decided to alternatively use the collector-emitter breakdown rating $V_{CEO}$ which is available in every datasheet and which can be expected to have a reasonable correlation to Early voltage. Figure 34 plots $V_{CEO}$ and THD at 10 Hz (calculated from the distortion spectrum plots as shown above) for the eleven transistor types whos distortion performance was shown above. When plotted on a logarithmic scale the correlation between high breakdown rating and low distortion becomes very obvious and confirms the assumptions regarding importance of Early effect.

Now we may also wonder about the correlation of low-frequency distortion with $h_{FE}$. For this the $h_{FE}$ of the eleven transistor specimens were measured at a meaningful operating point (i.e. at a collector current of 6 mA and a collector-emitter voltage of 15 V); the results are shown in figure 35. Surprisingly $h_{FE}$ is negatively correlated with low distortion. This however is not a fundamental contradiction to the used transistor theory but rather a result from the fact that transistors with high breakdown rating tend to have much lower $h_{FE}$. Apparently the distortion reduction which results from higher Early voltage is more important than the penalty we get from decreased $h_{FE}$.

[7][10] suggest a *figure of merit* for VAS transistors given by $h_{FE} \cdot V_A$ (actually used here is $h_{FE} \cdot V_{CEO}$). The correlation of this figure with low-frequency distortion is given in figure 36. However correlation of this figure of merit with low distortion appears to be no better (if not even worse) than the correlation of $V_{CEO}$ alone; so we're put back to the point where we may say that for low low-frequency distortion, high breakdown voltage is a primary, and high $h_{FE}$ only a secondary consideration.

Curiosity led me to also consider MOSFETs as VAS transistors; their very high drain-gate and source-gate resistance promises low low-frequency distortion. At the same time typical parts have substantial values of drain-gate capacitance which should result in considerable high-frequency distortion.

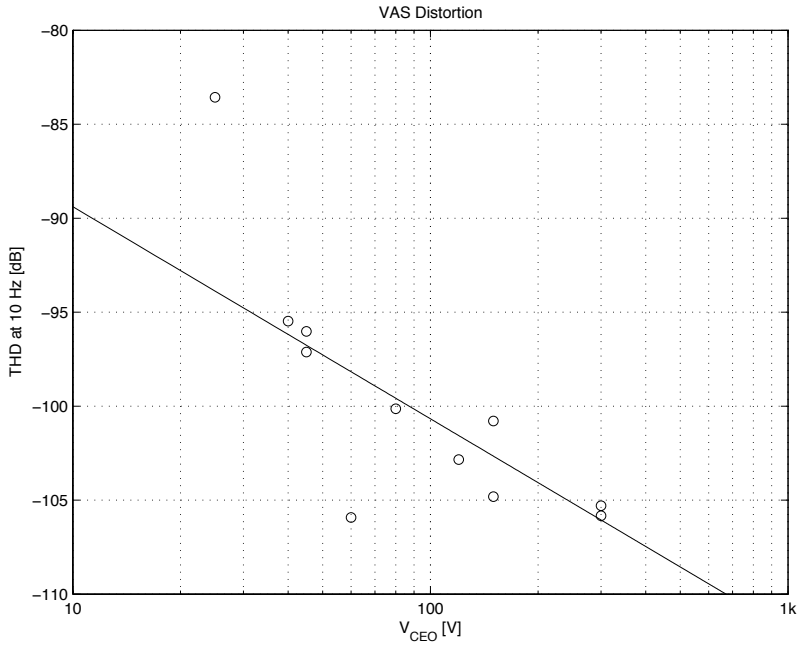


Figure 34: Correlation of low-frequency distortion with transistor breakdown rating.

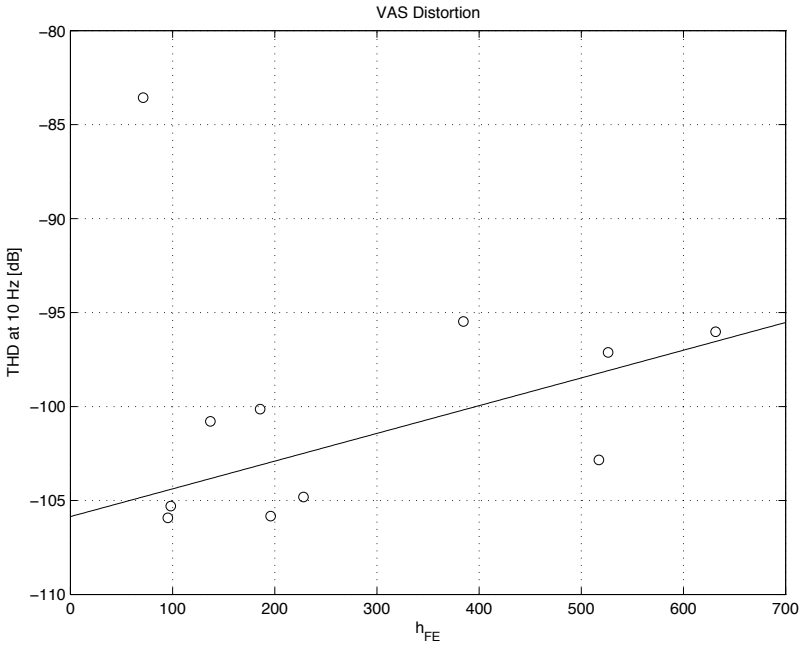


Figure 35: Correlation of low-frequency distortion with $h_{FE}$.

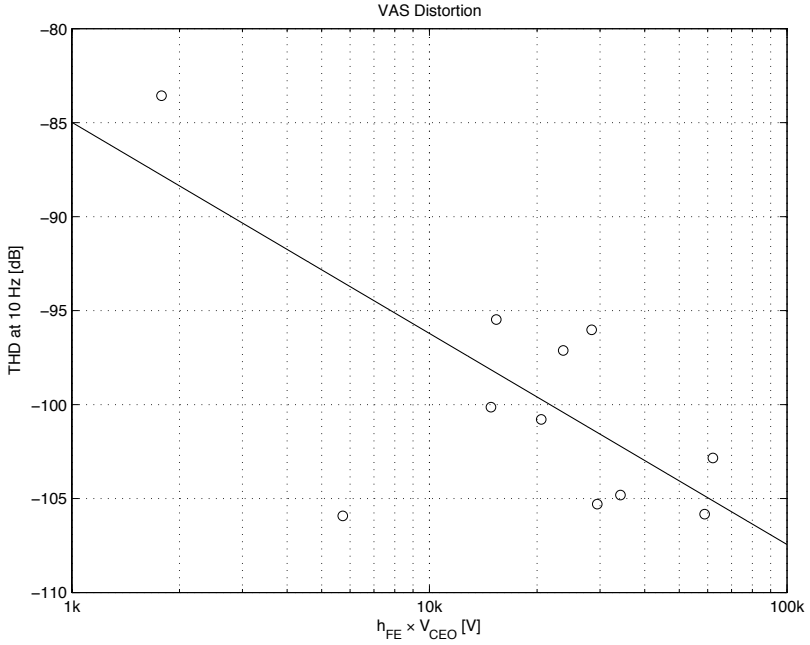


Figure 36: Correlation of low-frequency distortion with the figure of merit $h_{FE} \cdot V_{CEO}$.

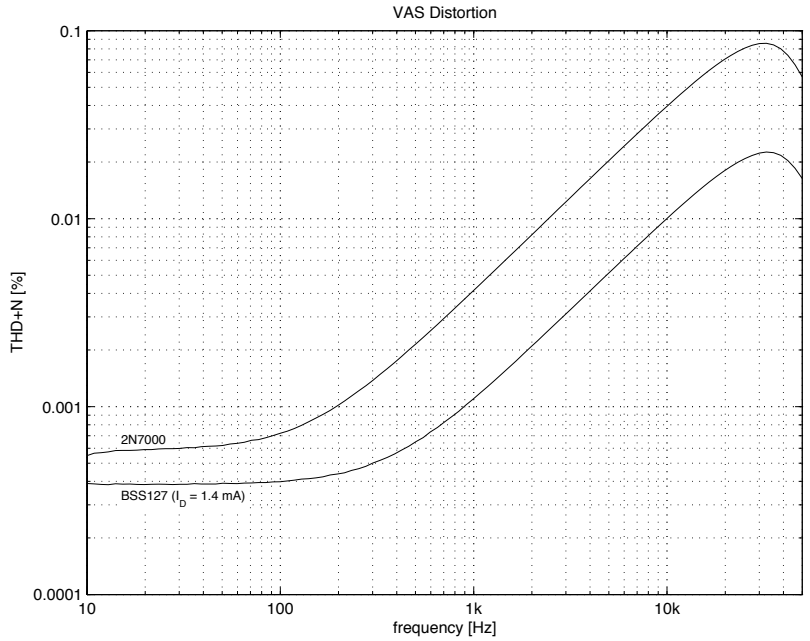


Figure 37: Distortion of the amplifier depicted in figure 6 at +20 dBu output level and 80 kHz measurement bandwidth. Two different transistor types for Q7 were used.

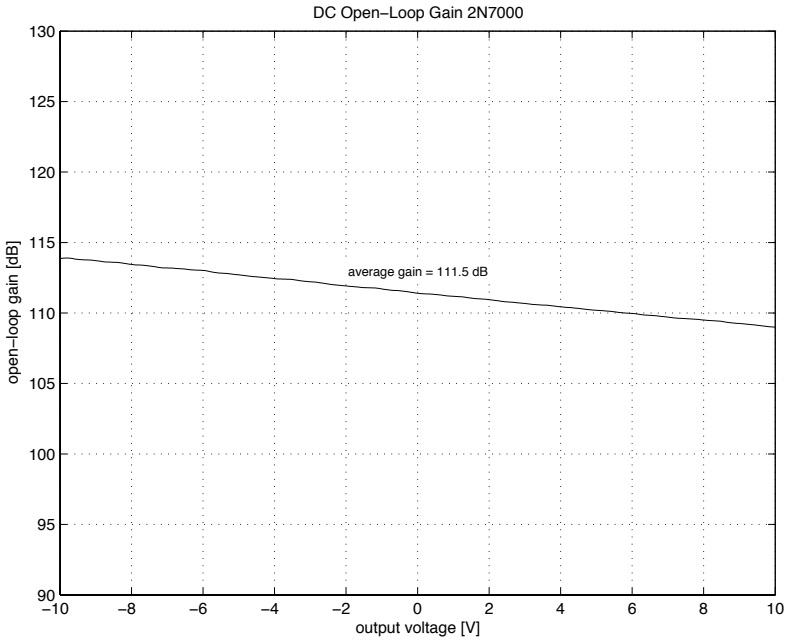


Figure 38: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a 2N7000 MOSFET type.

Figure 37 confirms these predictions for the 2N7000. Measurements of the BSS127 transistor are also included; its very small geometry substantially reduces junction capacitances which results in a proportional reduction in high-frequency distortion. However the corresponding high drain resistance drastically reduces maximum negative voltage swing; the VAS quiescent current had to be reduced to 1.4 mA for meaningful measurements. Along with the low power capability of this transistor, this defeats its use as VAS transistor for power amplifiers, as higher quiescent currents are needed for sufficient output stage drive capability.

DC open-loop gain and low-frequency distortion spectra were measured for these devices as well—corresponding figures are 111.5 dB (2N7000) and 132.1 dB (BSS127). The DC open-loop gain modulation with output voltage is distinctly different than for bipolar transistors. As shown for the 2N7000 transistor in figure 38 open-loop gain continuously falls towards positive output voltages without any sign of a symmetrical component. Consequently the low-frequency distortion residual is strongly dominated by the $2^{\text{nd}}$ harmonic as depicted in figure 39. The behaviour of the BSS127 is similar, although shifted towards much higher average open-loop gain (figure 40 and 41).

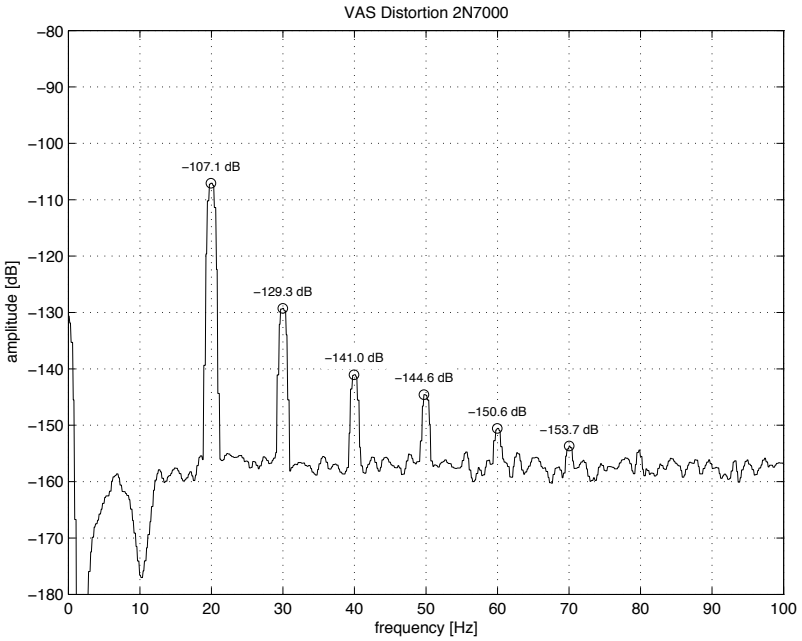


Figure 39: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a 2N7000 MOSFET type.

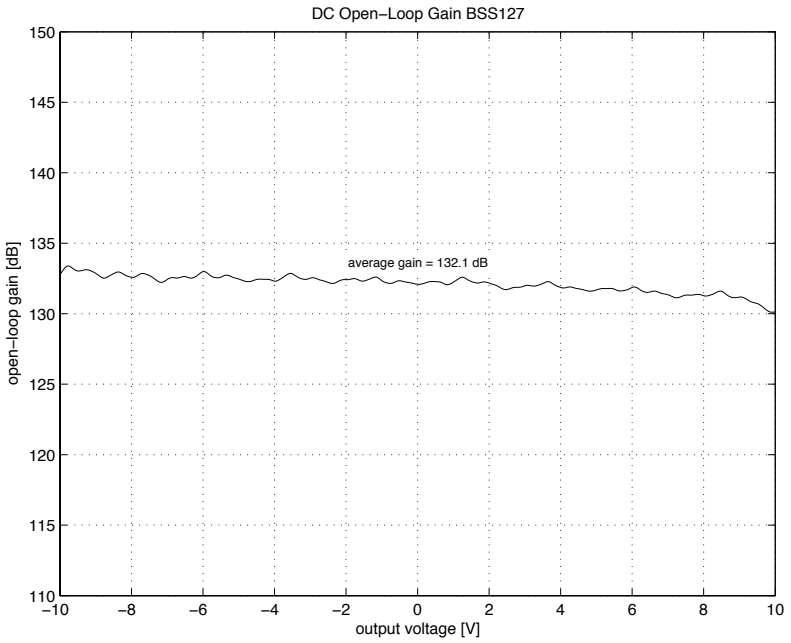


Figure 40: DC open-loop gain of the amplifier depicted in figure 6; Q7 was a BSS127 MOSFET type and VAS quiescent current was reduced to 1.4 mA.

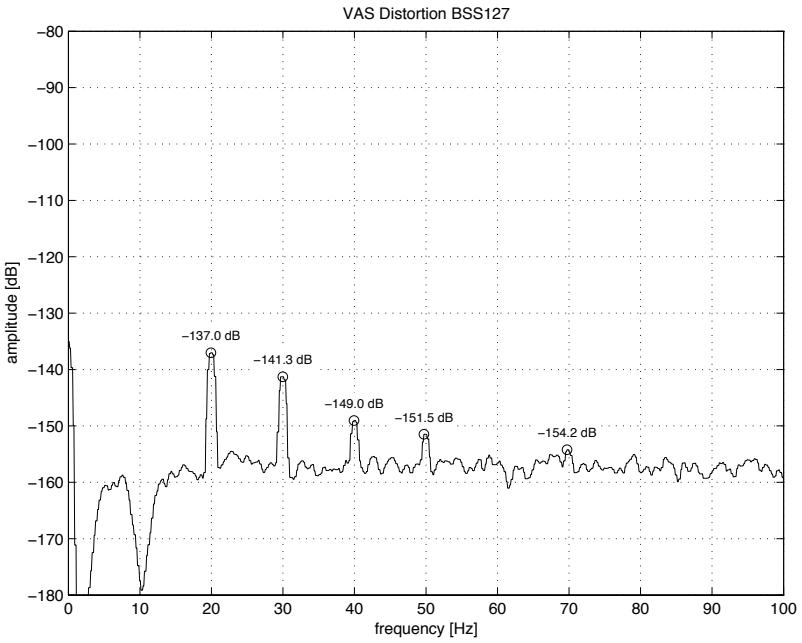


Figure 41: 10 Hz distortion spectrum of the amplifier depicted in figure 6; Q7 was a BSS127 MOSFET type and VAS quiescent current was reduced to 1.4 mA.

To my best knowledge no MOSFET device is currently available which would simultaneously offer low junction capacitances, low drain resistance, high breakdown voltage and sufficient power capability. Hence the bipolar transistor appears to be the more adequate choice.

The last VAS distortion mechanism to be discussed in detail is a more subtle one. As mentioned by Self the Miller compensation applies local feedback to the VAS which increases with frequency. Any feedback needs to be referenced to some voltage; for global feedback this is typically the ground voltage. In the case of local VAS feedback it is the base voltage of the VAS transistor. Unfortunately this voltage is not constant; rather it is both a function of $V_{be}$ and supply voltage. The later dependence causes a PSRR reduction as detailed by Self on page 293ff.

The dependence on $V_{be}$ implies that the reference voltage of the local VAS feedback is dependent on the collector current of the VAS transistor. As the voltage-current relationship is an exponential one it is clear that the reference voltage must carry a significant $2^{\text{nd}}$ harmonic distortion component even if the collector current is an undistorted sine wave. These are superimposed on the VAS output voltage by means of local feedback of the compensation capacitor, and this at a rate increasing with 6 dB/octave if we assume standard Miller compensation. Again, this distortion mechanism is not reduced by local feedback from the compensation capacitor; rather it is the local feedback which superimposes the distorted voltage from the VAS transistor base to the output voltage.

Due to the exponential voltage-current law, increasing the quiescent collector current of the VAS reduces the amount of $V_{be}$ modulation. Hence lower distortion is expected. To measure this effect the amplifier depicted in figure 42 was used. It incorporates a VAS with added emitter follower to make distortion from voltage-dependent collector-base junction capacitance negligible. Otherwise this distortion would mask the effect of nonlinear compensation capacitor reference voltage modulation. Figures 43 and 44 show the distortion spectrum at 20 kHz and an output level of +20 dB; the collector current of Q8 was set to 1.5 mA and 6 mA respectively. As is seen the $2^{\text{nd}}$ harmonic is about 10 dB higher for the 1.5 mA case and the $3^{\text{rd}}$ harmonic (which is probably contributed from the input stage) remains unchanged.

Unfortunately the standard means to reduce VAS distortion—the addition of an emitter follower or cascode transistor—does nothing about nonlinear modulation of compensation capacitor reference voltage. However as it seems, it is sufficient to just operate the VAS at a collector current of 6 mA or above to make this mechanism entirely irrelevant within the context of a power amplifier design. On the other hand we have neglected that the AC collector

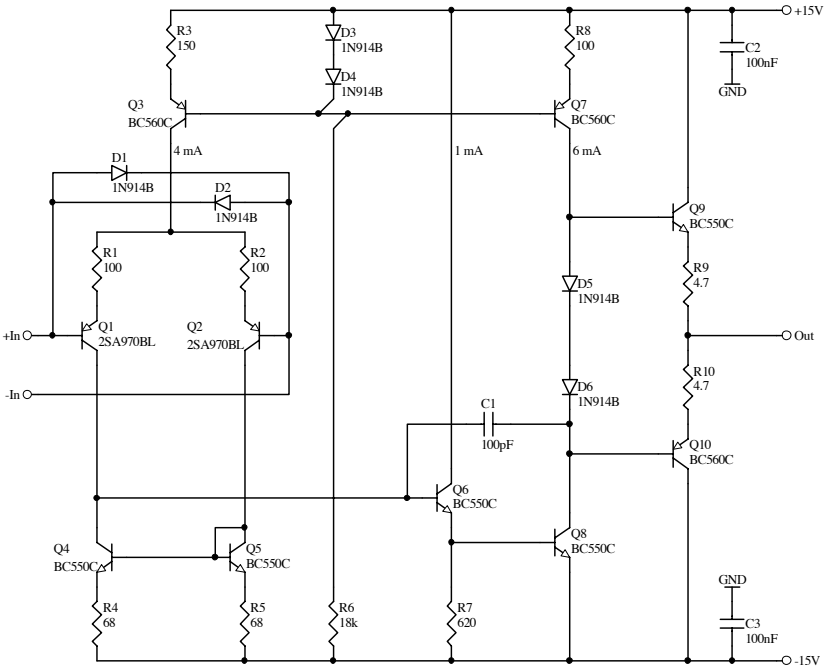


Figure 42: Model amplifier used to measure distortion from nonlinear compensation capacitor reference voltage modulation.

current of the VAS is substantially larger if a real power output stage with its rather low input impedance is used. We will deal with this issue in section 6.

To conclude this section I'd like to briefly touch upon another VAS distortion source: sometimes a clamp diode is put across the compensation capacitor for cleaner clipping and fast recovery (see e.g. [15]). The voltage dependent capacitance of this diode is similarly detrimental to the distortion performance as is the voltage dependent collector-base junction capacitance of the VAS transistor; however the improved VAS topologies (added emitter follower or cascode transistor) can obviously do nothing to reduce its effect. This clamping arrangement should hence be omitted if possible.

# 6 Distortion From VAS Loading

In the previous section we have analysed the basic distortion mechanisms of the VAS. Self notes that loading of the VAS output node may cause additional distortion (see page 194ff); in this section we will further consider this distortion source and reveal its detailed mechanisms.

To understand the significance of VAS loading, a model amplifier was measured with artificially added VAS loading. As load, a voltage-dependent network as shown in figure 45 was used. The voltage-dependent network

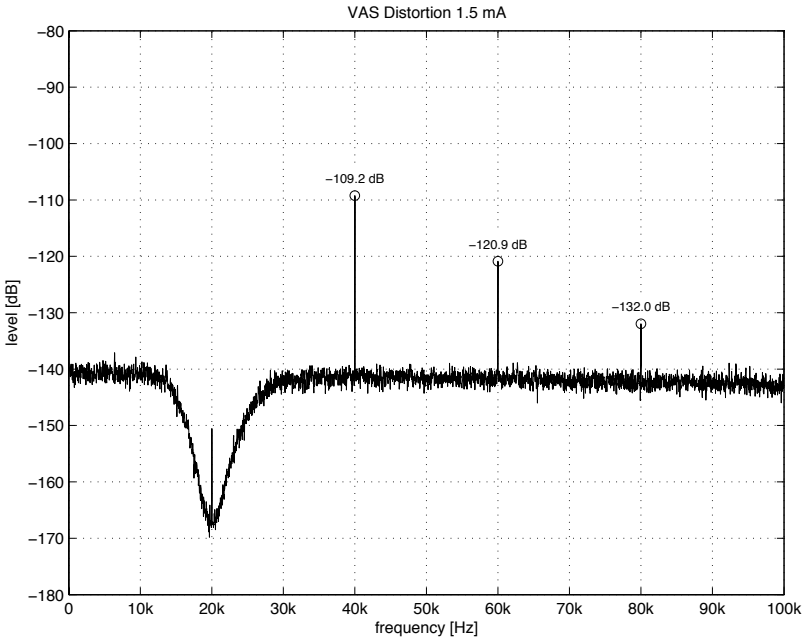


Figure 43: VAS distortion at 20kHz and a VAS collector current of 1.5 mA.

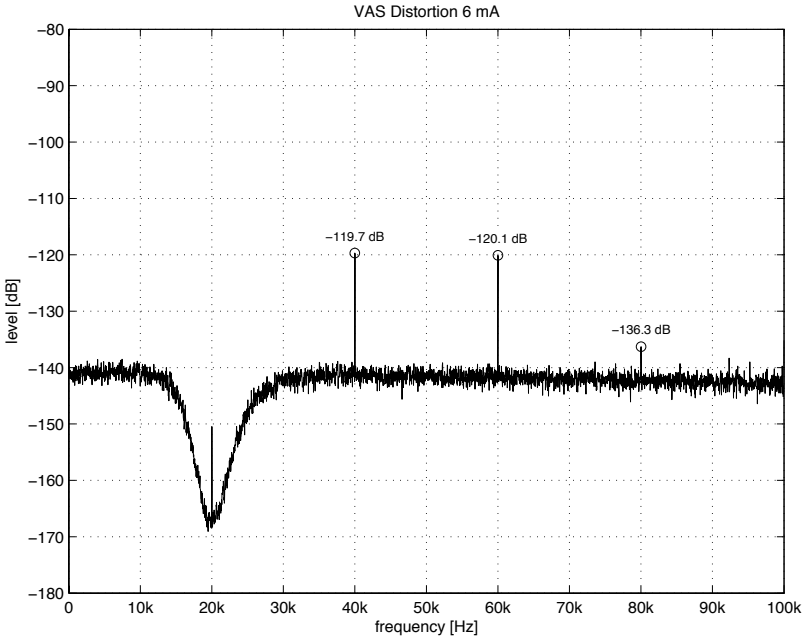


Figure 44: VAS distortion at 20kHz and a VAS collector current of 6 mA.

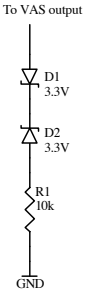


Figure 45: Voltage-dependent VAS load to emulate loading from a class B output stage.

serves as rough emulation of the input resistance of a class B output stage without introducing crossover distortion in the forward path of the amplifier. As shown it will not accurately model any possible power output stage but its use will be helpful to estimate the rough order of magnitude of the resulting distortion effect. Also comparison of the sensitivity to VAS loading between different amplifier topologies will be made possible.

Figure 46 shows the distortion performance of the model amplifier from figure 42 with and without VAS loading; output level was +20 dBu and measurement bandwidth 500 kHz. Without VAS load the amplifier shows—as a result of the degenerated input stage and emitter follower added VAS—very low distortion; only above 10 kHz some distortion products are faintly recognisable in the distortion residual. With the voltage-dependent VAS load distortion slowly rises above 2 kHz. Also visible is frequency-independent distortion at low frequencies which just slightly exceeds the noise floor. Overall performance is still rather good though. This changes drastically if we add a 68 Ω emitter resistor to the VAS transistor (as shown in figure 2); figure 47 depicts the resulting distortion, again for an output level of +20 dBu and a measurement bandwidth 500 kHz. Without VAS loading, distortion remains essentially unaltered as expected. However with the voltage-dependent loading network added, distortion is now substantial; clearly this distortion mechanism completely dominates overall performance.

In section 5 we have seen how nonlinear modulation of compensation capacitor reference voltage leads to additional high-frequency distortion. It must be expected that the relatively large and substantially nonlinear VAS currents enforced by the voltage-dependent VAS load greatly increase the harmonic distortion present at the VAS input (i.e. the compensation capacitor reference voltage); also it is clear that the addition of an emitter resistor must further increase compensation capacitor reference voltage distortion if the collector of the VAS transistors carries harmonic distortion—which is

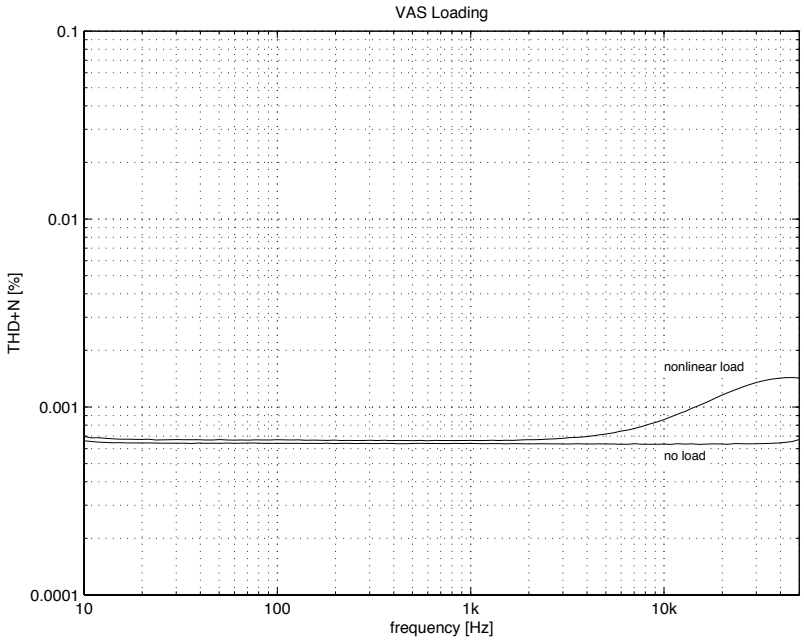


Figure 46: Distortion of the amplifier from figure 42 with and without voltage-dependent VAS load. +20 dBu output level and 500 kHz measurement bandwidth.

clearly the case with the voltage-dependent load connected. This explains the distortion rising at 6 dB/octave (following the falling loop gain) above a couple of kHz; however the low-frequency distortion floor cannot be attributed to the feedback action of the compensation capacitor.

As explained by Self on page 194ff finite VAS output impedance will interact with any voltage-dependent loading and that way generate distortion. The VAS output impedance and hence resulting distortion is falling at the same rate as loop gain, i.e. typically at 6 dB/octave. However due to the falling loop gain the effectively observed distortion is frequency independent. [7] shows that the VAS output impedance $Z_O$ can be estimated as follows:

$$Z_O \approx \frac{1}{R_L \cdot 2\pi f C_C \cdot g_m} + \frac{1}{g_m} \tag{4}$$

where $R_L$ denotes the lumped resistance at the VAS input node, $f$ the frequency of interest, $C_C$ the compensation capacitor value and $g_m$ the transconductance of the VAS transistor. Now it is clear why the VAS emitter resistor caused an increased sensitivity to VAS loading also at low frequencies; this resistor reduces the transconductance and hence leads to a proportionally higher VAS output impedance. If we assume that this resistor cannot be lowered because it is needed for current limiting, increasing the VAS quiescent

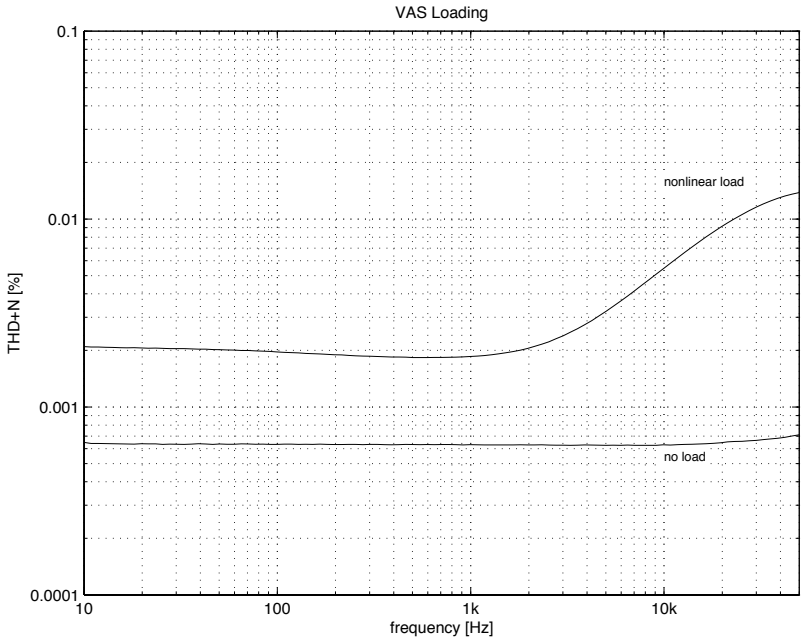


Figure 47: Distortion of the amplifier from figure 2 with and without voltage-dependent VAS load; +20 dBu output level and 500 kHz measurement bandwidth.

current will not significantly increase $g_m$ as the effective emitter resistance is dominated by the emitter resistor anyway. Also increasing $C_C$ is out of the question as it would alter open-loop gain.

The only choice left to reduce VAS output impedance is to increase the lumped resistance $R_L$ at the VAS input node. This resistance is comprised of three contributions:

- Output resistance of the input differential pair, or rather of this transistor of the differential pair which is connected to the VAS.
- Output resistance of the current mirror.
- Input resistance of the VAS.

Which contribution dominates depends very much on the exact amplifier design. Also the three figures are substantial functions of Early voltage and/or $h_{FE}$ so might not be very dependable in production. In the following we will assume that it is desirable to reduce any of these three contributions.

Consider figure 48 which shows a model amplifier with increased lumped resistance $R_L$ and thus reduced VAS output impedance. Increasing the output resistance from the input differential pair is done by using a cascode

formed by Q4 and Q5. Also a Wilson current mirror is used; while this configuration offers inherently higher output resistance over the standard two-transistor Widlar current mirror, this is further improved with large degeneration resistor values (these also reduce noise as shown in section 3). The input resistance of the VAS is brought up by the use of a MOSFET for the follower Q9. Note that in this position the usual disadvantages of MOSFETs over BJTs (lower transconductance and higher junction capacitances) are of little relevance; however the very low DC current which is drawn from the input stage will improve collector current balance of the input differential pair, at least as long as a Wilson current mirror (or any other mirror with very good DC balance) is used. To give sufficient voltage headroom for the Wilson mirror even at the lowest guaranteed threshold voltage of Q9, D6 and D7 are added; in many cases it might be advisable to provide even more voltage headroom for the current mirror by the addition of a third diode. This will also eliminate the need to capacitively bypass the current mirror emitter resistors for good slew-rate (see section 3).

The measurements for this model amplifier are shown in figure 49. We can see that the low-frequency distortion floor is now independent from voltage-dependent VAS loading and lower than before even without VAS loading—the latter being just a result from the reduced current mirror noise contribution. As expected the distortion rising at 6 dB/octave is unaltered so far; the circuit changes have just reduced VAS output impedance but done nothing about compensation capacitor reference voltage modulation.

On page 292ff Self shows how connection of the compensation capacitor to an input stage cascode improves PSRR; this node does not carry any voltage generated from voltage-dependent VAS loading so should reduce resulting distortion as well. Figure 50 shows the implementation chosen for experimental verification. As now the Miller compensation loop formed by C1 includes more transistors, the chance for local instability is substantially increased; to reduce this tendency C2 is included. This capacitor forms a feed forward path which bypasses the source follower Q9 at high frequencies [16]. As depicted in figure 51 the cascode compensation capacitor connection is very effective, but not a full cure. The exact mechanism of the remaining distortion has not been investigated; however it is clear that the VAS emitter resistor is still the main cause for the sensitivity to nonlinear VAS loading. Setting its value to 36 Ω reduces distortion at 10 kHz to 0.0013 %.

Furthermore it is notable that the changed compensation capacitor reference node also improved high-frequency distortion without VAS loading (compare figure 49 and 51). To the extent that I have investigated this I can say that this is also a result from reduced compensation capacitor reference voltage modulation. The voltage-dependent junction capacitances of the VAS transistor, its active collector load and the output stage draw nonlinear

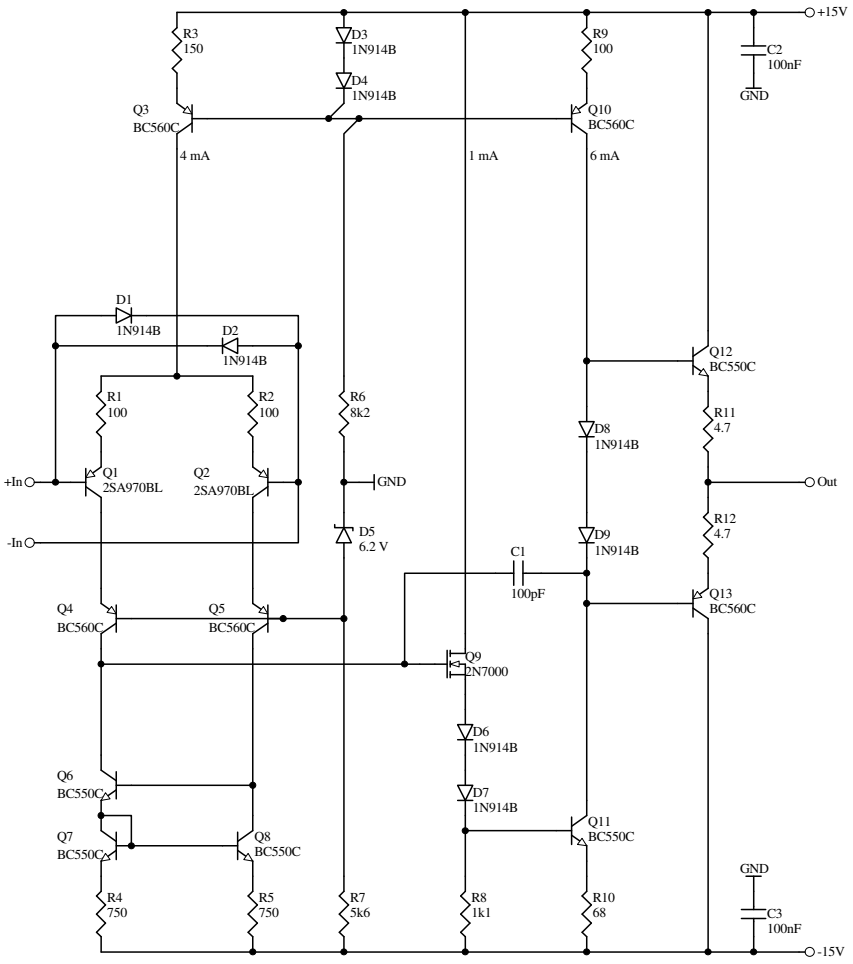


Figure 48: Model amplifier with reduced sensitivity to VAS loading. The input stage cascode, Wilson current mirror and VAS MOSFET source follower reduce VAS output impedance.

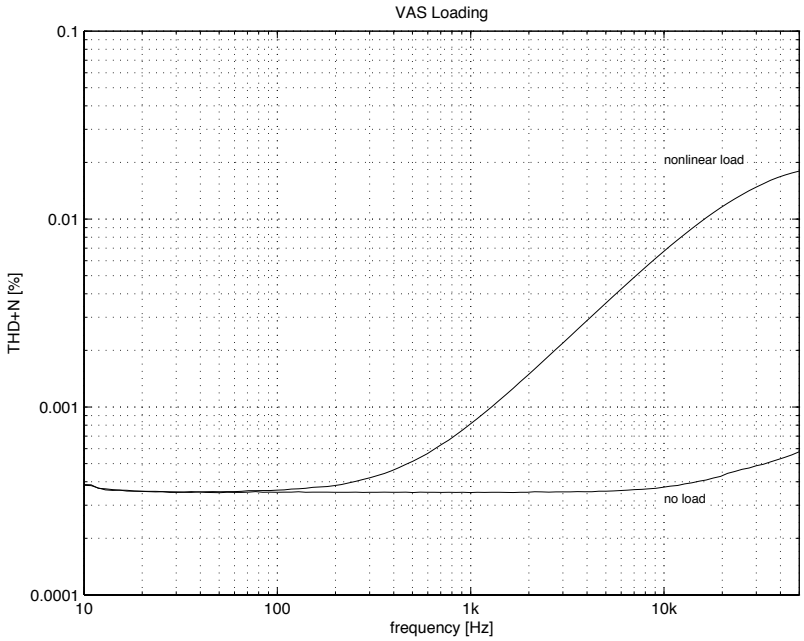


Figure 49: Distortion of the amplifier from figure 48 with and without voltage-dependent VAS load. +20 dBu output level and 500 kHz measurement bandwidth.

currents from the VAS transistor. Together with the 68 Ω VAS emitter resistor this is sufficient to cause significant modulation of the standard compensation capacitor reference node; detectable distortion at the upper end of the audio frequency range results which is eliminated by the cascode compensation scheme.

It might be argued that at lower complexity it would be possible to add an emitter follower to increase the input impedance of the output stage, presumably giving a similar if not more significant reduction in distortion. On the other hand the use of an input stage cascode, an improved current mirror and the altered compensation capacitor reference connection does have a couple of other advantages, such as improved PSRR and reduced noise. Also an additional emitter follower in the output stage might increase sensitivity to local parasitic oscillation in the output stage and worsen thermal stability of output stage bias conditions. Each power amplifier design will have its own set of trade-offs and hence the final decision must be left to the designer; if nothing else this research has given some interesting insight into rather subtle interactions inside typical amplifier topologies.

The results shown here are of particular importance if advanced compensation schemes such as two-pole and transitional Miller compensation [7][17] are used; while these compensation schemes can offer substantial reduction

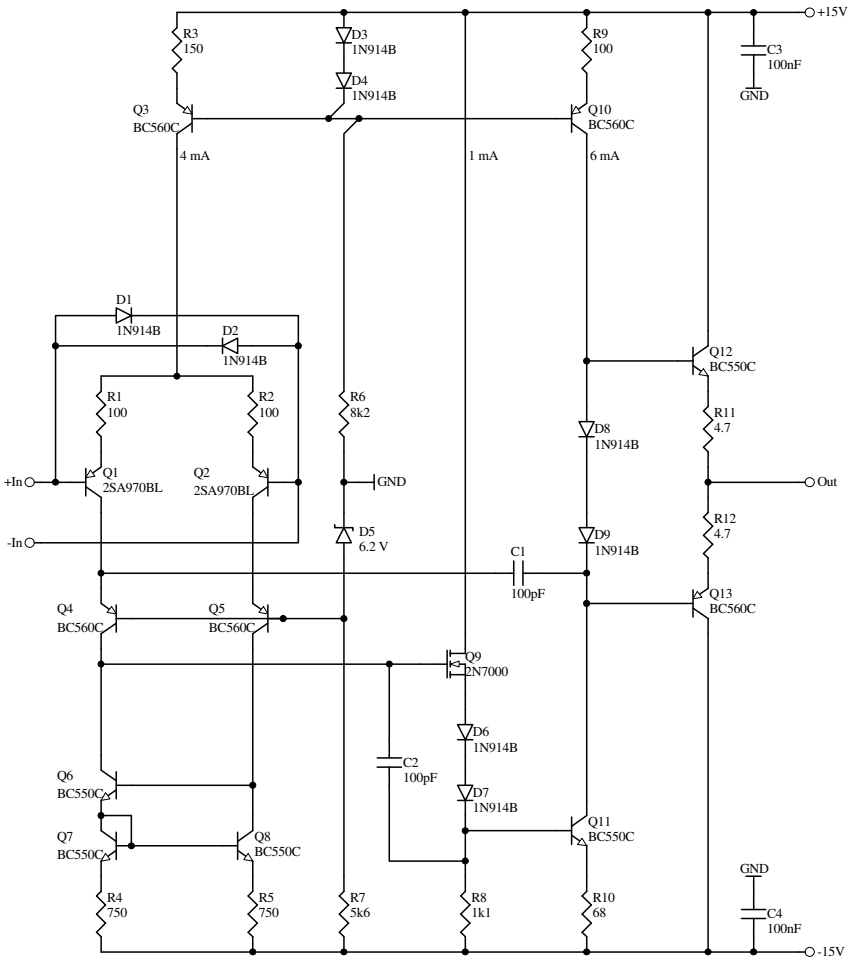


Figure 50: Model amplifier with reduced sensitivity to VAS loading. The cascode connection for the compensation capacitor C1 further improves distortion performance under extended VAS loading conditions.

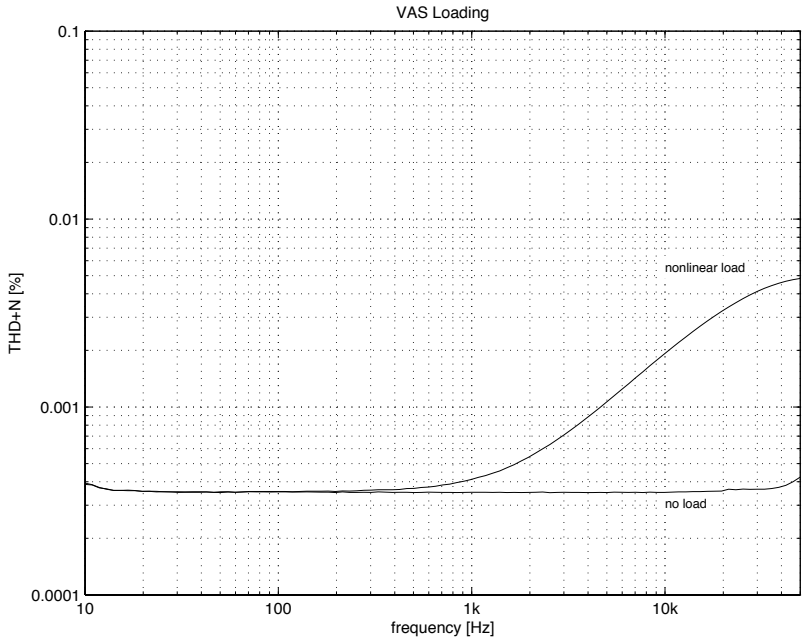


Figure 51: Distortion of the amplifier from figure 50 with and without voltage-dependent VAS load. +20 dBu output level and 500 kHz measurement bandwidth.

of basic crossover distortion they do not usually reduce sensitivity to VAS loading. To gain full advantage of their potential distortion reduction particular attention to this mechanism must hence be given. Most unfortunately lack of spare time has prevented me from implementing the topological enhancements presented in this section within a real power amplifier design so far; thus it is not yet fully clear if the reduced sensitivity to VAS loading will actually improve overall amplifier distortion. It is by all means possible that in certain implementations basic crossover distortion will mask the distortion reduction. Various simulation results however indicate that typically there is a possible improvement in the order of two to four times lower distortion at the upper end of the audio frequency range. That is with a 68 Ω VAS emitter resistor and transitional Miller compensation—implementations with lower emitter resistor values and/or straight Miller compensation benefit less from the circuit changes.

To complete this section some measurements on a model amplifier with cascode (rather than emitter follower added) VAS were done; the amplifier schematic is depicted in figure 52 while the measurement results are shown in figure 53 and 54. As noted by Self this VAS topology is substantially more sensitive to VAS loading. It's easy to think that the cascode increases VAS output impedance compared to a simple one-transistor VAS. However this

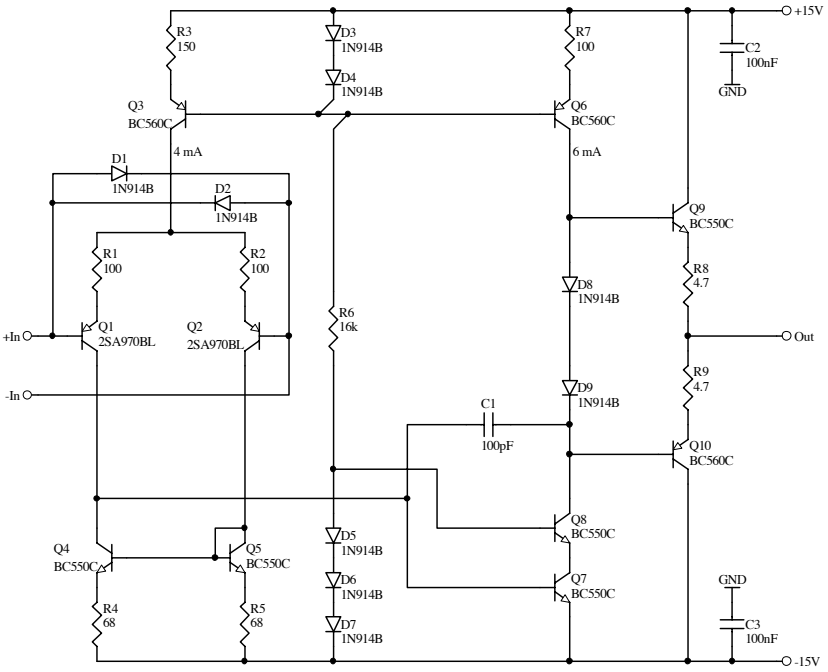


Figure 52: Model amplifier with cascode enhanced VAS.

increase only happens below the dominant pole frequency (which is moved downwards as a result of the increased low-frequency open loop gain) and the cascode VAS shows in fact the same sensitivity to VAS loading as the basic one-transistor VAS. It is the emitter follower of the EFA VAS which reduces VAS output impedance compared to the one-transistor VAS. This is because it increases the input resistance of the VAS and hence $R_L$. That way the emitter follower conveniently improves both fundamental VAS linearity and insensitivity to VAS loading. If for further reduced distortion a cascode is added to an EFA VAS this will not increase sensitivity to VAS loading; this is again because the cascode only increases VAS output impedance below the dominant pole.

# 7 Manipulating Open-Loop Bandwidth

On page 134ff Self shows how a resistor in parallel with the compensation capacitor may be used to increase open-loop bandwith by reducing the low-frequency open-loop gain. If second-order effects from the VAS (such as finite $h_{FE}$ and Early voltage) are negligible then the open-loop gain $A$ below the dominant pole is simply given by:

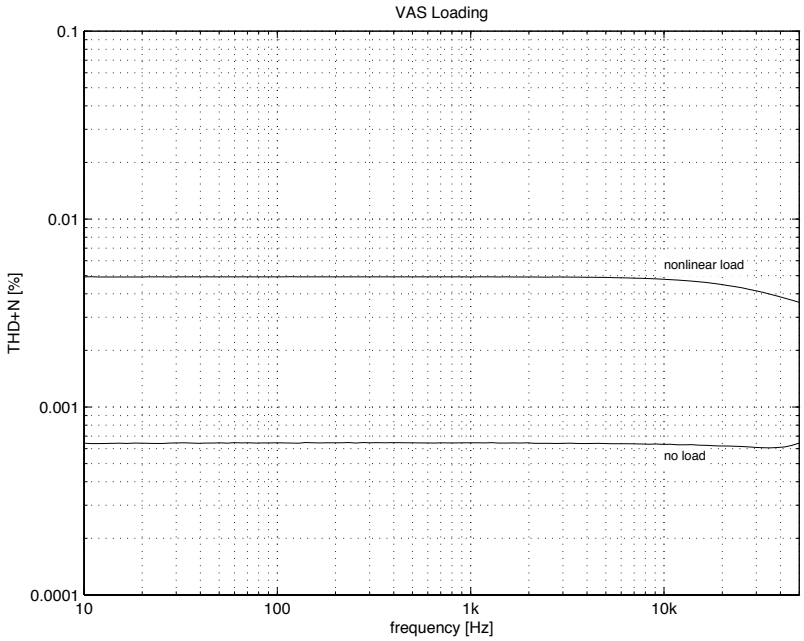


Figure 53: Distortion of the amplifier from figure 52 with and without voltage-dependent VAS load. +20 dBu output level and 500 kHz measurement bandwidth.

$$A \approx g_m \cdot R_C \tag{5}$$

where $g_m$ denotes the input stage transconductance and $R_C$ the resistor in parallel with the compensation capacitor.

The basic implementation shown in figure 5.16b (Self page 135) has the following disadvantages as noted by Self:

- Due to reduced open-loop gain more output stage distortion is present at low frequencies.
- The presence of this additional resistor worsens the collector current balance of the input stage.
- The low-frequency PSRR of the amplifier is strongly reduced.

I'd like to suggest an improved scheme which does not suffer from any of the above problems; as depicted in figure 55 this comes at the modest cost of one additional resistor. R4 represents the resistor which was previously connected in parallel with the compensation capacitor—it is now connected to the output of the third stage rather than the VAS output node. Any global

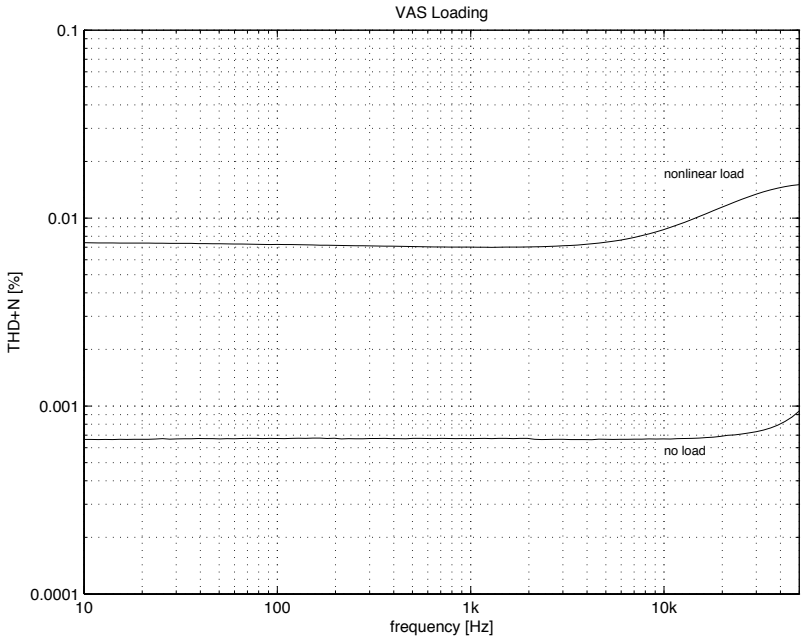


Figure 54: Distortion of the amplifier from figure 52 with 68 Ω emitter resistor for Q7 added. Measurements with and without voltage-dependent VAS load at +20 dBu output level and 500 kHz measurement bandwidth.

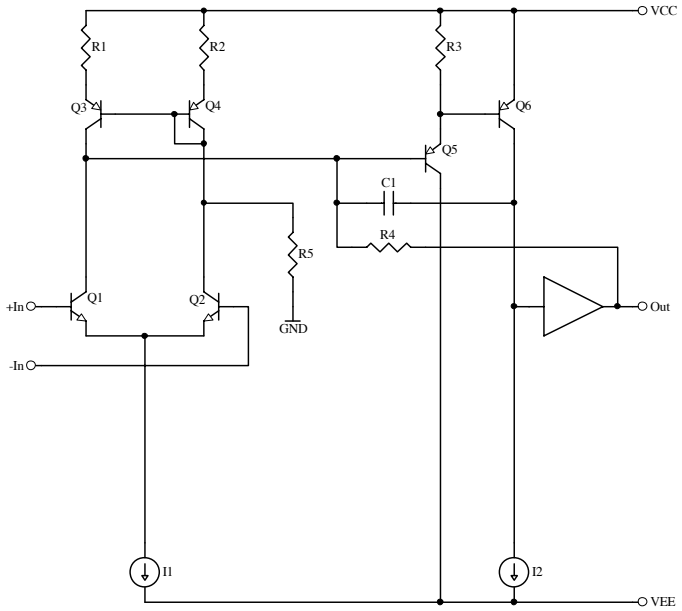


Figure 55: Two-stage amplifier with increased open-loop bandwidth (or reduced low-frequency open-loop gain).

loop gain which is transferred to local VAS loop gain now reduces output stage distortion; as input stage distortion is low at low frequencies and the linearity of the VAS remains unchanged the overall amplifier distortion performance remains unaltered. Stability is not impaired as at high frequencies the compensation capacitor dominates the local VAS feedback.

Resistor R5 is of equal value as R4 and connected to reestablish collector current balance of the input stage; at the same time it increases (for not further studied reasons) the PSRR back to a value which is similar to that of a standard amplifier without manipulated open-loop bandwidth.

# 8 Push-Pull VAS Topologies

On page 128ff Self discusses push-pull VAS topologies and distinguishes two basic implementations—those which start with a standard differential pair and such which use two complementary input stages. Figure 5.9a (Self page 129) depicts a basic implementation of the former, for which Self notes several issues. While I cannot follow all of these points because simulation and measurement show otherwise, I agree that this basic implementation is suboptimal. Figure 56 depicts an alternative which offers several advantages over the standard amplifier topology discussed by Self; in particular these are:

- The DC collector current balance of the input stage is exceptionally good as current mirror errors are related to the VAS where they have far less influence on the input stage. Also input currents drawn by the VAS appear as common-mode signal (at least to the extent that Q5 and Q6 have matched $h_{FE}$) and hence do not significantly affect the input stage balance.

- The input differential pair (Q1 and Q2) is operated at near-equal collector voltage which improves offset plus associated drift, CMRR and PSRR.

- Emitter followers Q5 and Q6 are operated at low collector voltage; hence low voltage parts with high $h_{FE}$ and corresponding improvement in open-loop gain and other parameters are easily chosen.

- The collector currents of Q8 and Q10 are inherently limited by I2; therefore no additional overload protection is needed for these transistors. Overload protection usually needs a VAS emitter resistor, or rather two of them for the differential configuration considered here. As shown in section 6 VAS emitter resistors greatly increase sensitivity to VAS loading, thus the possibility to omit them is of great benefit.

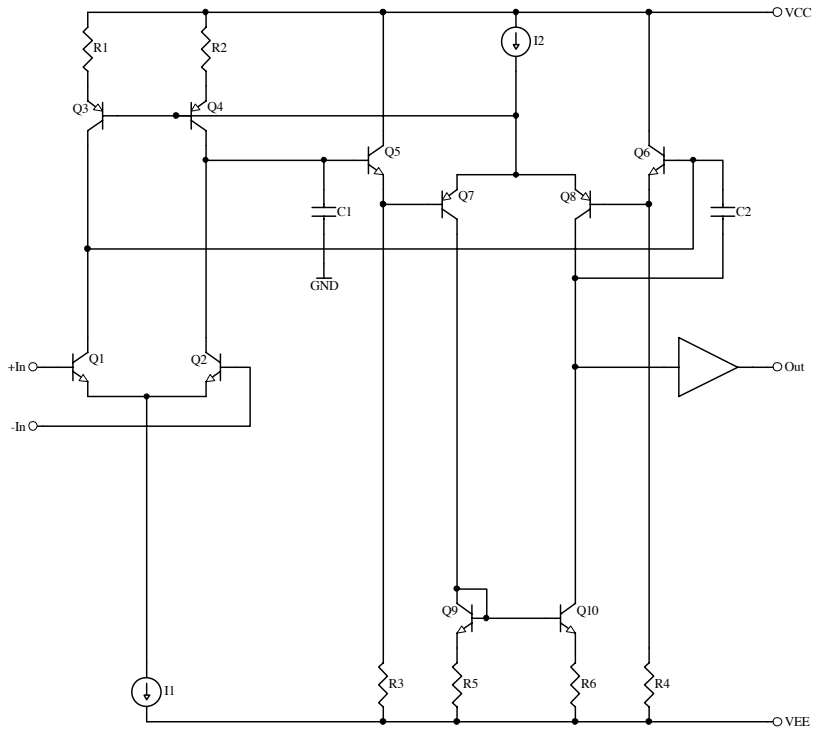


Figure 56: Amplifier topology with differential VAS.

- The PSRR of this amplifier topology is excellent. This is because the base of Q6 (and hence the local VAS feedback) is not referenced to a supply rail—rather Q8, Q7, Q5 and C1 reference it to ground at high frequencies.

The main disadvantage relates to the output voltage which is required by I2 for correct operation; this might reduce output swing by several 100 mV unless an additional supply rail for the small signal stages is used. At first perhaps surprisingly this topology does not offer inherently reduced VAS distortion; this is because Q7 does not follow the collector swing of Q8 which prevents any distortion cancellation expected from the differential configuration. If the current mirror formed by Q9, Q10, R5 and R6 is bootstrapped to the output voltage this is accomplished and an exceptionally linear VAS with high gain results.

The quiescent current of the VAS is—unlike Self notes on page 128—well defined by I2. This is not necessarily the case for the second group of push-pull VAS topologies which use two complementary input stages. For resistive input stage loads such as the amplifier depicted in figure 5.11 (Self page 131) and 5.13 (Self page 133) the VAS quiescent current is reasonably well defined by the voltage drop across the input stage collector resistor (e.g. R1 and

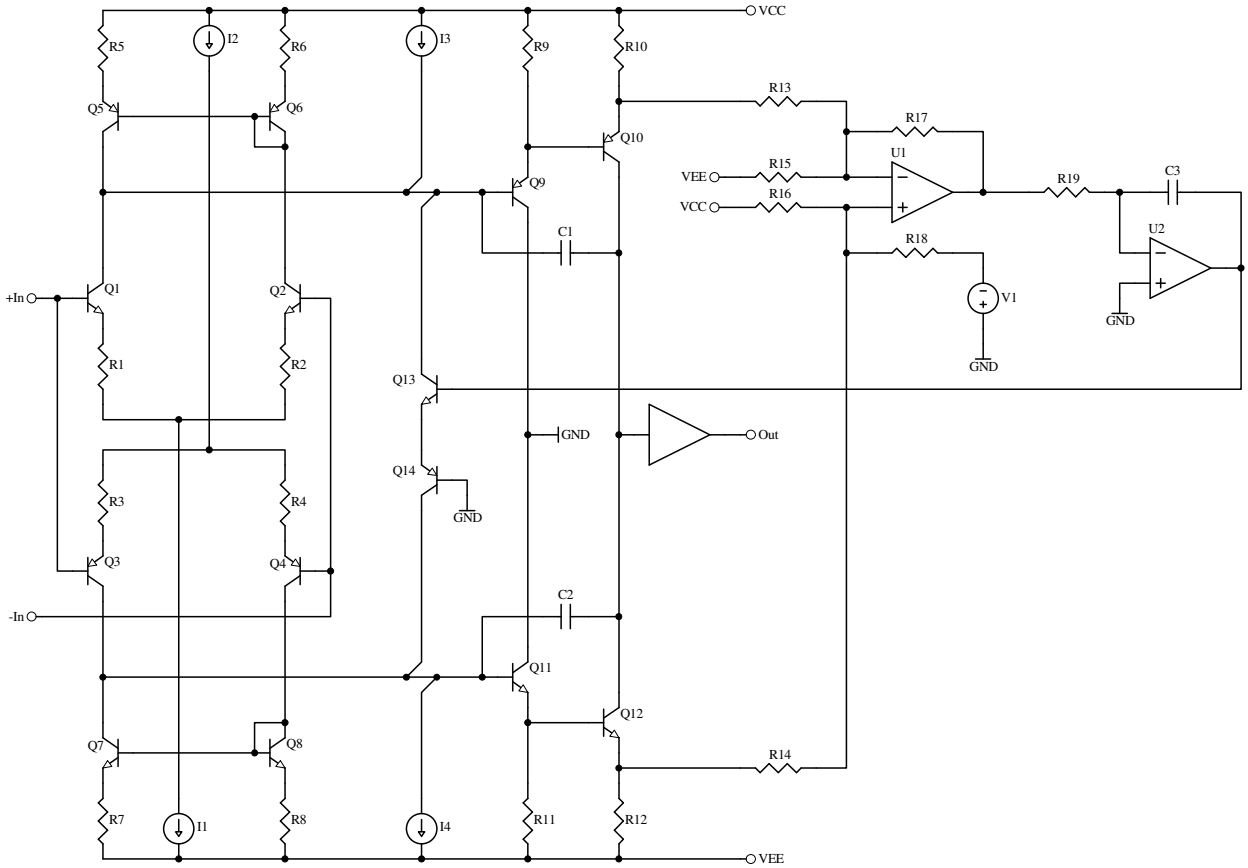


Figure 57: Push-pull VAS stage with common-mode control loop.

R3 in figure 5.11, Self page 131), which in turn biases the bases of the VAS transistors. However if current mirrors are used (as shown in figure 5.12, Self page 132) there is no first-order limit for VAS quiescent current as the output node of the input stages is floating and hence doesn't properly bias the bases of the VAS transistors. Significant production spread, thermal runaway and even not-at-all-working units must be expected.

Proper solution of this problem is possible by the use of a common-mode control loop as shown in figure 57. U1 senses the bias current of the VAS through the emitter resistors R10 and R12. After subtraction of a reference voltage this error signal is fed to an integrator stage formed by U2, R19 and C3. The output of the integrator drives Q13—if this transistor is turned on more it provides additional base current for Q9 and Q11, which in turn increases VAS quiescent current. The accuracy of the VAS quiescent current is mainly determined by the matching of R13–R18; if standard 1 % parts are employed there might be a need for a preset trim to keep production variation reasonably low.

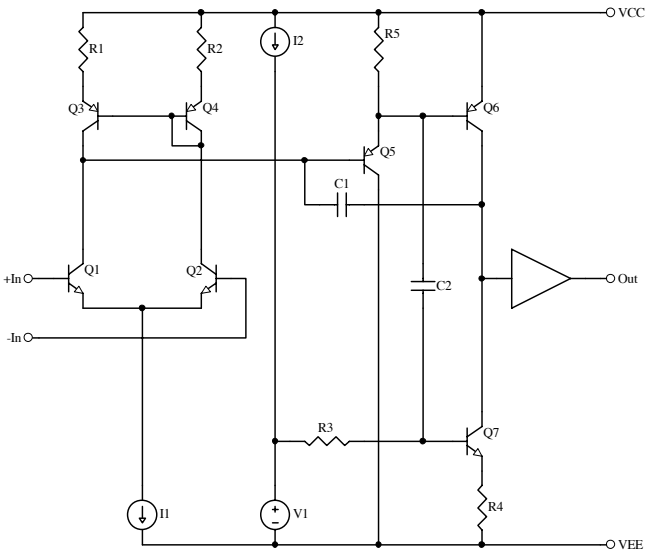


Figure 58: Amplifier with VAS slew-rate enhancement.

Other solutions to control quiescent current of a push-pull VAS typically artificially limit the resistance at the VAS input by the addition of a resistor to this node [7]. This will usually reduce both low-frequency open-loop gain, PSRR and CMRR. Furthermore it will increase VAS output impedance (see section 6) and hence sensitivity to VAS loading.

# 9 Slew-Rate Enhancement

On page 259ff Self discuss the slew-rate limitations which result from the VAS. The modified biasing system presented in figure 8.49 (Self page 262) has the disadvantage of potential instability; additionally it is disadvantageous that the current source of the input stage does not have feedback control as this might result in worse PSRR and CMRR. Figure 58 shows another possibility where capacitor C2 serves as level shifter which effectively converts the VAS to push-pull operation at high frequencies. This means that Q7 may source much higher peak currents which removes its slew-rate limitations. This works very effectively and the VAS may even be operated at somewhat lower quiescent current than the input stage without any effect on slew-rate. However for low distortion and sufficient output current at low frequencies (which is needed to drive the output stage) the VAS will still need a quiescent current of 6–10 mA.

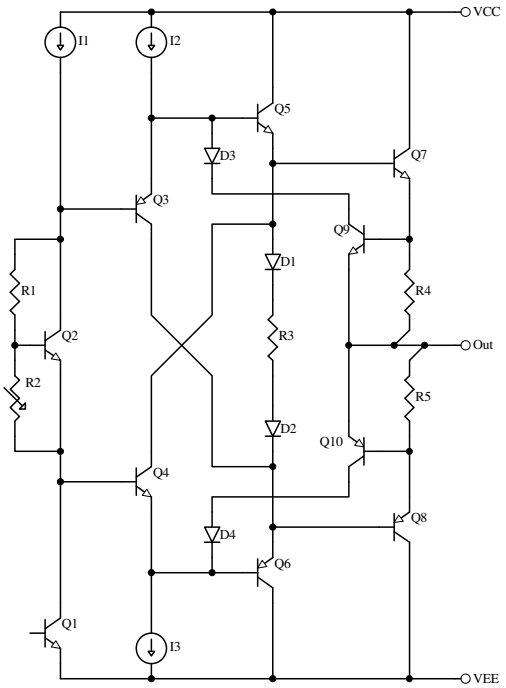


Figure 59: Triple emitter follower output stage. Q1 represents the VAS transistor.

## 10 Triple Output Stage

Self presents several triple output stages on page 154ff. I'd like to suggest another topology as shown in figure 59 which offers several advantages:

- The collectors of Q3 and Q4 are bootstrapped to the output voltage. This allows the use of transistors with low breakdown voltages which typically offer higher $h_{FE}$ compared to standard high-voltage parts. Higher $h_{FE}$ results in higher output stage input impedance which is beneficial to reduce VAS loading. Furthermore the bootstrapping greatly reduces input impedance terms from junction capacitances and Early effect.

- The temperature coefficient of Q3/Q5 and Q4/Q6 approximately cancel. This simplifies the design of the $V_{be}$ multiplier (formed by Q2, R1 and R2) which now only needs to correct for the thermal effects in Q7 and Q8.

- The collector currents of the current limiting transistors Q9 and Q10 are inherently limited by I2 and I3. The protection circuit will not draw excess current from the VAS, hence no emitter resistor or any other

form of protection is needed. This is beneficial to reduce nonlinear compensation capacitor reference voltage modulation and sensitivity to VAS loading (as detailed in section 6) and in some cases to improve voltage swing.

- Depending on the saturation characteristics of I2 and I3 this configuration will yield higher output swing compared to other triple output stages. For best efficiency these current sources could be replaced with bootstrapped resistor loads, although this might result in somewhat reduced bias stability with unregulated power supplies.

This output stage is more complex than other triple output stages, however the cost increase is modest as only small-signal parts are needed. This topology has found widespread use in IC opamps (see e.g. [18]) but is less known amongst power amplifier designers, although it is mentioned in [7].

## 11 Capacitor Distortion

On page 202ff Self shows how electrolytic capacitors cause distortion when used with significant AC voltage across them. There is an easy way to reduce this distortion; that is by the use of two capacitors which are connected in an anti-parallel fashion (i.e. with opposite polarities). This cancels even-order distortion products and shifts the onset of detectable distortion towards lower frequencies; the technique has probably been first published in [19].

Figure 60 compares the distortion generated from two 22 $\mu$F capacitors (Panasonic FC, rated for 100 V) when connected either as standard parallel or anti-parallel pair. The capacitors were connected as a low-pass filter together with a 1 k$\Omega$ resistor and driven from a +20 dBu source. The rise for frequencies above 50 Hz or 200 Hz is due to noise rather than actual distortion. Distortion cancellation always raises the question about its dependability in production; the capacitors for the measurements of figure 60 have been randomly selected but there is no guarantee that the cancellation achieved will be consistent for other specimens.

To investigate this ten Panasonic AM capacitors (again 22 $\mu$F, but now rated for 50 V) were measured at 80 Hz (otherwise equivalent conditions to the measurement shown above) with every possible combination—that makes 45 pairs. Each pair was measured once as normal parallel combination and then as anti-parallel pair; the ratio of these two measurements was then plotted against capacitance mismatch, as it was expected that distortion cancellation depends on this. Figure 61 shows the result. First of all it is surprising that the worst capacitance mismatch found is below 1.5 %. Second the distortion improvement seems to be only very weakly (if at all) correlated

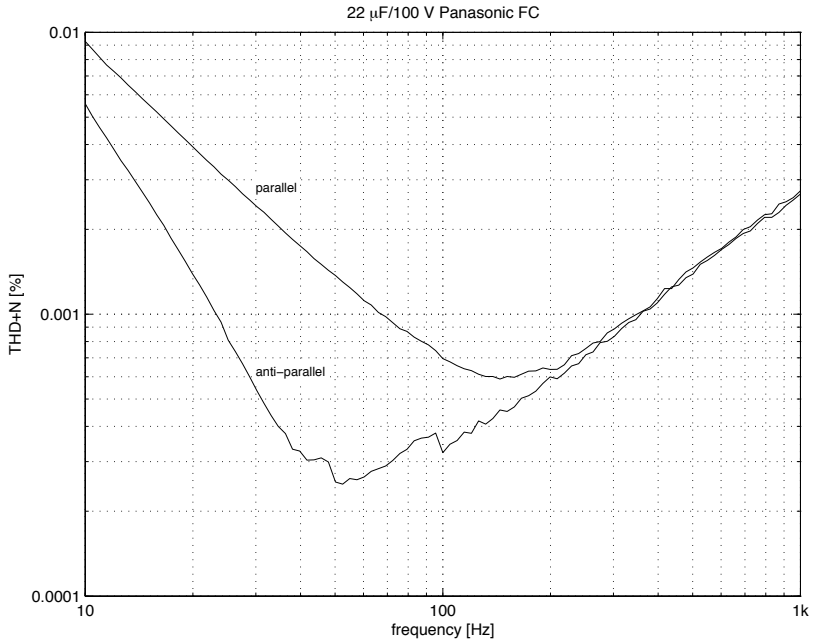


Figure 60: Distortion in electrolytic capacitors. Anti-parallel arrangement cancels even-order distortion products.

with capacitance match. Third, there are nine outliers with about 5 dB less distortion improvement. As might be guessed by the number nine these are all attributed to one specific capacitor which showed somewhat higher $2^{\text{nd}}$ harmonic distortion than the other specimen; this reduced the amount of cancellation.

These measurements suggest that the distortion cancellation achieved by anti-parallel connection of electrolytic capacitors is worthwhile and relatively dependable. However at the time of writing I cannot testify that other parts will show similar statistical behaviour.

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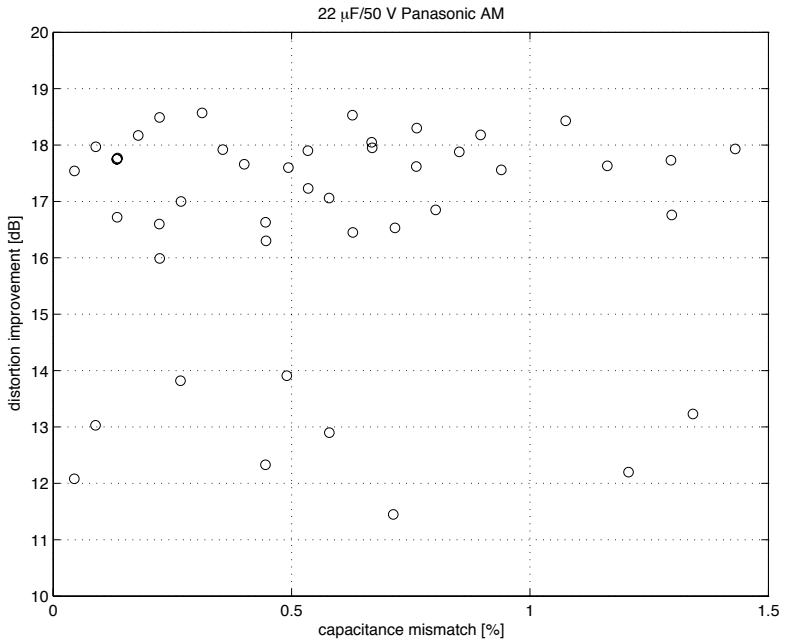


Figure 61: Distortion improvement by anti-parallel capacitor connection.

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