盛微先進科技
SAVITECH.COM

BRAVO
SA9023
USB Digital Audio Processor

V1.1
SAVITECH Corporation

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USB Digital Audio Processor

Features

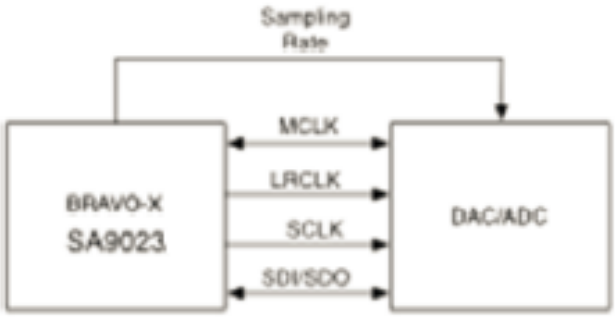
- USB 2.0 Full-Speed Compliant
- Certificated
  - USB IF logo and Microsoft WHQL logo certificated
- Isochronous input and output endpoints for recording and playback
- One interrupt endpoint for HID
- Support resolutions up to 24-bit and sampling rates up to 96KHz
- One I2S input and one I2S output interface
  - Independent sample rates for each interface
  - 32 / 44.1 / 48 / 88.2 / 96 KHz sampling rates
- Built in IEC60958 professional S/PDIF TX and SPDIF RX,
  - AES/EBU supported*
  - Stereo SPDIF Input and SPDIF Output
  - 32/ 44.1/ 48/ 88.2/ 96 KHz sampling rates
- Control and I/O
  - One I2C bus is designed in slave mode to configure the system and access real-time system information, including Resolution, Sampling Rate, SPDIF TX and SPDIF RX info
  - One 5-bit SAR ADC
  - 12-pin GPIO
- 48-pin TQFP packages

*AES：Audio Engineering Society
*EBU：European Broadcasting Union

Overview

The SA9023 is a high performance 24bit USB Full-Speed compliant digital audio processor. It features one stereo playback and recording pairs and one IEC60958 S/PDIF receive and transmit streaming pair. The SA9023 is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its resolution and sampling rate can be configurable with 16 / 24 bit and 32 / 44.1 / 48 / 88.2 / 96 KHz respectively.

Application Block diagram



Pin Assignment

1	DASYNC	13	GPIO7	25	VSS	37	XI
2	DADAT	14	SCL	26	TEST2	38	XO
3	DAMCLK	15	SDA	27	SPDTX	39	VSS
4	VDD33	16	RESETN	28	GPIO6	40	VDD18
5	VSS	17	SCLS	29	GPIO10	41	GPIO0
6	DASCLK	18	SDAS	30	GPIO3	42	GPIO2
7	ADSYNC	19	VDD18	31	GPIO1	43	GPIO4
8	ADDAT	20	TEST1	32	VSS	44	GPIO8
9	VDD18	21	GPIO5	33	SPDRX	45	VDD33
10	GPIO9	22	SAR	34	DP	46	VSS
11	ADMCLK	23	VDD33	35	DM	47	NC
12	ADSCLK	24	VDD18O	36	VDD33	48	GPIO11

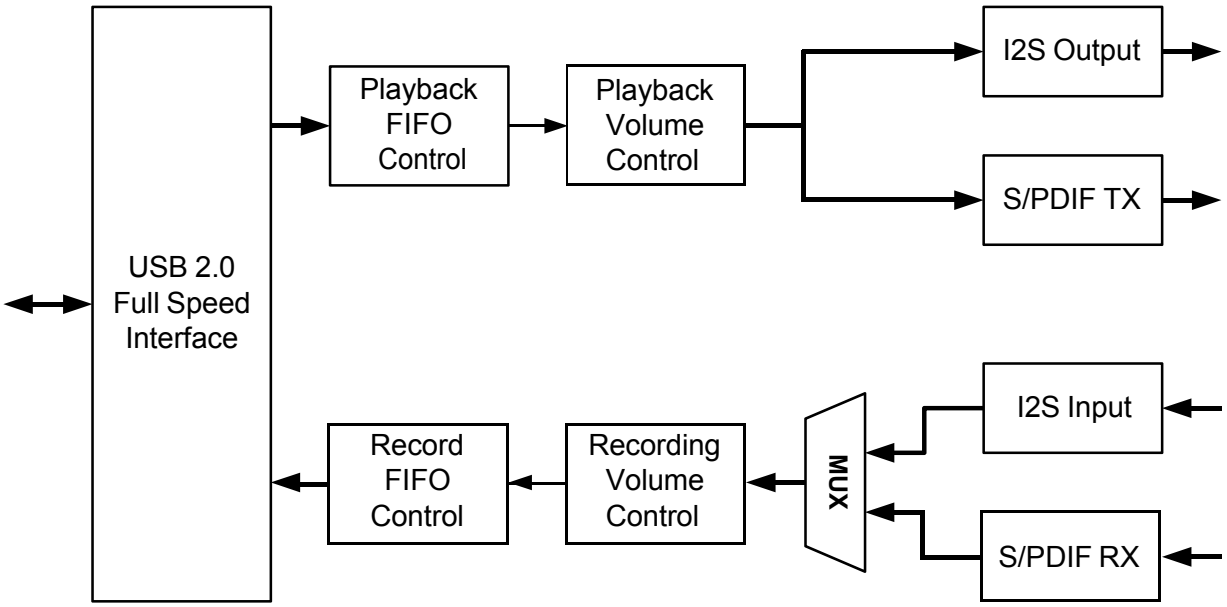
Pin Descriptions

Pin	Name	I/O/P	Description
1	DASYNC	I/O	I²S L/R sync clock: Input in slave mode and output in master mode.
2	DADAT	O	I²S data output
3	DAMCLK	I/O	I²S master clock: Input in slave mode and output in master mode.
4	VDD33	P	3.3V power supply
5	VSS	P	Ground
6	DASCLK	I/O	I²S Bit clock output: Input in slave mode and output in master mode. 256fs
7	ADSYNC	I/O	I²S L/R sync clock: Input in slave and output in master.
8	ADDAT	I	I²S data input
9	VDD18	P	1.8V power supply
10	GPIO9	I/O	General purpose Input/Output
11	ADMCLK	I/O	I²S master clock : Input in slave mode and output in master mode. 256fs
12	ADSCLK	I/O	I²S Bit clock: Input in slave mode and output in master mode.
13	GPIO7	I/O	General purpose Input/Output
14	SCL	I/O	I2C-master clock
15	SDA	I/O	I2C-master data
16	RESETN	I	Reset control pin. Active in “Low” state.
17	SCLS	I/O	I2C-slave clock
18	SDAS	I/O	I2C-slave data
19	VDD18	P	1.8V power supply
20	TEST1	I/O	FT test pin. Need pull-down.
21	GPIO5	I/O	General purpose Input/Output
22	SAR	I	SAR ADC input
23	VDD33	P	3.3V power supply
24	VDD18O	P	Internal 1.8V LDO output

PIN	NAME	I/O/P	Description
25	VSS	P	Ground
26	TEST2	I/O	FT test pin. Need pull-down.
27	SPDTX	O	S/PDIF TX interface
28	GPIO6	I/O	General purpose Input/Output
29	GPIO10	I/O	General purpose Input/Output
30	GPIO3	I/O	General purpose Input/Output
31	GPIO1	I/O	General purpose Input/Output
32	VSS	P	Ground
33	SPDRX	I	S/PDIF RX interface
34	DP	I/O	USB interface DP
35	DM	I/O	USB interface DM
36	VDD33	P	3.3V power supply
37	XI	I	X'tal clock input
38	XO	O	X'tal clock output
39	VSS	P	Ground
40	VDD18	P	1.8V power supply
41	GPIO0	I/O	General purpose Input/Output
42	GPIO2	I/O	General purpose Input/Output
43	GPIO4	I/O	General purpose Input/Output
44	GPIO8*	I/O	General purpose Input/Output
45	VDD33	P	3.3V power supply
46	VSS	P	Ground
47	NC	I	No connection
48	GPIO11	I/O	General purpose Input/Output

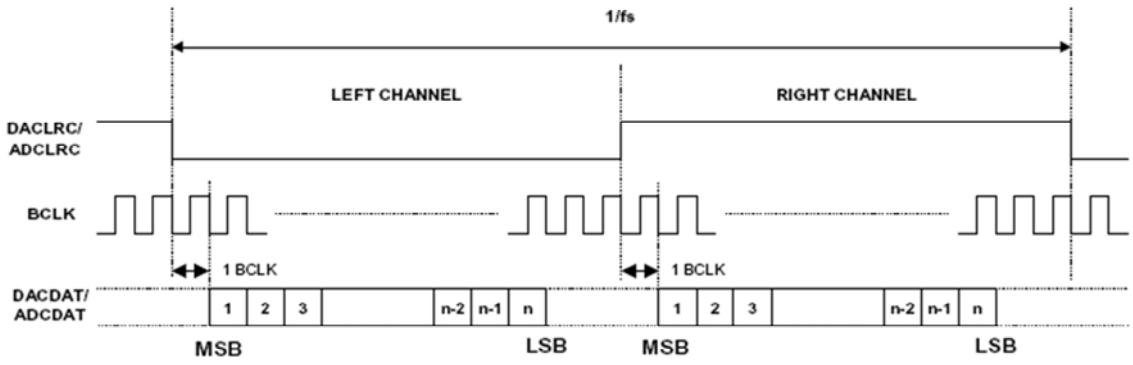
*GPIO8 have multi-function can be selected.
Please refer **GPIOs Function** chapter for get more detail.

I2S / SPDIF and Audio Data Streams Function Blocks



I2S Format

As shown in Figure, the Standard I2S bus has three lines.
1). Continuous Serial Clock (SCLK)
2). Word Select (LRCLK)
3). Serial Data (DAT)



GPIOs Function

SA9023 provides 12 GPIOs (GPIO0 ~ GPIO11). Each has its individual function in normal mode. GPIO0~6 are used for HID Report.
GPIO7~11 are used for audio stream status reporting.

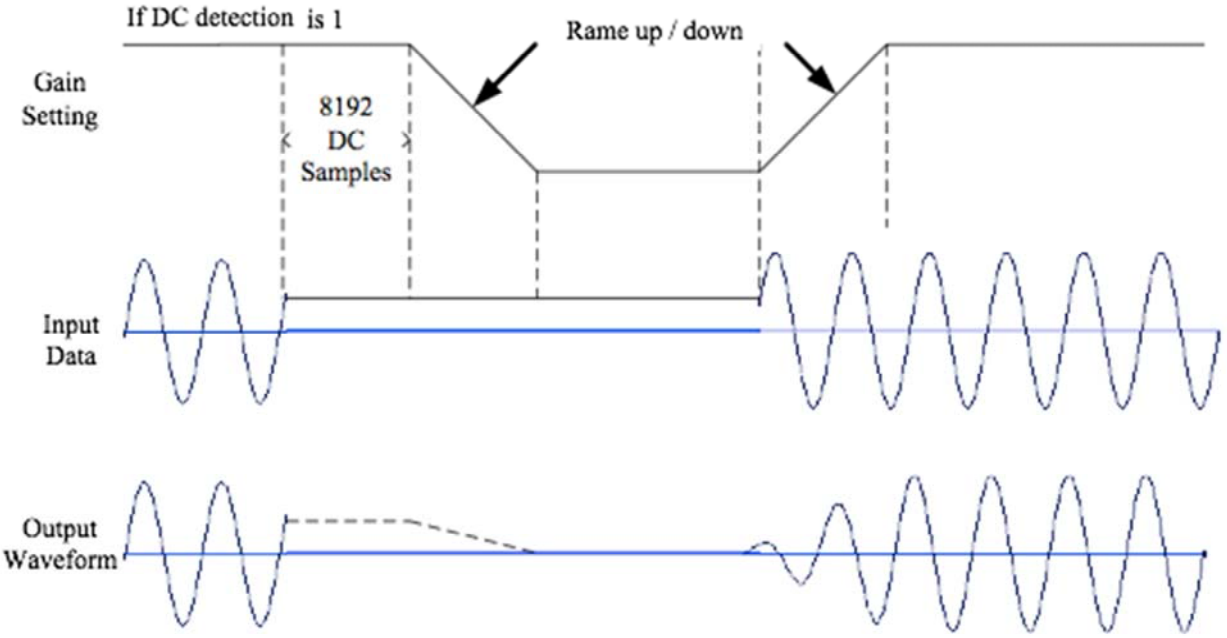
GPIOs	Description
GPIO0	Volume up (level trigger)
GPIO1	Volume down (level trigger)
GPIO2	Mute / Un-Mute (edge trigger)
GPIO3	Play / Pause (edge trigger)
GPIO4	Scan next track (edge trigger)
GPIO5	Scan previous track (edge trigger)
GPIO6	Stop (edge trigger)
GPIO [9, 8, 7]	Sampling rate encoded 000: 48KHz 001: 44.1KHz 010: 32KHz 100: 88.2KHz 101:96KHz
GPIO10	16/24 bit resolution 0: 16Bit 1: 24Bit
GPIO11	Playback status 0: playback OFF 1: playback ON

Volume Control and Soft mute Function

For playback stream, SA9023 can adjust volume gain range from 0dB to -55fB and mute. SA9023 also support disable “Volume Control Function” by external EEPROM which need USB Descriptor Software Tool.

For “Soft mute”, SA9023 support DC detection for soft mute / unmute. This function need enabled by external EEPROM which need USB Descriptor Software Tool.

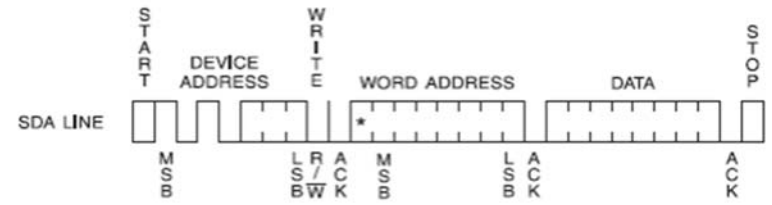
If the data is a constant value for 8192 samples, a ramp down process begins to attenuate the volume from the current setting down to mute. When the data changes, a ramp up process begins to amplify the volume from mute up to the original setting.



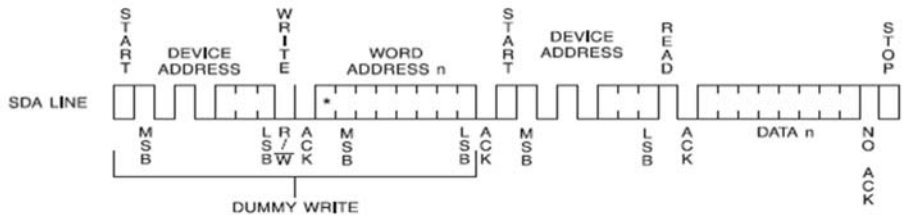
I2C Slave Function

SA9023 provided an I2C slave function which is used for CPU to read information or program some registers.This mode need to enable by EEPROM that need USB descriptor software tool. Default setting is disabled.

Byte Write



Random Read



Set SPDIF TX status

S/PDIF TX control register 0
Offset 0
Length: 1 byte

Bit	Type	Reset	Description
7:3	RW	0	Reserved
2	RW	0	S/PDIF TX control registers (offset 0 to 2) enable 1: Enable 0: Disable **(S/PDIF TX function cannot be controlled by I2CS)**
1	RW	0	1: Force TX data to 0 when Validity (bit 0) is 1 and bit 1 in offset 6h is 0 (PCM data) 0: Do not change data when Validity is 1. (default) This bit is for the SCMS compatibility issues sometimes found when interfacing with MD devices.
0	RW	0	Validity: This bit affects the “Validity Flag”, bit 28 transmitted in each sub frame, and enables the S/PDIF transmitter to maintain connection during error or mute conditions.

S/PDIF TX control register 1
Offset 1
Length: 1 byte

Bit	Type	Reset	Description
7:4	RW	0s	S/PDIF Sample Rate For Channel Status (Byte 3, bit [3:0] for Consumer Mode.) (Byte 0, bit [7:6] for Professional Mode.) 4'b0011: 32KHz 4'b0000: 44.1KHz 4'b0010: 48KHz 4'b1000: 88.2KHz 4'b1010: 96KHz Note: In professional mode, only 44.1K, 48K & 32K are reported in the Channel Status bit. (Byte 0, bit [7:6]) 2'b01: 44.1KHz 2'b10: 48KHz 2'b11: 32KHz 2'b00: Others This indicates other sample rates, not representable in byte 0 bits 6–7 In professional mode, 88.2K, 96K are reported in the Channel Status bit (Byte 4, bit [6:3]) 4'b0000: Not indicated (default) 4'b0010: 96KHz 4'b1010: 88.2KHz
3	RW	0	Pre-emphasis 0: None – 2 channel audio 1: 50/15us – 2 channel audio
2	RW	0	Copyright (Copy) 1: Non-copyright 0: Copyright
1	RW	0	Reserved.
0	RW	0	Professional mode (PRO) 1: Professional mode 0: Consumer mode

S/PDIF TX control register 2
Offset 2
Length: 1 byte

Bit	Type	Reset	Description
7	RW	0	Generation Level (L)
6:0	RW	0	Category code[6:0]

Get SPDIF RX status

S/PDIF RX control registers 0
Offset 3
Length: 1 bytes

Bit	Type	Reset	Description
7	RO	0	Reserved
6:4	RO	001	S/PDIF Sample Rate Decoded by Hardware 3'b001 : 44.1K 3'b000: 48K 3'b100: 88.2K 3'b101: 96K 3'b010: 32K
3:0	RO	0s	S/PDIF Sample Rate reported from channel status bit 4'b0000: 44.1KHz 4'b0010: 48KHz 4'b0011: 32KHz 4'b1000: 88.2KHz 4'b1010: 96KHz

S/PDIF RX control registers 1
Offset 4
Length: 1 bytes

Bit	Type	Reset	Description
7	RW	0	Reserved
6	RO	0	Lock Status 1: S/PDIF RX input is locked 0: S/PDIF RX input is unlocked
5	RO	0	Validity
4	RO	0	Generation Level
3	RO	0	Pre-emphasis
2	RO	0	Copyright 1: Non-copyright 0: Copyright
1	RO	0	Non-Audio Samples 1: Non-PCM audio samples 0: Linear PCM samples
0	RO	0	Professional mode 1: Professional mode 0: Consumer mode

S/PDIF RX control registers 2
Offset 5
Length: 1 bytes

Bit	Type	Reset	Description
7	RW	0	Reserved
6:0	RO	0	Category code

Sampling rate and resolution

Sampling Rate and resolution register
Offset 6
Length: 1 bytes

Bit	Type	Reset	Description
7:5	RO	000	Record stream sampling rate 000: 48KHz 001: 44.1KHz 010: 32KHz 100: 88.2KHz 101: 96KHz
4	RO	0	Record stream resolution 0: 16-bit 1: 24-bit
3:1	RO	000	Playback stream sampling rate 000: 48KHz 001: 44.1KHz 010: 32KHz 100: 88.2KHz 101: 96KHz
0	RO	0	Playback stream resolution 0: 16-bit 1: 24-bit

SAR ADC register

Offset 10h

Length: 1 bytes

Bit	Type	Reset	Description
7~5	R	0	Reserved
4	R	0	ADC[4]
3	R	0	ADC[3]
2	R	0	ADC[2]
1	R	0	ADC[1]
0	R	0	ADC[0]

External EEPROM Support

After power up, the I2C interface will read the external EEPROM to load customer specific descriptor data. The hardware automatically detects if there's an EEPROM populated on the board. If there's a valid ACK response from the EEPROM, SA9023 continues to read the EEPROM to decide whether the EEPROM has been programmed correctly.
If the data match, the EEPROM data content is considered valid, and the hardware will continue to read data for USB HOST request. Otherwise it switches automatically and read the internal ROM data.

Electrical Specifications

Maximum Ratings Electrical Specifications

Parameter		Min	Typ	Max	Unit
Storage Temperature				150	°C
Opera)ng Ambient Temperature		0		70	°C
DC Supply Voltage (Analog and Digital)		80.3		3.8	V
I/O Pin Voltage		80.3		VDD+0.3	V
Power Dissipation (θJA= 67°C/W)	Where Ambient Temperature = 25°C			1.5	W

Electrical Specifications DC Characteristics (TA=25°C, VDD = 3.3V ± 5%; GND = 0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Input Voltage Range	0		VDD	V
VIL	Input Low Voltage			0.3 x VDD	V
VIH	Input High Voltage	0.7 x VDD			V
VOL	Output Low Voltage		0	0.4	V
VOH	Output High Voltage	2.4	VDD		V
IIL / IIH	Input Leakage Current (include pull8up/ down pins)			60	µA
IOT	Output Tristate Leakage Current	81		1	µA
IOL	Output Buffer Sink Current	4			mA
IOH	Output Buffer Drive Current			84	mA

Power Consumption (TA=25°C, VDD = 3.3V ± 5%; GND = 0V; 50pF Load, 96KHz 24bit)

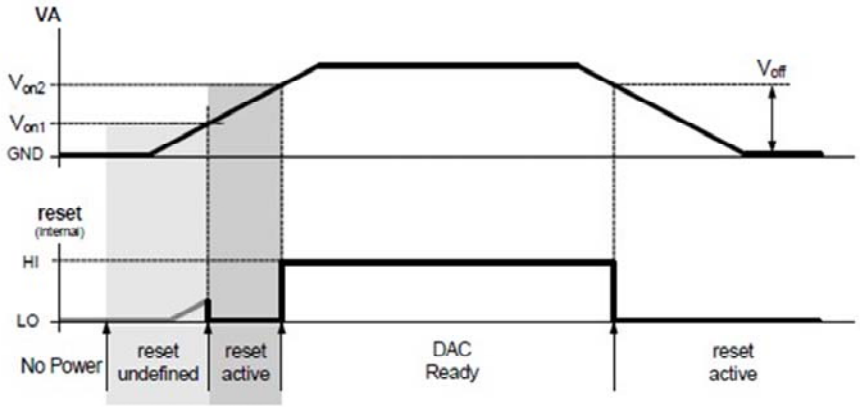
Symbol	Parameter	Min	Typ	Max	Unit
IVDD	Supply Current: Power Up		20		mA

INTERNAL POWER-ON RESET THRESHOLD VOLTAGES

Test conditions (unless otherwise specified): GND = 0 V; all voltages with respect to ground.

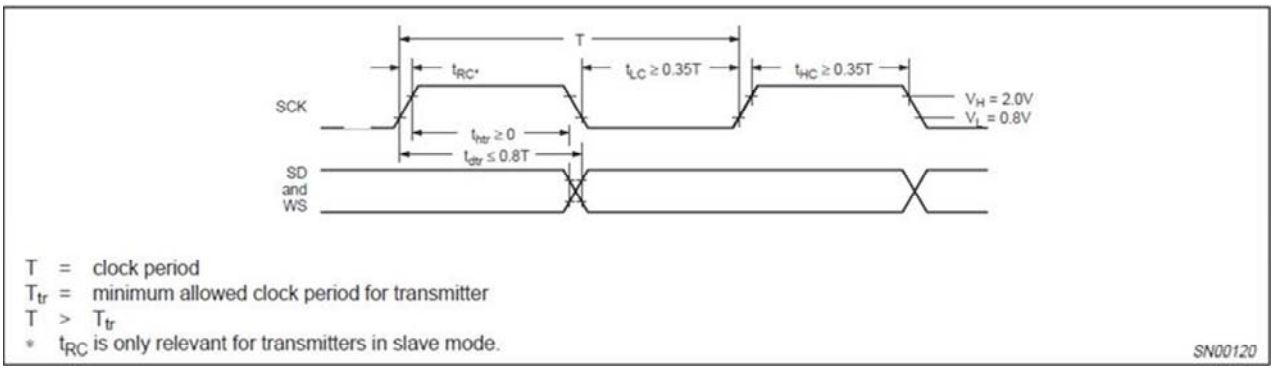
Parameters	Symbol	Min	Typ	Max	Units
Internal reset asserted at power-on	V_{on1}	-	0.2	-	V
Internal reset released at power-on	V_{on2}	-	3.6	-	V
Internal reset asserted at power-off	V_{off}	-	3.1	-	V

Power-On Reset Threshold Voltages



Power-On Reset Threshold Sequence

Timing for I2S Transmitter



44.1KHz

Master transmitter with data rate of 2.8224MHz(all values in ns)

Symbol	Parameter	Min	Typ	Max	Unit
T	Clock Period (354.3ns)	353.9ns		354.8ns	ns
tHC	clock HIGH		177ns		ns
tLC	clock LOW		177ns		ns
tdtr	delay		184ns		ns
thtr	hold time		180ns		ns
tRC	clock rise-time		6ns		ns

48KHz

Master transmitter with data rate of 3.072MHz(all values in ns)

Symbol	Parameter	Min	Typ	Max	Unit
T	Clock Period (325.52ns)	324.8ns		325.9ns	ns
tHC	clock HIGH		162ns		ns
tLC	clock LOW		162ns		ns
tdtr	delay		176ns		ns
thtr	hold time		160ns		ns
tRC	clock rise-time		6ns		ns

88.2KHz

Master transmitter with data rate of 5.6448MHz(all values in ns)

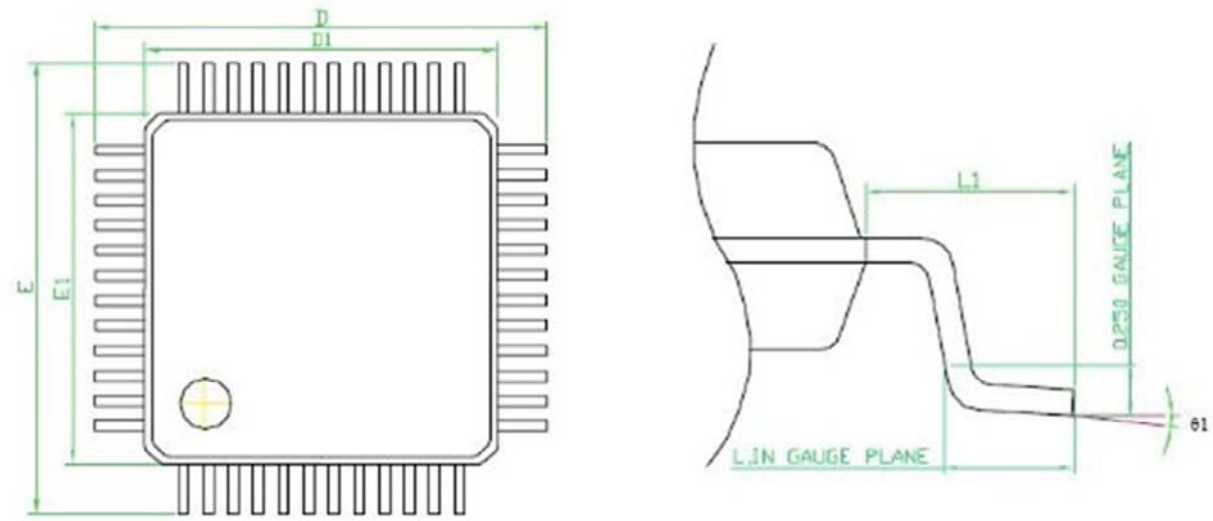
Symbol	Parameter	Min	Typ	Max	Unit
T	Clock Period (177.15ns)	176.5ns		177.5ns	ns
tHC	clock HIGH		88ns		ns
tLC	clock LOW		88ns		ns
tdtr	delay		100ns		ns
thtr	hold time		86ns		ns
tRC	clock rise-time		6ns		ns

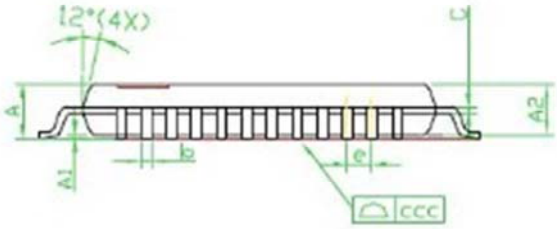
96KHz

Master transmitter with data rate of 6.144MHz(all values in ns)

Symbol	Parameter	Min	Typ	Max	Unit
T	Clock Period (162.76ns)	162.4ns		163ns	ns
tHC	clock HIGH		81ns		ns
tLC	clock LOW		81ns		ns
tdtr	delay		94ns		ns
thtr	hold time		82ns		ns
tRC	clock rise-time		6ns		ns

TQFP-48 MECHANICAL DATA





SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.006	0.008	0.011
C	0.09	-----	0.20	0.003	----	0.008
D1	6.90	7.00	7.10	0.271	0.275	0.279
D	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.90	7.00	7.10	0.271	0.275	0.279
E	8.80	9.00	9.20	0.346	0.354	0.362
e	—	0.50(TYP)	—	—	0.02(TYP)	—
L	0.45	0.60	0.75	0.018	0.024	0.029
L1	—	1.00(REF)	—	—	0.039(REF)	—
θ1	0°	3.5°	7°	0°	3.5°	7°
ccc	----	----	----	----	----	0.0035