

## CDB43198K Kit Manual

### Features

- Configurable serial audio headers for PCM, DSD and DoP audio
- Headphone and line outputs
- Analog and S/PDIF audio input
- USB audio module capability
- WISCE™ I<sup>2</sup>C-based software control
- Windows® compatible

### Description

The CDB43198K is a dedicated platform for testing and evaluating the CS43198. The CS43198 is a high-performance audio DAC with integrated impedance detection and headphone drivers. To allow comprehensive testing and evaluation of the performance of the CS43198, extensive software-configurable options are available through the CDB43198 evaluation kit. The kit also included the CDB-HDR-MEAS, for measuring the 130 dB dynamic range performance of the CS43198.

Software options, such as register settings for the CS43198, are configured via the WISCE software tool, which communicates with the CDB43198K via an Aardvark I<sup>2</sup>C/SPI host adapter from a Windows computer, or via Mini-USB cable.

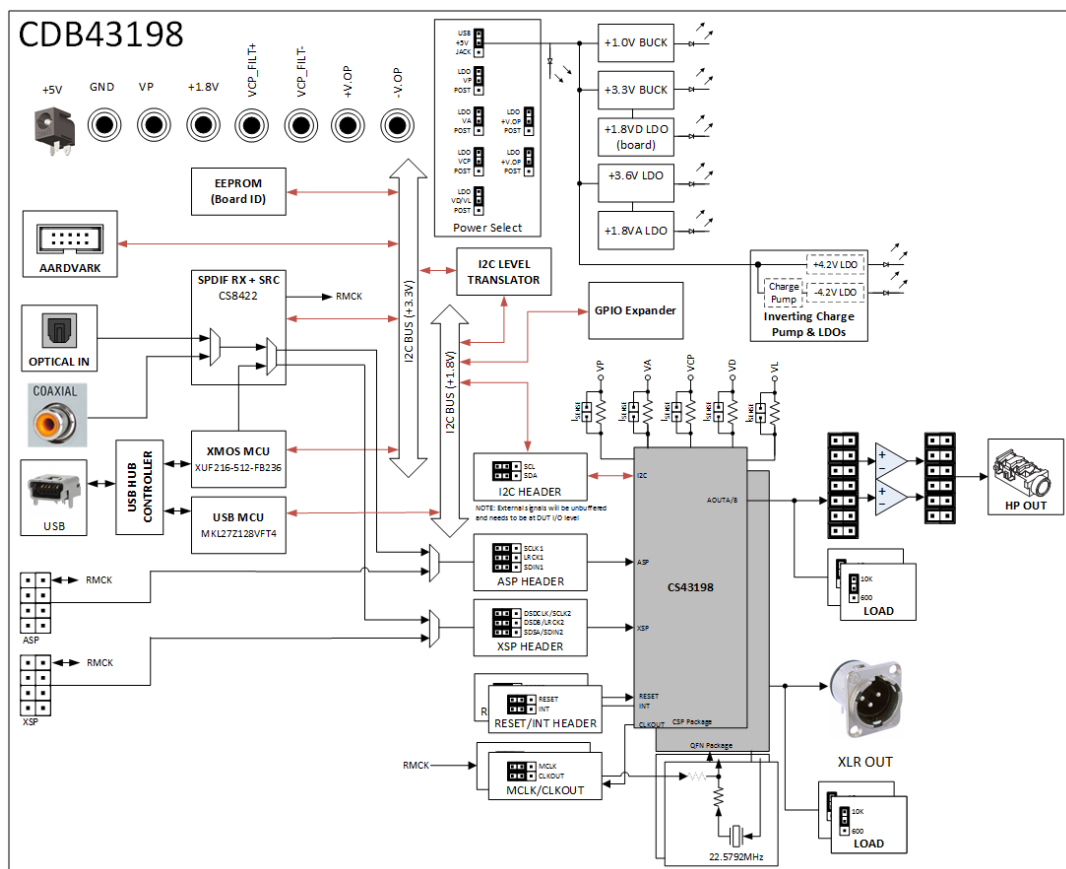


Figure 1 CDB43198 Board Block Diagram

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## 1 CDB43198K Kit Overview

The CDB43198K kit consists of an evaluation board, a high dynamic range (HDR) measurement board, and a USB cable. Each of these component boards is described in the following sections.

### 1.1 CDB43198 Board

The CDB43198 is shown in the following figure.

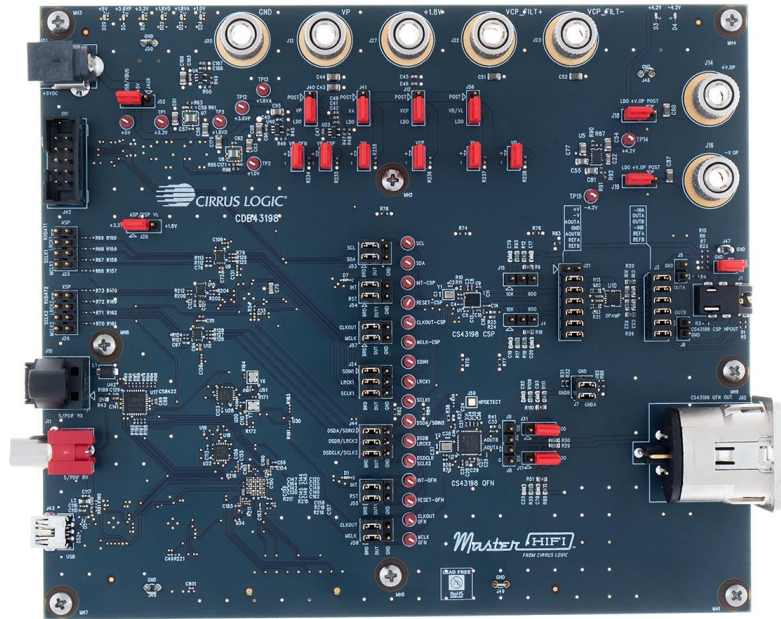


Figure 2 CDB43198 Base Board

### 1.2 CDB-HDR-MEAS Board

The CDB-HDR-MEAS is shown in the following figure. This board is used for measuring the very low HDR of the device with an Audio Precision SYS-2700 or APx555 audio analyzer.



Figure 3 CDB-HDR-MEAS Board

## 2 CDB43198 Board Overview

The CDB43198 is the board for evaluating the performance of the CS43198. It supports multiple power supplies and signal I/O configurations.

The CDB43198 board uses five buffers with direction control to direct clock from the digital input sources to/from the CS43198 DUTs. Two buffers, the PCM/DoP buffer and the DSD/DoP buffer, support voltage translation from 3.3 V to 1.8 V and vice versa. The voltage selection is done through headers: J28 for the PCM/DoP buffer and the DSD/DoP buffer. The S/PDIF buffer is a unidirectional buffer and supports 3.3 V to 1.8 V translation. The remaining buffers only support 1.8 V signals. These buffers are controlled by an I/O Expander. The I/O Expander can be controlled through its I<sup>2</sup>C interface. The register map for I/O Expander is described in [Section 3](#). The direction of clock signals is determined by the CS43198's operating mode (master or slave mode).

The CDB43198 can also communicate with a smart codec through the use of J42. The purpose of using a smart codec is to allow the user to perform listening tests with various equalizer (EQ) filters based on the impedance of the attached headphone. The CDB43198 board allows the PCM input to be routed to the smart codec. The codec can then apply an EQ filter on this data, based on the impedance of the attached headphone and send EQ-filtered data to the CS43198, for an optimal listening experience. The following diagram shows an overview of the CDB43198 board.

Since the CDB43198 does not have an integrated headphone driver, there is an OPA1622 High-Fidelity Audio Amplifier on the output of the CSP device, which is able to drive headphone type loads.

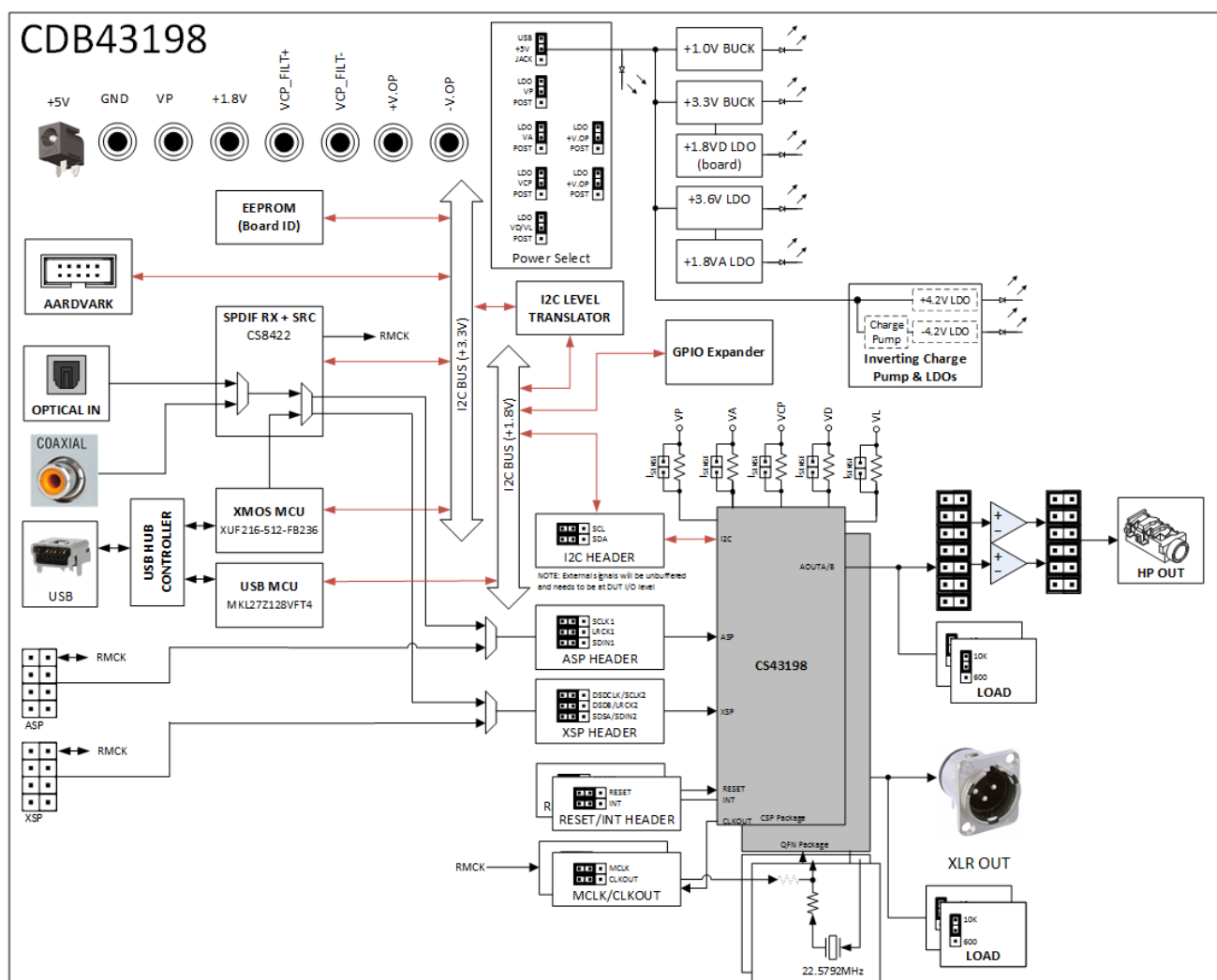


Figure 4 CDB43198 Block Diagram

## 2.1 Power Supply Circuitry

The CDB43198 board is powered from a 5-volt, 1.2-amp AC adapter. All the supply rails for both the smart codec and the CS43198s are generated using a combination of switched-mode power supplies (switchers) and LDOs. In addition to these internal supplies, the CDB43198 board also provides the option of powering the CS43198 supply rails from external bench supplies via banana jacks.

The switchers and LDOs step down the +5 V supply to 3.6 V, 3.3 V, 1.0 V, 1.8 V (analog), and 1.8 V (digital) levels.

If the device is set into External VCP\_FILT Supply Mode and bypass the internal Class-H charge pump circuit, then a  $\pm 3$ -volt supply must be applied to VCP\_FILT+ and VCP\_FILT-. The banana jacks are connected to each device through a set of resistors (R24/R25 for the CSP device, and R40/R41 for the QFN device). These resistors are unpopulated by default and will need to be populated with a 0- $\Omega$  resistor to connect the jack to the DUT.

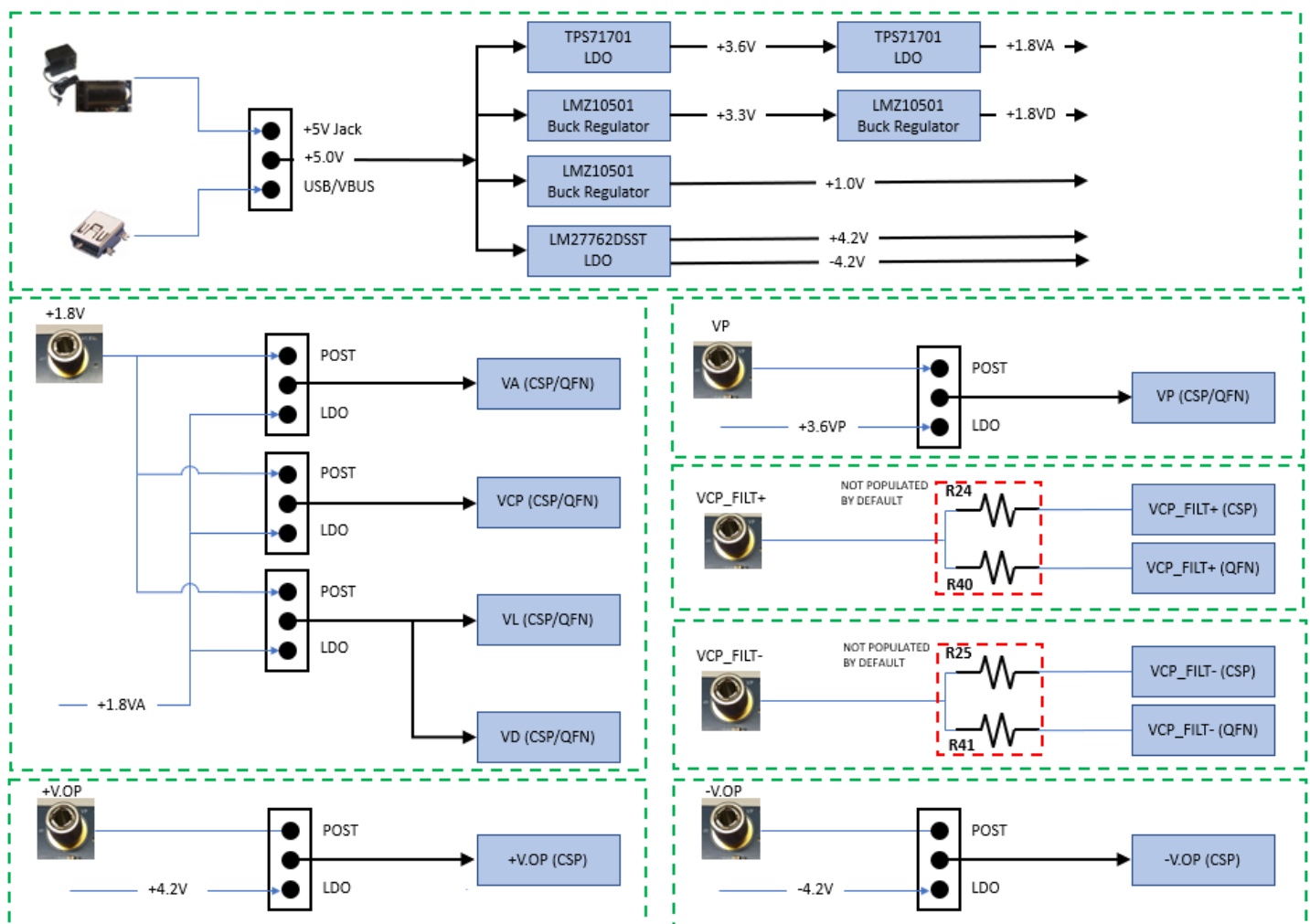


Figure 5 CDB43198 Power Supplies

## 2.2 Digital Audio Input

### 2.2.1 Serial Audio I/O Headers

Headers J25 and J26, labeled ASP and XSP respectively, provide an interface for serial audio clocks and data. The source of the clocks and data can be an external audio source such as a Audio Precision audio analyzer. The header signals are described in the table below. The logic level on these pins is selectable by jumping J28 to 3.3 V or 1.8V.

**Table 1 Serial Audio Header Pinout**

| Reference Designator | Pins    | Pin Designation | Direction        | Description  |
|----------------------|---------|-----------------|------------------|--------------|
| J25                  | 7       | MCLK            | I/O              | Master clock |
|                      | 5       | SCLK            | I/O              | Bit clock    |
|                      | 3       | LRCLK           | I/O              | Frame clock  |
|                      | 1       | RXDAT           | Input            | Serial data  |
|                      | 2,4,6,8 | Ground          | Ground reference | Board ground |
| J26                  | 7       | MCLK            | I/O              | Master clock |
|                      | 5       | SCLK            | I/O              | Bit clock    |
|                      | 3       | LRCLK           | I/O              | Frame clock  |
|                      | 1       | RXDAT           | Input            | Serial data  |
|                      | 2,4,6,8 | Ground          | Ground reference | Board ground |

Audio signals to/from these headers are routed to/from the CS43198 using voltage-level translation buffers. The direction of clock and data through these buffers is controlled using on-board TCA6424 I/O Expander IC. U9, U12, and U15 translate the signals on J25 and J26 from a voltage of 3.3 V or 1.8 V to the operational voltage of 1.8 V. The ASP signals are then fed into J24, while the XSP signals are fed into J44. These 3x3 pin headers are for passing the I<sup>2</sup>S data from the CS8422 S/PDIF transceiver to the DUTs.

To avoid the latency caused by buffers for higher clock frequencies like 352.8 kHz or 384 kHz, the user can connect the external audio source directly to pins on headers J24 and J44. The pinouts for headers J24 and J44 are shown in the following tables.

**Table 2 Pinouts for Header J24**

| Pin # | Signal             |
|-------|--------------------|
| 1     | SCLK1 from Buffer  |
| 2     | SCLK1 to DAC       |
| 4     | LRCLK1 from Buffer |
| 5     | LRCLK1 to DAC      |
| 7     | SDIN1 from Buffer  |
| 8     | SDIN1 to DAC       |
| 3,6,9 | Ground             |

**Table 3 Pinouts for Header J44**

| Pin # | Signal             |
|-------|--------------------|
| 1     | SCLK2 from Buffer  |
| 2     | SCLK2 to DAC       |
| 4     | LRCLK2 from Buffer |
| 5     | LRCLK2 to DAC      |
| 7     | SDIN2 from Buffer  |
| 8     | SDIN2 to DAC       |
| 3,6,9 | Ground             |

To source the signals from the output of the buffers to the DAC, place jumpers between the two columns of pins labeled BRD and DUT. For example, in order to send SCLK1, LRCLK1 and SDIN1 signals from the buffer to the DAC, place jumpers between pins of the BRD and DUT group as shown in the following figure.

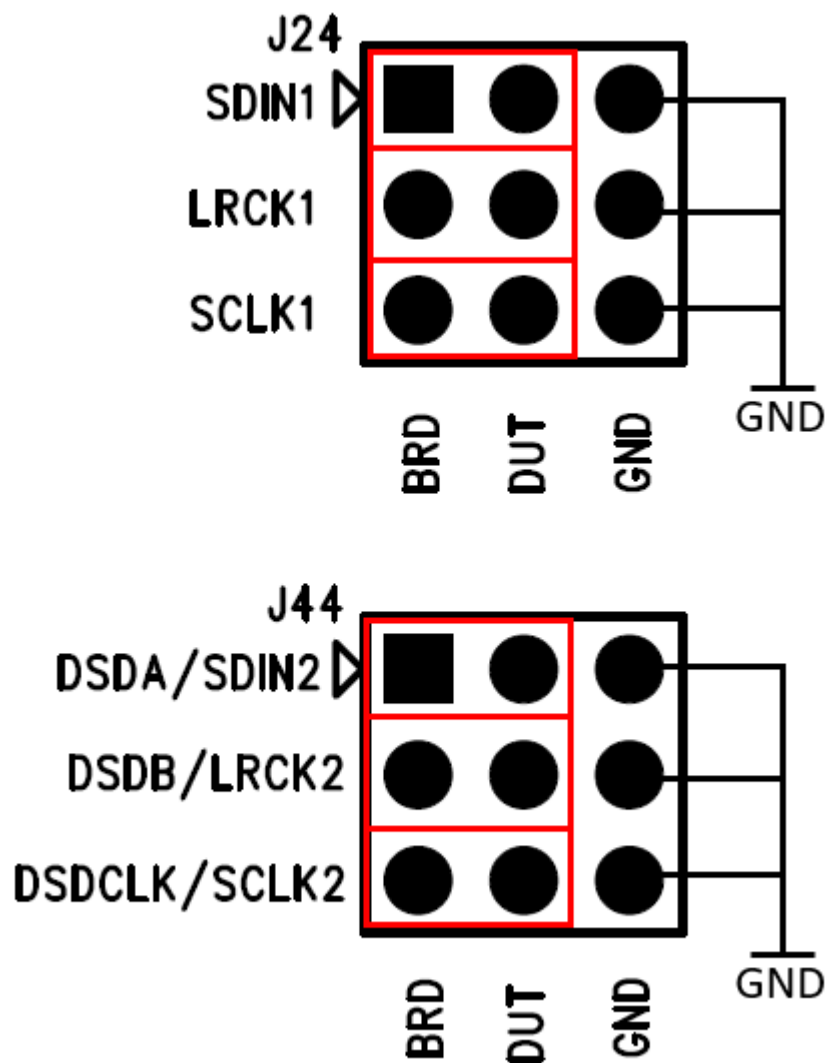


Figure 6 Jumper Settings to Route Signals from Buffers to DUT



To source the signals from external audio source like a Audio Precision APx555, connect the cable that fits onto a 2-pin header onto the pins labeled DUT and GND. For example, in order to send SCLK1, LRCLK1 and SDIN1 signals from a APx to the DAC, connect the BITCLK output from the APx to the SCLK1 pins in the AP group, Frame CLK output from the APx to LRCLK1 pins in the AP group, and the RXDAT1 output from the APx to SDIN1 pins in the AP group as shown in the following figure.

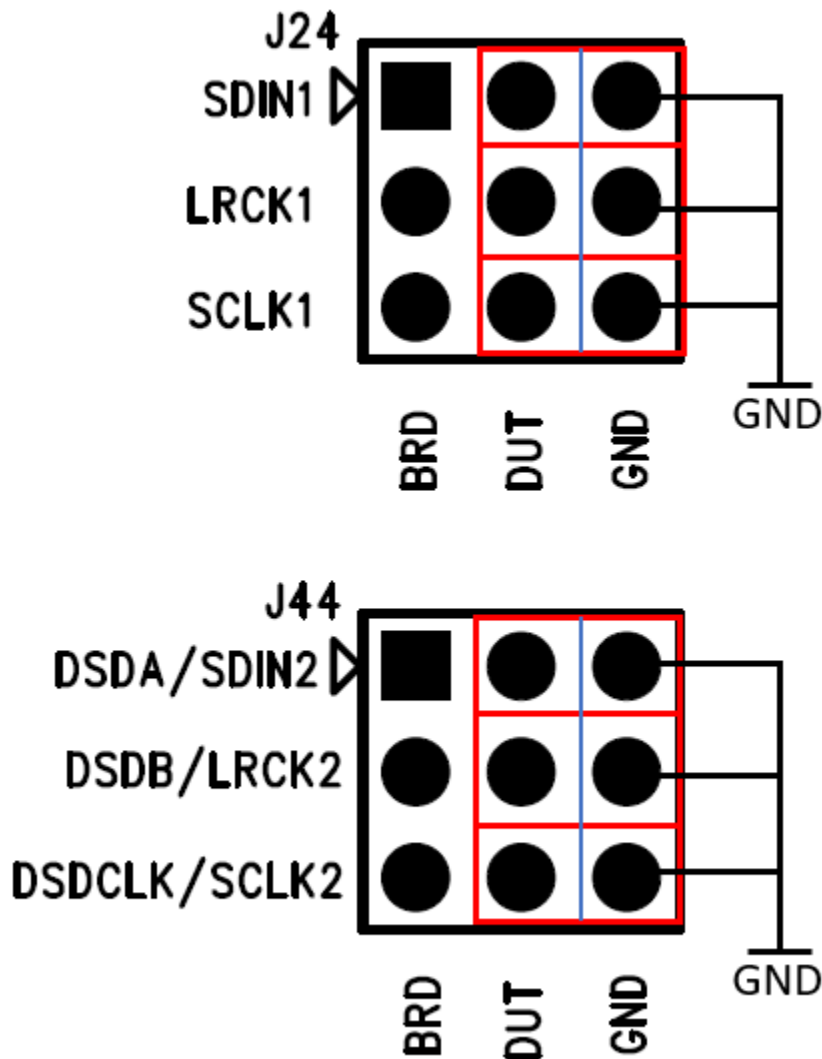


Figure 7 External Audio Source to DUT

## 2.2.2 S/PDIF Receiver

The CS8422 S/PDIF receiver provides two-channel digital input either from an optical or coax connector. The CS8422 can support sample rates up to 211 kHz and data output with either 16-, 18-, 20-, or 24-bit word lengths. The user should make sure that only one source, either S/PDIF or coax, is used at one time to provide the input. The CS8422 is configured to operate in Hardware Mode.



## 2.3 Analog Audio Output

The CDB43198 board has one 1/8" stereo headphone output jack (J1) for the CSP and one XLR cable output jack (J60) for the QFN.

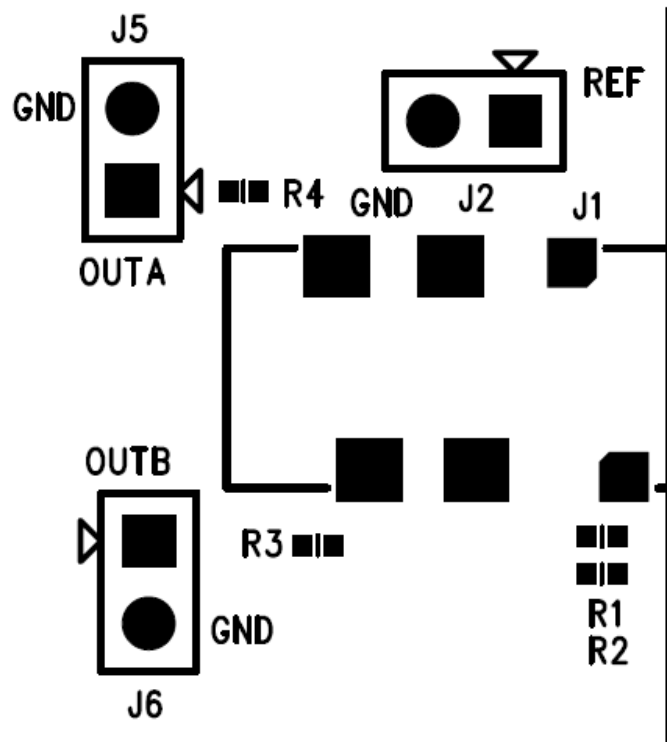
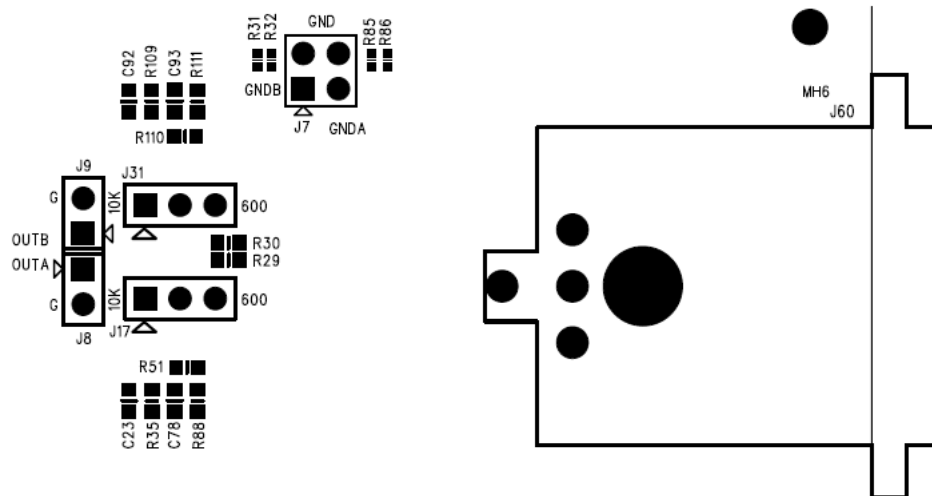
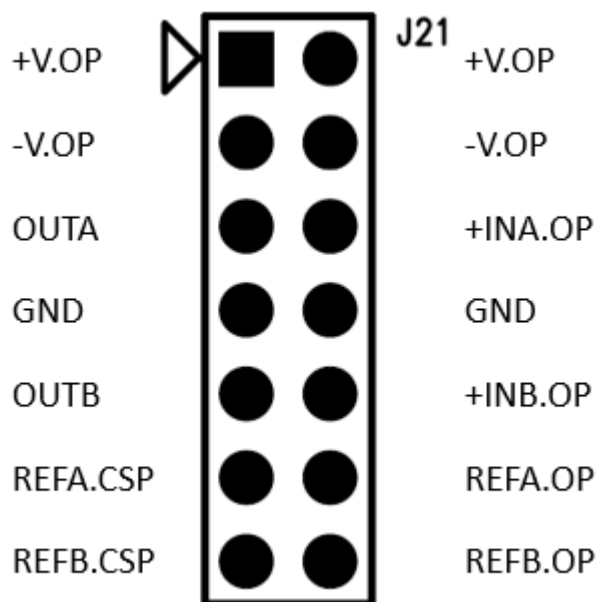


Figure 8 1/8" Headphone Jack/APx Connectors/Loading Jumpers for CSP



## 2.4 OPA1622 Output

On the CS43198-CSP, there is a OPA1622 high-fidelity audio opamp. This is used for driving headphone loads of 600  $\Omega$  or less. The opamp is dual channel, with 1 channel connected to OUTA and the other channel connected to OUTB. The opamp circuit connects to the CS43198 through header J21. The signal mapping is shown below. By default, the jumpers are installed horizontally.

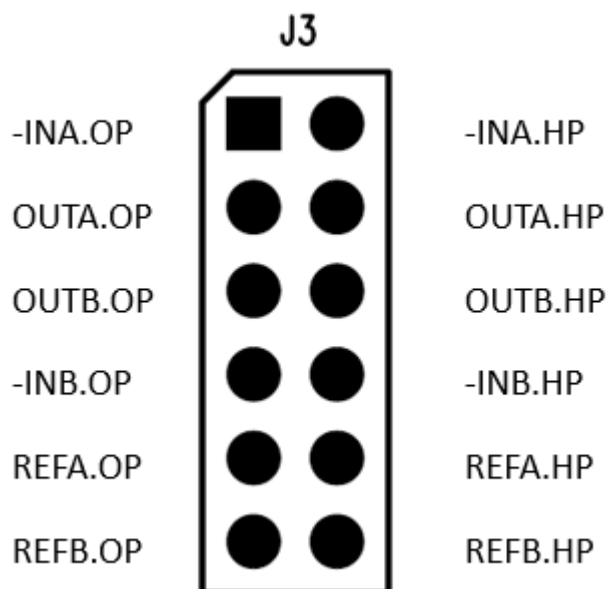


**Figure 9 J21 Opamp Header**

**Table 4 J21 Header Pinout**

| Header | Pins | Designation | Description                                      |
|--------|------|-------------|--------------------------------------------------|
| J42    | 1, 2 | +V.OP       | +4.2 V OP-AMP Power                              |
|        | 3, 4 | -V.OP       | -4.2 V OP-AMP Power                              |
|        | 5    | OUTA        | Signal coming from OUTA of the CS43198           |
|        | 6    | +INA.OP     | Input to OP-AMP-A (Non-Inverting)                |
|        | 7, 8 | GND         | Ground                                           |
|        | 9    | OUTB        | Signal coming from OUTB of the CS43198           |
|        | 10   | +INB.OP     | Input to OP-AMP-B (Non-Inverting)                |
|        | 11   | REFA.CSP    | OUTA Reference                                   |
|        | 12   | REFA.OP     | OUTA reference passing through the opamp section |
|        | 13   | REFB.CSP    | OUTB Reference                                   |
|        | 14   | REFB.OP     | OUTA reference passing through the opamp section |

The output stage of the opamp connects to the headphone jack J1 through header J3. The signal mapping is shown below. By default, the jumpers are installed horizontally.



**Figure 10 J3 Opamp Header**

**Table 5 J3 Header Pinout**

| Header | Pins | Designation | Description                                         |
|--------|------|-------------|-----------------------------------------------------|
| J42    | 1    | -INA.OP     | Input to OP-AMP-A (Inverting)                       |
|        | 2    | -INA.HP     | Reference from HP Jack for Inverting OP-AMP-A Input |
|        | 3    | OUTA.OP     | Output of OP-AMP-A                                  |
|        | 4    | OUTA.HP     | Output of OP-AMP-A to Channel A of Headphone Jack   |
|        | 5    | OUTB.OP     | Output of OP-AMP-B                                  |
|        | 6    | OUTB.HP     | Output of OP-AMP-B to Channel B of Headphone Jack   |
|        | 7    | -INB.OP     | Input to OP-AMP-B (Inverting)                       |
|        | 8    | -INB.HP     | Reference from HP Jack for Inverting OP-AMP-B Input |
|        | 9    | REFA.OP     | OUTA Reference passing through the OP-AMP Section   |
|        | 10   | REFA.HP     | GND Headphone Reference for CS43198                 |
|        | 11   | REFB.OP     | OUTB Reference passing through the OP-AMP Section   |
|        | 12   | REFB.HP     | GND Headphone Reference for CS43198                 |

## 2.5 I<sup>2</sup>C Control

Header J42 (labeled I<sup>2</sup>C/SPI) provides an interface to connect a Total Phase Aardvark I<sup>2</sup>C/SPI Host Adapter. The header signals are described in the following table. The logic level on these pins is 3.3 V. Through this header, a user can communicate with a smart codec, the TCA6424 I/O Expander, and the CS43198.

**Table 6 I<sup>2</sup>C/SPI Header Pinout**

| Header | Pins  | Designation | Description             |
|--------|-------|-------------|-------------------------|
| J42    | 1     | I2C SCL     | I <sup>2</sup> C clock  |
|        | 3     | I2C SDA     | I <sup>2</sup> C data   |
|        | 5     | SPI MISO    | SPI master in slave out |
|        | 7     | SPI SCLK    | SPI clock               |
|        | 9     | SPI SS      | SPI chip select         |
|        | 8     | SPI MOSI    | SPI master out slave in |
|        | 2, 10 | GND         | Ground reference        |
|        | 4, 6  | NC          | No connect              |

## 2.6 LEDs

The status LEDs on the CDB43198 board show the status of the power rails and S/PDIF input. A summary of the LEDs is shown in the table below.

**Table 7 Status LEDs**

| LED Function | LED Reference | LED Color | Description                  |
|--------------|---------------|-----------|------------------------------|
| INT_QFN      | D1            | Orange    | Interrupt from QFN           |
|              |               | OFF       | No Interrupt                 |
| +3.6VP       | D2            | Green     | Presence of +3.6 V rail      |
| +4.2V        | D3            | Green     | Presence of +4.2 V rail      |
| -4.2V        | D4            | Green     | Presence of -4.2 V rail      |
| VP           | D7            | Orange    | Interrupt from CSP           |
|              |               | OFF       | No Interrupt                 |
| +5V          | D20           | Green     | Presence of the +5 V rail    |
| +3.3V        | D21           | Green     | Presence of the +3.3 V rail  |
| +1.8VD       | D22           | Green     | Presence of the +1.8 VD rail |
| +1.8VA       | D23           | Green     | Presence of the +1.8 VA rail |
| +1.0V        | D24           | Off       | Presence of the +1.0 V rail  |

## 2.7 List of Headers and Jumper Settings

The following table lists all the available headers, jacks, and plugs on CDB43198 board.

**Table 8 Header and Jumper Settings**

| Reference Designator | Connection            | Type                  | I/O | Description                                                                                                                                                               |
|----------------------|-----------------------|-----------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| J1                   | CSP-AOUT              | 3.5-mm headphone jack | O   | The headphone out jack for the CS43198 CSP device                                                                                                                         |
| J2                   | CSP-AOUT-REF          | 2x1 header            | —   | This header is for tying HPREF(A/B) to GND                                                                                                                                |
| J3                   | CSP-OP AMP-OUT        | 6x2 header            | —   | This header is for connecting the output of the op-amp circuit to the Headphone output.                                                                                   |
| J4                   | CSP-AOUTB Loading     | 3x1 header            | —   | Selectable loading resistance of 600/10k $\Omega$ for CSP-AOUTB                                                                                                           |
| J5                   | CSP-AOUTA Test Point  | 2x1 header            | O   | 2-pin test point for Audio Precision                                                                                                                                      |
| J6                   | CSP-AOUTB Test Point  | 2x1 header            | O   | 2-pin test point for Audio Precision                                                                                                                                      |
| J7                   | QFN-GND-REF-SEL       | 2x2 header            | —   | Jumper between 1-3 and 2-4 to make outputs differential. Jumper between 1-2 and 3-4 to make outputs single ended                                                          |
| J8                   | QFN-AOUTA Test Point  | 2x1 header            | O   | 2-pin test point for Audio Precision                                                                                                                                      |
| J9                   | QFN-AOUTB Test Point  | 2x1 header            | O   | 2-pin test point for Audio Precision                                                                                                                                      |
| J10                  | Optical S/PDIF IN     | Optical connector     | I   | Optical connector for S/PDIF Signals                                                                                                                                      |
| J11                  | Coaxial S/PDIF IN     | RCA connector         | I   | Coaxial connector for S/PDIF Signals                                                                                                                                      |
| J12                  | VCP Source Select     | 3x1 header            | —   | Jumper between 1-2 to get VCP from 1.8 V banana jack (J27). Jumper between 2-3 to get VCP from 1.8 VA LDO                                                                 |
| J13                  | VP Banana Jack        | Banana jack           | I   | External source for 3.6 VP                                                                                                                                                |
| J14                  | +V.OP Banana Jack     | Banana jack           | I   | External source for +4.2V rail for external OP AMP                                                                                                                        |
| J15                  | CSP-AOUTA Loading     | 3x1 header            | —   | Selectable loading resistance of 600/10k $\Omega$ for CSP-AOUTA                                                                                                           |
| J16                  | -V.OP Banana Jack     | Banana jack           | I   | External source for -4.2V rail for external OP AMP                                                                                                                        |
| J17                  | QFN-AOUTA Loading     | 3x1 header            | —   | Selectable loading resistance of 600/10k $\Omega$ for QFN-AOUTA                                                                                                           |
| J18                  | +V.OP Source Select   | 3x1 header            | —   | Jumper between 1-2 to get +V.OP from +4.2 V banana jack (J14). Jumper between 2-3 to get +V.OP from +4.2V regulator                                                       |
| J19                  | -V.OP Source Select   | 3x1 header            | —   | Jumper between 1-2 to get +V.OP from +4.2 V banana jack (J16). Jumper between 2-3 to get -V.OP from -4.2V regulator                                                       |
| J20                  | GND Banana Jack       | Banana jack           | I   | GND                                                                                                                                                                       |
| J21                  | CSP-OP AMP-IN         | 7x2 header            | —   | This header is for connecting the output of the CS43198 CSP to the OP AMP Input                                                                                           |
| J22                  | VCP_FILT+ Banana Jack | Banana jack           | I   | External source for VCP_FILT+                                                                                                                                             |
| J23                  | VCP_FILT- Banana Jack | Banana jack           | I   | External source for VCP_FILT-                                                                                                                                             |
| J24                  | ASP DUT Connection    | 3x3 header            | —   | Connect shunt between (DUT-BRD) to connect DUT and ASP data. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure ASP data directly |
| J25                  | ASP DATA              | 2x4 header            | I/O | Header for MCLK1/LRCLK1/SCLK1/RX Data1                                                                                                                                    |
| J26                  | XSP DATA              | 2x4 header            | I/O | Header for MCLK2/LRCLK2/SCLK2/RX Data2                                                                                                                                    |
| J27                  | 1.8V Banana Jack      | Banana jack           | I   | External Source for +1.8 V                                                                                                                                                |
| J28                  | ASP/XSP VL            | 3x1 header            | —   | Shunt between pins 1-2 for ASP/XSP to be translated to 3.3 V. Shunt between pins 2-3 for ASP/XSP to be translated to 1.8 V                                                |
| J29 (Rev B Only)     | USB Data Select       | 3x1 header            | —   | If ENABLE is selected, the CDB will use the USB connection for data and power. If DISABLE is selected, the CDB will use the USB connection for power only.                |

| Reference Designator | Connection                          | Type                       | I/O | Description                                                                                                                                                                           |
|----------------------|-------------------------------------|----------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| J31                  | QFN-AOUTB Loading                   | 3x1 header                 | —   | Selectable loading resistance of 600\10k $\Omega$ for QFN-AOUTB                                                                                                                       |
| J40                  | VP Source Select                    | 3x1 header                 | —   | Jumper between 1-2 to get VP from VP banana jack (J13). Jumper between 2-3 to get VP from 3.6-V LDO                                                                                   |
| J41                  | VA Source Select                    | 3x1 header                 | —   | Jumper between 1-2 to get VA from 1.8 V banana jack (J27). Jumper between 2-3 to get VA from 1.8 VA LDO                                                                               |
| J42                  | Aardvark I <sup>2</sup> C Interface | 5x2 header (shrouded)      | I/O | Interface connector for Aardvark I <sup>2</sup> C test module                                                                                                                         |
| J43                  | USB Connector                       | Mini-USB receptacle        | I/O | Provides USB Data and +5 V power to the CDB                                                                                                                                           |
| J44                  | XSP DUT Connection                  | 3x3 header                 | —   | Connect shunt between (DUT-BRD) to connect DUT and XSP data. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure XSP data directly             |
| J45                  | XMOS Connector                      | 10x2 right-angle connector | I/O | Connects to XMOS programmer                                                                                                                                                           |
| J46-J50              | GND test point                      | GND test point             | O   | GND test point                                                                                                                                                                        |
| J51                  | External 5 V Supply                 | 2.5 mm PIN receptacle      | I   | Provides external +5 V if USB VBUS is not used                                                                                                                                        |
| J52                  | V5 Source Select                    | 3x1 header                 | —   | Jumper between 1-2 to get 5 V from external supply (J52). Jumper between 2-3 to get 4 V from USB VBUS (J43)                                                                           |
| J53                  | I <sup>2</sup> C DUT Connection     | 3x2 header                 | —   | Connect shunt between (DUT-BRD) to connect DUT and I2C data. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure I2C data directly             |
| J54                  | /RST /INT CSP Connection            | 3x2 header                 | —   | Connect shunt between (DUT-BRD) to connect /RST and /INT data. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure /RST and /INT data directly |
| J55                  | /RST /INT QFN Connection            | 3x2 header                 | —   | Connect shunt between (DUT-BRD) to connect /RST and /INT data. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure /RST and /INT data directly |
| J56                  | VD/VL Source Select                 | 3x1 header                 | —   | Jumper between 1-2 to get VD/VL from 1.8 V banana jack (J27). Jumper between 2-3 to get VD/VL from 1.8 VA LDO                                                                         |
| J57                  | MCLK CSP Connection                 | 3x2 header                 | —   | Connect shunt between (DUT-BRD) to connect MCLK. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure MCLK directly                             |
| J58                  | MCLK QFN Connection                 | 3x2 header                 | —   | Connect shunt between (DUT-BRD) to connect MCLK. Disconnect shunt and use 2-pin test point for Audio Precision between (DUT-GND) to measure MCLK directly                             |
| J60                  | QFN-XLR OUT                         | XLR connector              | O   | The XLR out jack for the CS43198 QFN Device                                                                                                                                           |
| J802                 | MCU Programmer                      | 5x2 header (shrouded)      | I/O | Programmer for MCU                                                                                                                                                                    |

## 2.7.1 Current Measurement Headers

The table below shows a list of current measurement headers and the associated rails. To measure current of a particular voltage rail, remove the jumper and place a current probe across the pins of the header.

**Table 9 Current Measurement Headers**

| Header | Voltage Rail |
|--------|--------------|
| VP-QFN | VP-QFN       |
| VP-CSP | VP-CSP       |
| VA     | VA           |
| VCP    | VCP          |
| VL     | VL           |
| VD     | VD           |

## 2.7.2 Push-Button Resets (Revision B only)

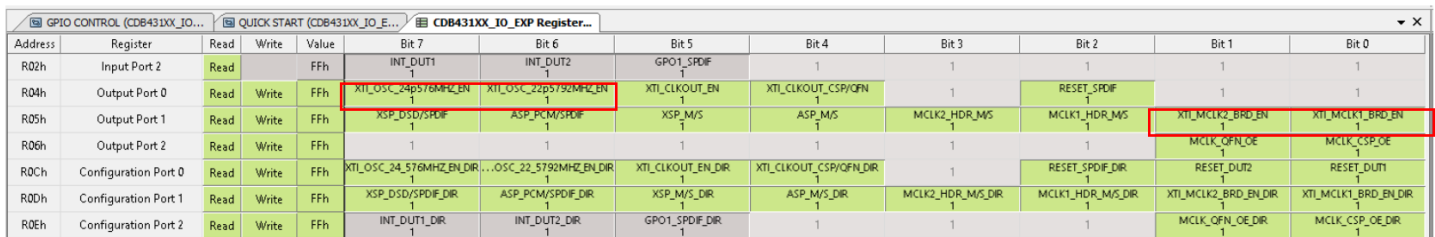
There are 2 SPST push buttons for resetting the board in case something enters an unknown state. There are 2 buttons, S1 for a system-wide reset, and S2 for a DAC-only reset.

**Table 10 Push-Button Resets**

| Button Name | Descriptor | Reset Tied To                                                        |
|-------------|------------|----------------------------------------------------------------------|
| S1          | SYS RESET  | CS43198-CSP, CS43198-QFN, CS8422 Smart Codec, USB MCU, USB HUB, XMOS |
| S2          | DAC RESET  | CS43198-CSP, CS43198-QFN                                             |

## 2.8 Codec MCLK Selection

The MCLK input to the smart codec can come either from the on-board 24.576 MHz clock oscillator, a 22.579 MHz clock oscillator, MCLK1 from ASP(J25), MCLK2 from XSP(J26) or from the CLKOUT pin on the DAC or the MCLK output from an external audio source. The selection is controlled by WISCE.

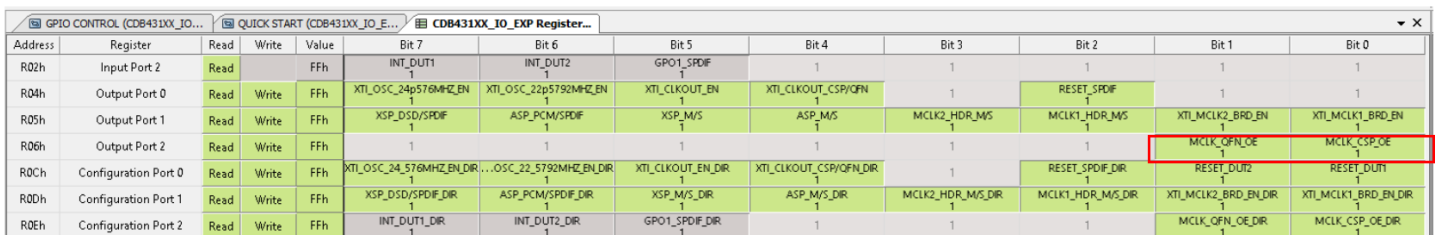


| Address | Register             | Read | Write | Value | Bit 7                    | Bit 6                    | Bit 5             | Bit 4                  | Bit 3             | Bit 2             | Bit 1                | Bit 0                |
|---------|----------------------|------|-------|-------|--------------------------|--------------------------|-------------------|------------------------|-------------------|-------------------|----------------------|----------------------|
| R02h    | Input Port 2         | Read | Write | FFh   | INT_DUT1                 | INT_DUT2                 | GPO1_SPDIF        | 1                      | 1                 | 1                 | 1                    | 1                    |
| R04h    | Output Port 0        | Read | Write | FFh   | XTL_OSC_24p576MHZ_EN     | XTL_OSC_22p579MHZ_EN     | XTL_CLKOUT_EN     | XTL_CLKOUT_CSP/QFN     | 1                 | RESET_SPDIF       | 1                    | 1                    |
| R05h    | Output Port 1        | Read | Write | FFh   | XSP_DSD/SPDIF            | ASP_PCM/SPDIF            | XSP_M/S           | ASP_M/S                | MCLK2_HDR_M/S     | MCLK1_HDR_M/S     | XTL_MCLK2_BRD_EN     | XTL_MCLK1_BRD_EN     |
| R06h    | Output Port 2        | Read | Write | FFh   | 1                        | 1                        | 1                 | 1                      | 1                 | 1                 | MCLK_QFN_OE          | MCLK_CSP_OE          |
| R0Ch    | Configuration Port 0 | Read | Write | FFh   | XTL_OSC_24p576MHZ_EN_DIR | XTL_OSC_22p579MHZ_EN_DIR | XTL_CLKOUT_EN_DIR | XTL_CLKOUT_CSP/QFN_DIR | 1                 | RESET_SPDIF_DIR   | RESET_DUT2           | RESET_DUT1           |
| R0Dh    | Configuration Port 1 | Read | Write | FFh   | XSP_DSD/SPDIF_DIR        | ASP_PCM/SPDIF_DIR        | XSP_M/S_DIR       | ASP_M/S_DIR            | MCLK2_HDR_M/S_DIR | MCLK1_HDR_M/S_DIR | XTL_MCLK2_BRD_EN_DIR | XTL_MCLK1_BRD_EN_DIR |
| R0Eh    | Configuration Port 2 | Read | Write | FFh   | INT_DUT1_DIR             | INT_DUT2_DIR             | GPO1_SPDIF_DIR    | 1                      | 1                 | 1                 | MCLK_QFN_OE_DIR      | MCLK_CSP_OE_DIR      |

**Figure 11 CODEC MCLK Selection**

## 2.9 Clock Sources

The CDB43198 Board has 2 separate onboard 22.5792 MHz crystals to act as the MCLK source for the CS43198 CSP and QFN DUTs. In addition to the crystal, the board also provides an option to supply MCLK either from an external source, such as a function generator. These oscillators are Y1 (CSP) and Y2(QFN). By default, these crystals are enabled. In order to use an external clock source, you need to depopulate R11(CSP) and R28(QFN) and solder in a 0-Ω resistor in R10(CSP) and R39(QFN). To enable the external MCLK, you need to select it in the IO expander in WISCE.



| Address | Register             | Read | Write | Value | Bit 7                    | Bit 6                    | Bit 5             | Bit 4                  | Bit 3             | Bit 2             | Bit 1                | Bit 0                |
|---------|----------------------|------|-------|-------|--------------------------|--------------------------|-------------------|------------------------|-------------------|-------------------|----------------------|----------------------|
| R02h    | Input Port 2         | Read | Write | FFh   | INT_DUT1                 | INT_DUT2                 | GPO1_SPDIF        | 1                      | 1                 | 1                 | 1                    | 1                    |
| R04h    | Output Port 0        | Read | Write | FFh   | XTL_OSC_24p576MHZ_EN     | XTL_OSC_22p579MHZ_EN     | XTL_CLKOUT_EN     | XTL_CLKOUT_CSP/QFN     | 1                 | RESET_SPDIF       | 1                    | 1                    |
| R05h    | Output Port 1        | Read | Write | FFh   | XSP_DSD/SPDIF            | ASP_PCM/SPDIF            | XSP_M/S           | ASP_M/S                | MCLK2_HDR_M/S     | MCLK1_HDR_M/S     | XTL_MCLK2_BRD_EN     | XTL_MCLK1_BRD_EN     |
| R06h    | Output Port 2        | Read | Write | FFh   | 1                        | 1                        | 1                 | 1                      | 1                 | 1                 | MCLK_QFN_OE          | MCLK_CSP_OE          |
| R0Ch    | Configuration Port 0 | Read | Write | FFh   | XTL_OSC_24p576MHZ_EN_DIR | XTL_OSC_22p579MHZ_EN_DIR | XTL_CLKOUT_EN_DIR | XTL_CLKOUT_CSP/QFN_DIR | 1                 | RESET_SPDIF_DIR   | RESET_DUT2           | RESET_DUT1           |
| R0Dh    | Configuration Port 1 | Read | Write | FFh   | XSP_DSD/SPDIF_DIR        | ASP_PCM/SPDIF_DIR        | XSP_M/S_DIR       | ASP_M/S_DIR            | MCLK2_HDR_M/S_DIR | MCLK1_HDR_M/S_DIR | XTL_MCLK2_BRD_EN_DIR | XTL_MCLK1_BRD_EN_DIR |
| R0Eh    | Configuration Port 2 | Read | Write | FFh   | INT_DUT1_DIR             | INT_DUT2_DIR             | GPO1_SPDIF_DIR    | 1                      | 1                 | 1                 | MCLK_QFN_OE_DIR      | MCLK_CSP_OE_DIR      |

**Figure 12 EXT MCLK Selection**



## 3 Board Control Register Quick Reference

| Address | Register             | Read | Write | Value | Bit 7                         | Bit 6                          | Bit 5                  | Bit 4                       | Bit 3                  | Bit 2                  | Bit 1                     | Bit 0                     |
|---------|----------------------|------|-------|-------|-------------------------------|--------------------------------|------------------------|-----------------------------|------------------------|------------------------|---------------------------|---------------------------|
| R02h    | Input Port 2         | Read |       | FFh   | INT_DUT1<br>1                 | INT_DUT2<br>1                  | GPO1_SPDIF<br>1        | 1                           | 1                      | 1                      | 1                         | 1                         |
| R04h    | Output Port 0        | Read | Write | FCh   | XTI_OSC_24p576MHZ_EN<br>1     | XTI_OSC_22p5792MHZ_EN<br>1     | XTI_CLKOUT_EN<br>1     | XTI_CLKOUT_CSP/QFN<br>1     | 1                      | RESET_SPDIF<br>1       | 0                         | 0                         |
| R05h    | Output Port 1        | Read | Write | FFh   | XSP_DSD/SPDIF<br>1            | ASP_PCM/SPDIF<br>1             | XSP_M/S<br>1           | ASP_M/S<br>1                | MCLK2_HDR_M/S<br>1     | MCLK1_HDR_M/S<br>1     | XTI_MCLK2_BRD_EN<br>1     | XTI_MCLK1_BRD_EN<br>1     |
| R06h    | Output Port 2        | Read | Write | FFh   | 1                             | 1                              | 1                      | 1                           | 1                      | 1                      | MCLK_QFN_OE<br>1          | MCLK_CSP_OE<br>1          |
| R0Ch    | Configuration Port 0 | Read | Write | 0Bh   | XTI_OSC_24_576MHZ_EN_DIR<br>0 | XTI_OSC_22_5792MHZ_EN_DIR<br>0 | XTI_CLKOUT_EN_DIR<br>0 | XTI_CLKOUT_CSP/QFN_DIR<br>0 | 1                      | RESET_SPDIF_DIR<br>0   | RESET_DUT2<br>1           | RESET_DUT1<br>1           |
| R0Dh    | Configuration Port 1 | Read | Write | 00h   | XSP_DSD/SPDIF_DIR<br>0        | ASP_PCM/SPDIF_DIR<br>0         | XSP_M/S_DIR<br>0       | ASP_M/S_DIR<br>0            | MCLK2_HDR_M/S_DIR<br>0 | MCLK1_HDR_M/S_DIR<br>0 | XTI_MCLK2_BRD_EN_DIR<br>0 | XTI_MCLK1_BRD_EN_DIR<br>0 |
| R0Eh    | Configuration Port 2 | Read | Write | FCh   | INT_DUT1_DIR<br>1             | INT_DUT2_DIR<br>1              | GPO1_SPDIF_DIR<br>1    | 1                           | 1                      | 1                      | MCLK_QFN_OE_DIR<br>0      | MCLK_CSP_OE_DIR<br>0      |

Figure 13 CDB43198 IO EXP Registers

### 3.1 Register Descriptions

#### 3.1.1 Output Port 0

|                      |                      |            |
|----------------------|----------------------|------------|
| <b>Address: 0x04</b> | <b>Default: 0xFC</b> | <b>R/W</b> |
|----------------------|----------------------|------------|

| Bit Position  | 7                    | 6                     | 5             | 4                  | 3        | 2           | 1        | 0        |
|---------------|----------------------|-----------------------|---------------|--------------------|----------|-------------|----------|----------|
| Bitfield Name | XTI_OSC_24p576MHZ_EN | XTI_OSC_22p5792MHZ_EN | XTI_CLKOUT_EN | XTI_CLKOUT_CSP/QFN | RESERVED | RESET_SPDIF | RESERVED | RESERVED |
| Default Value | 1                    | 1                     | 1             | 1                  | X        | 1           | X        | X        |

| Bits | Name                  | Description                                                                              |
|------|-----------------------|------------------------------------------------------------------------------------------|
| 7    | XTI_OSC_24p576MHZ_EN  | Enable 24.576 MHz CLK to be used as input to CODEC<br>0 Enabled<br>1 Disabled (Default)  |
| 6    | XTI_OSC_22p5792MHZ_EN | Enable 22.5792 MHz CLK to be used as input to CODEC<br>0 Enabled<br>1 Disabled (Default) |
| 5    | XTI_CLKOUT_EN         | Select SPDIF Clock Master<br>0 External CLK<br>1 CS43198 CLKOUT (Default)                |
| 4    | XTI_CLKOUT_CSP/QFN    | Select Device to be SPDIF Clock Master<br>0 CSP CLKOUT<br>1 QFN CLKOUT (Default)         |
| 3    | Reserved              | —                                                                                        |
| 2    | Reset_SPDIF           | Enable SPDIF Buffer<br>0 Disabled<br>1 Enabled (Default)                                 |
| 1:0  | Reserved              | —                                                                                        |

### 3.1.2 Output Port 2

|                      |                      |            |
|----------------------|----------------------|------------|
| <b>Address: 0x05</b> | <b>Default: 0x0F</b> | <b>R/W</b> |
|----------------------|----------------------|------------|

| Bit Position  | 7              | 6              | 5       | 4       | 3              | 2              | 1                | 0                |
|---------------|----------------|----------------|---------|---------|----------------|----------------|------------------|------------------|
| Bitfield Name | XSP_DSD/S PDIF | ASP_PCM/S PDIF | XSP_M/S | ASP_M/S | MCLK2_HD R M/S | MCLK1_HD R M/S | XTI_MCLK2_BRD_EN | XTI_MCLK1_BRD_EN |
| Default Value | 1              | 1              | 1       | 1       | 0              | 0              | 0                | 0                |

| Bits | Name             | Description                                                                       |
|------|------------------|-----------------------------------------------------------------------------------|
| 7    | XSP_DSD/SPDIF    | Set Codec in DSD/SPDIF Mode<br>0 DSD<br>1 SPDIF (Default)                         |
| 6    | ASP_PCM/SPDIF    | Set Codec in PCM/SPDIF Mode<br>0 PCM<br>1 SPDIF (Default)                         |
| 5    | XSP_M/S          | Set XSP as Master/Slave<br>1 Master (Default)<br>0 Slave                          |
| 4    | ASP_M/S          | Set ASP as Master/Slave<br>1 Master (Default)<br>0 Slave                          |
| 3    | MCLK2_HDR_M/S    | Set Codec as Master to MCLK2<br>1 Master (Default)<br>0 Slave                     |
| 2    | MCLK1_HDR_M/S    | Set Codec as Master to MCLK1 1 Master (Default)<br>0 Slave                        |
| 1    | XTI_MCLK2_BRD_EN | Enable ASP MCLK to be used as input to CODEC<br>0 Enabled<br>1 Disabled (Default) |
| 0    | XTI_MCLK1_BRD_EN | Enable XSP MCLK to be used as input to CODEC<br>0 Enabled<br>1 Disabled (Default) |

### 3.1.3 Output Port 3

|                      |                      |            |
|----------------------|----------------------|------------|
| <b>Address: 0x06</b> | <b>Default: 0xFF</b> | <b>R/W</b> |
|----------------------|----------------------|------------|

| Bit Position  | 7        | 6 | 5 | 4 | 3 | 2 | 1           | 0           |
|---------------|----------|---|---|---|---|---|-------------|-------------|
| Bitfield Name | Reserved |   |   |   |   |   | MCLK_QFN_OE | MCLK_CSP_OE |
| Default Value | x        | x | x | x | x | x | 1           | 1           |

| Bits | Name        | Description                                                 |
|------|-------------|-------------------------------------------------------------|
| 7:2  | Reserved    | —                                                           |
| 1    | MCLK_QFN_OE | Set Codec as Master to CSP<br>1 Master (Default)<br>0 Slave |
| 0    | MCLK_CSP_OE | Set Codec as Master to QFN<br>1 Master (Default)<br>0 Slave |

### 3.1.4 Port Config 1

|                      |                      |            |
|----------------------|----------------------|------------|
| <b>Address: 0x0C</b> | <b>Default: 0x0B</b> | <b>R/W</b> |
|----------------------|----------------------|------------|

| Bit Position  | 7                        | 6                        | 5                   | 4                      | 3        | 2               | 1          | 0          |
|---------------|--------------------------|--------------------------|---------------------|------------------------|----------|-----------------|------------|------------|
| Bitfield Name | XTI_OSC_24_576MHZ_EN_DIR | XTI_OSC_22_5792HZ_EN_DIR | XTI_CLKOUT_T_EN_DIR | XTI_CLKOUT_CSP/QFN_DIR | Reserved | RESET_SPDIF_DIR | RESET_DUT2 | RESET_DUT1 |
| Default Value | 0                        | 0                        | 0                   | 0                      | x        | 0               | 1          | 1          |

| Bits | Name                     | Description                                                                    |
|------|--------------------------|--------------------------------------------------------------------------------|
| 7    | XTI_OSC_24_576MHZ_EN_DIR | Direction of the XTI_OSC_24_576MHz_EN signal<br>0 Output (Default)<br>1 Input  |
| 6    | XTI_OSC_22_5792HZ_EN_DIR | Direction of the XTI_OSC_22_5792MHz_EN signal<br>0 Output (Default)<br>1 Input |
| 5    | XTI_CLKOUT_EN_DIR        | Direction of the XTI_CLKOUT_EN signal<br>0 Output (Default)<br>1 Input         |
| 4    | XTI_CLKOUT_CSP/QFN_DIR   | Direction of the XTI_CLKOUT_CSP/QFN signal<br>0 Output (Default)<br>1 Input    |
| 3    | Reserved                 | —                                                                              |
| 2    | RESET_SPDIF_DIR          | Direction of the RESET_SPDIF signal<br>0 Output (Default)<br>1 Input           |
| 1    | RESET_DUT2               | Reset DUT2<br>0 Disabled<br>1 Enabled (Default)                                |
| 0    | RESET_DUT1               | Reset DUT1<br>0 Disabled<br>1 Enabled (Default)                                |

### 3.1.5 Port Config 2

|                      |                      |            |
|----------------------|----------------------|------------|
| <b>Address: 0x0D</b> | <b>Default: 0x00</b> | <b>R/W</b> |
|----------------------|----------------------|------------|

| Bit Position  | 7                     | 6                     | 5               | 4               | 3                     | 2                     | 1                            | 0                            |
|---------------|-----------------------|-----------------------|-----------------|-----------------|-----------------------|-----------------------|------------------------------|------------------------------|
| Bitfield Name | XSP_DSD/S<br>PDIF_DIR | ASP_DSD/S<br>PDIF_DIR | XSP_M/S_D<br>IR | ASM_M/S_D<br>IR | MCLK2_HD<br>R_M/S_DIR | MCLK1_HD<br>R_M/S_DIR | XTI_MCLK2<br>_BRD_EN_<br>DIR | XTI_MCLK1<br>_BRD_EN_<br>DIR |
| Default Value | 0                     | 0                     | 0               | 0               | 0                     | 0                     | 0                            | 0                            |

| Bits | Name                 | Description                                                               |
|------|----------------------|---------------------------------------------------------------------------|
| 7    | XSP_DSD/SPDIF_DIR    | Direction of the XSP_DSD/SPDIF signal<br>0 Output (Default)<br>1 Input    |
| 6    | ASP_PCM/SPDIF_DIR    | Direction of the ASP_PCM/SPDIF signal<br>0 Output (Default)<br>1 Input    |
| 5    | XSP_M/S_DIR          | Direction of the XSP_M/S signal<br>0 Output (Default)<br>1 Input          |
| 4    | ASP_M/S_DIR          | Direction of the ASP_M/S signal<br>0 Output (Default)<br>1 Input          |
| 3    | MCLK2_HDR_M/S_DIR    | Direction of the MCLK2_HDR_M/S signal<br>0 Output (Default)<br>1 Input    |
| 2    | MCLK1_HDR_M/S_DIR    | Direction of the MCLK1_HDR_M/S signal<br>0 Output (Default)<br>1 Input    |
| 1    | XTI_MCLK2_BRD_EN_DIR | Direction of the XTI_MCLK2_BRD_EN signal<br>0 Output (Default)<br>1 Input |
| 0    | XTI_MCLK1_BRD_EN_DIR | Direction of the XTI_MCLK1_BRD_EN signal<br>0 Output (Default)<br>1 Input |

### 3.1.6 Port Config 3

|                      |                      |            |
|----------------------|----------------------|------------|
| <b>Address: 0x0E</b> | <b>Default: 0xFC</b> | <b>R/W</b> |
|----------------------|----------------------|------------|

| Bit Position  | 7        | 6 | 5 | 4 | 3 | 2 | 1               | 0               |
|---------------|----------|---|---|---|---|---|-----------------|-----------------|
| Bitfield Name | Reserved |   |   |   |   |   | MCLK_QFN_OE_DIR | MCLK_CSP_OE_DIR |
| Default Value | 1        | 1 | 1 | x | x | x | 0               | 0               |

| Bits | Name            | Description                                                          |
|------|-----------------|----------------------------------------------------------------------|
| 7:2  | Reserved        | —                                                                    |
| 1    | MCLK_QFN_OE_DIR | Direction of the MCLK_QFN_OE signal<br>0 Output (Default)<br>1 Input |
| 0    | MCLK_CSP_OE_DIR | Direction of the MCLK_CSP_OE signal<br>0 Output (Default)<br>1 Input |

## 4 CDB-HDR-MEAS High Dynamic Range Measurement Preamplifier

The CDB-HDR-MEAS is an ultralow-noise preamplifier circuit with +13.66 dB of gain. The CDB-HDR-MEAS is designed to be used as a preamplifier to a high-performance audio analyzer to allow measurement of the high dynamic range (DNR) of the CS43198. The CDB-HDR-MEAS preserves the dynamic range of the input signal while amplifying the input signal by +13.66 dB to overcome noise floor limitations of the audio analyzer.

### 4.1 Powering the CDB-HDR-MEAS

The CDB-HDR-MEAS board requires a triple-output DC power supply capable of providing  $\pm 15$  V and GND connection at 100 mA, as shown in the figure below. Standard binding posts are provided for convenient connection of +15 V, GND, and -15 V.

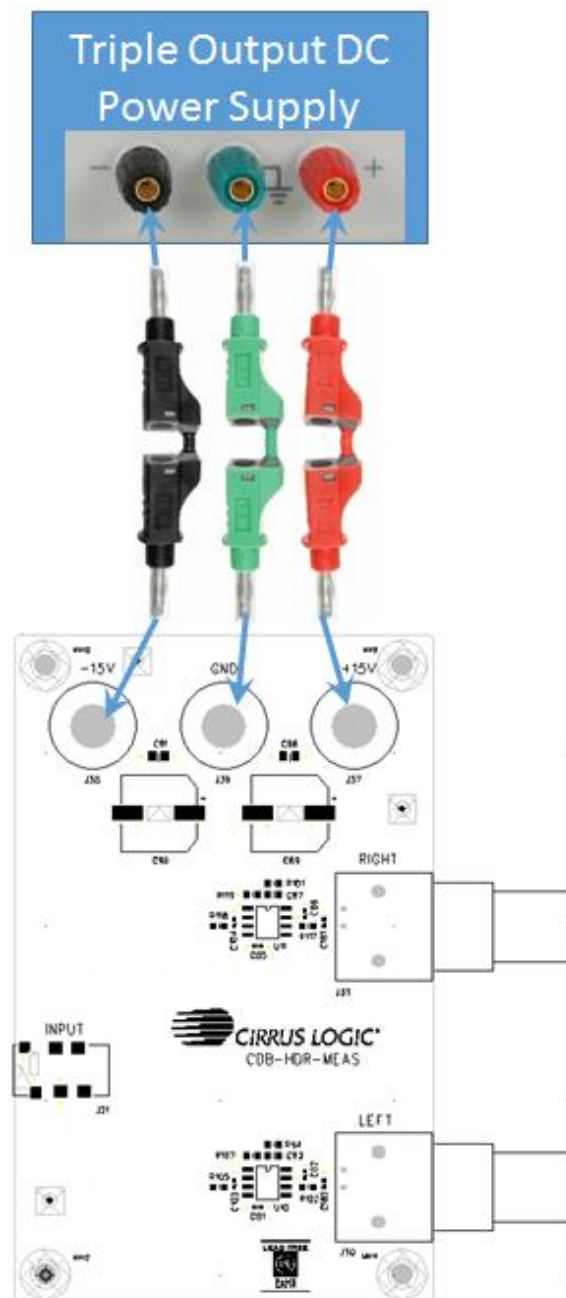
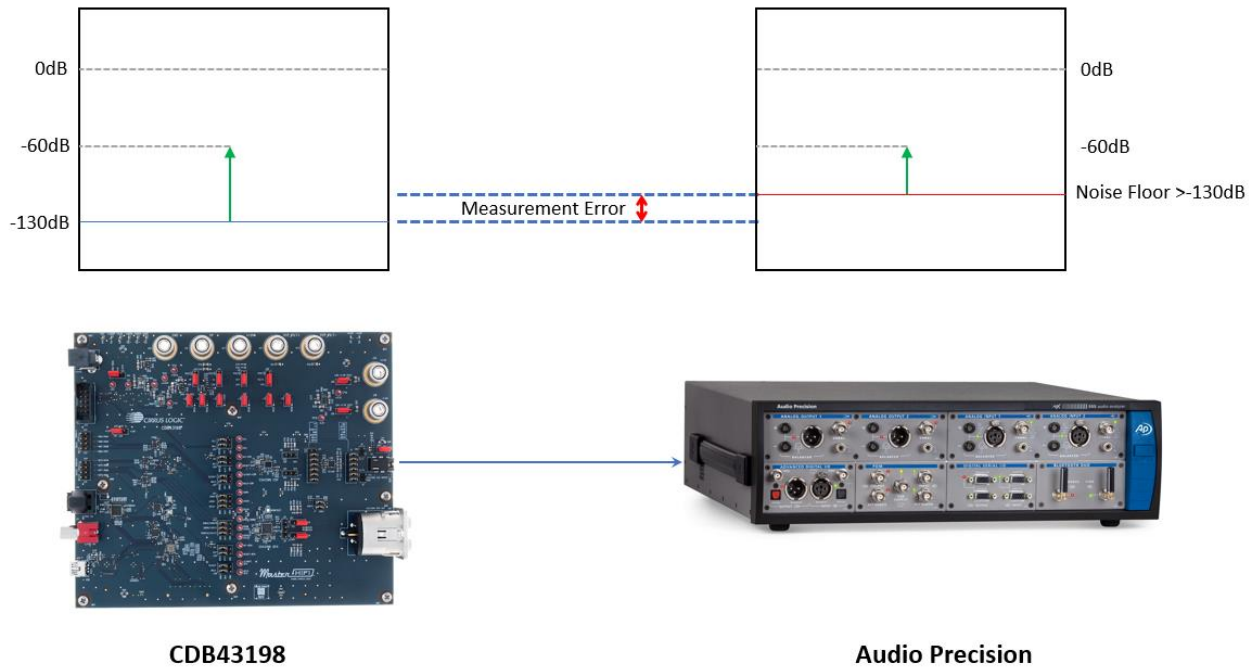


Figure 14 Powering CDB-HDR-MEAS

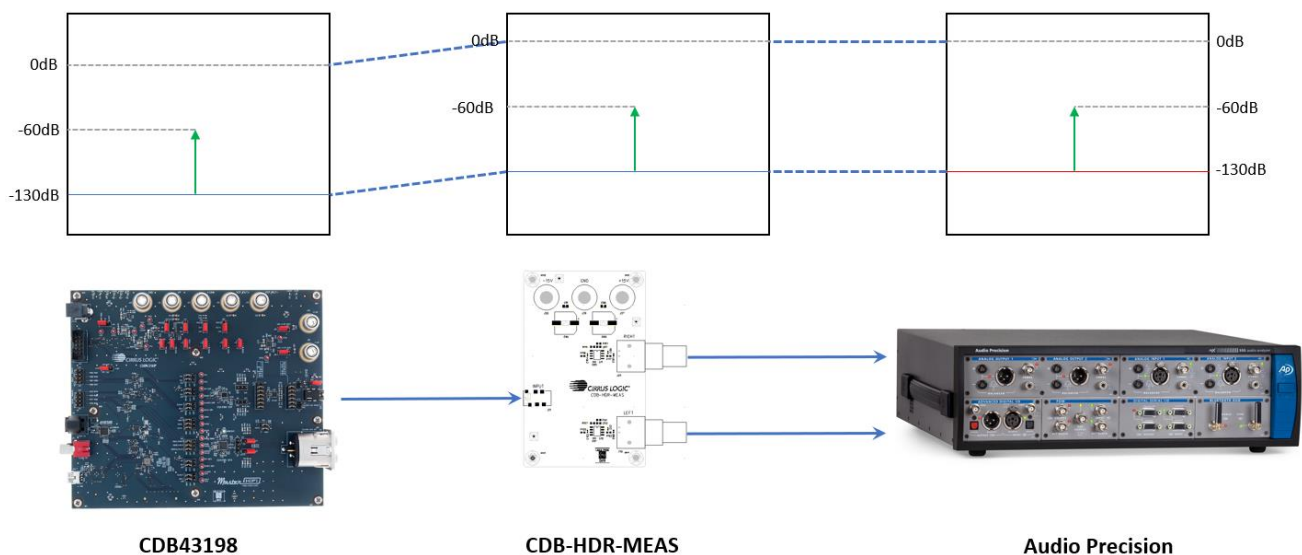
## 4.2 How the CDB-HDR-MEAS Works

Since the noise floor of the APx555 is around  $-124$  dB, and the CS43198 has a DNR of 130 dB, the signal needs to be amplified to make it measurable. The following image illustrates this issue. In an ideal situation, the  $-60$  dB signal during DNR tests would yield a total dynamic range of 130 dB. However, due to a higher noise floor of the measurement equipment, the difference results in a measurement error that hampers performance.



**Figure 15 Testing Without CDB-HDR-MEAS**

To rectify this issue, the input signal can be amplified (in this case by 13.3 dB). This will also amplify the noise floor; however, since the noise floor is small compared to the signal, the signal will dominate the amplification. In the figure below, the signal and noise floor have been shifted up to be at least on par with the noise floor of the measurement equipment. Now when using the  $-60$  dB signal for the DNR measurement, the full range of 130 dB can be measured.



**Figure 16 Testing With CDB-HDR-MEAS**

## 5 Testing the CS43198 using WISCE

The WISCE™ interactive setup and configuration environment is an interactive tool for setting up and configuring Cirrus Logic devices and software. The following sections show how to use WISCE to configure and test CS43198 and using the CDB43198 board and the CDB43198 Board.

### 5.1 Launching WISCE

Click on the Start Button -> All Programs -> Wolfson Evaluation Software and select "WISCE™ V3" to launch WISCE.

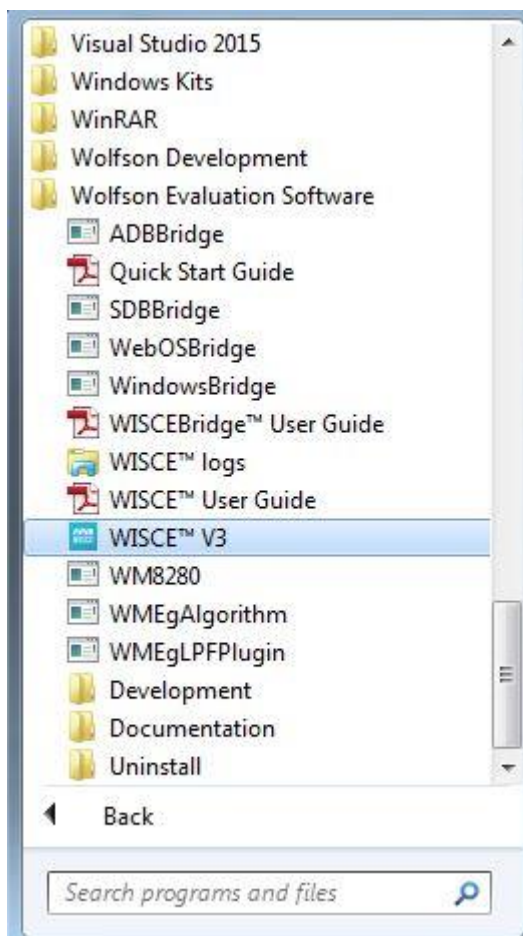
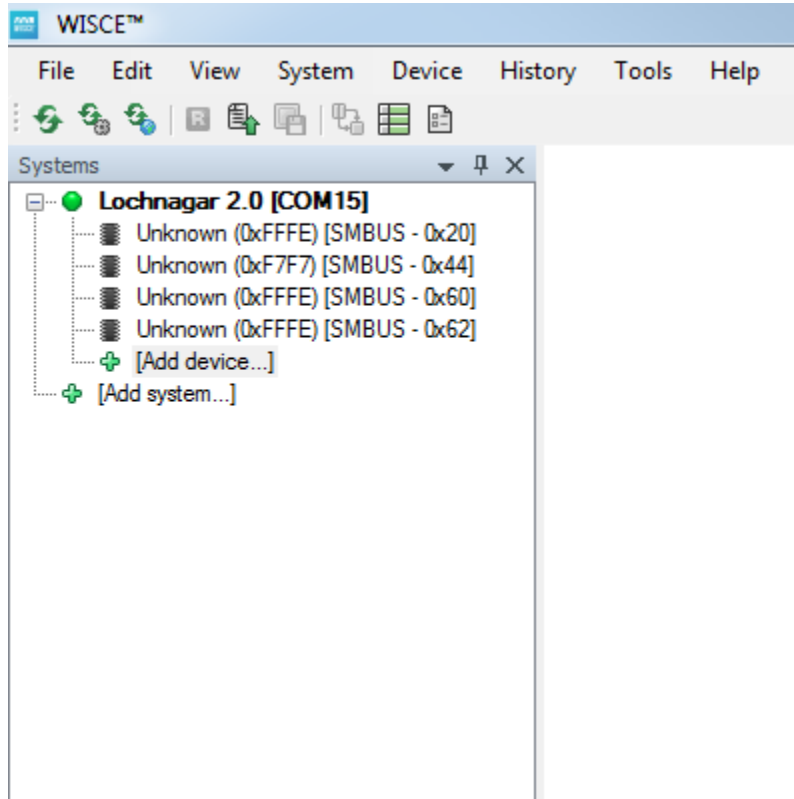


Figure 17 Launch WISCE

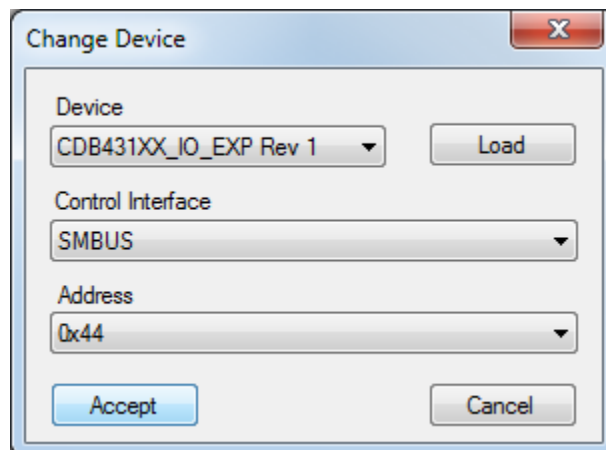
WISCE is configured, by default, to scan the I<sup>2</sup>C bus and report the presence of any devices attached to this bus. When WISCE is launched, it will report the presence of four unknown devices, one each at address 0x22, 0x44, 0x60 and 0x62 respectively. The device at address 0x22 is the CS8422 Codec, 0x44 is TCA6424, which is an IO Expander. The device at address 0x60 is CS43198 CSP DUT, and the device at address 0x62 is the CS43198 QFN DUT.



**Figure 18 Found Devices**

## 5.2 Loading the CDB43198 board Panel and Register Map

To load the CDB43198 board panel and register map, double click on the Unknown device at address 0x44 to launch "Change Device" pop-up window. Alternatively, the "Change Device" pop-up window can also be launched by right clicking on the Unknown Device and selecting Properties.



**Figure 19 Select TCA6424**

Select "CDB431XX\_IO\_EXP Rev1" from the drop down menu under Device.



Click "Accept" to load the CDB43198 board Panel and Register Map shown in the following figures.

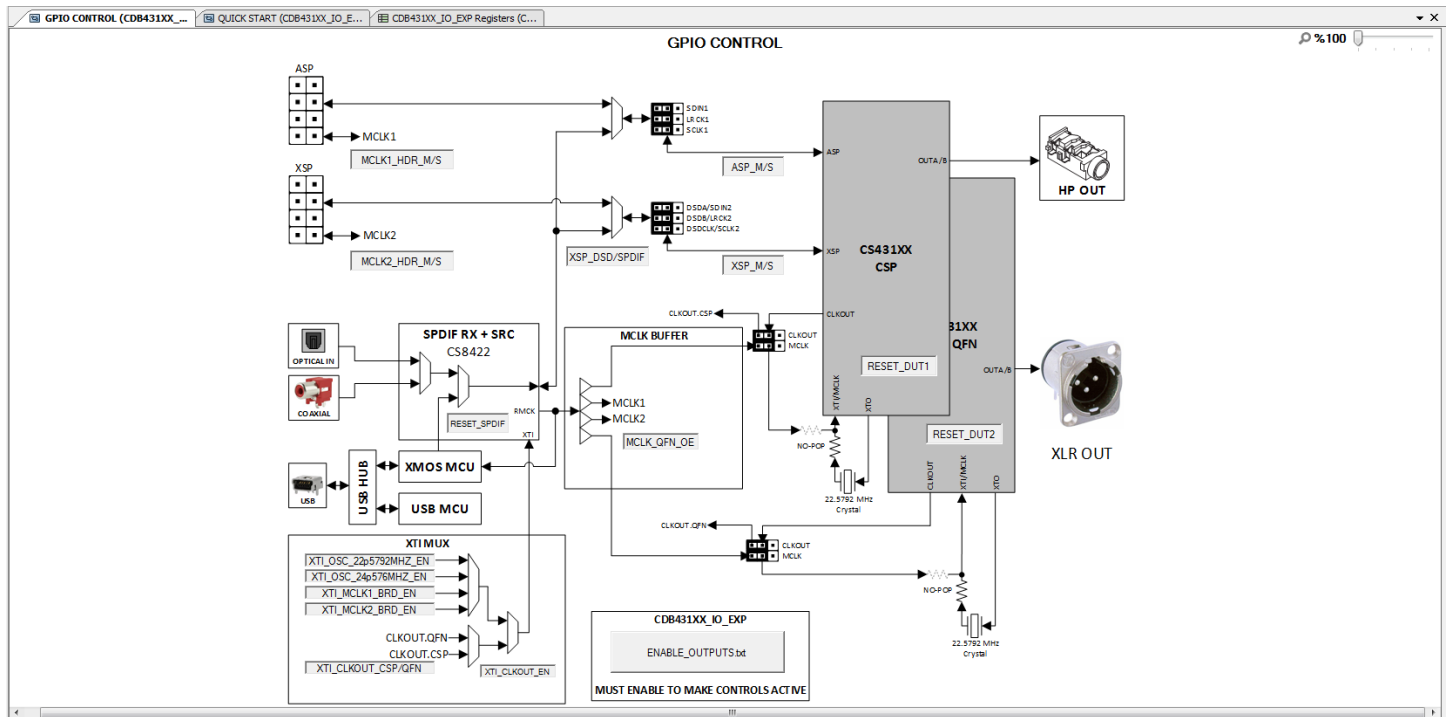


Figure 20 TCA6424 Panel

| Address | Register             | Read | Write | Value | Bit 7                       | Bit 6                 | Bit 5             | Bit 4                  | Bit 3             | Bit 2             | Bit 1                | Bit 0                |
|---------|----------------------|------|-------|-------|-----------------------------|-----------------------|-------------------|------------------------|-------------------|-------------------|----------------------|----------------------|
| R02h    | Input Port 2         | Read |       | FFh   | INT_DUT1                    | INT_DUT2              | GPO1_SPDIF        | 1                      | 1                 | 1                 | 1                    | 1                    |
| R04h    | Output Port 0        | Read | Write | FFh   | XTL_OSC_24p576MHz_EN        | XTL_OSC_22p5792MHz_EN | XTL_CLKOUT_EN     | XTL_CLKOUT_CSP/QFN     | 1                 | RESET_SPDIF       | 1                    | 1                    |
| R05h    | Output Port 1        | Read | Write | FFh   | XSP_DSD/SPDIF               | ASP_PCM/SPDIF         | XSP_M/S           | ASP_M/S                | MCLK2_HDR_M/S     | MCLK1_HDR_M/S     | XTL_MCLK2_BRD_EN     | XTL_MCLK1_BRD_EN     |
| R06h    | Output Port 2        | Read | Write | FFh   | 1                           | 1                     | 1                 | 1                      | 1                 | 1                 | MCLK_QFN_OE          | MCLK_CSP_OE          |
| R0Ch    | Configuration Port 0 | Read | Write | FFh   | XTL_OSC_24p576MHz_EN_DIR... | OSC_22_5792MHz_EN_DIR | XTL_CLKOUT_EN_DIR | XTL_CLKOUT_CSP/QFN_DIR | 1                 | RESET_SPDIF_DIR   | RESET_DUT2           | RESET_DUT1           |
| R0Dh    | Configuration Port 1 | Read | Write | FFh   | XSP_DSD/SPDIF_DIR           | ASP_PCM/SPDIF_DIR     | XSP_M/S_DIR       | ASP_M/S_DIR            | MCLK2_HDR_M/S_DIR | MCLK1_HDR_M/S_DIR | XTL_MCLK2_BRD_EN_DIR | XTL_MCLK1_BRD_EN_DIR |
| R0Eh    | Configuration Port 2 | Read | Write | FFh   | INT_DUT1_DIR                | INT_DUT2_DIR          | GPO1_SPDIF_DIR    | 1                      | 1                 | 1                 | MCLK_QFN_OE_DIR      | MCLK_CSP_OE_DIR      |

Figure 21 TCA6424 Register Map

## 5.3 Loading the CS43198 Plugins and Register Map

To load the CS43198 Plugin and Register Map, launch the "Change Device" pop-up window by either double clicking on Unknown Device or right clicking on Unknown Device at address 0x60 and selecting Properties. Select "CS43198 Rev A1" from the Device drop down menu and click Accept to load the plugin and register map for the CS43198.

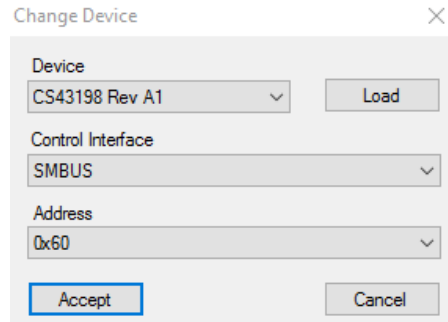


Figure 22 Select CS43198 CSP

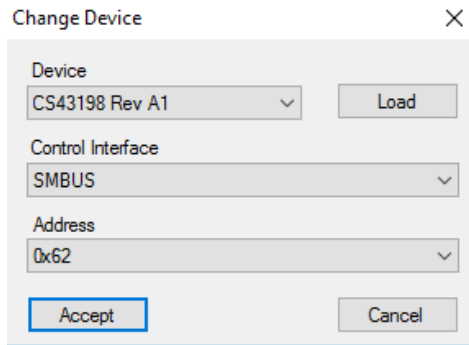


Figure 23 Select CS43198 QFN

| GP10 CONTROL (CDB43198_0x... |                             |      |       | QUICK START (CDB43198_0x... |                          |              |               | CDB43198_0x...         |                    |                           |                          | CS8422 Registers (CS8422) |                            |  |               | CS43198 Registers (CS43198) |   |  |   | CS43198 Registers (CS43198_... |  |  |  |
|------------------------------|-----------------------------|------|-------|-----------------------------|--------------------------|--------------|---------------|------------------------|--------------------|---------------------------|--------------------------|---------------------------|----------------------------|--|---------------|-----------------------------|---|--|---|--------------------------------|--|--|--|
| Address                      | Register                    | Read | Write | Value                       | Bit 7                    | Bit 6        | Bit 5         | Bit 4                  | Bit 3              | Bit 2                     | Bit 1                    | Bit 0                     |                            |  |               |                             |   |  |   |                                |  |  |  |
| R10000h                      | Device ID A and B           | Read |       | 43h                         | DEVID=0100_0011          |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R10001h                      | Device ID C and D           | Read |       | 19h                         | DEVID=0001_1001          |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R10002h                      | Device ID E                 | Read |       | 80h                         | DEVID=1000               |              |               |                        |                    |                           |                          |                           |                            |  | 0             |                             | 0 |  | 0 |                                |  |  |  |
| R10004h                      | Revision ID                 | Read |       | A1h                         | AREVID=1010              |              |               |                        |                    |                           |                          |                           |                            |  | MTLREVID=0001 |                             |   |  |   |                                |  |  |  |
| R10005h                      | Sub-Revision ID             | Read |       | 00h                         | SUBREVID=0000_0000       |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R10006h                      | System Clocking Control     | Read | Write | 06h                         | 0                        | 0            | 0             | 0                      | 0                  | 0                         | MCLK_INT<br>22.5792MHz   | MCLK_SRC_SEL=RCO          |                            |  |               |                             |   |  |   |                                |  |  |  |
| R10008h                      | Serial Port Sample Rate     | Read | Write | 01h                         | 0                        | 0            | 0             | 0                      | 0                  | ASP_SPRATE=44.1kHz        |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R1000Ch                      | Serial Port Sample Bit Size | Read | Write | 05h                         | 0                        | 0            | 0             | 0                      | XSP_SPSIZE=24 bits |                           |                          |                           | ASP_SPSIZE=24 bits         |  |               |                             |   |  |   |                                |  |  |  |
| R1000Dh                      | Pad interface Configuration | Read | Write | 03h                         | 0                        | 0            | 0             | 0                      | 0                  | 0                         | XSP_3ST<br>Hi-Z          | ASP_3ST<br>Hi-Z           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R20000h                      | Power Down Control          | Read | Write | FEh                         | PON_XSP<br>1             | PON_ASP<br>1 | PON_DSDF<br>1 | PON_HP<br>1            | PON_XTAL<br>1      | PON_PLL<br>1              | XTAL_BIAS=12.5uA         |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R20052h                      | Crystal Setting             | Read | Write | 04h                         | 0                        | 0            | 0             | 0                      | 0                  | 0                         |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R30001h                      | PLL Setting 1               | Read | Write | 00h                         | 0                        | 0            | 0             | 0                      | 0                  | 0                         | 0                        | 0                         | PLL_START<br>0             |  |               |                             |   |  |   |                                |  |  |  |
| R30002h                      | PLL Setting 2               | Read | Write | 00h                         | PLL_DIV_FRAC_0=0000_0000 |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R30003h                      | PLL Setting 3               | Read | Write | 00h                         | PLL_DIV_FRAC_1=0000_0000 |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R30004h                      | PLL Setting 4               | Read | Write | 00h                         | PLL_DIV_FRAC_2=0000_0000 |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R30005h                      | PLL Setting 5               | Read | Write | 40h                         | PLL_DIV_INT=0100_0000    |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R30009h                      | PLL Setting 6               | Read | Write | 10h                         | PLL_OUT_DIV=0001_0000    |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R3000Ah                      | PLL Setting 7               | Read | Write | 80h                         | PLL_CAL_RATIO=1000_0000  |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R30018h                      | PLL Setting 8               | Read | Write | 13h                         | 0                        | 0            | 0             | 0                      | 1                  | 0                         | 0                        | 0                         | PLL_MODE<br>1              |  |               |                             |   |  |   |                                |  |  |  |
| R40002h                      | PLL Setting 9               | Read | Write | 02h                         | 0                        | 0            | 0             | 0                      | 0                  | 0                         | 0                        | 0                         | PLL_REF_PREDIV=Divide by 4 |  |               |                             |   |  |   |                                |  |  |  |
| R40004h                      | CLKOUT Control              | Read | Write | 00h                         | 0                        | 0            | 0             | CLKOUT_DIV=Divide by 2 |                    |                           |                          | CLKOUT_SEL=Internal MCLK  |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40010h                      | ASP Numerator 1             | Read | Write | 01h                         | ASP_N_LSB=0000_0001      |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40011h                      | ASP Numerator 2             | Read | Write | 00h                         | ASP_N_MSB=0000_0000      |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40012h                      | ASP Denominator 1           | Read | Write | 00h                         | ASP_M_LSB=0000_1000      |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40013h                      | ASP Denominator 2           | Read | Write | 00h                         | ASP_M_MSB=0000_0000      |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40014h                      | ASP LRCK High Time 1        | Read | Write | 1Fh                         | ASP_L_CH1_LSB=0001_1111  |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40015h                      | ASP LRCK High Time 2        | Read | Write | 00h                         | ASP_L_CH1_MSB=0000_0000  |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40016h                      | ASP LRCK Period 1           | Read | Write | 3Fh                         | ASP_L_CPR1_LSB=0011_1111 |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40017h                      | ASP LRCK period 2           | Read | Write | 00h                         | ASP_L_CPR1_MSB=0000_0000 |              |               |                        |                    |                           |                          |                           |                            |  |               |                             |   |  |   |                                |  |  |  |
| R40018h                      | ASP Clock Configuration     | Read | Write | 0Ch                         | 0                        | 0            | 0             | 0                      | ASP_M_MSB<br>Slave | ASP_SCPOL_OUT<br>Inverted | ASP_SCPOL_IN<br>Inverted | ASP_LCPOL_OUT<br>Normal   | ASP_LCPOL_IN<br>Normal     |  |               |                             |   |  |   |                                |  |  |  |
| R40019h                      | ASP Frame Configuration     | Read | Write | 0Ah                         | 0                        | 0            | 0             | 0                      | ASP_STP            | ASP_S0SD                  | ASP_FSD=1.0 delay        |                           |                            |  |               |                             |   |  |   |                                |  |  |  |

Figure 24 CS43198 Register Map

To view CS43198 plugin, click on Tuning and select "CS43198\_Plugin."

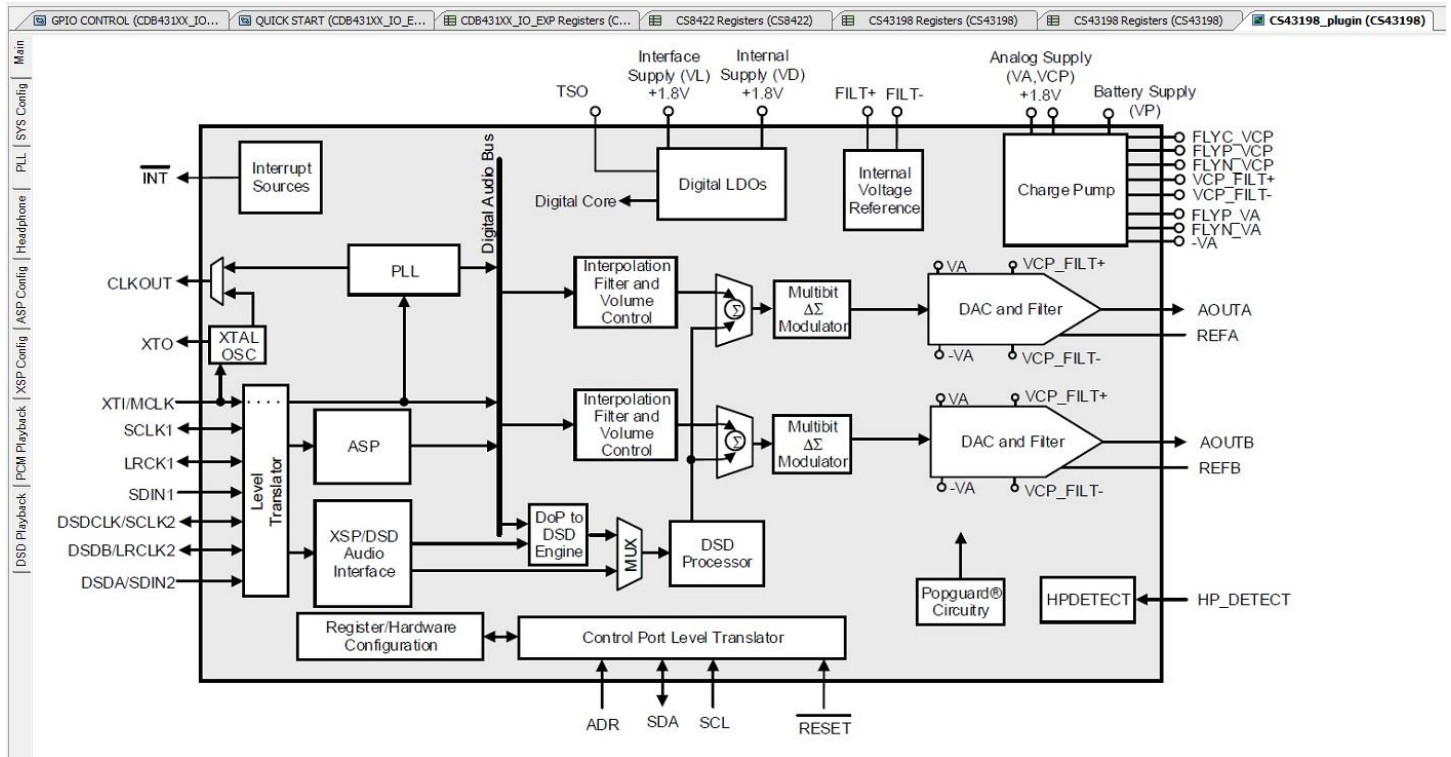
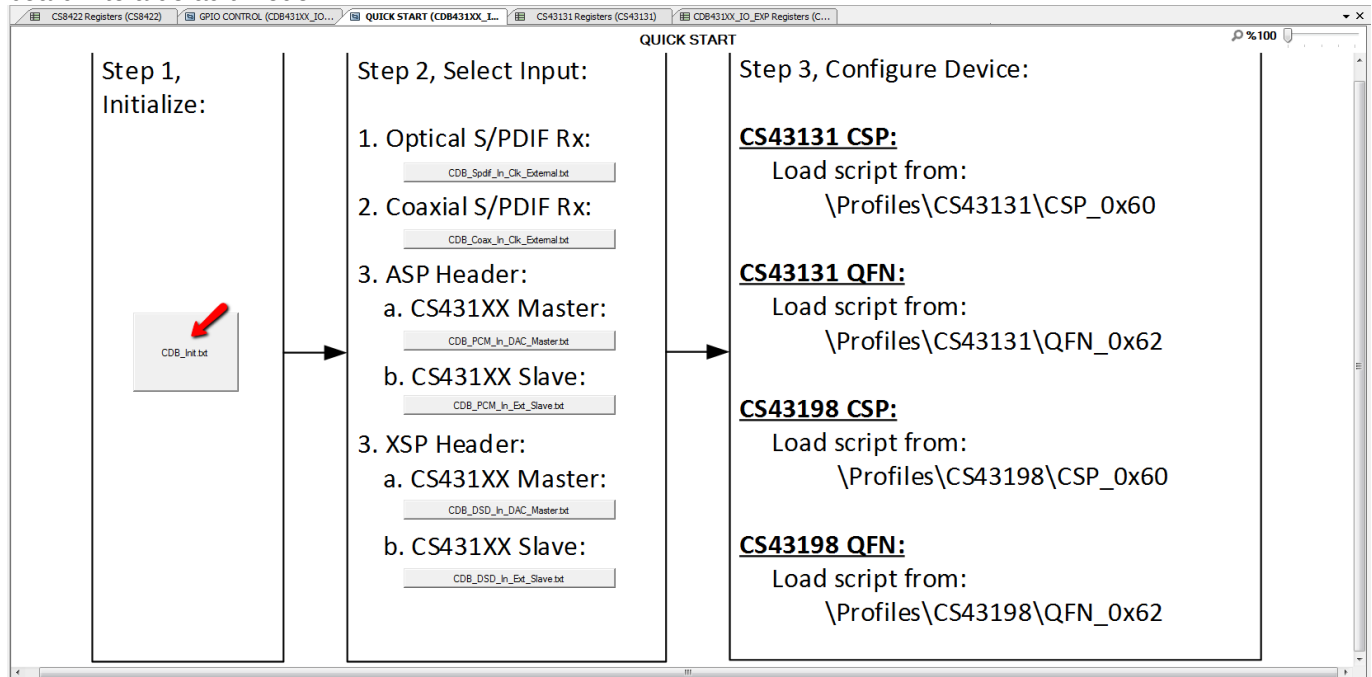


Figure 25 CS43198 Plugin

## 5.4 Initializing the Devices on the CDB43198 Board

The following steps show how to detect the presence of the CS43198s on the CDB43198 Board.

1. Under the CDB431XX\_I2C\_GPIP\_EXP menu, click on QUICK\_START, and click CDB\_INIT.txt. This will reset the board into a default mode.



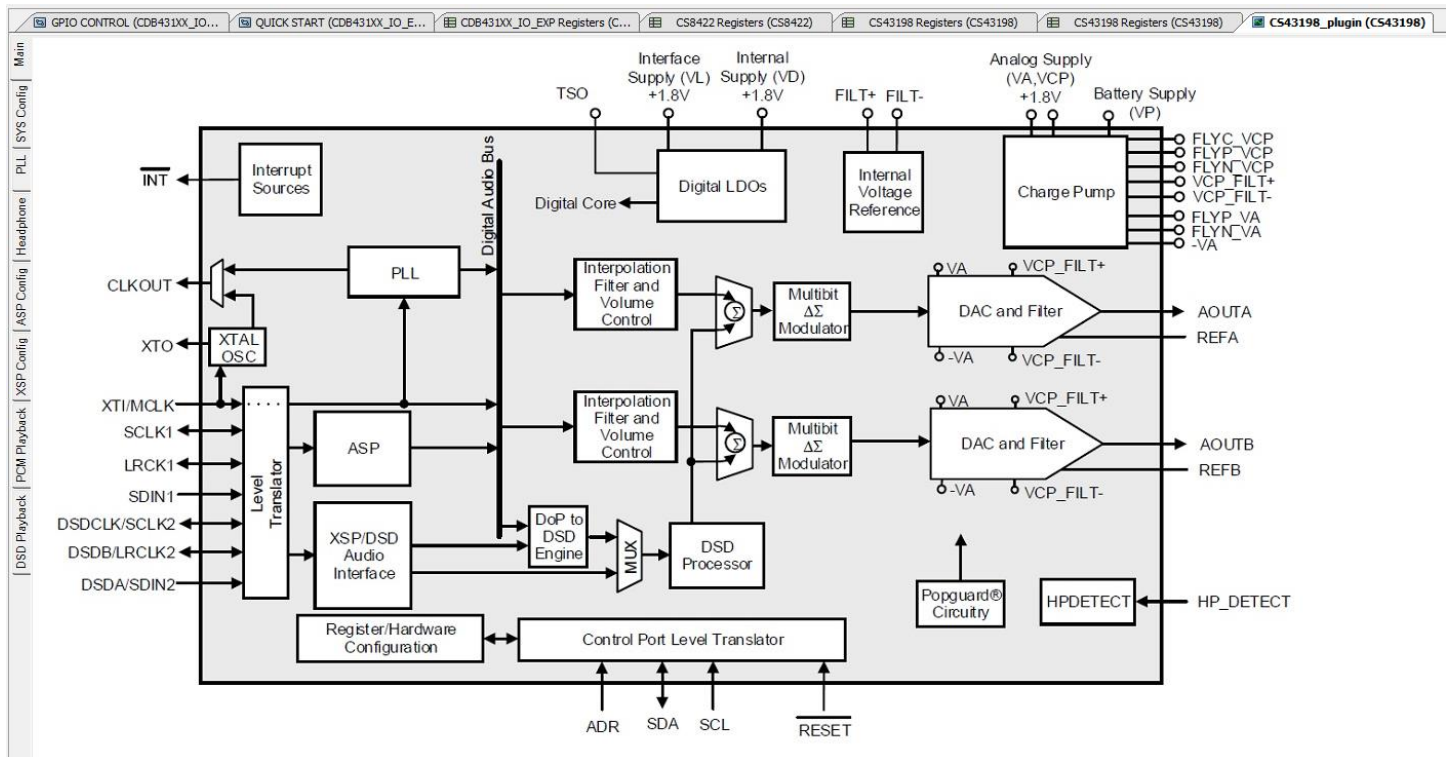
**Figure 26 Initialize DACs**

## 5.5 CS43198 Plugin

The CS43198 plugin has multiple tabs. Each tab provides an interface to configure and control specific IP Block(s) in the CS43198. The following sections describe each tab and its function. The user can configure the CS43198 using these tabs. However, it is recommended that the user initially use the profile scripts that are provided with the plugin to configure and control the CS43198 since each field will be preconfigured correctly for the proper mode.

### 5.5.1 Main Tab

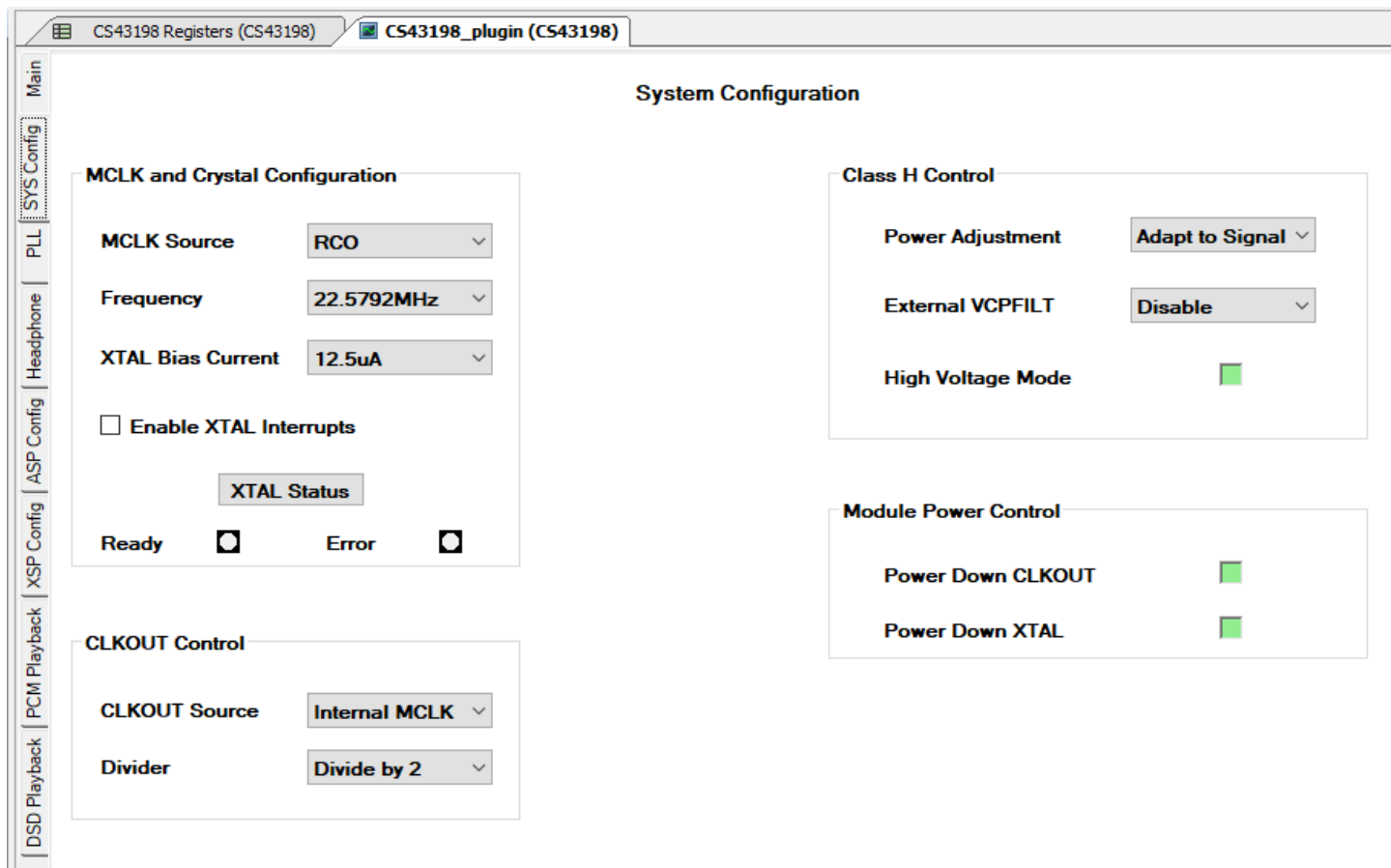
This tab shows the block diagram of the internal architecture of the CS43198.



**Figure 27 Main Tab**

## 5.5.2 Sys\_Config Tab

This tab allows user to configure the CS43198 clock input settings. It also allows the user to configure CLKOUT and Class-H amplifier settings.



The screenshot displays the 'Sys\_Config' tab within the 'CS43198\_plugin (CS43198)' window. The interface is organized into several sections:

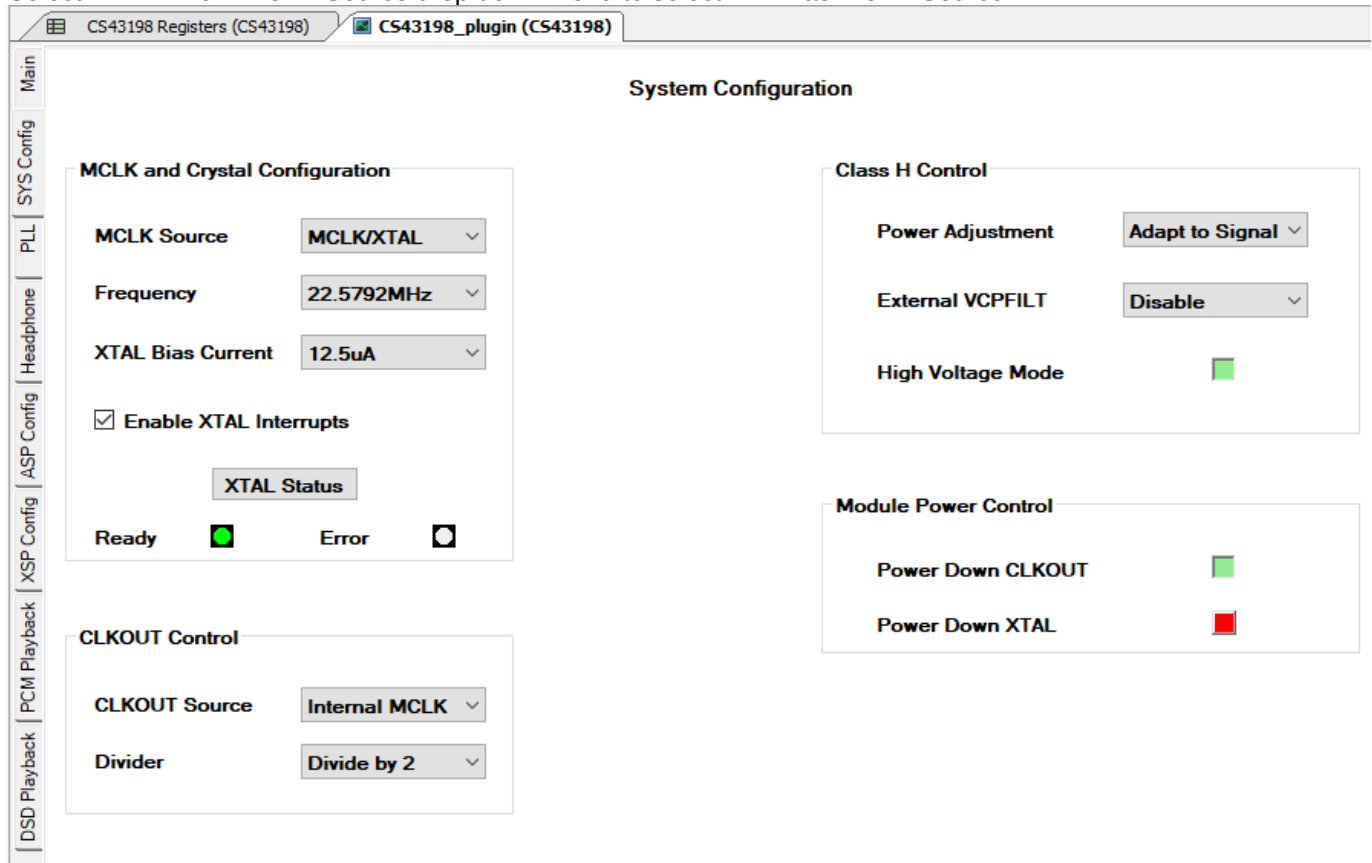
- System Configuration**: The main title of the configuration page.
- MCLK and Crystal Configuration**:
  - MCLK Source**: Set to 'RCO' (dropdown).
  - Frequency**: Set to '22.5792MHz' (dropdown).
  - XTAL Bias Current**: Set to '12.5uA' (dropdown).
  - Enable XTAL Interrupts**: An unchecked checkbox.
  - XTAL Status**: A button to check the status.
  - Ready** and **Error**: Each with a radio button, both currently unselected.
- CLKOUT Control**:
  - CLKOUT Source**: Set to 'Internal MCLK' (dropdown).
  - Divider**: Set to 'Divide by 2' (dropdown).
- Class H Control**:
  - Power Adjustment**: Set to 'Adapt to Signal' (dropdown).
  - External VCPFILT**: Set to 'Disable' (dropdown).
  - High Voltage Mode**: A green indicator light, currently on.
- Module Power Control**:
  - Power Down CLKOUT**: A green indicator light, currently on.
  - Power Down XTAL**: A green indicator light, currently on.

A vertical sidebar on the left contains navigation links: Main, Sys Config (highlighted), PLL, Headphone, ASP Config, XSP Config, PCM Playback, and DSD Playback.

Figure 28 Sys\_Config Tab

The example below shows the sequence of steps that should be followed to select On-board Crystal as MCLK source using Sys\_Config tab.

1. XTAL bias is set by default to 12.5  $\mu$ A.
2. Click on the Enable XTAL Interrupts check box to enable crystal interrupts.
3. Power up the Crystal Interface by clicking on the Power Down XTAL LED (LED color will change to Red).
4. Click on XTAL Status button. If "Ready" LED is lit, the crystal Interface has been configured successfully, and the CS43198 is ready to use XTAL as MCLK source. Go to step 6.
5. If "Error" LED is lit, then the crystal interface is not configured. Power down the board. Check the crystal and the crystal circuit on the board.
6. Select "XTAL" from MCLK Source drop down menu to select XTAL as MCLK Source.



**CS43198 Registers (CS43198)** **CS43198\_plugin (CS43198)**

**System Configuration**

**MCLK and Crystal Configuration**

MCLK Source: **MCLK/XTAL** ▾

Frequency: **22.5792MHz** ▾

XTAL Bias Current: **12.5uA** ▾

☒ Enable XTAL Interrupts

**XTAL Status**

Ready  Error 

**CLKOUT Control**

CLKOUT Source: **Internal MCLK** ▾

Divider: **Divide by 2** ▾

**Class H Control**

Power Adjustment: **Adapt to Signal** ▾

External VCPFLT: **Disable** ▾

High Voltage Mode: 

**Module Power Control**

Power Down CLKOUT: 

Power Down XTAL: 

Figure 29 Sys\_Config Tab with XTAL as MCLK Source

### 5.5.3 PLL Tab

This tab allows the user to configure the CS43198 PLL. The PLL can be used as an alternate source for the CS43198 MCLK.

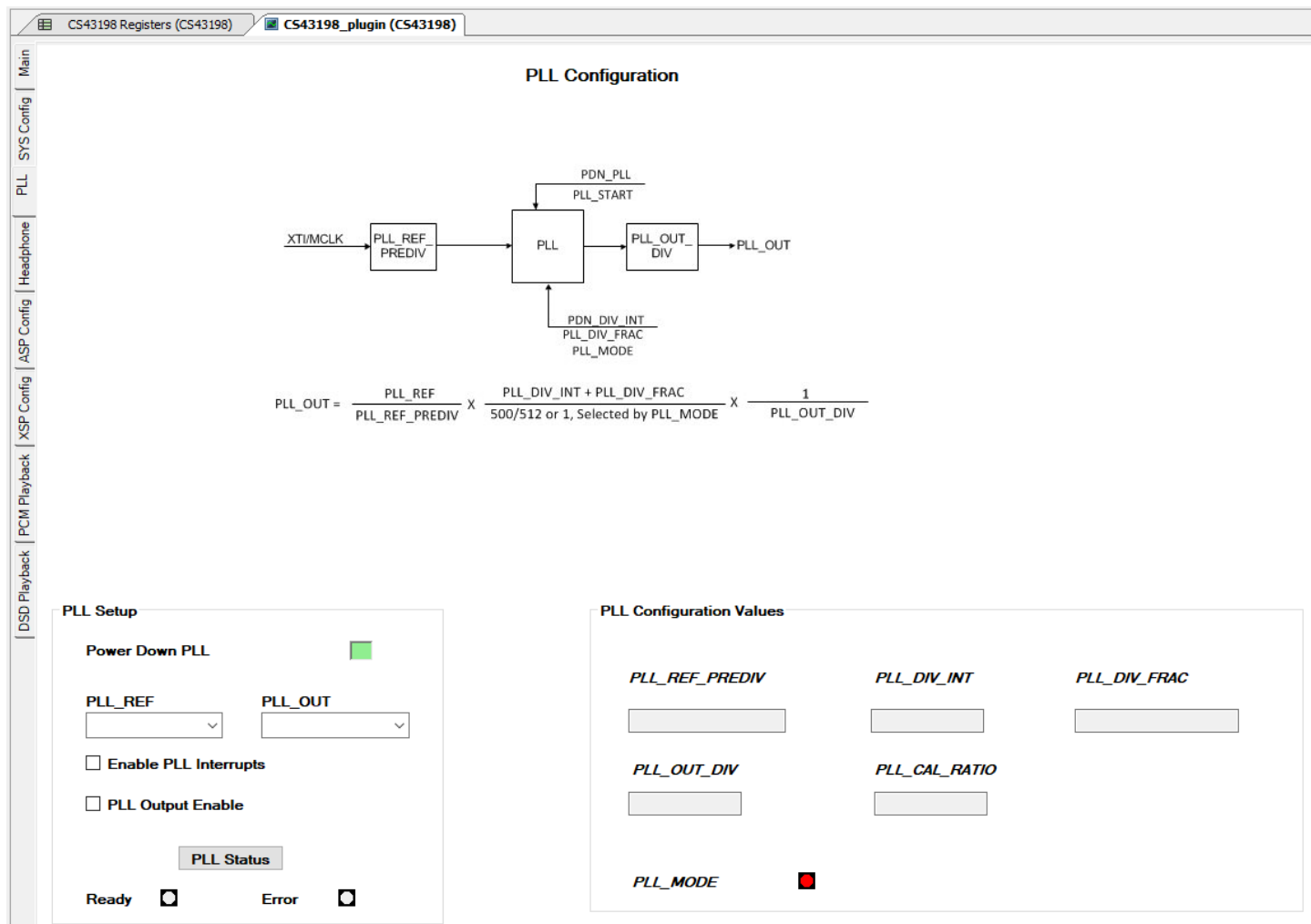


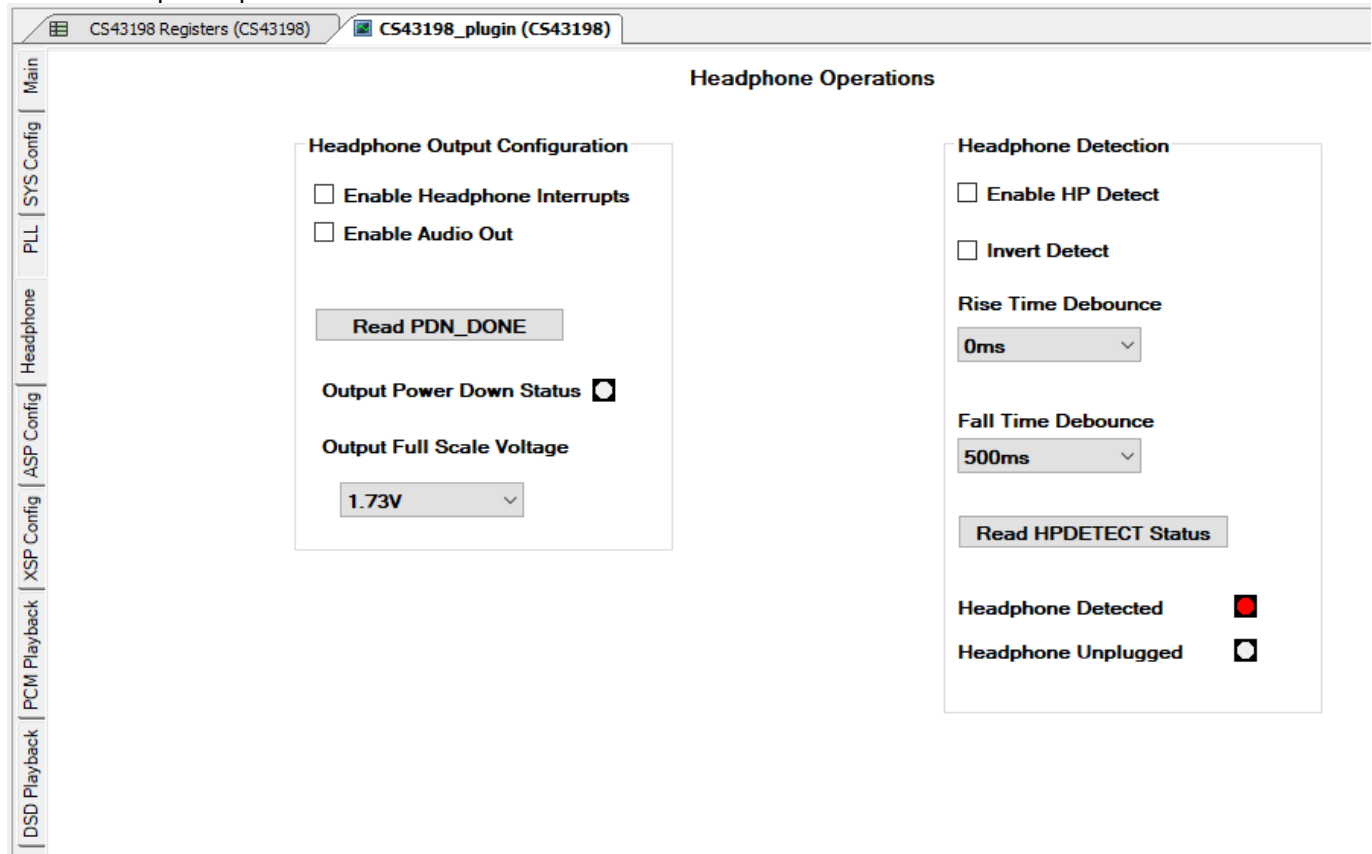
Figure 30 PLL Tab



### 5.5.4 Headphone Tab

This tab allows the user to perform the following functions:

1. Enable/disable headphone output
2. Enable headphone presence detection



The screenshot shows the 'Headphone Operations' tab within the 'CS43198\_plugin (CS43198)' window. The interface includes a sidebar with navigation options: Main, SYS Config, PLL, Headphone (selected), ASP Config, XSP Config, PCM Playback, and DSD Playback. The main content area is divided into two panels:

- Headphone Output Configuration:**
  - ☐ Enable Headphone Interrupts
  - ☐ Enable Audio Out
  - 
  - Output Power Down Status ☒
  - Output Full Scale Voltage:
- Headphone Detection:**
  - ☐ Enable HP Detect
  - ☐ Invert Detect
  - Rise Time Debounce:
  - Fall Time Debounce:
  - 
  - Headphone Detected: ☒
  - Headphone Unplugged: ☐

Figure 31 Headphone Tab

#### 5.5.4.1 Enabling Headphone Output

The following steps show how to enable the headphone output using the Headphone tab.

1. Enable headphone interrupts by checking the Enable Headphone Interrupts check box.
2. Configure MCLK source. Configure audio input port.
3. Power up headphone by checking the Enable Headphone Output check box.
4. The headphone output should be powered up.

### **5.5.4.2 Disabling Headphone Output**

The following steps show how to disable the headphone output using the Headphone tab.

1. If the CS43198 just came out of reset, the headphone output is already disabled, so the remaining steps can be skipped.
2. Enable headphone interrupts by checking the Enable Headphone Interrupts check box.
3. Uncheck the Enable Headphone Output check box to power down headphone.
4. Click on Read PDN\_HP Status button to read the status of PDN\_HP bit.
5. If the PDN\_HP bit is set, then the Power Down HP Status LED will turn red to indicate headphone has been powered down.

### **5.5.4.3 Headphone Presence Detection**

The following steps show how to enable headphone presence detection.

1. Enable headphone interrupts by checking the Enable Headphone Interrupts check box.
2. Enable invert detection (to account for the tip detect pin setup of the headphone jack) by checking the Invert Detect check box.
3. Enable headphone presence detection by checking the Enable HP Detect check box.
4. Click on the Read HPDETECT Status button to read status.
5. If a headphone is plugged into the headphone jack, then the Headphone Detected LED will turn green.

### **5.5.5 ASP Config Tab**

This tab allows the user to configure the ASP port. The following figure shows ASP Config tab contents when ASP is configured to operate in Slave mode.

CS43198 Registers (CS43198)

CS43198\_plugin (CS43198)

Main

SYS Config

PULL

Headphone

ASP Config

XSP Config

PCM Playback

DSD Playback

Port Config

☐ Enable ASP Interrupts
   
☐ Power Up ASP
   

ASP Mode

Slave

Sample Rate

44.1kHz

Sample Size

24 bits

Frame Configuration

ASP Data Type

I2S

ASP Frame Start

LRCK High to Low

ASP Configuration

Channel Configuration

Channel1

Enable

☒

Location (ASP SCLKs)

0

255

0

Channel Size

24bits

Active Phase

LRCK/FSYNC Low

Channel2

Enable

☒

Location (ASP SCLKs)

0

255

0

Channel Size

24bits

Active Phase

LRCK/FSYNC High

Clock Configuration

SCLK

Input Polarity

Inverted

Output polarity

Inverted

LRCLK

Input polarity

Normal

Output Polarity

Normal

LRCLK high Time (in SCLK cycles)

32

LRCLK Period

64

ASP Status

Overflow

☐

LRCLK Error

☐

LRCLK Late

☐

LRCLK Early

☐

No LRCLK

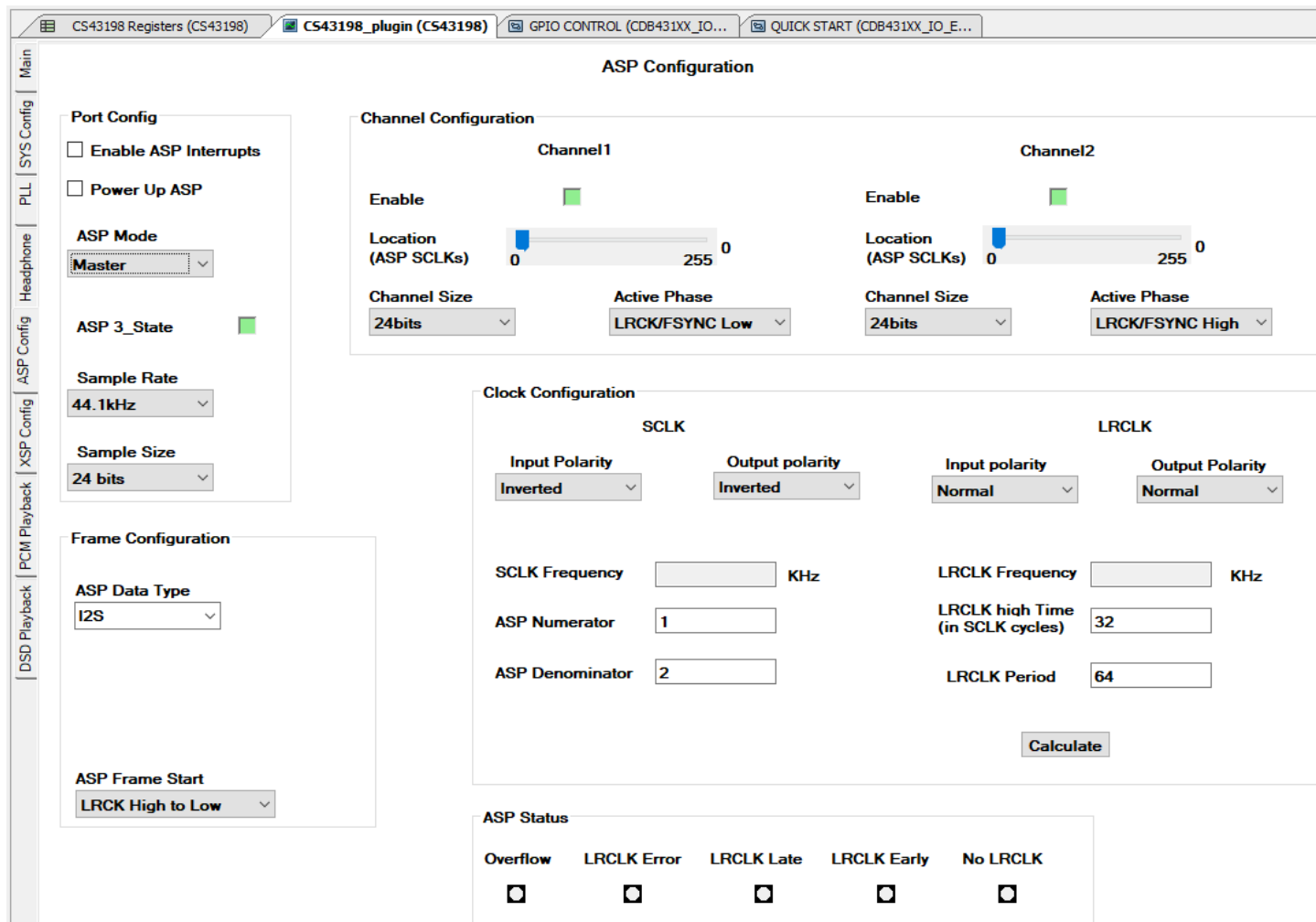
☐

Figure 32 ASP Config Tab

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DS1156DB2

The following figure shows the contents of ASP Config tab when ASP is configured to operate in Master mode.



**ASP Configuration**

**Port Config**

- ☐ Enable ASP Interrupts
- ☐ Power Up ASP
- ASP Mode: **Master** (dropdown)
- ASP 3\_State: ☒
- Sample Rate: **44.1kHz** (dropdown)
- Sample Size: **24 bits** (dropdown)

**Channel Configuration**

| Channel1             |                                     | Channel2             |                                     |
|----------------------|-------------------------------------|----------------------|-------------------------------------|
| Enable               | <input checked="" type="checkbox"/> | Enable               | <input checked="" type="checkbox"/> |
| Location (ASP SCLKs) | 0 (slider to 255)                   | Location (ASP SCLKs) | 0 (slider to 255)                   |
| Channel Size         | <b>24bits</b> (dropdown)            | Channel Size         | <b>24bits</b> (dropdown)            |
| Active Phase         | <b>LRCK/FSYNC Low</b> (dropdown)    | Active Phase         | <b>LRCK/FSYNC High</b> (dropdown)   |

**Clock Configuration**

| SCLK                      |                            | LRCLK                            |                          |
|---------------------------|----------------------------|----------------------------------|--------------------------|
| Input Polarity            | <b>Inverted</b> (dropdown) | Input polarity                   | <b>Normal</b> (dropdown) |
| Output polarity           | <b>Inverted</b> (dropdown) | Output Polarity                  | <b>Normal</b> (dropdown) |
| SCLK Frequency            | <input type="text"/> KHz   | LRCLK Frequency                  | <input type="text"/> KHz |
| ASP Numerator             | <b>1</b> (input)           | LRCLK high Time (in SCLK cycles) | <b>32</b> (input)        |
| ASP Denominator           | <b>2</b> (input)           | LRCLK Period                     | <b>64</b> (input)        |
| <b>Calculate</b> (button) |                            |                                  |                          |

**Frame Configuration**

- ASP Data Type: **I2S** (dropdown)
- ASP Frame Start: **LRCK High to Low** (dropdown)

**ASP Status**

|                                     |                                     |                                     |                                     |                                     |
|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| Overflow                            | LRCLK Error                         | LRCLK Late                          | LRCLK Early                         | No LRCLK                            |
| <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |

Figure 33 ASP Config Tab in Master Mode

Click the Calculate button to determine the frequencies of the SCLK and LRCLK signals. When this button is clicked, the SCLK and LRCLK values will be calculated based on the selected frequency of Internal MCLK (MCLK\_INT) and the values in ASP Numerator, ASP Denominator, LRCLK high Time and LRCLK Period text boxes. The value in the LRCLK Frequency text box will be used to set the new sample rate (if it is not already set by user) when the ASP is powered up.

**Clock Configuration**

SCLK

Input Polarity

Inverted ▾

Output polarity

Inverted ▾

LRCLK

Input polarity

Normal ▾

Output Polarity

Normal ▾

SCLK Frequency

2822.4

KHz

LRCLK Frequency

44.1

KHz

ASP Numerator

1

LRCLK high Time  
(in SCLK cycles)

32

ASP Denominator

8

LRCLK Period

64

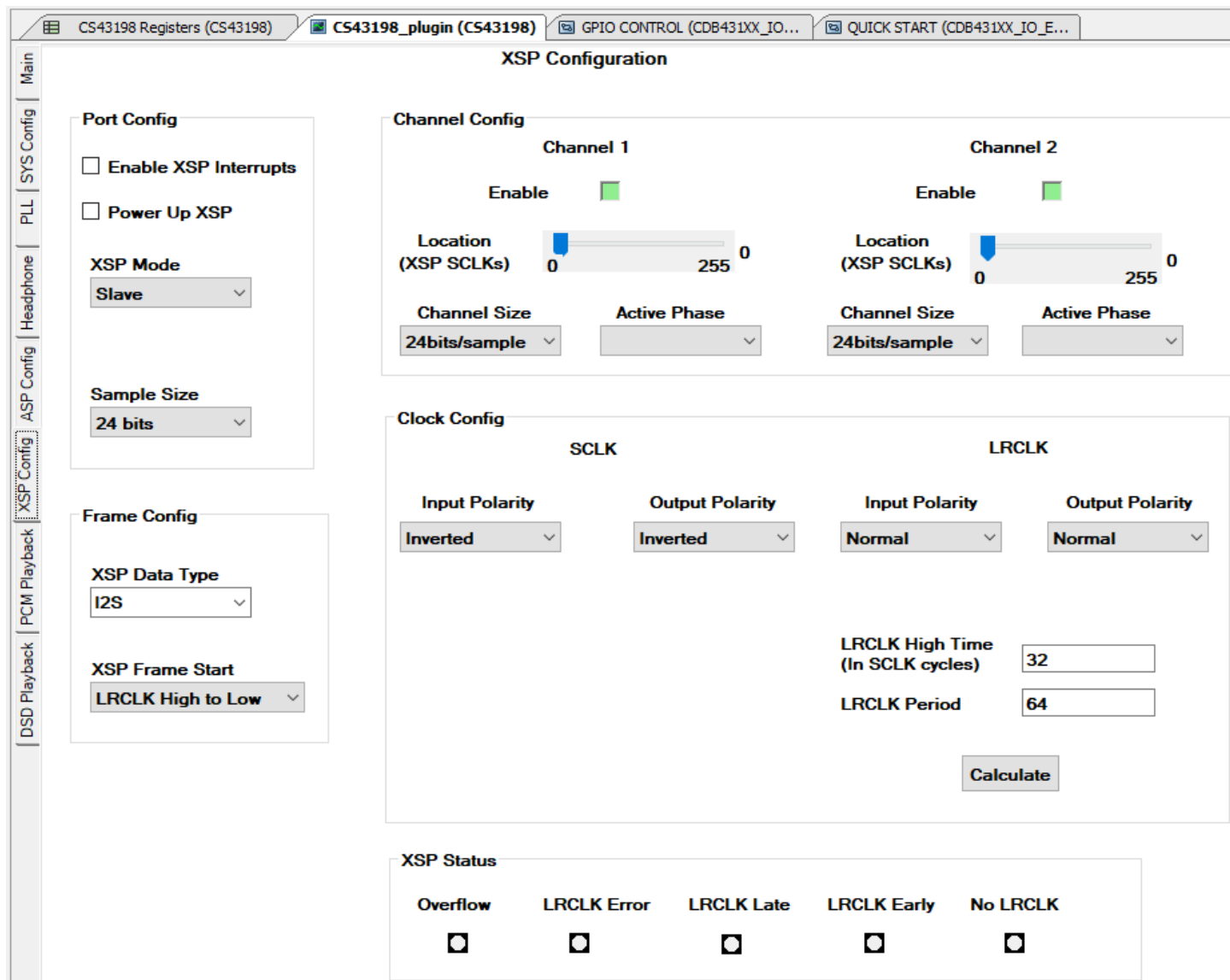
Calculate

**Figure 34 Calculating ASP Clock Frequencies**

It is recommended to use a profile script to configure this port since each field will be preconfigured correctly for the proper mode.

## 5.5.6 XSP Config Tab

This tab allows the user to configure the XSP port. The following figure shows XSP Config tab contents when XSP is configured to operate in Slave mode.



**XSP Configuration**

**Port Config**

- ☐ Enable XSP Interrupts
- ☐ Power Up XSP
- XSP Mode**: Slave
- Sample Size**: 24 bits

**Channel Config**

**Channel 1**

- Enable: ☒
- Location (XSP SCLKs): 0 to 255
- Channel Size: 24bits/sample
- Active Phase:

**Channel 2**

- Enable: ☒
- Location (XSP SCLKs): 0 to 255
- Channel Size: 24bits/sample
- Active Phase:

**Clock Config**

**SCLK**

- Input Polarity: Inverted
- Output Polarity: Inverted

**LRCLK**

- Input Polarity: Normal
- Output Polarity: Normal
- LRCLK High Time (In SCLK cycles): 32
- LRCLK Period: 64
- Calculate

**XSP Status**

- Overflow: ☐
- LRCLK Error: ☐
- LRCLK Late: ☐
- LRCLK Early: ☐
- No LRCLK: ☐

Figure 35 XSP Config Tab in Slave Mode

The following figure shows the contents of XSP Config tab when XSP is configured to operate in Master mode.

CS43198 Registers (CS43198)

CS43198\_plugin (CS43198)

GPIO CONTROL (CDB431XX\_IO...

QUICK START (CDB431XX\_IO\_E...

Main

SYS Config

PLL

Headphone

ASP Config

XSP Config

PCM Playback

DSD Playback

Port Config

☐ Enable XSP Interrupts
   
☐ Power Up XSP
   

XSP Mode

Master

XSP 3\_State

Sample Size

24 bits

Frame Config

XSP Data Type

I2S

XSP Frame Start

LRCLK High to Low

XSP Configuration

Channel 1

Enable

Location (XSP SCLKs)

0 255 0

Channel Size

24bits/sample

Active Phase

Channel 2

Enable

Location (XSP SCLKs)

0 255 0

Channel Size

24bits/sample

Active Phase

Clock Config

SCLK

Input Polarity

Inverted

Output Polarity

Inverted

SCLK Frequency

KHz

XSP Numerator

1

XSP Denominator

2

LRCLK

Input Polarity

Normal

Output Polarity

Normal

LRCLK Frequency

KHz

LRCLK High Time (In SCLK cycles)

32

LRCLK Period

64

Calculate

XSP Status

Overflow

LRCLK Error

LRCLK Late

LRCLK Early

No LRCLK

Figure 36 XSP Config Tab in Master mode

38

DS1156DB2

Click the Calculate button to determine the frequencies of the SCLK and LRCLK signals. When this button is clicked, the SCLK and LRCLK values will be calculated based on the selected frequency of Internal MCLK (MCLK\_INT) and the values in XSP Numerator, XSP Denominator, LRCLK high Time and LRCLK Period text boxes. The value in the LRCLK Frequency text box will be used to set the new sample rate (if it is not already set by user) when the XSP is powered up.

Clock Config

SCLK

LRCLK

Input Polarity

Inverted ▾

Output Polarity

Inverted ▾

Input Polarity

Normal ▾

Output Polarity

Normal ▾

SCLK Frequency

2822.4

KHz

LRCLK Frequency

44.1

KHz

XSP Numerator

1

LRCLK High Time  
(In SCLK cycles)

32

XSP Denominator

8

LRCLK Period

64

Calculate

**Figure 37 Calculating XSP Clock Frequencies**

It is recommended to use a profile script to configure this port since each field will be preconfigured correctly for the proper mode.



## 5.5.7 PCM Playback Tab

This tab allows the user to configure PCM playback path. This tab allows the user to change PCM filter dynamically during playback. The impulse and magnitude responses of the selected filter are displayed. It is recommended to use a profile script to configure this part since each field will be preconfigured correctly for the proper mode.

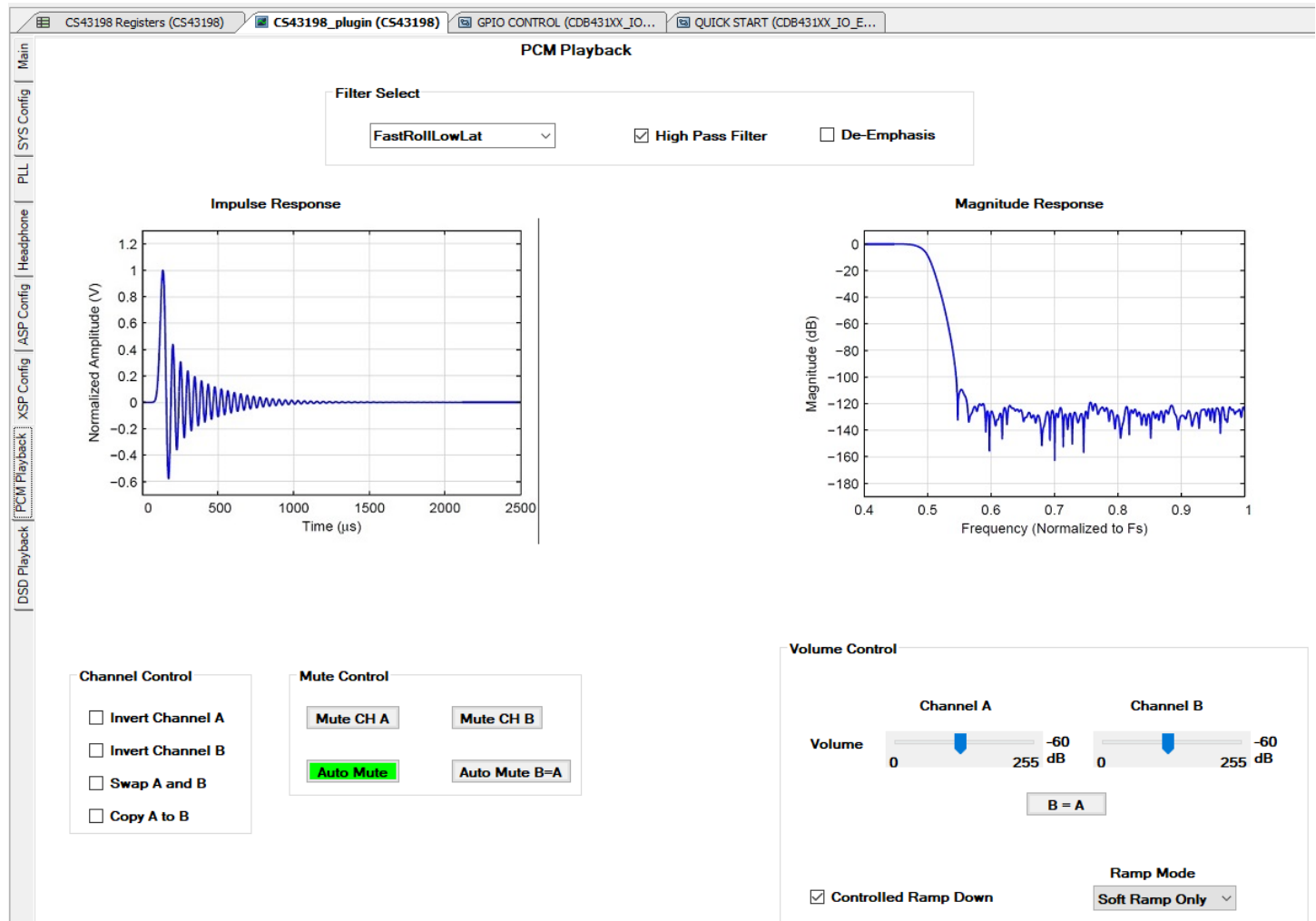


Figure 38 PCM Playback Tab

### 5.5.8 DSD Playback Tab

This tab allows the user to configure the DSD/DoP playback path. It is recommended to use a profile script to configure this port.

CS43198 Registers (CS43198)

CS43198\_plugin (CS43198)

GPIO CONTROL (CDB431XX\_IO...

QUICK START (CDB431XX\_IO\_E...

Main

SYS Config

PLL

Headphone

ASP Config

ASP Config

XSP Config

PCM Playback

DSD Playback

#### DSD Playback

##### DSD Interface Config

☐ Enable DSD Interrupts

☐ Enable DoP Interrupts

Power Down DSD Interface ■

DSDIF Mode Slave

DSD PM Enable ■

DSD PM Mode 128\*Fs

##### DSD PCM Mixing

☐ Enable PCM Playback Path

☐ Mix PCM and DSD

##### Mute Control

Mute CH A

Mute CH B

Auto Mute

Auto Mute B=A

##### DSD/DoP Status

|                          |                          |                          |                          |                          |                          |                          |                          |
|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Stuck                    | Invalid CH A             | Invalid CH B             | Silence CH A             | Silence CH B             | Rate Error               | DoP Marker               | DoP Decoder              |
| <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |

##### DSD processor Config

☐ DSD Enable

DSD Source DSDIF

DSD Speed 64\*Fs

☒ Static DSD Detect

PCM 0dB Match SACD 3.1dB

☐ Invalid DSD Detect

DSD = PCM

☒ High Pass Filter

☐ Invert CH A

☐ Invert CH B

☐ Swap A and B

☐ Copy A to B

##### Volume Control

Channel A

Channel B

Volume

0

255

-60 dB

0

255

-60 dB

B = A

##### Soft Ramp Control

Soft Ramp Soft Ramp

Figure 39 DSD Playback Tab

## 6 Testing Various Use cases

Profile scripts are provided along with the plugin to allow the user to test various common use cases. The profile scripts for CS43198 can be found in {WISCE\_INSTALL\_FOLDER}/Profiles/CS43198. If needed, users can create their own profile scripts to suit their requirements. Individual scripts are provided for each combination of Sample Rate and Output Voltage level for both PCM and DSD modes. The following table shows the list of supported use cases along with corresponding profile scripts.

**Table 11 Profile Scripts**

| Use Case                  | DAC mode | Scripts (for CS43198)                                                                                                                          | Audio Input Source           |
|---------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| PCM Playback              | Master   | CDB_PCM_In_DAC_Master,<br>ASP_Master_PCM_Playback_xxx_yyy <sup>1</sup><br>xxx is the sample rate<br>yyy is the output voltage level            | PCM through ASP header (J25) |
| PCM Playback              | Slave    | CDB_Spdif_In_Clk_External,<br>XTAL_In_ASP_Slave_PCM_Playback_xxx_yyy <sup>2</sup><br>xxx is the sample rate<br>yyy is the output voltage level | S/PDIF (J10)                 |
|                           |          | CDB_Coax_In_Clk_External,<br>XTAL_In_ASP_Slave_PCM_Playback_xxx_yyy <sup>2</sup><br>xxx is the sample rate<br>yyy is the output voltage level  | Coaxial (J11)                |
|                           |          | CDB_PCM_In_Ext_Slave<br>XTAL_In_ASP_Slave_PCM_Playback_xxx_yyy <sup>2</sup><br>xxx is the sample rate<br>yyy is the output voltage level       | PCM through ASP header (J25) |
| DSD Playback              | Slave    | CDB_DSD_In_Ext_Slave,<br>Slave_DSD_Playback_xxx_yyy <sup>3</sup><br>xxx is the DSD Speed<br>yyy is the output voltage level                    | DSD through XSP header (J26) |
| DoP Playback (64fs Mode)  | Slave    | CDB_PCM_In_Ext_Slave,<br>DoP_DSD64_playback_XTAL_Slave                                                                                         | PCM through ASP header (J25) |
|                           |          | CDB_Spdif_In_Clk_External,<br>DoP_DSD64_playback_XTAL_Slave                                                                                    | S/PDIF (J10)                 |
|                           |          | CDB_Coax_In_Clk_External,<br>DoP_DSD64_playback_XTAL_Slave                                                                                     | Coaxial (J11)                |
| DoP Playback (128fs Mode) | Slave    | CDB_PCM_In_Ext_Slave,<br>DoP_DSD128_playback_XTAL_Slave                                                                                        | PCM through ASP header (J25) |
| Switch MCLK frequency     | —        | Switch_MCLK_Frequency                                                                                                                          | —                            |

Notes:

1. For example, if the desired sample rate is 48 kHz and desired output voltage is 1 V, then load the ASP\_Master\_PCM\_Playback\_48K\_1V0 script.
2. For example, if the incoming sample rate is 48 kHz and desired output voltage is 1 V, then load the XTAL\_In\_ASP\_Slave\_PCM\_Playback\_48K\_1V0 script.
3. For example, if playing back DSD stream at 64 Fs and the desired output voltage is 1.7 V, then load the Slave\_DSD\_Playback\_64fs\_1v7 script.

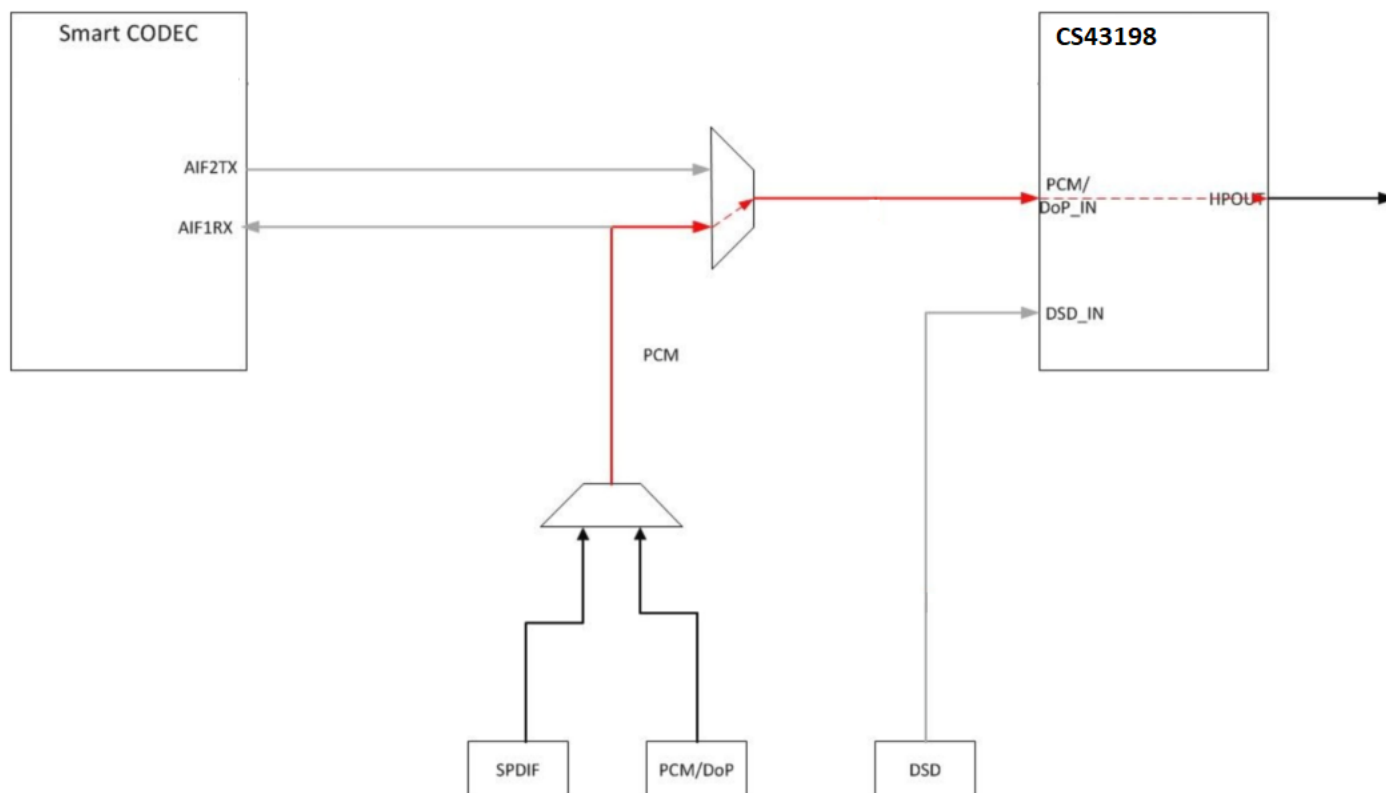
**Table 12 Additional Profile Scripts for CS43198**

| Script                 | Function                                   |
|------------------------|--------------------------------------------|
| Power_Up_HP            | Power up HP and ASP (for PCM/DoP playback) |
| Power_Up_HP_DSD_mode   | Power up HP (for DSD playback)             |
| Power_Down_HP_PCM_mode | Power down ASP and HP                      |
| Power_Down_HP_DSD_mode | Power down HP                              |

## 6.1 Data Flow for Various Use Cases

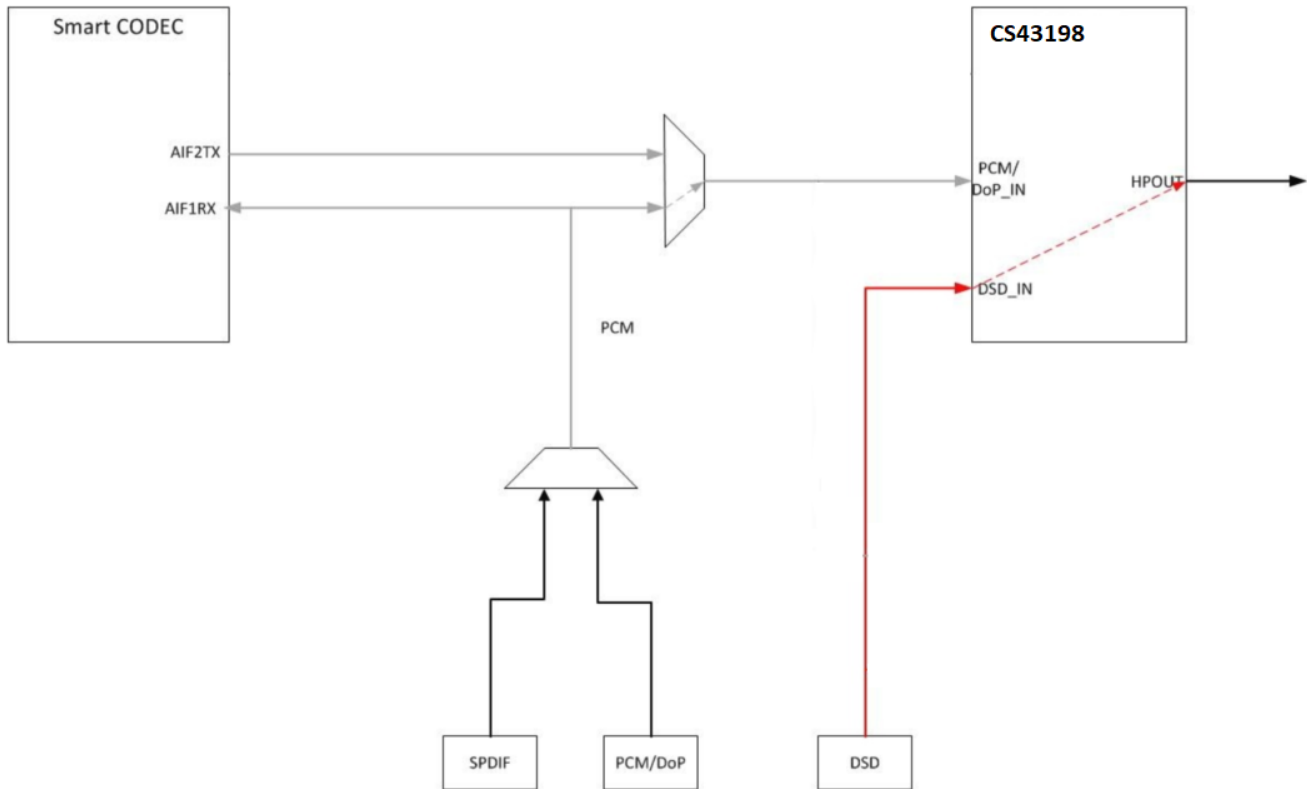
The following sections depict the flow of data, in red, for various common use cases.

### 6.1.1 PCM Playback



**Figure 40 PCM Playback Data Flow**

### 6.1.2 DSD Playback



**Figure 41 DSD Playback Data Flow**

## 6.2 Measuring Dynamic Range and THD+N for the CS43198

This section describes the test setup and the procedure to measure dynamic range and THD+N for CS43198.

### 6.2.1 Test Program Setup

The following steps show how to setup the CDB43198 for THD+N measurement. Please make sure that the CDB43198 jumpers are set to factory default mode.

1. Power up the CDB43198 by applying +5 V or VBUS through a USB connection.
2. Connect a cable from "Digital Serial IO" Transmitter port of an APx (e.g. APx555) to header J25 on CDB43198 board. There is no need to connect the MCLK signal.
3. Follow the steps described in the Quick Setup Guide to launch WISCE and load plugins.
4. Load the profile script CDB\_PCM\_In\_Ext\_Slave from {WISCE\_INSTALL\_FOLDER}/Profiles/CS43198 .

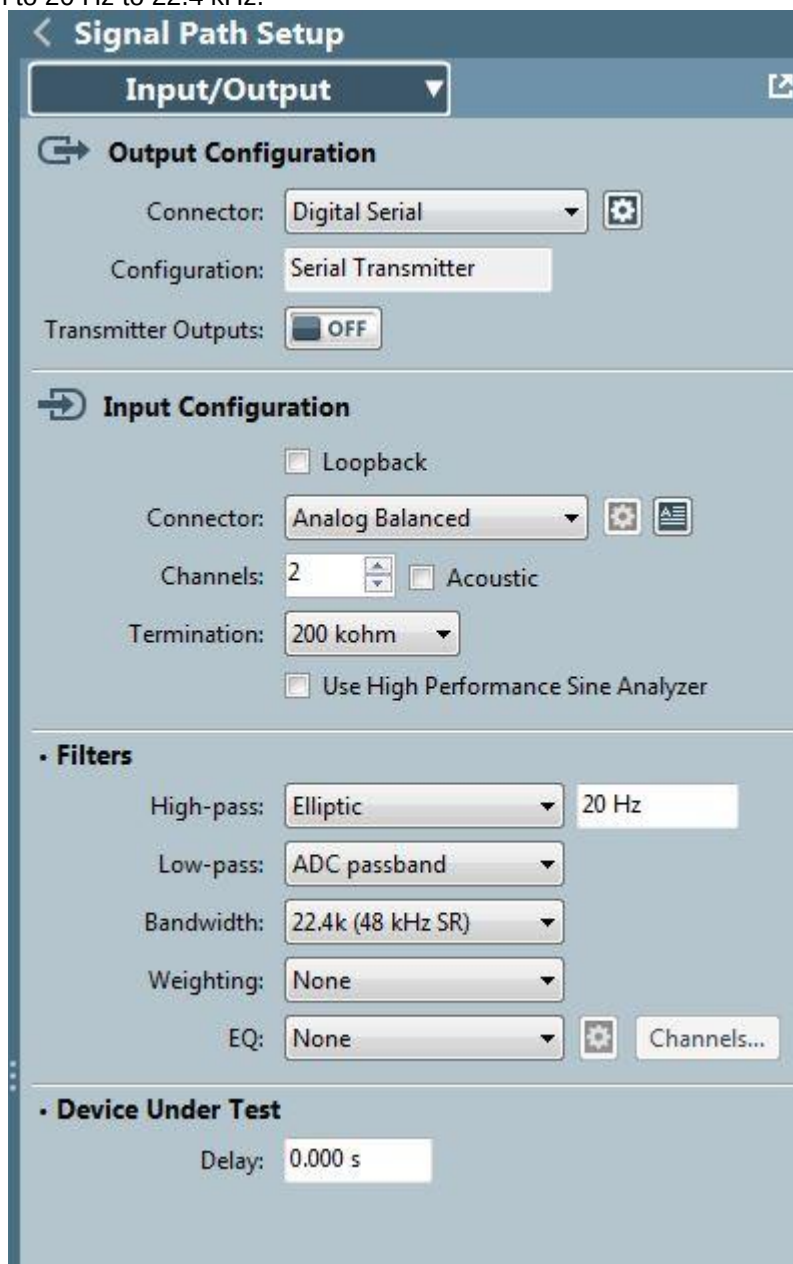


Figure 42 Test Setup

## 6.2.2 APx Setup

The following steps show how to configure the APx for running the tests. This procedure was tested using an APx555.

1. Run the APx software. (APx500 v4.2 if using an APx555)
2. Set the APx Output to Digital Serial and Input to Analog Balanced.
3. Set the Input Bandwidth to 20 Hz to 22.4 kHz.



**Signal Path Setup**

**Input/Output**

**Output Configuration**

Connector: Digital Serial

Configuration: Serial Transmitter

Transmitter Outputs: OFF

**Input Configuration**

☐ Loopback

Connector: Analog Balanced

Channels: 2 ☐ Acoustic

Termination: 200 kohm

☐ Use High Performance Sine Analyzer

**Filters**

High-pass: Elliptic 20 Hz

Low-pass: ADC passband

Bandwidth: 22.4k (48 kHz SR)

Weighting: None

EQ: None Channels...

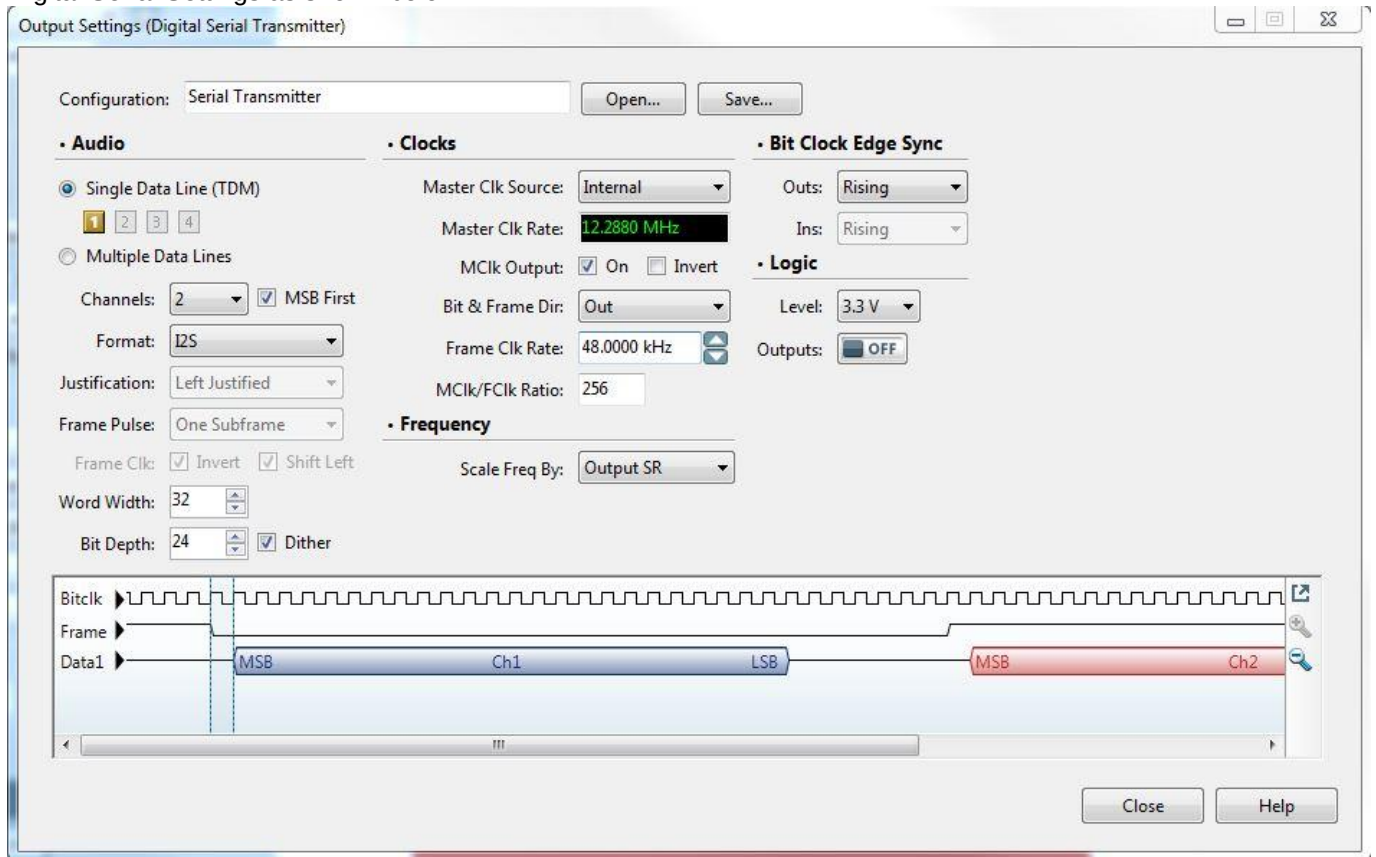
**Device Under Test**

Delay: 0.000 s

Figure 43 APx Signal Path Setup



- In the Signal Path Setup panel, click on the settings button next to Connector drop down menu and configure Digital Serial Settings as shown below.



**Figure 44 Digital Serial Settings**



- To launch the Dynamic Range Measurement test, click on Project-> Add Measurement -> Meters -> Dynamic Range - AES17. This will launch the dynamic range test screen.

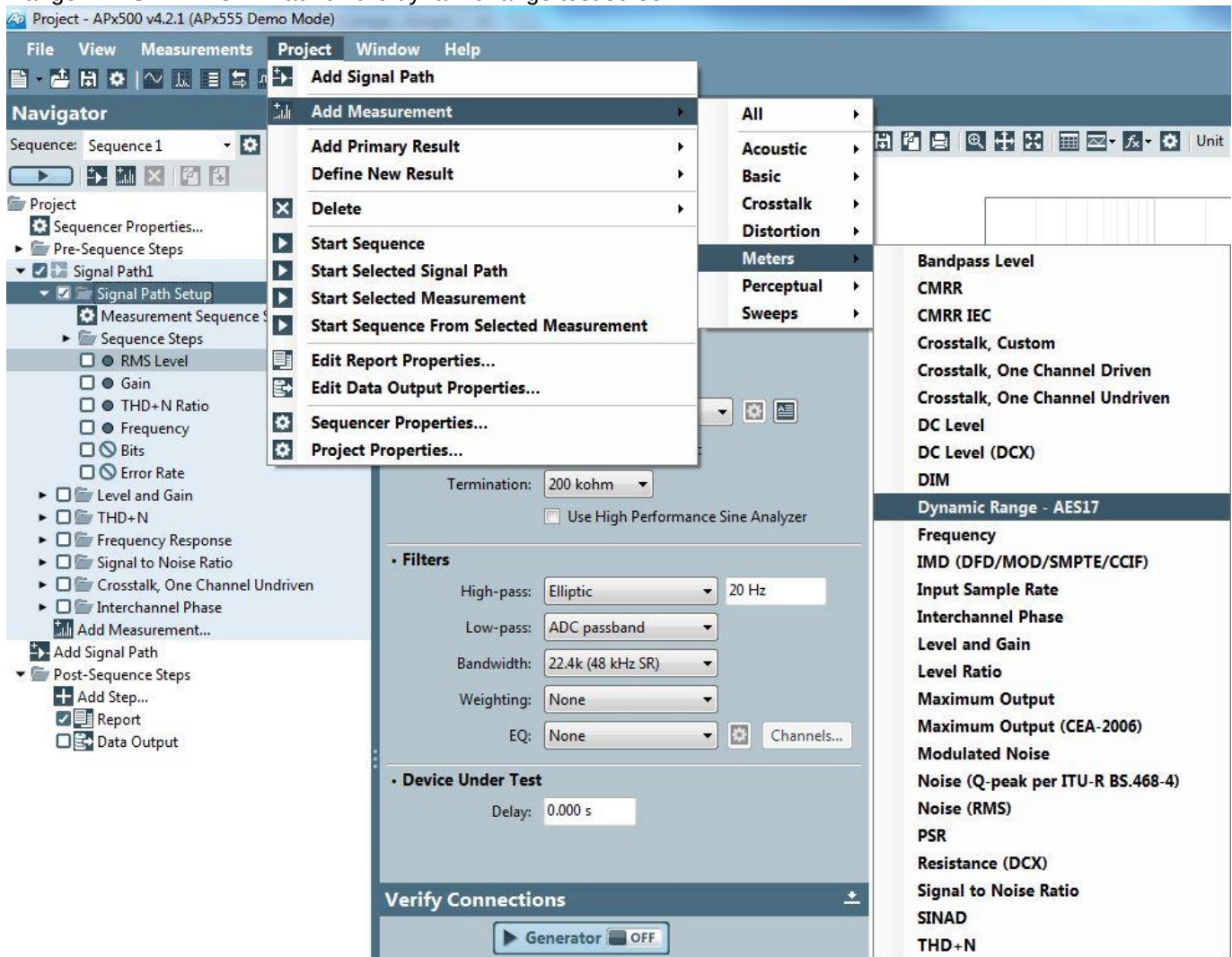
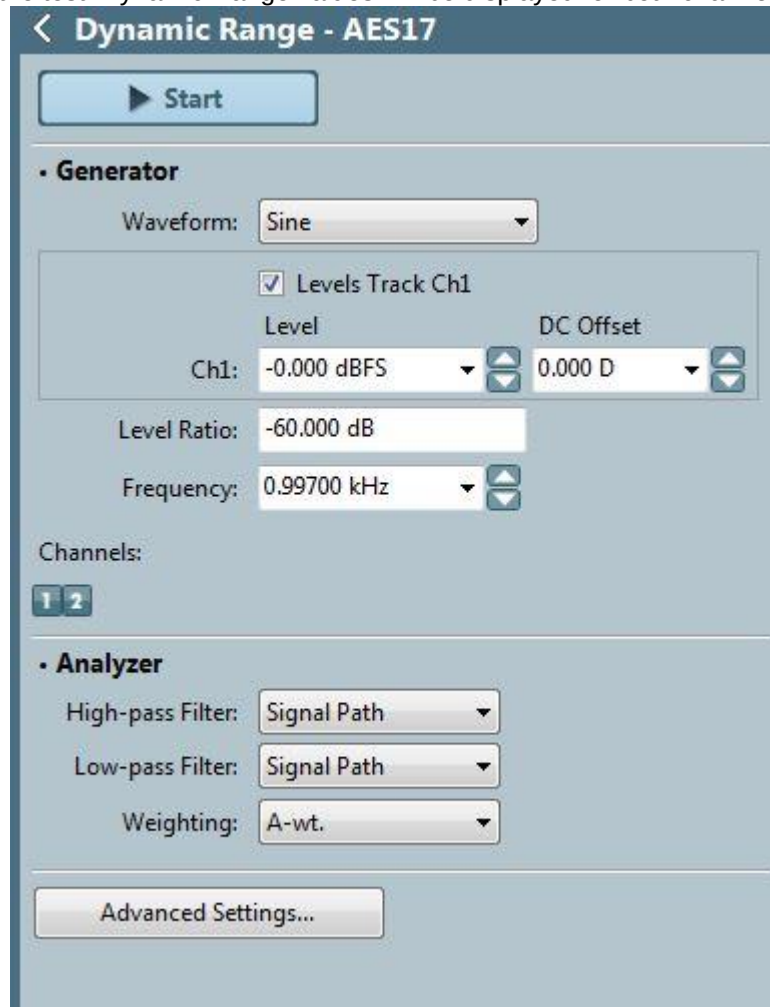


Figure 45 Launch Dynamic Range Test

6. To run the Dynamic Range Measurement test, configure the Input Level and Bandwidth as shown below. Click on the "Start" button to run the test. Dynamic Range values will be displayed for both channels.



**< Dynamic Range - AES17**

**Start**

**• Generator**

Waveform: Sine

☒ Levels Track Ch1

Level: Ch1: -0.000 dBFS

DC Offset: 0.000 D

Level Ratio: -60.000 dB

Frequency: 0.99700 kHz

Channels: 1 2

**• Analyzer**

High-pass Filter: Signal Path

Low-pass Filter: Signal Path

Weighting: A-wt.

**Advanced Settings...**

Figure 46 Dynamic Range Test

7. To launch THD+N test, click on Project-> Add Measurement -> Meters ->THD+N to launch THD+N measurement window.

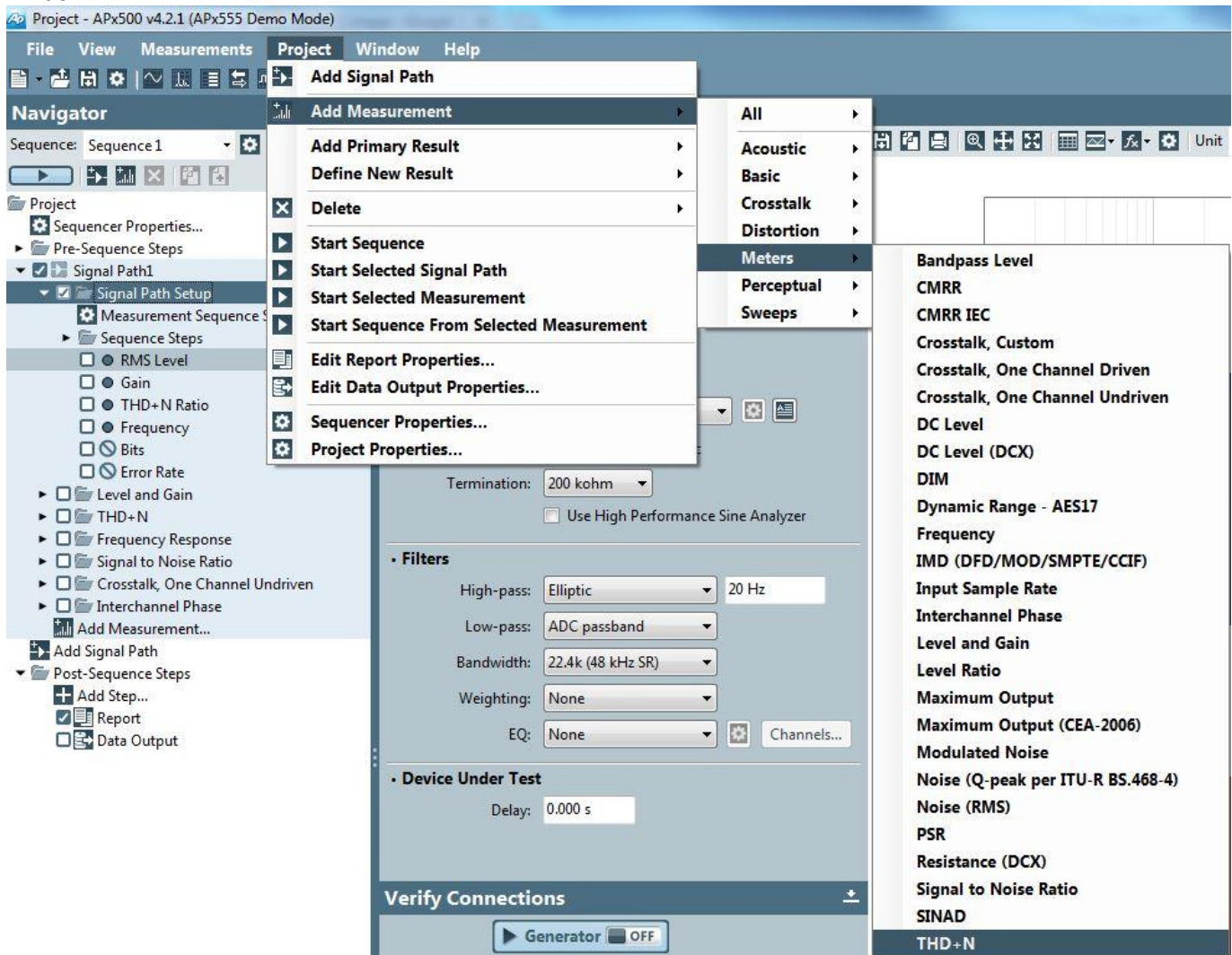
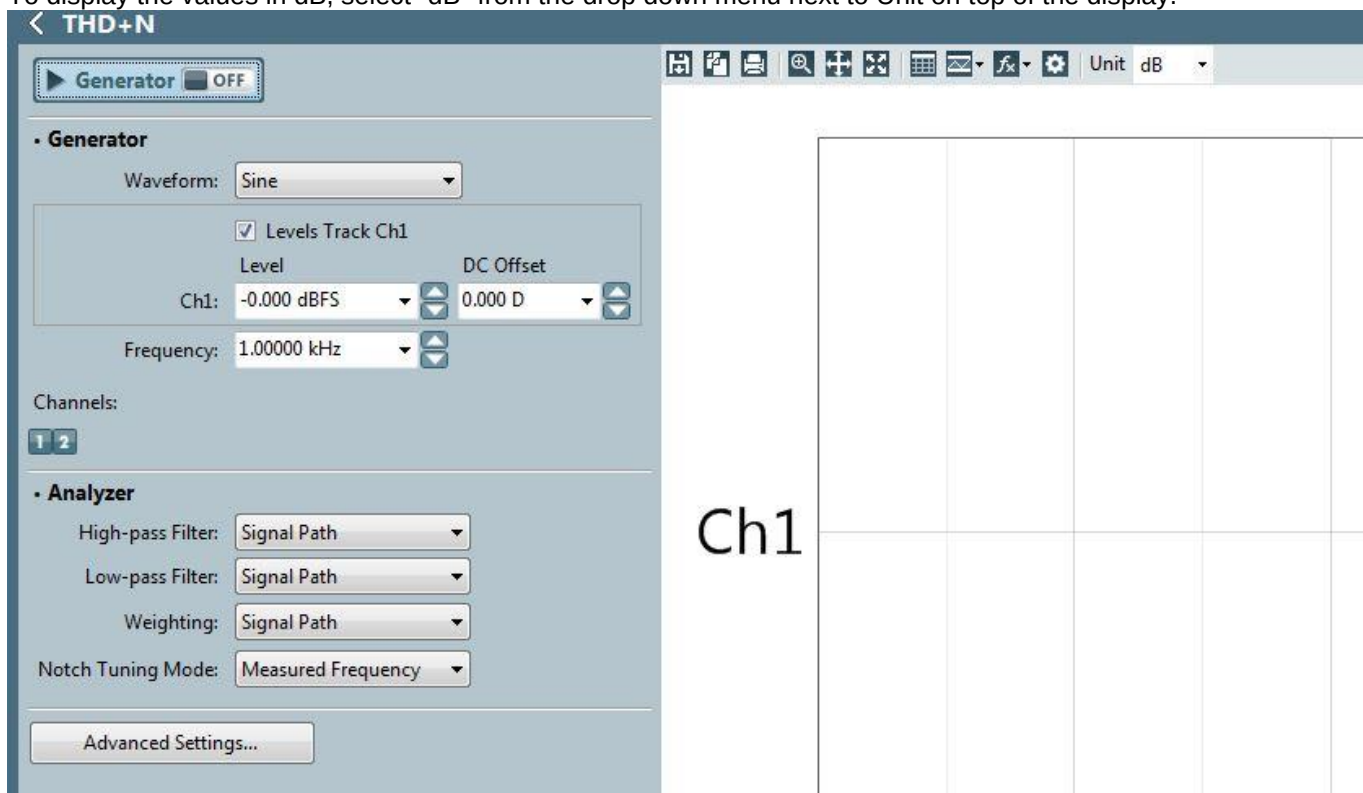


Figure 47 Launch THD+N Test

8. To run THD+N test, configure the Input Level and Bandwidth as shown below. Click on the "Generator" button to run the test. THD+N ratio will be displayed for both channels. THD+N ratio is typically displayed in Percentage (%). To display the values in dB, select "dB" from the drop down menu next to Unit on top of the display.



**Figure 48 THD+N Measurement Settings**



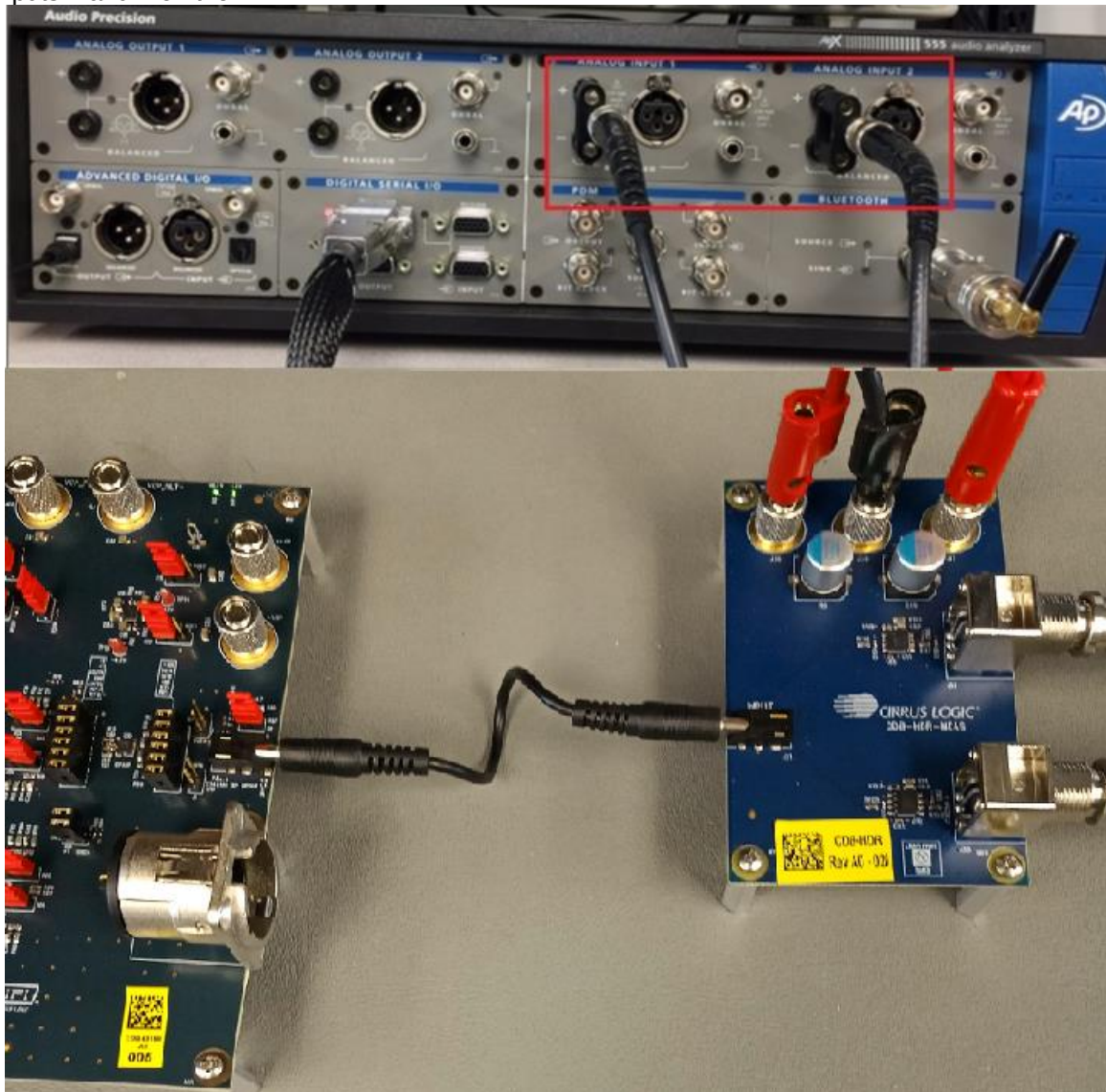
## 6.2.3 Measuring Dynamic Range for the CS43198

To measure dynamic range in WISCE click File->Load and select XTAL\_In\_ASP\_Slave\_PCM\_Playback\_48K\_1v7.txt file from {WISCE\_INSTALL\_FOLDER}/profiles/CS43198 to configure CS43198 for audio playback in Slave Mode. Note, this method only works when measuring the CSP device. The QFN device (with mono output) does not interface easily with the CDB-HDR-MEAS board.

### 6.2.3.1 Measuring Dynamic Range

The following steps show the procedure to measure dynamic range.

1. Place a jumper connecting the 600- $\Omega$  load on J15.
2. Place a jumper connecting the 600- $\Omega$  load on J4.
3. Connect a headphone cable between CSP-AOUT(J1) and the input of the CDB-HDR-MEAS.
4. Power up the CDB-HDR-MEAS board with  $\pm 15V$  and GND.
5. For each channel, connect a cable between the BNC jacks (Left Channel, Right Channel) and Balanced port on Analog Inputs 1 and 2 on the APx.



**Figure 49 Dynamic Range Setup for CS43198**

6. Configure APx and run Dynamic Range Measurement test as described in section 6.2.2.

## 6.2.4 Measuring THD+N for the CS43198

To measure THD+N in WISCE click File->Load and select XTAL\_In\_ASP\_Slave\_PCM\_Playback\_48K\_1v7.txt file from {WISCE\_INSTALL\_FOLDER}/profiles/CS43198 to configure CS43198 for audio playback in Slave Mode.

### 6.2.4.1 Measuring THD+N on CSP Device

The following steps show the procedure to measure THD+N.

1. Place a jumper connecting the 600- $\Omega$  load on J15.
2. Place a jumper connecting the 600- $\Omega$  load on J4.
3. Connect a headphone-RCA or headphone-BNC cable between CSP-AOUT(J1) and the Balanced port on Analog inputs 1 and 2 on the APx.

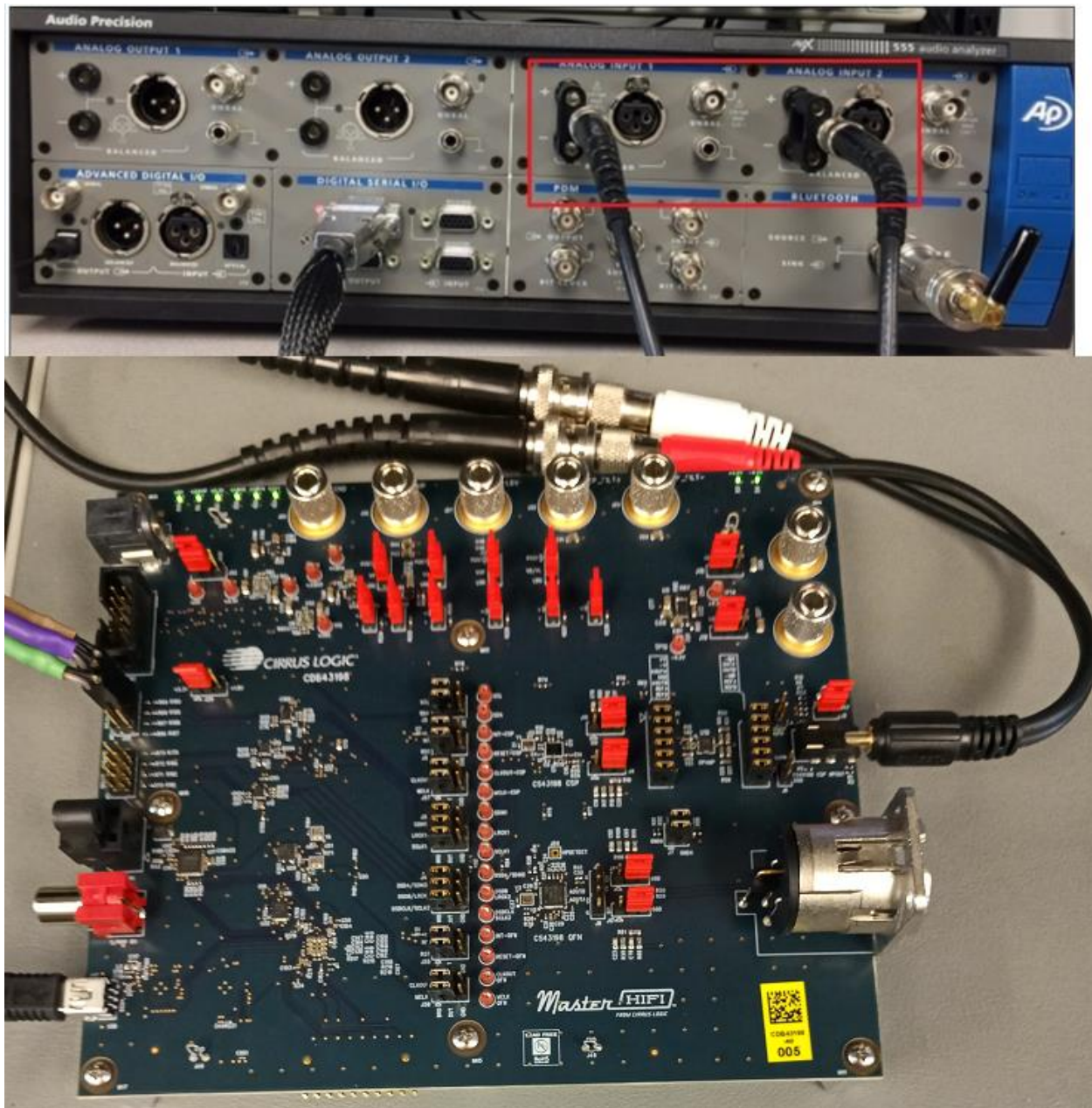


Figure 50 THD+N Measurement for CS43198 CSP

4. Configure APx and run THD+N Measurement test as described in section 6.2.2.



### 6.2.4.2 Measuring THD+N on QFN Device

The following steps show the procedure to measure THD+N.

1. Place a jumper connecting the 600- $\Omega$  load on J17.
2. Place a jumper connecting the 600- $\Omega$  load on J31.
3. Connect a XLR cable between QFN-OUT(J60) and the Balanced XLR port on Analog input 1 on the APx.

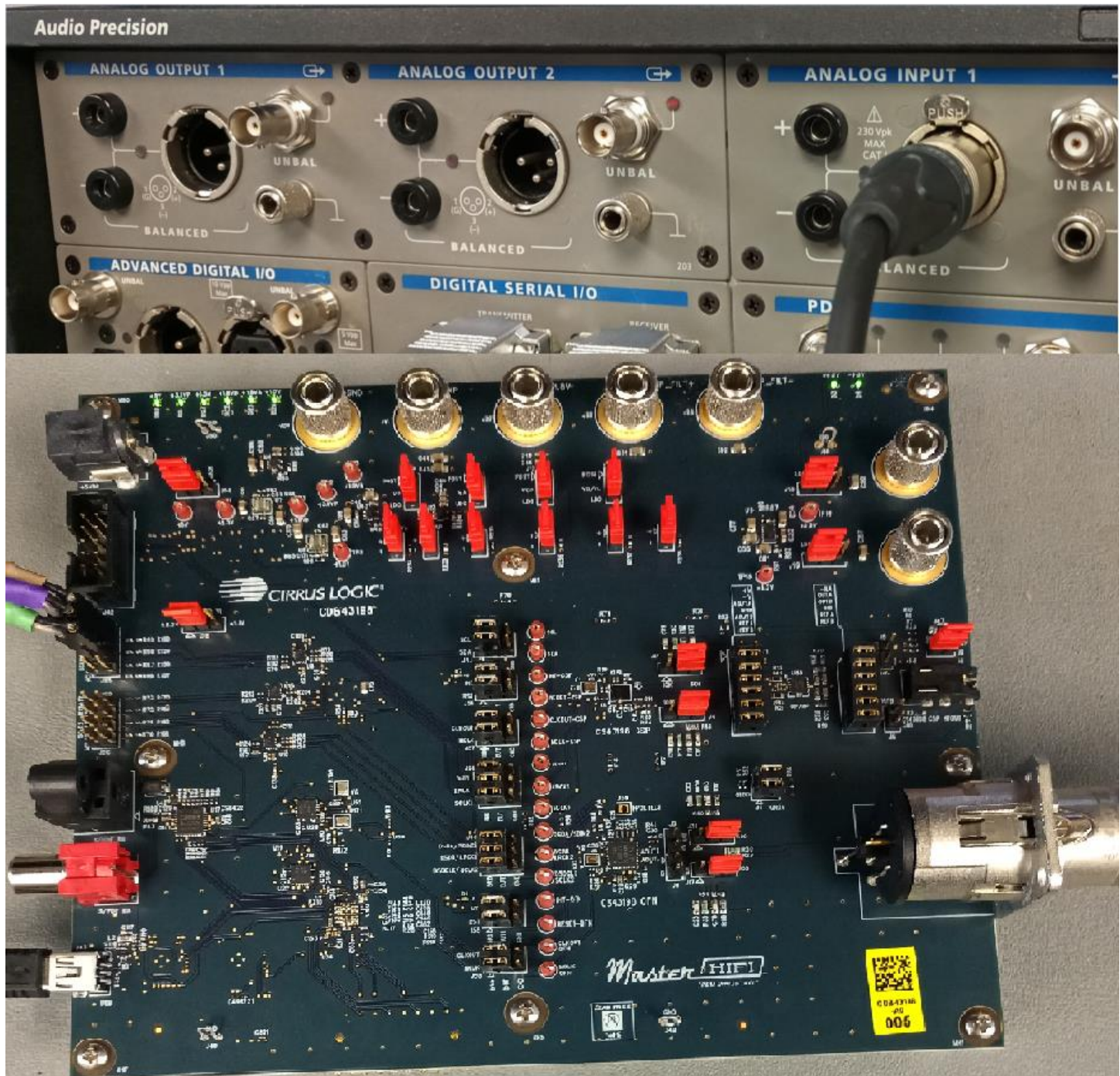


Figure 51 THD+N Measurement for CS43198 QFN

4. Configure APx and run THD+N Measurement test as described in section 6.2.2.

## 6.3 Measured Results

This section shows some measured dynamic range and THD+N results from the CDB43198K kit.

### 6.3.1 Test Waveforms

All test waveforms were generated using the APx Waveform Generator Utility that can be found on the Audio Precision website.

**Table 13 Test Waveforms**

| Test Type | Waveform Name          | Sample Rates | Resolution | Channels |
|-----------|------------------------|--------------|------------|----------|
| THD+N     | Reference Level (0 dB) | 44.1 kHz     | 24 bit     | 2        |
| DNR       | Dynamic Range (1 kHz)  | 44.1 kHz     | 24 bit     | 2        |

### 6.3.2 THD+N Results

The table below lists measured THD+N results using the test waveforms under varying load and full-scale voltage conditions.

**Table 14 Measured THD+N Results**

| Output Load ( $R_L$ ) | Full Scale Voltage (VRMS) | Channel | Datasheet Spec (Typical) | Measured Result <sup>1</sup> |
|-----------------------|---------------------------|---------|--------------------------|------------------------------|
| 10k                   | 1.7                       | A       | -115 dB                  | -113.9 dB                    |
|                       |                           | B       |                          | -113.6 dB                    |
|                       |                           | XLR     |                          | -114.4 dB                    |
| 600                   | 1.7                       | A       | -115 dB                  | -113.4 dB                    |
|                       |                           | B       |                          | -113.7 dB                    |
|                       |                           | XLR     |                          | -114.9 dB                    |

Notes:

1. Refer to CS43198 data sheet for test conditions

### 6.3.3 Dynamic Range (DNR) Results

The table below lists measured DNR results using the test waveforms under varying load and full-scale voltage conditions.

**Table 15 Measured DNR Results**

| Output Load ( $R_L$ ) | Full Scale Voltage (VRMS) | Channel | Datasheet Spec (Typical) | Measured Result <sup>1</sup> |
|-----------------------|---------------------------|---------|--------------------------|------------------------------|
| 600                   | 1.7                       | A       | 130 dB                   | 129.0 dB <sup>2</sup>        |
|                       |                           | B       |                          | 129.1 dB <sup>2</sup>        |
|                       |                           | XLR     |                          | 131.5 dB                     |

Note:

1. Refer to CS43198 data sheet for test conditions
2. Tested with CDB-HDR-MEAS Board

## 7 Revision History

| Revision       | Changes                         |
|----------------|---------------------------------|
| DB1<br>AUG '18 | • Initial release               |
| DB2<br>SEP '18 | • Updated kit name to CDB43198K |



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