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High-Efficiency AC-DC Switch-Mode Power Supply Using Full-Bridge Converter Circuits

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Abstract

This paper presents a high-efficiency AC-DC switch-mode power supply (SMPS) using the full-bridge converter circuits. The proposed converter utilizes three full-bridge converter circuits: two full-bridge diode converter circuits and one full-bridge MOSFET converter circuit. The two full-bridge converters are utilized at the primary AC input and the secondary DC output, respectively, and the full-bridge MOSFET converter is used to convert a DC voltage to a high-frequency AC voltage that is converted to another DC voltage with the transformer and the secondary full-bridge diode converter, which is simply referred to as the full-bridge DC-DC converter. However the conventional full-bridge converter has a limit in its operating duty ratio in normal operation, because it results in more conduction loss in light load operation. Therefore, the proposed converter resolves the drawbacks of the conventional full-bridge converter using a modified full-bridge circuit with a DC blocking capacitor in the primary. Thus, the proposed converter has improved total efficiency and performance. The operation principle of the proposed converter is described in detail, and a design example of a prototype is shown. The good performance of the proposed converter is demonstrated through experimental results of the implemented prototype based on the design example.

Keywords: *AC-DC switch-mode power supply, Full-bridge diode/MOSFET converter*

1. Introduction

Recently, many high-efficiency and high-power-density AC-DC switch-mode power supplies (SMPS's) have been proposed for the power control of many electrical/electronic devices in industry or home appliances [1-13]. Among these SMPSs, AC-DC SMPSs using zero-voltage-switching (ZVS) DC-DC full-bridge converter circuits [1-9] are popular topologies for medium/high-power applications, since they combine the benefits of the ZVS quasi-resonant converters (QRC) and pulse-width modulation (PWM) techniques, while avoiding their major drawbacks.

The primary switches in the ZVS DC-DC full-bridge converter are zero-voltage switched and subjected to a relatively low current stress. As a result, switching losses are significantly reduced without the penalty of a significant increase in conduction loss. Further, because the converter operates with a fixed frequency, the design optimization of the circuit can be attained easily. However, it has a drawback of conduction loss, which becomes serious when the input current is high and the input voltage has wide variation [2-4].

A high-efficiency AC-DC SMPS using a full-bridge converter circuits is proposed. The proposed converter utilizes three full-bridge converter circuits, including two full-bridge diode converter circuits and one full-bridge MOSFET converter circuit. The two full-bridge

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converters are utilized for the rectification at the primary AC input and the secondary DC output, respectively, and the full-bridge MOSFET converter is used to convert a DC voltage to a high-frequency AC voltage. The input DC voltage of the full-bridge MOFET converter or the output of the full-bridge diode converter at the AC input is converted to another output DC voltage using the full-bridge MOSFET converter, the transformer, and the secondary full-bridge diode converter, which are simply referred to as the full-bridge DC-DC converter. The proposed converter overcomes the drawbacks of the conventional full-bridge converter by using a modified full-bridge circuit and inserting a DC blocking capacitor in the primary. Thus, the proposed SMPS has improved total efficiency.

2. The Proposed SMPS

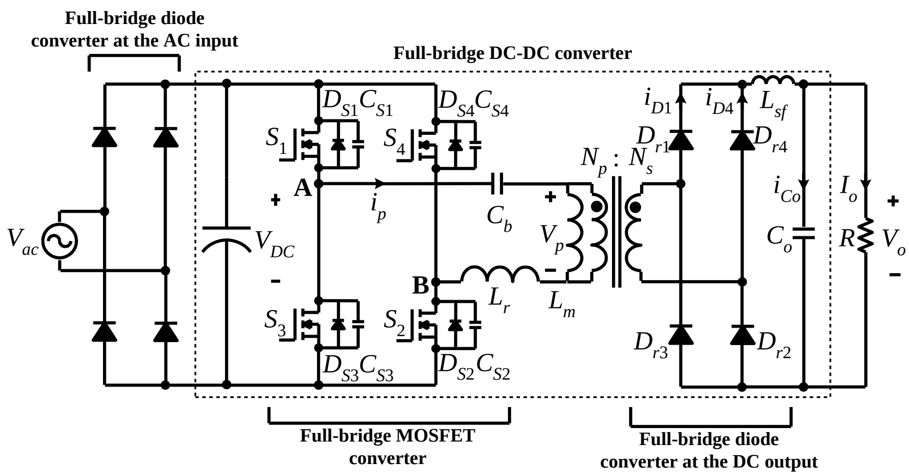


Figure 1. Circuit Diagram of the Proposed SMPS

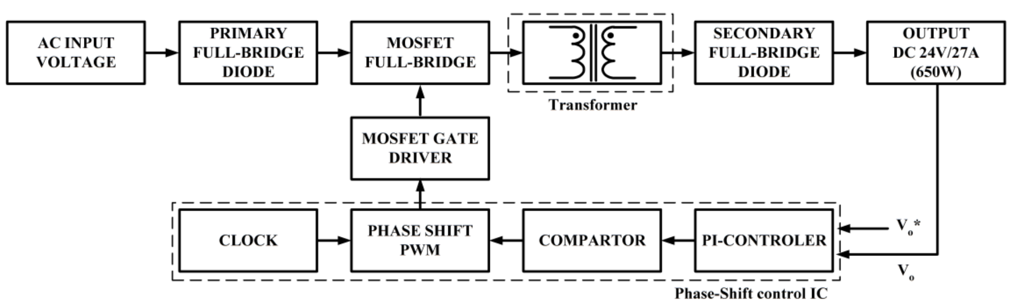


Figure 2. Block Diagram of the Operation Principle of the Proposed Converter

Figure 1 shows the circuit diagram of the proposed SMPS using three full-bridge converter circuits. The core of the proposed SMPS is the full-bridge DC-DC converter after the full-bridge diode converter at the AC input. Therefore, the operation explanation of the full-bridge diode converter at the AC input is omitted, and only the full-bridge DC-DC converter after the input converter is explained. The proposed full-bridge DC-DC converter operates with ZVS at a fixed switching frequency and a series LC resonant circuit. The proposed converter overcomes the drawbacks of the conventional converter and improves the performance by inserting a blocking capacitor in the primary. Thus, the total efficiency of the proposed converter can be improved as its freewheeling interval is reduced.

Figure 2 shows a block diagram of the operation principle of the proposed converter. If the AC voltage gives power to the input stage, the phase-shift control IC operates and generates a PWM signal. The PWM signals drive the switches S_1-S_4, and then the electric power is transferred from the primary to the secondary through the transformer. The output voltage is controlled and kept constant using voltage sensing by the photo-coupler and a phase-shift control IC that controls the output voltage by proportional-integral (PI) control.

3. The Mode Analysis of the Proposed Converter

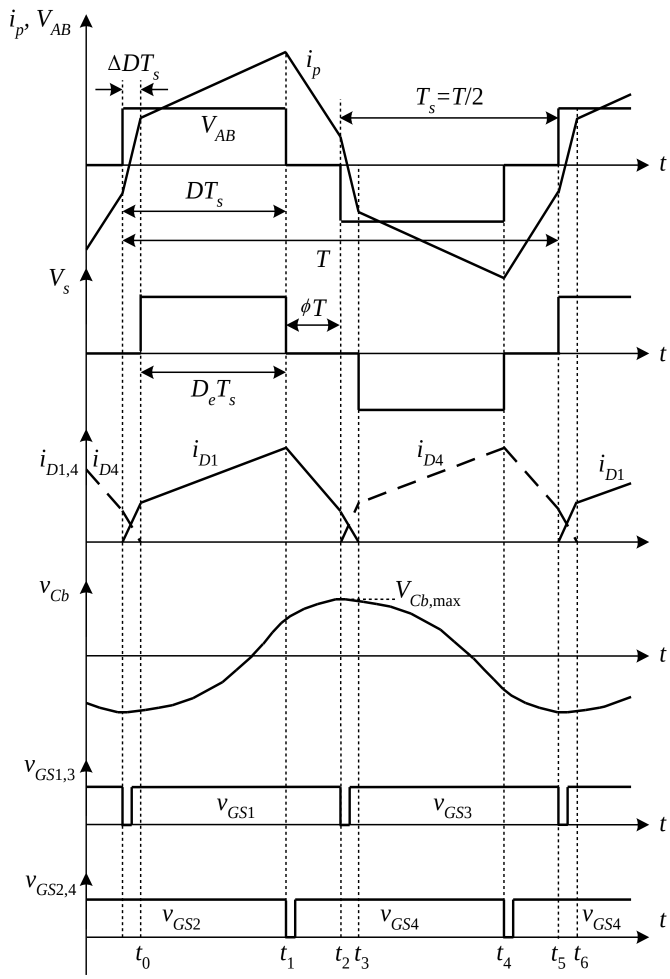


Figure 3. The Theoretical Waveforms of the Main Parts of the Proposed Converter

Figure 3 shows the theoretical waveforms of the main parts of the proposed converter, and figure 4 shows the equivalent circuits of each mode. The modes are determined by the conducting paths and the voltage states of each switching device. For easy mode analysis, it is assumed that the following appropriate conditions:

- The transformer has the magnetizing inductance L_m and a leakage inductance L_r that can be ignored, because it is very small compared with L_m. The turn ratio of the transformer is n (=N_s/N_p).

- Each switch is an ideal component except for its output capacitor and internal diode.
- The output voltage V_o is constant.

Mode 1 (t_0-t_1): Mode 1, which is the powering interval, starts at time t=t_0. The power is transferred from the primary to the secondary through the switch S_1 and S_2 that are turned on as ZVS. At this time, the secondary diode D_{r1} and D_{r2} are turned on, and the diode D_{r3} and D_{r4} are turned off. The output voltage $V_o$is reflected to the primary and the primary current i_p charges the blocking capacitor C_b. Thus, the blocking capacitor voltage v_{Cb} increases nonlinearly. The average voltage of $v_{Cb}$is negative during this mode. As a result, the bridge voltage V_{AB} is increased. The primary current i_p and the blocking capacitor voltage v_{Cb} are given as follows:

$$i_p(t) = \frac{V_{DC}-V_o/n-v_{Cb}}{L_r}(t-t_0)+i_p(t_0) \tag{1}$$

$$v_{Cb}(t) = \frac{1}{C_b}\int i_p\,(t)dt \tag{2}$$

This mode ends when the switch S_2 is turned off at time t=t_1.

Mode 2 (t_1-t_2): Mode 2, which is the freewheeling interval, starts at time t=t_1. When the switch S_2 turns off, the parasitic diode D_{S4} of switch S_4 turns on. The power transferred from the primary to the secondary flows through the secondary diode D_{r1} and D_{r2}, and then the parasitic capacitor C_{S2} of the switch S_2 is charged. The energy of the blocking capacitor C_b and the resonant inductance L_r discharge the parasitic diode C_{S4} of the switch S_4. So, the switch S_4 turns on with ZVS. In this mode, the slope of the primary current i_p decreases more quickly than the conventional converter without the blocking capacitor C_b, and then the circulation energy by the freewheeling current decreases quickly as well. The primary current i_p is given as follows:

$$i_p(t) = -\frac{V_o/n+v_{Cb}}{L_r}(t-t_1)+i_p(t_1) \tag{3}$$

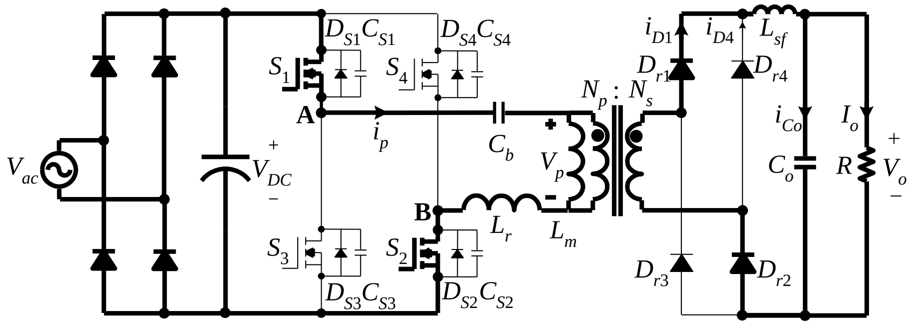
When the switch S_1 turns off at time t=t_2, this mode ends.

Mode 3 (t_2-t_3): Mode 3, which is the regeneration interval, starts at time t=t_2. The parasitic diode D_{S3} turns on, and then the parasitic capacitor C_{S3} discharges and the primary current i_p flows reversely toward the power source. The voltage across of the resonant inductance L_r becomes V_{DC}+v_{Cb}, and the primary current i_p decreases more quickly than the primary current i_p of mode 2. The parasitic diode D_{S4} and capacitor C_{S4} maintain a state like that of mode 2. Because the secondary diode currents i_{D1} and i_{D4} are rectified, the output current of the secondary full-bridge diode flows in the same direction. At this time, all the secondary diodes turn on simultaneously. In this mode, the primary current i_p and the blocking capacitor voltage v_{Cb} are given as follows:

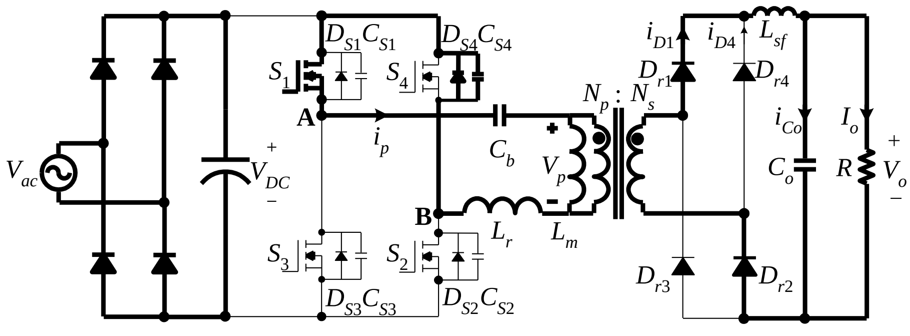
$$i_p(t) = -\frac{V_{DC}+v_{Cb}}{L_r}(t-t_2)+i_p(t_2) \tag{4}$$

$$v_{Cb}(t) \cong V_{Cb,\max} \tag{5}$$

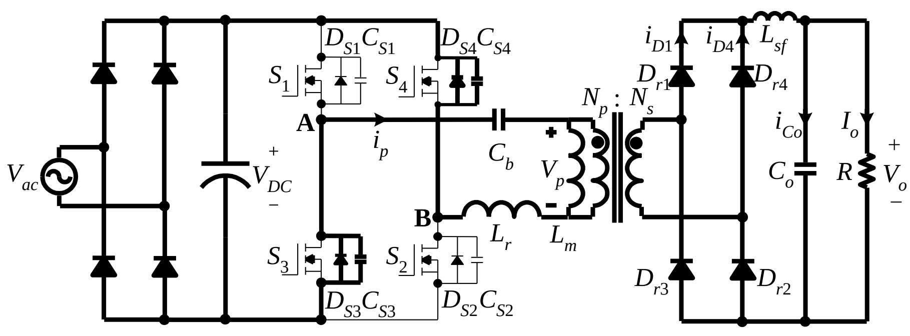
This mode ends when the parasitic capacitors C_{S3} and C_{S4} finish discharging and the parasitic diodes D_{S3} and D_{S4} are turned on.



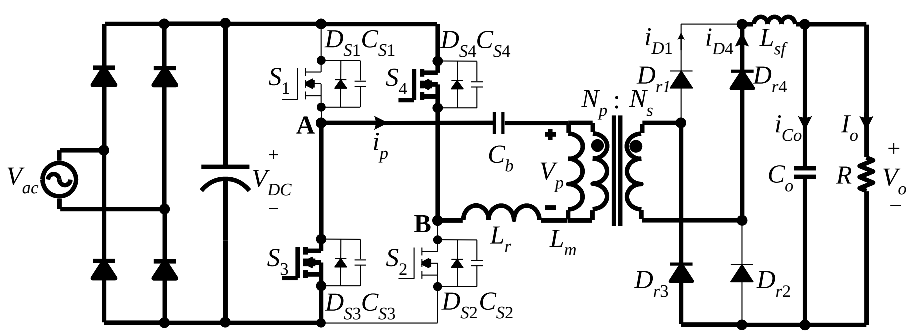
(a) Mode 1 (t_0-t_1)



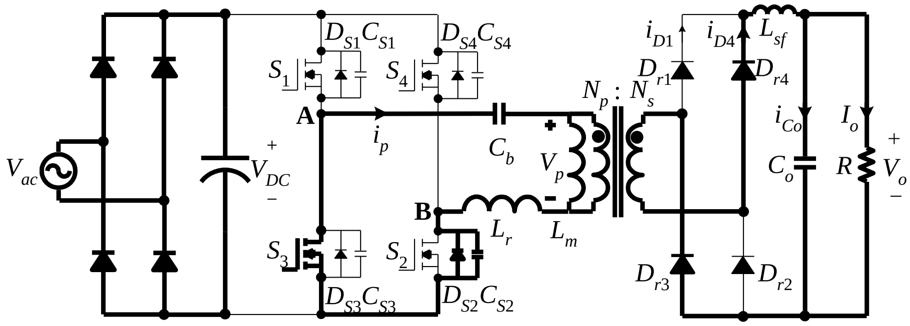
(b) Mode 2 (t_1-t_2)



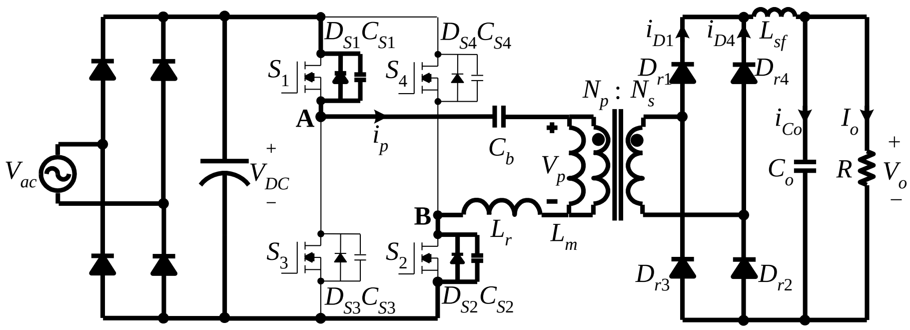
(c) Mode 3 (t_2-t_3)



(d) Mode 4 (t_3-t_4)



(e) Mode 5 (t_4-t_5)



(f) Mode 6 (t_5- t_6)

Figure 4. The Equivalent Circuits of each Mode of the Proposed Converter

Mode 4 (t_3-t_4): Mode 4 starts at time t=t_3. This mode is a powering mode like in mode 1. The power is transferred from the primary to the secondary through the switches S_3 and S_4that are turned on.At this time, the primary current $i_p$charges the blocking capacitor C_b, and because the primary current $i_p$flows reversely, the blocking capacitor voltage v_{Cb}increases nonlinearly toward the negative direction. The secondary diodes D_{r1} and $D_{r2}$are turned off. In this mode, the primary current i_p and the blocking capacitor voltage v_{Cb} are given as follows:

$$i_p(t) = -\frac{V_{DC}-V_o/n-v_{Cb}}{L_r}(t-t_3)+i_p(t_3) \tag{6}$$

$$v_{Cb}(t) = \frac{1}{C_b}\int i_p\,(t)dt \tag{7}$$

This mode ends when the switch S_2 is turned off at time t=t_3.

Mode 5 (t_4-t_5): Mode 5 starts at time t=t_4. This mode becomes the freewheeling state when the switch S_4 turns off, the parasitic capacitor $C_{S4}$is charged, and diode $D_{S2}$is turned on. The operations of the blocking capacitor C_b, the resonant inductanceL_r, and the secondary diodes are the same as those in mode 2. The primary current i_p is given as follows:

$$i_p(t) = \frac{V_o/n+v_{Cb}}{L_r}(t-t_4)+i_p(t_4) \tag{8}$$

When the switch S_3turns off at time t=t_5, this mode ends.

Mode 6 (t_5-t_6): Mode 6 starts at time t=t_5. The parasitic capacitor $C_{S3}$is charged when the switch S_3 turns off. Then, the rest of the operation is the same as in mode 3. In this mode, the primary current i_p and the blocking capacitor voltage v_{Cb} are given as follows:

$$i_p(t) = \frac{V_{DC}+v_{Cb}}{L_r}(t - t_5) + i_p(t_5) \tag{9}$$

$$v_{Cb}(t) \cong -V_{Cb,\max} \tag{10}$$

This mode ends when the parasitic capacitors C_{S1} and C_{S2} finish discharging and the parasitic diodesD_{S1} and $D_{S2}$are turned on.

4. Design Example

In order to show the performance of the proposed converter, the prototype converter is designed with the followingdesign specifications.

Table 1. The Design Specifications of a prototype Converter

Input AC voltage(V_{DC})	380V
Output DC voltage(V_o)	24V
Maximum power($P_{o,\max}$)	650W
Switching frequency(f_s)	100kHz
Duty ratio at phase shift(D_e)	0.5

Table 1 shows the design specifications of a prototype converter. From the normal operation of the conventional DC-DC full-bridge converter, the relationship of the output voltage V_o to the input voltage $V_{DC}$is given as follows:

$$V_o = nD_eV_{DC} \tag{11}$$

$$n = \frac{V_o}{V_{DC}D_e} = \frac{24}{380\times 0.5} = 0.126 \tag{12}$$

where$n$(=N_s/N_p) is the turn ratio, andD_e is the effective duty ratio as shown in figure 2.

The primary current$i_p$flows symmetrically with positive or negative direction during one switching period. Therefore, the AC average of the primary current $i_p$during the switching period is the same as half of the output current reflected to the primary. Therefore, the ripple voltage Δv_{Cb} of the blocking capacitor is given as follows:

$$\Delta v_{Cb} = \frac{nI_o}{2}\cdot\frac{1}{C_b}\cdot\frac{T}{2} = \frac{nI_oT}{4C_b} \tag{13}$$

So, the peakvoltage $V_{Cb,pk}$ of the blocking capacitor voltagev_{Cb} is given as follows:

$$V_{Cb,pk} = \frac{nI_oT}{8C_b} \tag{14}$$

From equation (14), a smaller blocking capacitance$C_b$results in the peak voltage $V_{Cb,pk}$increasing, which means that the turn ratio n decreases. However, if the peak voltage

$V_{Cb,pk}$ is bigger than $V_{DC} - \frac{V_o}{n}$ in mode 1, contradiction occurs in that the slope of the primary current becomes negative, because the voltage across the resonant inductance L_r becomes negative. Therefore, because the voltage $V_{Cb,pk}$ should be smaller than $V_{DC} - \frac{V_o}{n}$, the range of the blocking capacitance C_b must be satisfied as follows:

$$C_b > \frac{nI_oT}{8\left(V_{DC}-\frac{V_o}{n}\right)} \tag{15}$$

The peak voltage $V_{Cb,pk}$ is set as about 10% (about 22V) of $V_{DC} - \frac{V_o}{n}$ considering the ZVS operations and the conduction loss, and the blocking capacitor C_b ensures normal operation of the proposed converter as well as ZVS operations by satisfaction of the following equation:

$$C_b > \frac{n^2 I_o \emptyset T^2}{8\times\left(nL_r i_p(t_1) - V_o \emptyset T\right)} \tag{16}$$

where ϕT is the time of mode 2 and ϕ is set as 0.1. Also, the resonant inductance L_r can be calculated by considering the following equation of energy E_{Lr} stored in the resonant inductance L_r:

$$E_{L_r} = \frac{1}{2} L_r {i_p}^2 = \frac{1}{2} L_r \left(\frac{V_{DC}-\frac{V_o}{n}-v_{Cb}}{L_r} \cdot \frac{D_e T}{2} \right)^2 \tag{17}$$

where the primary current is the resonant inductance current approximated from equation (1). The energy E_{Lr} must be larger than the energy required to charge/discharge the parasitic capacitors of the switches when the main switches are switched, because, it must be so, each switch can be switched with ZVS.So, the resonant inductance L_r shouldsatisfy the following condition:

$$L_r < \frac{\left(\left(V_{DC}-\frac{V_o}{n}\right)D_e T\right)^2}{8\times 2\times \frac{2}{3} C_S \times V_{DC}^2} \tag{18}$$

where the blocking capacitor voltage v_{Cb} is neglected for design convenience, because the blocking capacitor voltage v_{Cb} fluctuates within a small range compared with the voltage $V_{DC} - \frac{V_o}{n}$. Thus, the main switches of the prototype converter are selected as 630V/47A-class MOSFETs, and their parasitic capacitance C_S is 2200pF.

The sum of the rectified current of the secondary full-bridge diode is given as follows:

$$i_{D1} + i_{D4} = i_{C_o} + I_o \tag{19}$$

The peak-to-peak of the secondary diode current i_{D1} is the same as that of the output capacitor ripple current Δi_{Co} in mode 1.Therefore, the magnetizing inductance L_m can be calculated by determining the ripple current of the output capacitor C_o. Based on the design specifications, the peak-to-peak of the output capacitor ripple current Δi_{Co} is approximated and given from the primary current i_p of mode 1 as follows:

$$\Delta i_{Co} \approx \frac{1}{n^2}\left(\frac{nV_{DC}-V_o}{L_r}-\frac{V_o}{L_m}\right)\frac{D_eT}{2} \tag{20}$$

From equation (20), the magnetizing inductance L_m is given as follows:

$$L_m = V_o\left(\frac{L_r}{nV_{DC}-V_o}-\frac{D_eT}{2\times n^2\times\Delta i_{Co}}\right) \tag{21}$$

In order to guaranteeoperation in continuous conductionmode, theoutput capacitor ripple current Δi_{Co} is set as 1A. Then, the magnetizing inductance L_m is set as 19.5mH.

5. Experimental Results

In order to show the performance of the proposed converter, a prototype converter was implemented and experimented with.

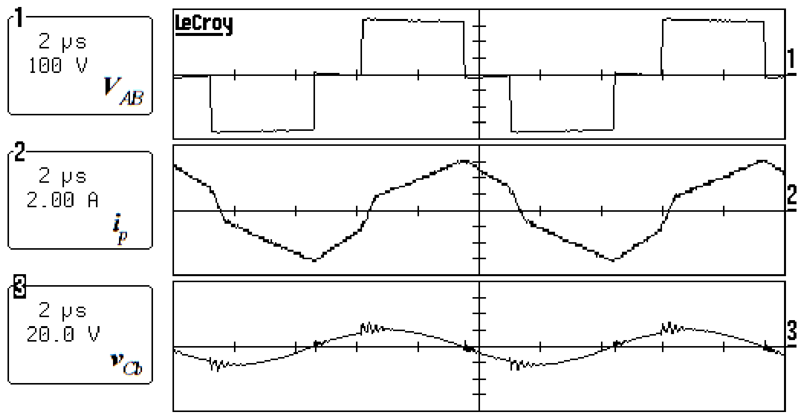


Figure 5. The Experimental Waveforms of the Bridge Voltage V_{AB}, the Primary Current i_p and the Blocking Capacitor Voltage V_{Cb}

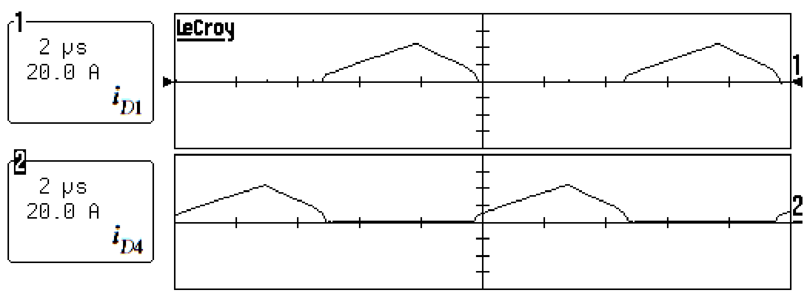


Figure 6. The Experimental Waveforms of the Secondary Diode Currents i_{D1} and i_{D2}

Figure 5 shows the experimental waveforms of the bridge voltage V_{AB}, the primary current i_p, and the blocking capacitor voltage v_{Cb}. These waveforms coincide with the theoretical waveforms of Figure 3. So, it can be known that the power circuit design of the proposed converter in Section 3 is accurate, and the proposed converter operates well and stably.

Figure 6 shows the experimental waveforms of the secondary diode currents i_{D1} and i_{D2}. From these experimental waveforms, it can be known that the commutation between the diode currentsi_{D1} and i_{D4} occurs, and its commutation interval exists as shown in Figure 3.

Figure 7 shows the experimental waveforms of the output voltage V_o and the output current I_o. It can be confirmed that the output power of the prototype converter is 650W (24V/27A)-class. From this, it can be known that the proposed converter controls the output power well and maintains the output voltage and current at constant values.

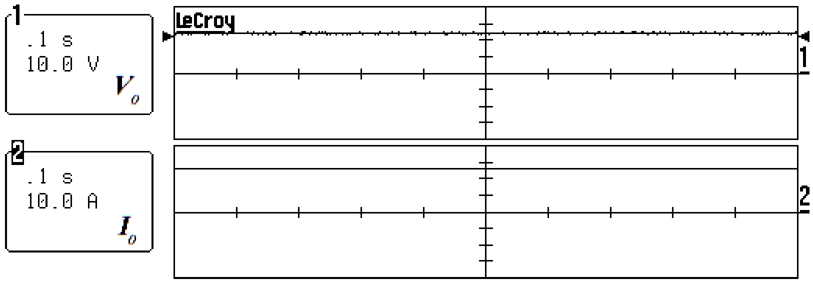


Figure 7. The Experimental Waveforms of the Output Voltage V_o and the output current I_o

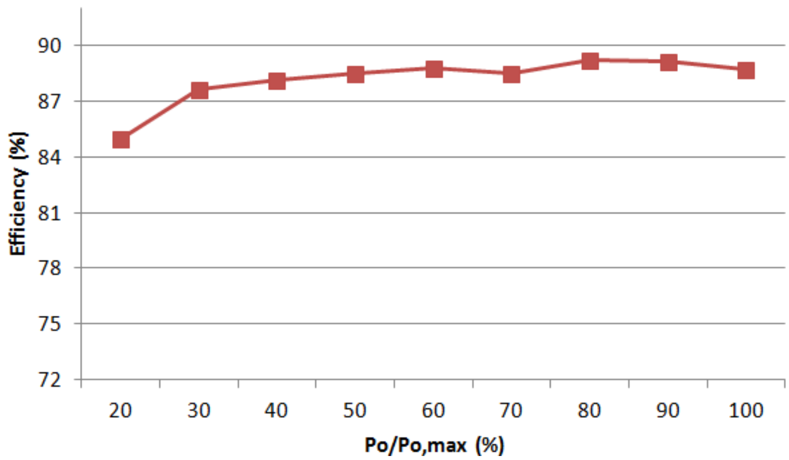


Figure 8. The Efficiency Graph of the Proposed Converter according to the Output Power

Figure 8 shows the efficiency graph of the proposed converter according to the output power. The total efficiency is high roughly around the load condition of the maximum or rating power. This demonstrates the good performance of the proposed converter as a high-efficiency AC-DC SMPS.

6. Conclusion

A high-efficiency AC-DC SMPS using three full-bridge converter circuits has been presented. The three full-bridge converter circuits include two full-bridge diode converter circuits and one full-bridge MOSFET converter circuit. The two full-bridge converters are utilized at the primary AC input and the secondary DC output for the rectification, respectively, and the full-bridge MOSFET converter is used to convert a DC voltage to a high-frequency AC voltage. The input DC voltage or the output of the full-bridge diode converter at the AC input is converted to another output DC voltage using a modified DC-DC full-bridge converter that is composed of a full-bridge converter, a transformer, and a full-bridge diode converter, which is the core of the proposed SMPS. The proposed converter overcomes thedrawbacks of the conventional full-bridge converter by inserting a DC blocking capacitor in the primary of the conventional converter circuit. The proposed converter has good performance as a high-efficiency AC-DC SMPS, which was shown through various experimental results.

Acknowledgements

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