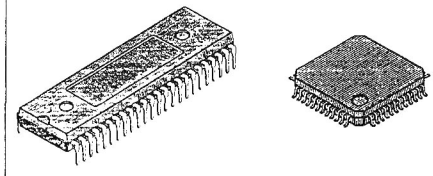
Dolby S-type Noise Reduction System

Description

The CXA1417S/Q is a bipolar IC designed for the Dolby S-type noise reduction system. The device provides all of the functions required for a Dolby S-type noise reduction encoder. The decoder is made by adding an operational amplifier externally.

48pin SDIP (Plastic) 48pin QFP (Plastic)



Features

- Complete S-type encoder in one chip
- Accurate encode characteristics
- Low distortion with poly-silicon resistors
- Identical Dolby level with CXA1332 B-C type IC

Functions

- HLS and LLS summing amplifiers (main path)
- HL/LF/FB side chain and control path
- HL/HF/SB side chain and control path
- HL/HF/FB side chain and control path
- LL/HF/SB side chain and control path
- LL/HF/FB side chain and control path
- Modulation control paths
- Bias and reference circuits

Note) HL (S) : High Level (Stage)
LL (S) : Low Level (Stage)
LF (S) : Low Frequency (Stage)
HF (S) : High Frequency (Stage)
FB : Fixed Band
SB : Sliding Band

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

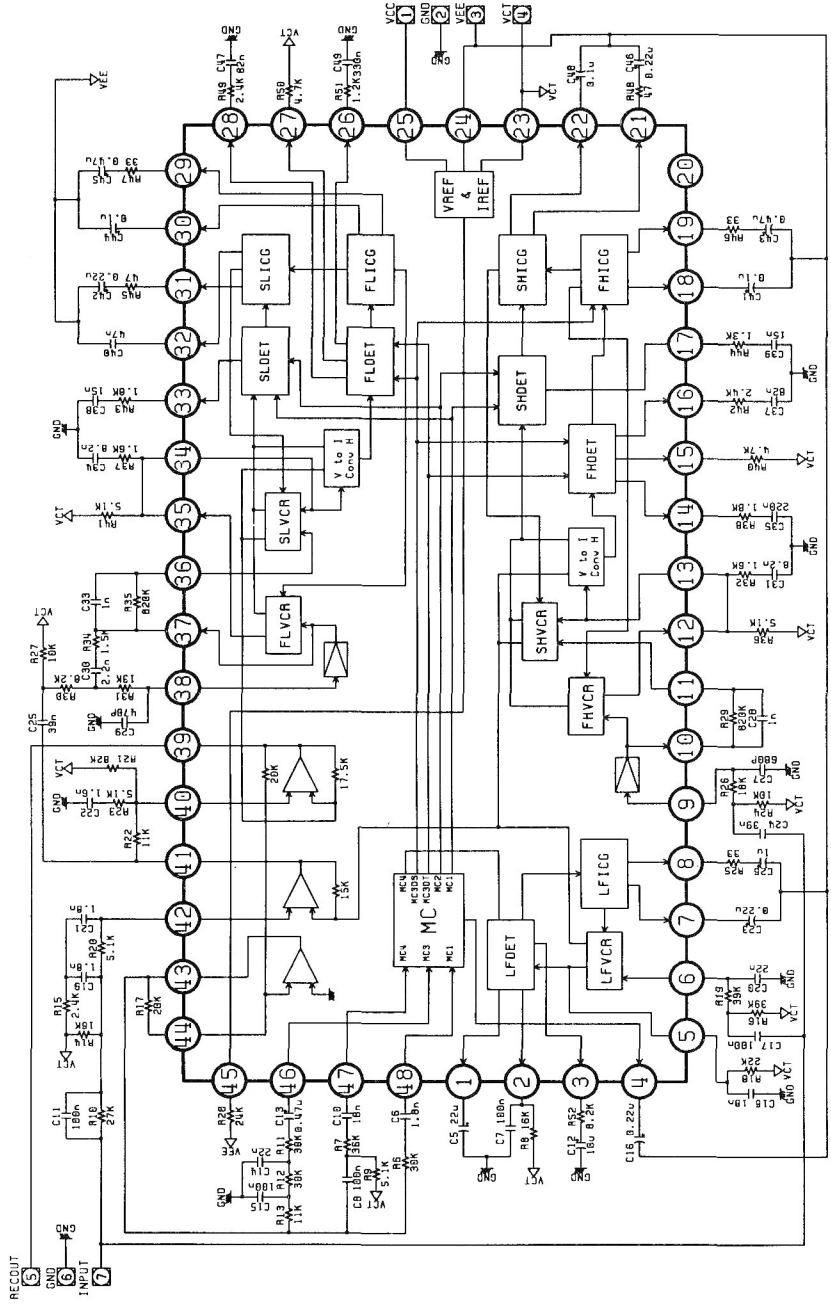
• Supply voltage	V_{CC}~V_{EE}	14	V
• Operating temperature range	T_{opr}	−20 to +75	°C
• Storage temperature range	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D		
SDIP48 (CXA1417S)		2200	mW
QFP48 (CXA1417Q)		600	mW

Operating Condition

Supply voltage	V_{CC}	4.50 to 6.50	V
	V_{EE}	−4.50 to −6.50	V

* The IC is available only to the licensees of Dolby Laboratories Licensing Corporation from whom licensing and application information may be obtained.
* "Dolby" and the double D symbol are trade marks of Dolby Laboratories Licensing Corporation.

Block Diagram, Application Circuit

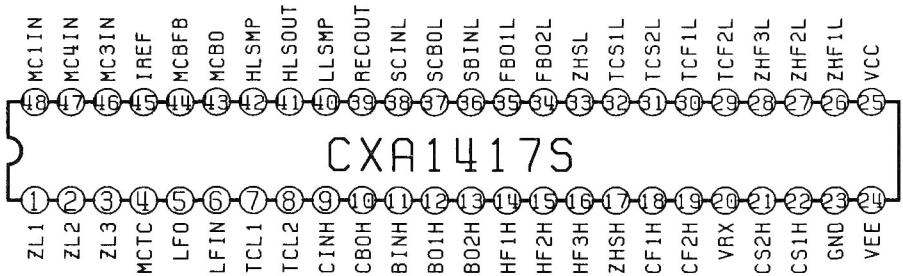


(Pin No.: CXA1417S)

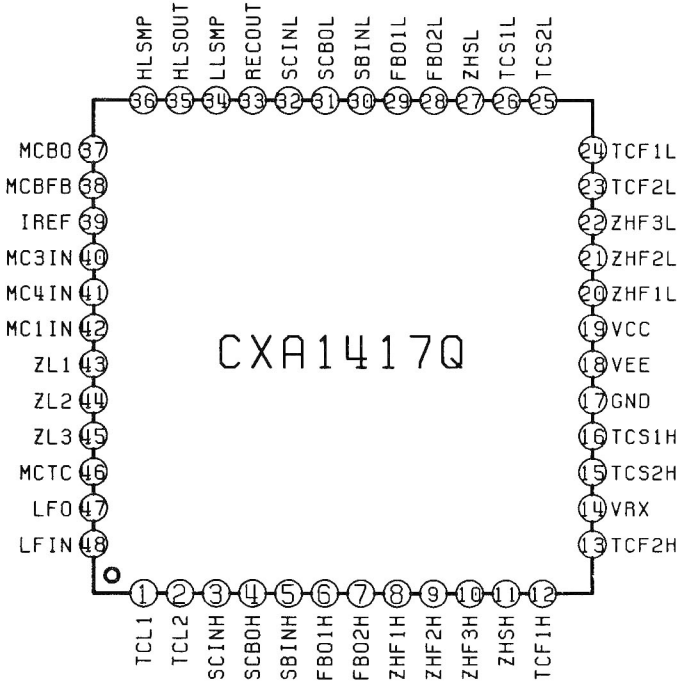
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Pin Configuration

CXA1417S

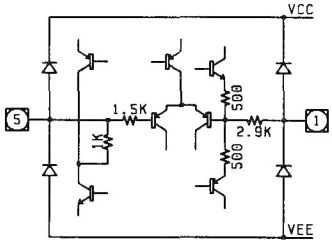
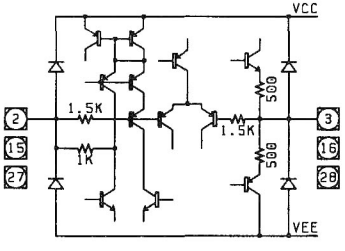
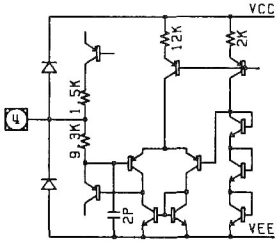
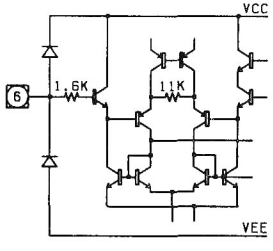


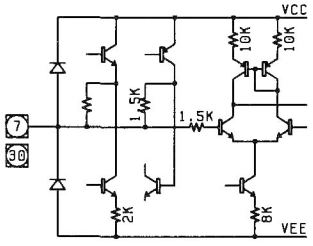
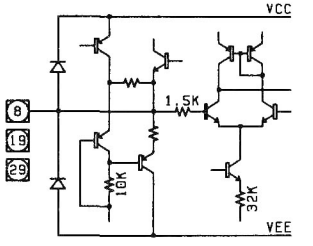
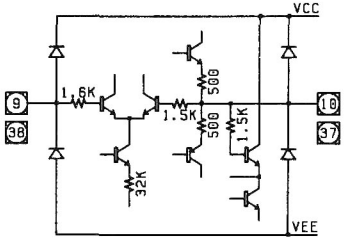
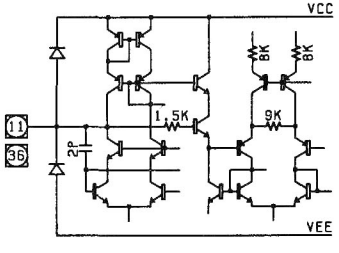
CXA1417Q

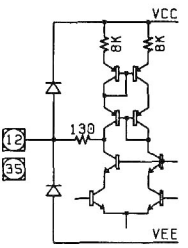
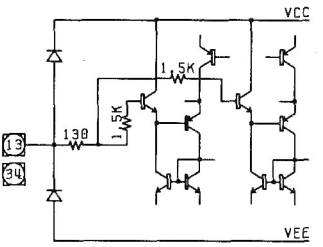
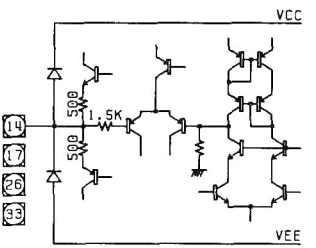
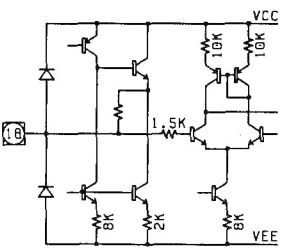


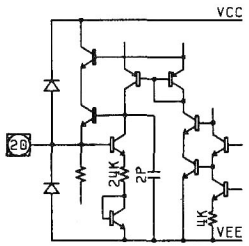
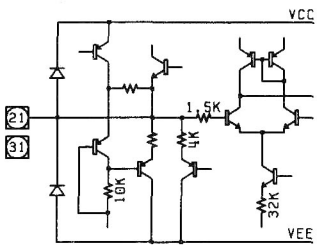
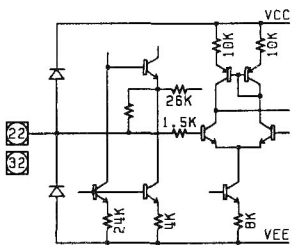
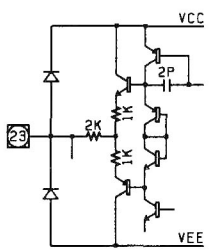
Pin Description and Equivalent Circuit

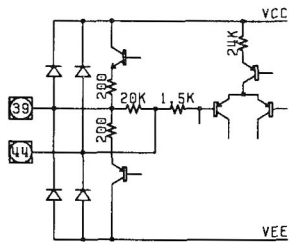
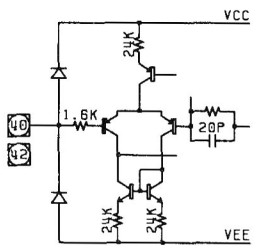
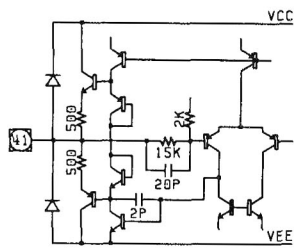
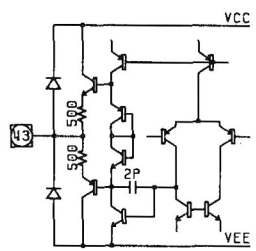
V_{CC}=6.0V, V_{EE}=−6.0V

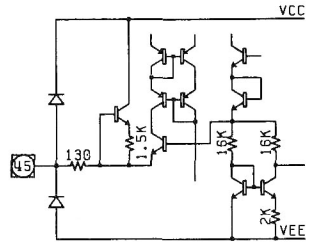
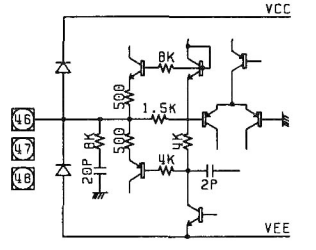
Pin No. SDIP	Pin No. QFP	Symbol	DCV (V)	Equivalent Circuit	Description
1	43	ZL1	0.0		Weighting pin of the HL/LF/FB main band rectifier
5	47	LF0	0.0		Input pin of the HL/LF/FB main band rectifier
2	44	ZL2	0.0		Input pin of the HL/LF/FB pass band rectifier
3	45	ZL3	0.0		Weighting pin of the HL/LF/FB pass band rectifier
15	9	ZHF2H	0.0		Input pin of the HL/HF/FB pass band rectifier
16	10	ZHF3H	0.0		Weighting pin of the HL/HF/FB pass band rectifier
27	21	ZHF2L	0.0		Input pin of the LL/HF/FB pass band rectifier
28	22	ZHF3L	0.0		Weighting pin of the LL/HF/FB pass band rectifier
4	46	MCTC	−3.9		Time constant pin of the MC2
6	48	LFIN	0.0		Input pin of the HL/LF/FB stage

Pin No. SDIP	Pin No. QFP	Symbol	DCV (V)	Equivalent Circuit	Description
7	1	TCL1	−4.6		Primary time constant pin of the HL/LF/FB detector
30	24	TCF1L	−4.6		Primary time constant of the LL/HF/FB detector
8	2	TCL2	−4.6		2ndary time constant pin of the HL/LF/FB detector
19	13	TCF2H	−4.6		2ndary time constant pin of the HL/HF/FB detector
29	23	TCF2L	−4.6		2ndary time constant pin of the LL/HF/FB detector
9	3	SCINH	0.0		Input pin of the HL/HFside chain
10	4	SCBOH	0.0		Output pin of the HL/HF side chain buffer amplifier
37	31	SCBOL	0.0		Output pin of the LL/HF side chain buffer amplifier
38	32	SCINL	0.0		Input pin of the LL/HF side chain
11	5	SBINH	0.0		Input pin of the HL/HF/SB VCR
36	30	SBINL	0.0		Input pin of the LL/HF/SB VCR

Pin No. SDIP	Pin No. QFP	Symbol	DCV (V)	Equivalent Circuit	Description
12	6	FBO1H	0.0		Output pin of the HL/HF/FB VCR
35	29	FBO1L	0.0		Output pin of the LL/HF/FB VCR
13	7	FBO2H	0.0		Input pin of the HL/HF/FB V to I converter
34	28	FBO2L	0.0		Input pin of the LL/HF/FB V to I converter
14	8	ZHF1H	0.0		Weighting pin of the HL/HF/FB main band rectifier
17	11	ZHSH	0.0		Weighting pin of the HL/HF/SB rectifier
26	20	ZHF1L	0.0		Weighting pin of the LL/HF/FB main band rectifier
33	27	ZHSL	0.0		Weighting pin of the LL/HF/SB rectifier
18	12	TCF1H	−4.6		Primary time constant pin of the HL/HF/FB detector

Pin No. SDIP	Pin No. QFP	Symbol	DCV (V)	Equivalent Circuit	Description
20	14	VRX	−3.4		Voltage source pin inversely proportional to shift of the *internal R*
21	15	TCS2H	−4.6		2ndary time constant pin of the HL/HF/SB detector
31	25	TCS2L	−4.6		2ndary time constant pin of the LL/HF/SB detector
22	16	TCS1H	−4.6		Primary time constant pin of the HL/HF/SB detector
32	26	TCS1L	−4.6		Primary time constant pin of the LL/HF/SB detector
23	17	GND	0.0		For split supply: *GND pin* For single supply: voltage source pin of $V_{CC}/2$
24	18	VEE	−6.0		For split supply: V_{EE} pin For single supply: GND pin
25	19	VCC	6.0		V_{CC} pin

Pin No. SDIP	Pin No. QFP	Symbol	DCV (V)	Equivalent Circuit	Description
39	33	RECOUT	0.0		Recording (Encode) output pin
44	38	MCBFB	0.0		MC buffer feedback pin
40	34	LLSMP	0.0		Input pin of the LL stage main path
42	36	HLSMP	0.0		Input pin of the HL stage main path
41	35	HLSOUT	0.0		HL stage output pin
43	37	MCBO	0.0		MC buffer output pin

Pin No. SDIP	Pin No. QFP	Symbol	DCV (V)	Equivalent Circuit	Description
45	39	IREF	−4.8		Reference current input pin
46	40	MC3IN	0.0		MC3 input pin
47	41	MC4IN	0.0		MC4 input pin
48	42	MC1IN	0.0		MC1 input pin

Note)
Pin numbers in the equivalent circuits show the CXA1417S shrink DIP.

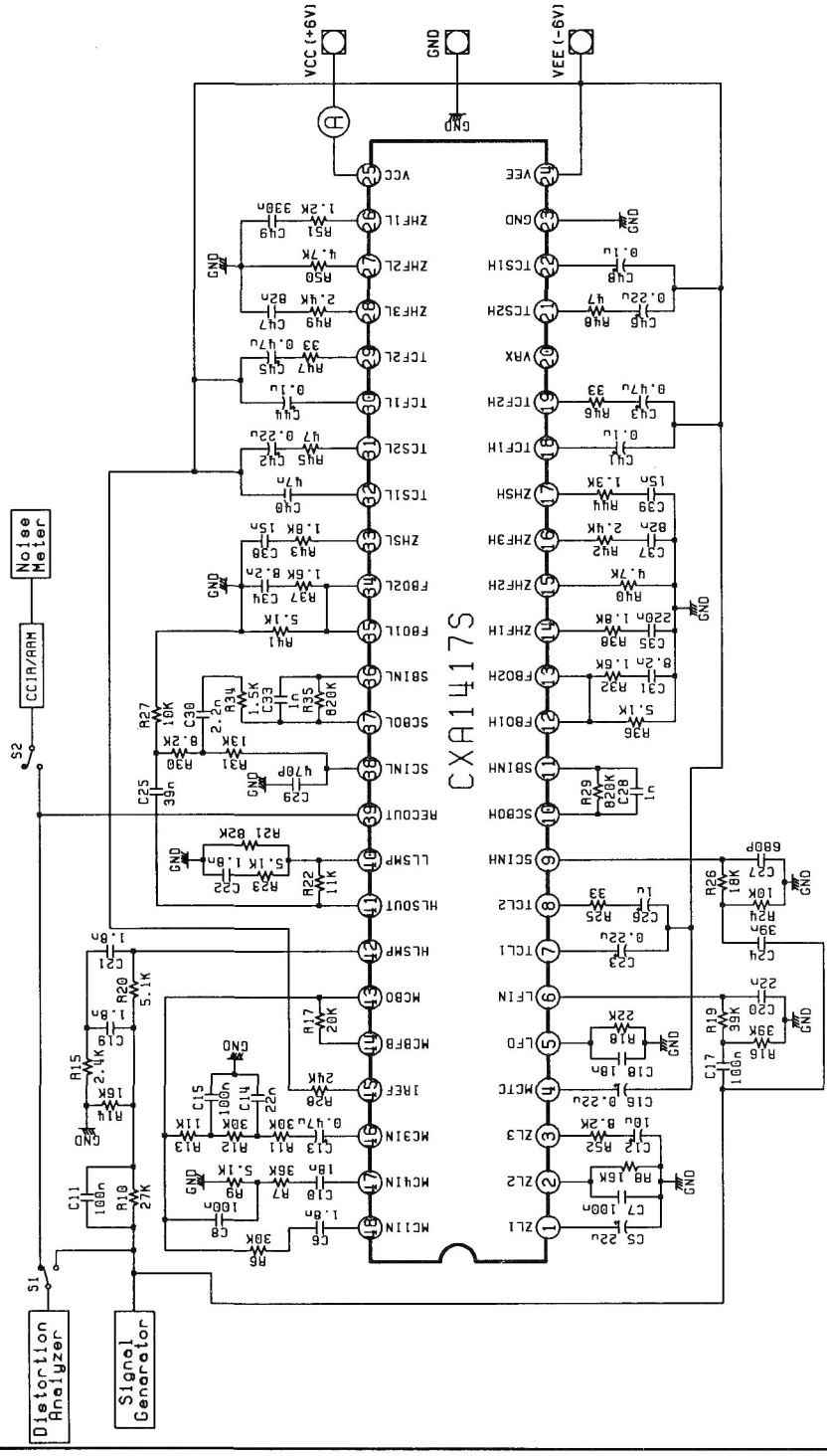
Electrical Characteristics

Ta = 25°C, Dolby Level : −6dB (=388mVrms) at encoder input, V_{CC} = +6V, V_{EE} = −6V

unless otherwise specified

Characteristics	Symbol	Test Condition f(kHz)	Test Condition V_{IN}	Test Condition Other	Min.	Typ.	Max.	Unit
Operating Voltage	V_{OPR}	1	15dB	THD≦1%	±4.5		±6.5	V
Current Consumption	I_{CC}			No signal	8.0	11.0	15.0	mA
Encode Boost								
(1)	EB-1	2	−60		22.0	23.5	25.0	dB
(2)	EB-2	0.05	−40		5.9	7.4	8.9	dB
(3)	EB-3	0.3	−40		15.0	16.5	18.0	dB
(4)	EB-4	12	−40		12.8	14.3	15.8	dB
(5)	EB-5	0.3	−20		6.2	7.7	9.2	dB
(6)	EB-6	2	−20		4.4	5.9	7.4	dB
(7)	EB-7	0.05	0		−3.5	−2.0	−0.5	dB
(8)	EB-8	12	0		−7.3	−5.8	−4.3	dB
Overload Margin	Vomax	1		THD=1%	17.0	19.3	—	dB
Total Harmonic Distortion	THD	1	10		—	0.03	0.15	%
S/N Ratio	SNR			Rg=600Ω CCIR/ARM	62.0	65.0	—	dB

Electrical Characteristics Test Circuit



Notes on application

General

The CXA1417 is an encode IC for the Dolby S type noise reduction system. An external operational amplifier is required to build the decoder. The Dolby level voltage of the device is −6dBm (388mVrms), which is the same as that of the CXA1332 Dolby B/C type IC. Therefore, it is possible to use the CXA1332 to build a switchable B/C/S type processor.

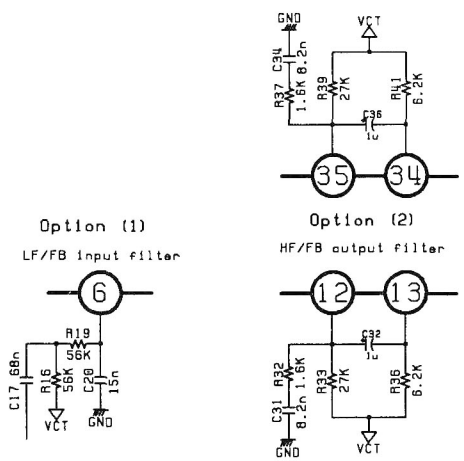
Power Supply

The CXA1417 will operate with either split or single supplies. The supply voltage range is from ±4.5 to ± 6.5 volts and from 9 to 13 volts for split and single supplies respectively. However, the minimum supply voltage is limited by maximum voltage swing of an external operational amplifier. Since general purpose operational amplifiers have approximately ($V_{CC} - V_{EE}$) −2 volts maximum voltage swing, actual minimum supply voltages, which satisfy the 15dB overload margin, are ± 5.0 and 10 volts for split and single supplies respectively. The supply current does not depend on the supply voltage roughly, but does depend on the signal level and frequency. The maximum supply current for the worst case will be approximately 20mA.

Encoder Unit

Fig. 1 shows the schematic of the encoder unit, which is a basic functional block for the following applications. The device is designed so that the gain is unity, so the reference levels of the input (INPUT) and the output (RECOUT) are −6dBm (388mVrms). The circuit has the capability of either split or single supply operation. The VCT terminal has to be connected to the GND terminal under split supply operation. Under single supply operation, the VEE terminal has to be connected to the GND terminal, and the VCT terminal has to be opened. The reference voltage of VCC/2 is generated internally on the VCT terminal.

There are two options regarding the external circuit as follows. Option (1) is to reduce capacitances in the LF/FB input filter. Option (2) is to improve the dynamic offset. The CXA1417 has acceptable dynamic offset performance in either case, but option (2) should be used for the best audio quality.



Recording Processor

Fig. 2 shows the recording processor. The gain is defined as follows

$G_{REC} = 20 \cdot \text{Log}\ (1 + R62/R63)$

The processor in Fig. 2 has a gain of 14dB, therefore the input sensitivity is −20dBm (77.5mVrms). An input sensitivity higher than −25dBm (44mVrms) will generally be unacceptable due to the noise performance, though this is affected by the operational amplifier used and the input circuit. An important parameter for the external operational amplifier is the noise performance for around a 20kΩ input impedance. A bipolar input type is better than a JFET input type for the recording processor.

Playback Processor

Fig. 3 shows the playback processor. The gain is defined as follows

$G_{PB} = 20 \cdot \text{Log}\ (1 + R64/R65)$

The processor in Fig. 3 has a gain of 20dB, so the input sensitivity is −26dBm (39mVrms). Important characteristics of the playback processor are the frequency response and the feedback loop stability, which depend on the gain of the feedback loop and the slew rate of the external operational amplifier. The slew rate has to be higher than $3V/\mu S$. The loop gain can be estimated using the gain bandwidth product BG (Hz) of the operational amplifier and the decode gain A_{PB}. The lower limit of BG/A_{PB} is approximately 500 kHz, and the recommended range is from 1 to 3 MHz.

Switchable Processor

Fig. 4 shows the switchable processor. The gains are the same as in equations (1) and (2). An operational amplifier is required with low noise, average slew rate ($> 3V/\mu S$) and wide bandwidth ($\fallingdotseq 10MHz$) for this gain setting. A bipolar input type with wide bandwidth like the 4560 and the NE5532 is required for the switchable processor.

The processor in Fig. 4 may generate significant switching noise, especially when switch S2 is make-break-make type. When switch S2 is make to make type or has quick switching characteristics, the swichting noise will be acceptable for cassette decks with output muting circuits.

B/C/S type Recording Processor

Fig. 5 shows the recording processor with a multiplex filter and capability to switch to B and C type. The CXA1332 is used as the B/C type processor, and is active in the B, C and NR off modes. It is recommended that the S-type mode be used for recording level calibration. Since the processor in Fig. 5 is designed so that the input level which provides Dolby level for the CXA1417 also provides Dolby level for the CXA1332, calibrations for the B and C type modes are unnecessary. The resistances of R62, R63, R84 and R85 defining the relative gains between the S type and the B/C type processor should be accurate to avoid reference level error.

B/C/S type Playback Processor

Fig. 6 shows the playback processor switchable to the B and C type modes. It is recomended that the S-type mode be used for playback level calibration, and calibrations for the B and C type mode are unnecessary for the same reason as with the B/C/S recording processor. The resistances of R64 and R65 should be accurate since the relative reference level error depends on the ratio.

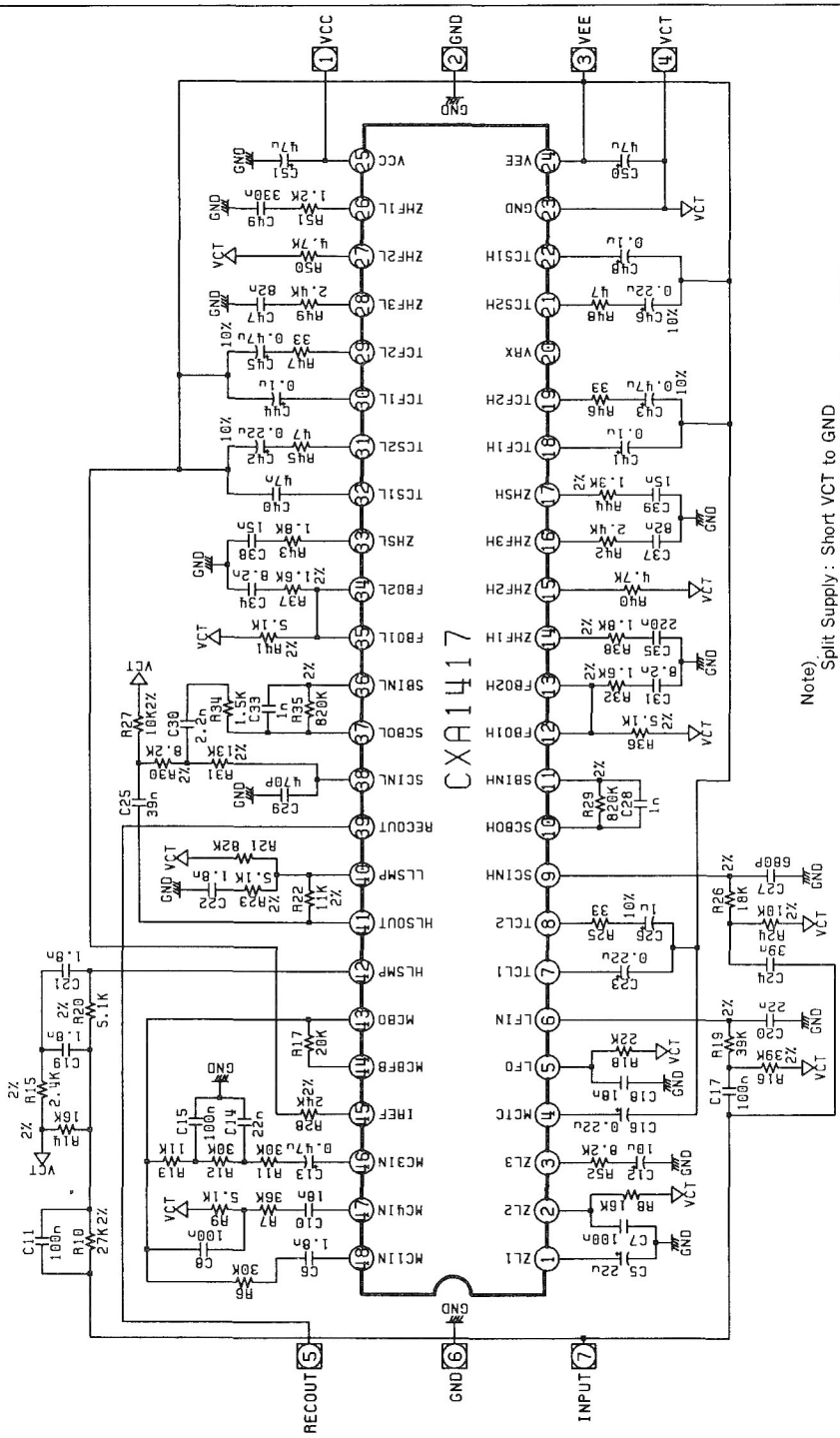


Fig. 1 Schematic of Encoder unit

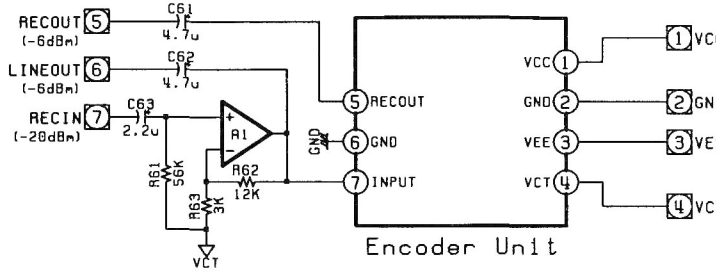


Fig. 2 Recording Processor

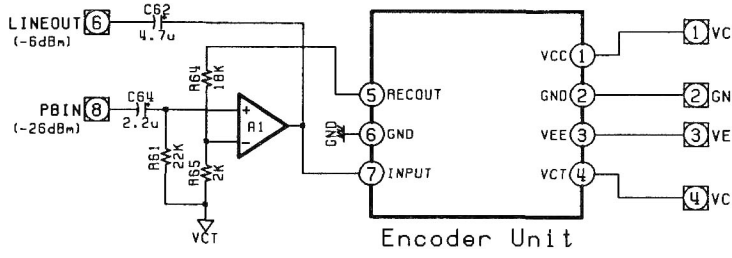


Fig. 3 Playback Processor

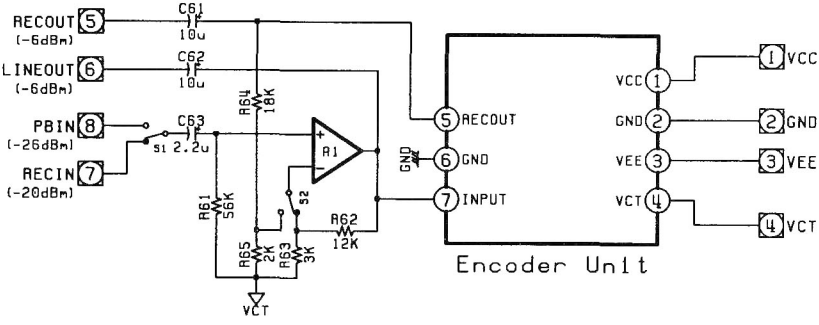


Fig. 4 Switchable Processor

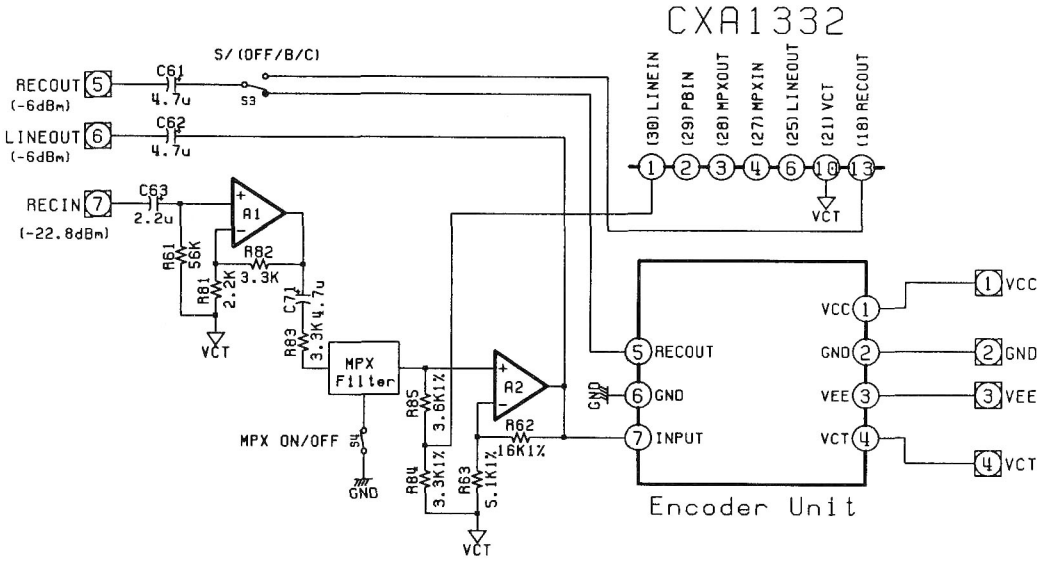


Fig. 5 Recording Processor With B/C type

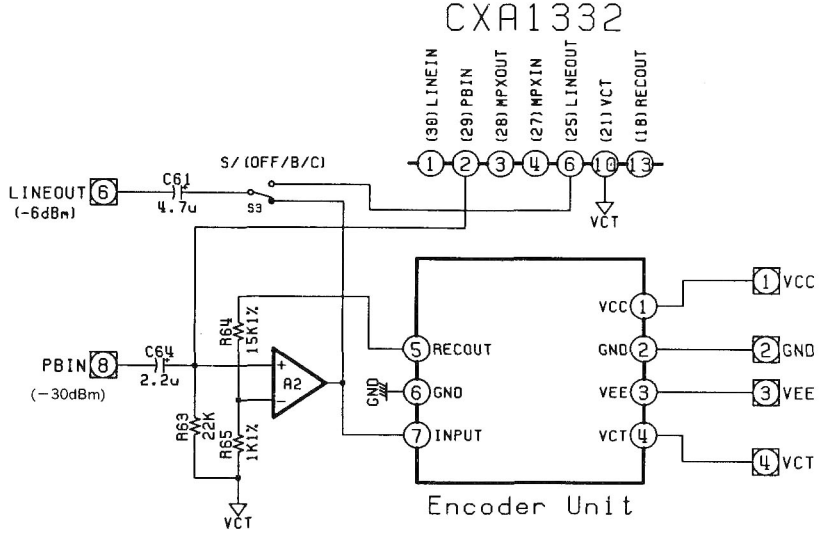
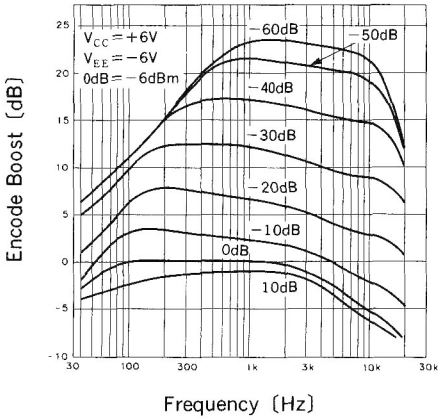


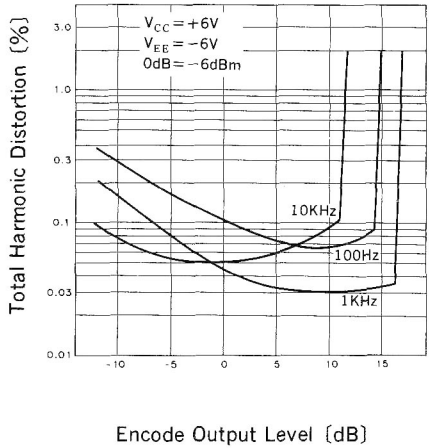
Fig. 6 Playback Processor with B/C type

Notes for Power Supply
Split Supply: Short VCT to GND
Single Supply: Short GND to VEE and open VCT

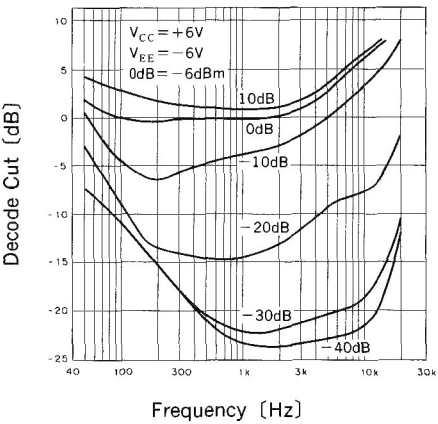
Encode Characteristics



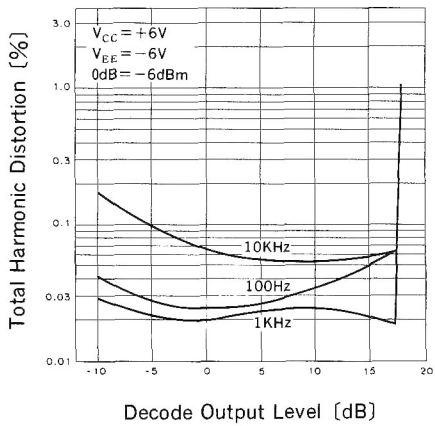
Encode THD Characteristics



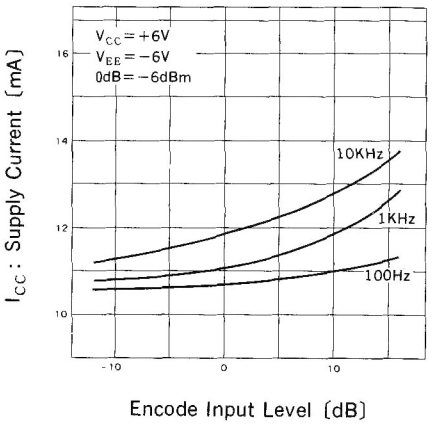
Decode Characteristics



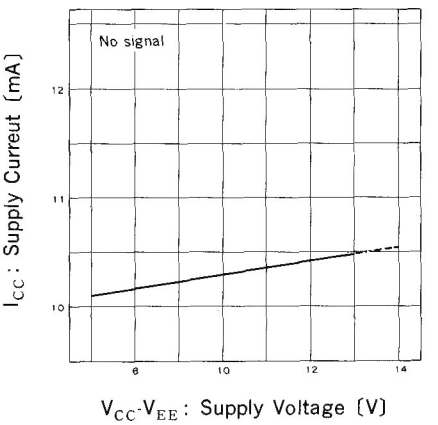
Decode THD Characteristics



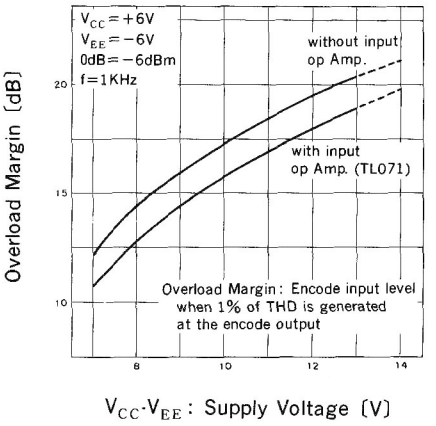
Supply Current vs Input Level



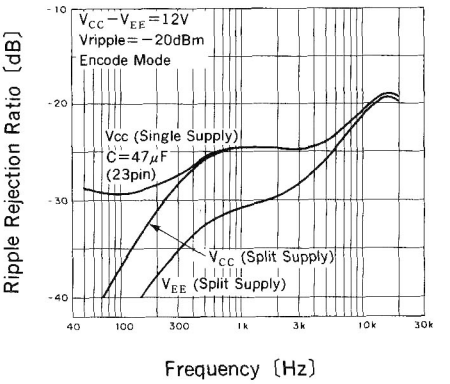
Supply Current vs Supply Voltage



Overload Margin vs Supply Voltage



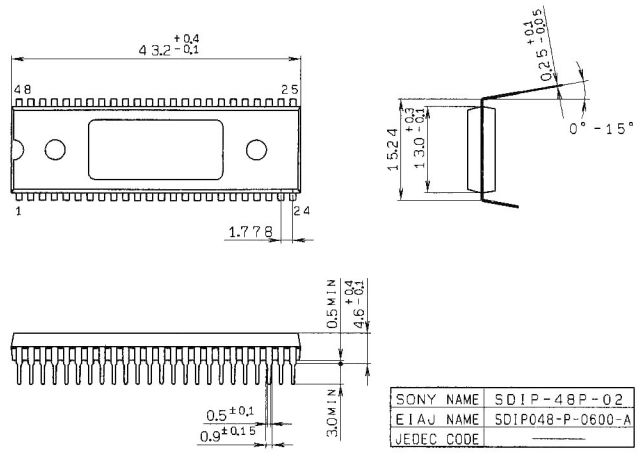
Ripple Rejection Ratio



Package Outline Unit : mm

CXA1417S

48pin SDIP (Plastic) 600mil 5.1g



CXA1417Q

48pin QFP (Plastic) 0.7g