

## Application Note

# DESIGN NOTES FOR A 2-POLE FILTER WITH DIFFERENTIAL INPUT

by Steven Green

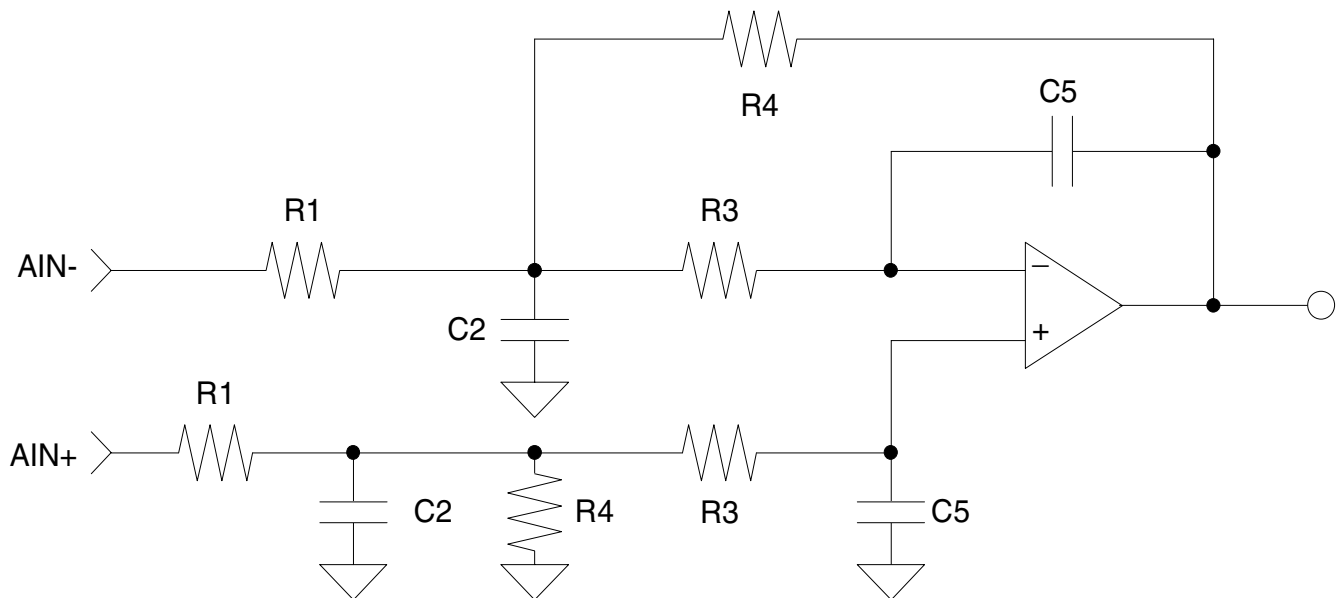
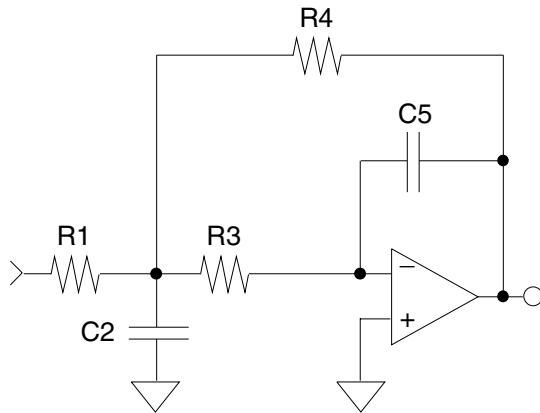


Figure 1. 2-Pole Low-Pass Filter with Differential Input

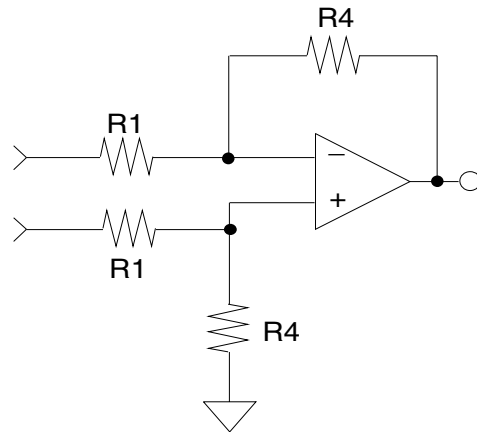
### 1. Introduction

Many of today's Digital-to-Analog Converters (DACs) require a circuit that has a differential input and will remove common-mode errors, reduce the out-of-band noise produced by the delta-sigma modulator and produce a single-ended output. The circuit in Figure 1 includes a differential input and a two-pole analog filter to achieve these design requirements. This application note outlines the design steps required to select component values.

Notice the similarities between Figure 1 and the multiple-feedback low-pass filter shown in Figure 2. The 2-Pole Low-Pass Filter with Differential Input is easily designed using the design equations for the multiple-feedback low-pass filter. Also, notice the similarities between Figure 1 and Figure 3. The differential input function is accomplished by simply duplicating the component values generated in the filter design



**Figure 2. Multiple-Feedback Low-Pass Filter**



**Figure 3. Differential Input Circuit**

## 2. Design Steps

**Step 1:** Determine the required pass band gain,  $H_o$ . The circuit parameters require that the magnitude of  $H_o$  be greater than or equal to one.  $H_o$  is also negative due to the inverting op-amp configuration.

**Step 2:** Determine the minimum input impedance.

**Step 3:** Select the desired filter type, Butterworth, Bessel, etc. and the corner frequency,  $F_c$ , for the final design. The filter response and corner frequency determine the pass band phase and amplitude response. The filter type determines the pole-locations and therefore alpha and beta. Table 1 lists the normalized pole locations for several filter types.

**Table 1: Normalized Pole Locations**

FILTER TYPE	$\alpha$	$\beta$
Butterworth	0.7071	0.7071
Bessel	1.1030	0.6368
0.01 dB Chebyshev	0.6743	0.7075
0.1 dB Chebyshev	0.6104	0.7106

**Step 4:** Select convenient values for  $C_5$  and  $C_2$ . Notice in Step 5 that  $K$  and  $H_o$  must be selected such that  $\sqrt{\zeta^2 - K(1 - H_o)}$  is real.

**Step 5:** Given  $F_c$ ,  $H_o$ ,  $C_2$ ,  $C_5$ , alpha and beta, calculate  $R_1$ ,  $R_2$  and  $R_3$  using the following equations.

$$\zeta = \frac{\alpha}{\sqrt{\alpha^2 + \beta^2}}$$

$$\omega_o = 2\pi F_c \sqrt{\alpha^2 + \beta^2}$$

$$K = \frac{C_5}{C_2}$$

$$R_1 = \frac{R_4}{(-H_o)}$$

$$R_3 = \frac{1}{\omega_o C_2 [\zeta \pm \sqrt{\zeta^2 - K(1 - H_o)}]}$$

$$R_4 = \frac{\zeta \pm \sqrt{\zeta^2 - K(1 - H_o)}}{\omega_o \cdot C_5}$$

**Step 6:** Review the resistor and capacitor values. It is desirable to keep the capacitor values sufficiently large to minimize the effects of stray capacitance. It may be necessary to adjust the capacitor values chosen in Step 4 to achieve this requirement. Also verify that R1 is larger than the minimum required input impedance.

**Step 7:** The resistor values calculated in Step 5 are generally not standard values. Select standard values which are nearest the calculated values. This should not create a large change in the filter characteristics since metal film resistors are available in approximately 2.5% increments which allows for component selection near the calculated values. However, it is advisable to calculate the actual filter parameters, using the selected values, using the equations in Step 5.

**Step 8:** The conversion from the singled-ended circuit to the differential circuit requires duplicating the values of R1, C2, R3, R4 and C5 in the non-inverting input, as shown in Figure 1.

### 3. Design Example

**Step 1:** The required pass band gain,  $H_o$ , is -1 for this example.

**Step 2:** Minimum input impedance is 10 k $\Omega$ .

**Step 3:** Select a Butterworth response with a corner frequency of 50kHz. (A two-pole Butterworth

with a corner frequency of 50 kHz attenuates the signal at 20 kHz by approximately 0.1 dB and has nearly ideal phase linearity within the audio band.)

$F_c = 50 \text{ kHz}$   
 $\alpha = .7071$   
 $\beta = .7071$

**Step 4:** Select convenient values for C5 and C2.

C5 = 220 pF  
 C2 = 1000 pF

**Step 5:** Given  $F_c$ ,  $H_o$ , C2, C5, alpha and beta, calculate R1, R3 and R4.

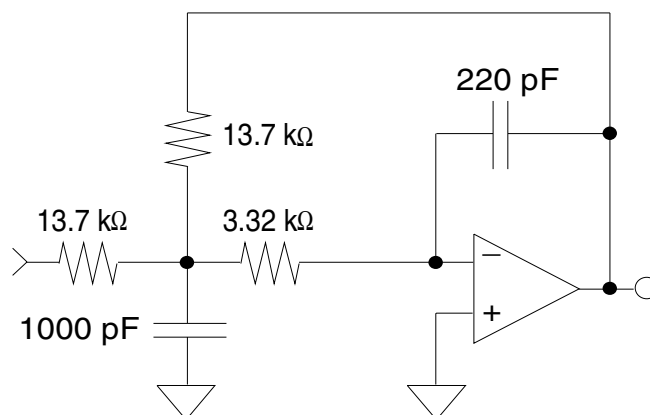
R1 = 13.77 k $\Omega$   
 R3 = 3.343 k $\Omega$   
 R4 = 13.77 k $\Omega$

**Step 6:** Review the filter component values and filter parameters. Verify that R1 is greater than 10 k $\Omega$  and the capacitor values are sufficiently large to negate stray capacitance effects.

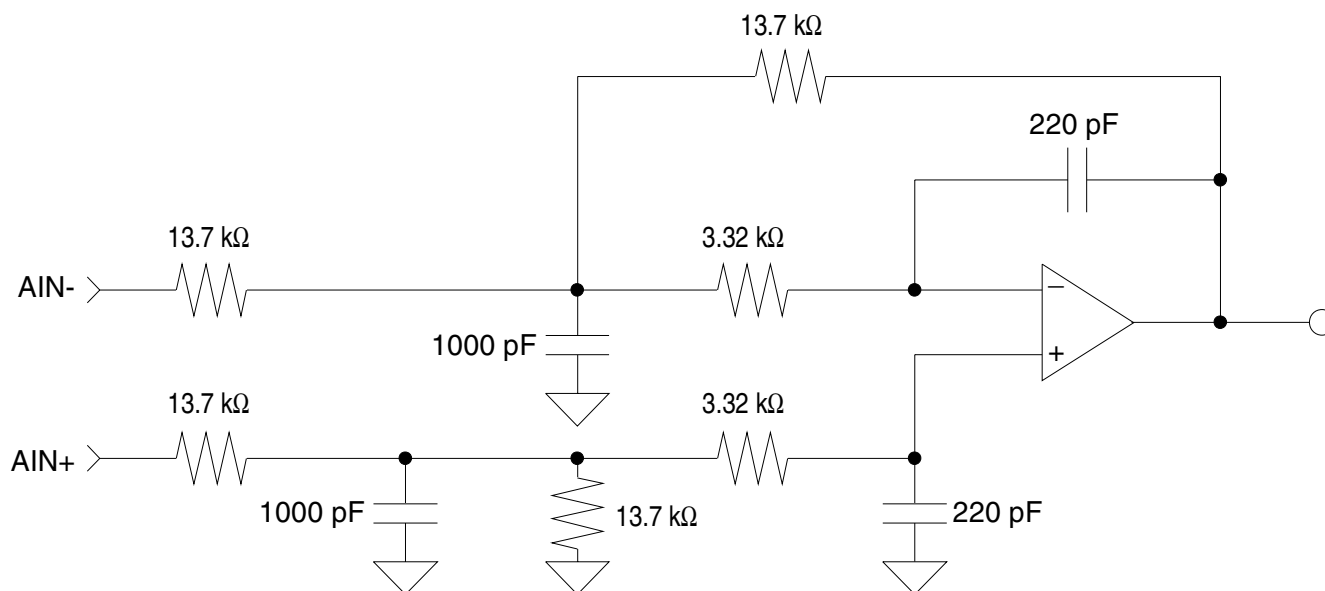
**Step 7:** Select standard resistor values which are nearest the calculated values.

R1 = 13.7 k $\Omega$   
 R3 = 3.32 k $\Omega$   
 R4 = 13.7 k $\Omega$

**Step 8:** The conversion from the singled-ended to the differential circuit requires duplicating the values of R1, C2, R3, R4 and C5 in the non-inverting input as shown in Figure 4 and 5.



**Figure 4. 2-Pole Multiple Feedback Filter Design**



**Figure 5. 2-Pole Filter with Differential Input**

## REFERENCES

- [1] C. L. Lindquist, "Active Network Design with Signal Filtering Applications", Steward & Sons
- [2] A. B. Williams, "Electronic Filter Design Handbook", McGraw-Hill
- [3] "Reference Data for Radio Engineers" (Fourth Edition), International Telephone and Telegraph Corporation

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