A Wide-Band, Low-Power, High Slew Rate Voltage-Feedback Operational Amplifier

Farhood Moraveji

Abstract— **A wide-band low-power voltage-feedback operational amplifier on a 3 GHz, 40 V complementary bipolar technology is described. The class AB input stage takes advantage of some current-boost transistors which enhance and linearize the slew-rate during large-signal operation without increasing the power consumption. The triple-buffered output stage provides 100 mA of load current maintaining good linearity. Since the circuit design and technology development were concurrent, several different circuits were stepped into one wafer to fully characterize the process and identify the best product candidates. The low-current version of this chip has a quiescent current of 2.5 mA, 2000 V/μs slew rate and gain bandwidth of 110 MHz. The medium-current version draws only 6.5 mA of current at the same supply voltage while the slew rate increases to 3500 V/μs and bandwidth to 210 MHz. Both parts are operational from +/−2.75 V to +/−18 V supply range. Die size is 51 mils by 76 mils on a poly-emitter CB process.**

I. Introduction

In the past several years, IC op-amp's bandwidth and slew rate continue to climb, while they consume less power. Comparing to the more traditional amplifiers, these figures of merit have improved by at least an order of magnitude. The emergence of various complementary bipolar (CB) processes and new architectures, such as current-feedback, class AB input stage, and dynamic current mirrors, are the driving forces behind all these new and interesting developments. Despite the widespread availability of these high-speed complementary processes, generally they give up breakdown voltage (BV_{ceo}) for bandwidth. Amplifiers fabricated on these processes have relatively high quiescent current, poor input and output dynamic range, low open-loop gain, low output current drive capability, and not very attractive distortion figures. These types of amplifiers generally fit into the high-end RF requirements where signal swing is limited and distortion is not a big concern.

To realize high-precision, high-frequency, and low-power analog circuits for a wide range of applications, a high-performance, high-voltage complementary bipolar process was developed. The technology, referred to as VIP3, offers poly-emitter transistors with BV_{ceo} of 45 V for NPN and 60 V for PNP. The device $BV_{ceo} \times ft$ and $\beta \times$ Va figures of merit are 135 GHz.V/ 20 000 V for NPN and 130 GHz.V/6500 V for PNP [1].

To utilize the process to its maximum performance and to optimize it for a real-world application, a precision, high-speed voltage-feedback operational amplifier was defined and concurrently developed with the process. Quasi-saturation inherent in a high-speed, high-voltage process is due to thicker and lighter epi layer. This quasi-saturation made the ac models of the transistors operating at low V_{ce} inaccurate. Therefore, circuit design for optimum performance became very difficult and required a radical change in development methodology. In Section II, circuit design challenges in a developing technology and quasi-saturation modeling will be discussed. In Section III, various high-speed op-amp architectures are examined. Circuit design aspects of VIP3 amplifiers are covered in Section IV. Device cross section and process considerations are described in Section V. Experimental results and performance graphs are presented in Section VI.

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II. High-Speed Analog Design in a High-Speed, High Voltage Developing Technology

A. Circuit Design Issues

The design methodology for high-speed analog design with a process under development is quite different from that with a mature process. Here, the specs desired and targeted for during early product definition are subject to change on the final silicon. The designer should have a good understanding of process, device aspects, and a more dynamic approach toward the circuit design and silicon evaluation. The design engineer needs to work closely with the process-development group. He should be able to relate the results of his device and circuit evaluations to device and process characteristics and constantly provide accurate and constructive feedback. High-speed circuit design, circuit tweak, and debugging of silicon can be very challenging for well-established and stable processes. However, if you are doing circuit design for a process under development, where everything is moving, your initial models are not truly representative of your final silicon; therefore, SPICE simulation has limited value and sometimes might lead you in the wrong direction, especially if you have signal path transistors operating at low V_{ce} where quasi-saturation becomes significant and ft start crashing.

In the design of the high-speed amplifiers on this new process, several versions of the circuits were stepped into one single wafer to identify the best product candidate. The circuits were designed in such a way that quiescent current, transconductance of the input stage, all capacitors and resistors in the critical parts of the circuit, etc. were tweakable by opening metal links. Many different types of current mirrors with different geometries and circuit structures were included in the

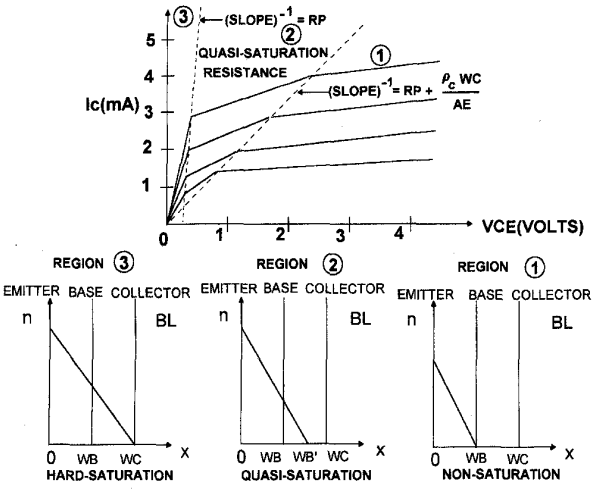


Fig. 1. Transistor behavior in different regions of operation.

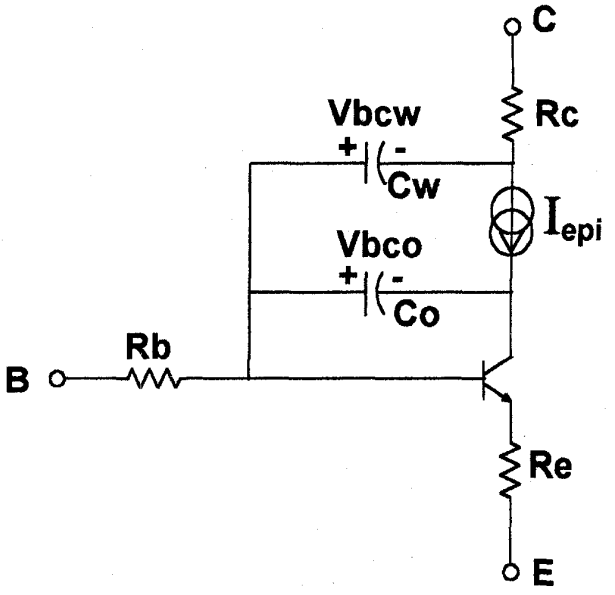


Fig. 2. Modeling quasi-saturation via a controlled current source.

wafer. This enabled us to test the circuits and characterize the process under different conditions. A very simple op-amp was designed and included for maximum bandwidth estimation. This test circuit together with the other ones were used to monitor the SPICE model parameters and do a sanity check on the ac parameters.

One of the advantages of this design methodology, though time consuming, was that several circuits came out at the same time and it made it feasible to define realistic products to fit the process.

B. Quasi-Saturation

Quasi-saturation is an inherent part of a high-speed, high-voltage process. In order to achieve higher breakdown voltage, generally the epi region is made thicker and is lightly doped. When a BJT fabricated on this process is operated at high injection levels, quasi-saturation or base push-out effect arise. In this operation region, the internal base-collector junction is forward biased, while the external base-collector terminals remain reverse biased. Transistor behavior in the three regions of operation is shown in Fig. 1 [2]. Region 1 shows the normal nonsaturation region where the internal base-collector junction is reverse biased. Here, the total collector emitter voltage is equal to

$$V_{\rm ce} = V_d + VR_c + VR_p \tag{1}$$

where V_d is the voltage across the collector depletion region

$$VR_c = \frac{\rho_c W_c}{A_e} \tag{2}$$

is the voltage across the undepleted part of collector region and

$$VR_p = R_p I_c \tag{3}$$

is the voltage drop across the ohmic region. Also ρ_c is the collector resistivity, A_e is the emitter area, and W_c is the width of the collector region.

In the quasi-saturation which is shown in region 2 of Fig. 1, base-collector diode becomes forward biased, depletion region disappears, and $V_{\rm ce}$ is only determined by the ohmic drops. In this region, holes from the base are injected into part of collector region and the base extends from WB to WB′. The minority carrier distribution terminates at this extended base. Because of this extended base width, dc current gain falls from its maximum value and also ft crashes. In the quasi-saturation region the total collector emitter voltage is given by

$$V_{\rm ce} = I_c R_p + \frac{I_c \rho_c}{A_e} X(W_c - WB'). \tag{4}$$

As it was mentioned earlier, the base-widening effect modifies both ac and dc performance of the transistors by effectively increasing the forward transit time τ_f. The analysis and modeling of this phenomenon is very complicated, and in SPICE there is no explicit expression for that.

Some work has been done to model quasi-saturation through a controlled current source representing the epitaxial region [3]. One such model, which is an extension of the Gummel–Poon model, is shown in Fig. 2. Here, the controlled current source $I_{\rm epi}$ represents the collector epitaxial region. The external base-collector voltage $V_{\rm bcw}$ and internal base-collector voltage $V_{\rm bco}$ control this current source. Capacitances C_w and C_0 represent the charge stored in the epitaxial region.

To get this model to work, four parameters should be added to the simulation cards. These parameters are defined as following:

R_{co}	Resistance of the epitaxial region.
GAMMA	Epitaxial doping factor.
V_0	Epitaxial velocity saturation voltage.
Q_{co}	Epitaxial charge factor.

Extraction of these model parameters is not trivial and after all, the model is not very accurate. Now the question is, "How can circuit design be done when quasi-saturation is present?" In circuit simulation, using multiple SPICE model cards for a

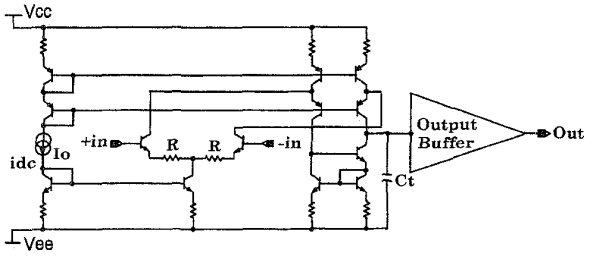


Fig. 3. Simplified schematic diagram of a traditional folded-cascode amplifier.

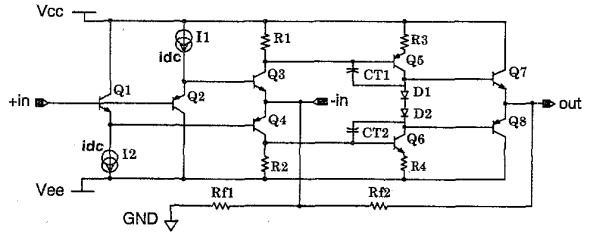


Fig. 4. Simplified schematic diagram of a current-feedback amplifier.

single transistor operating at different V_{ce} levels is very useful. This simply means that ac SPICE model parameters should be extracted for a single transistor for a wide range of voltages optimized for the design. In the circuit design, avoid smaller size emitters for transistors operating at low V_{ce} such as current mirrors. Also, effective collector resistance can be decreased by using multi-emitter structure without increasing the size of transistor significantly.

III. High-Speed Op-Amp Architectures

In the last few years, several papers have been written about the evolution of high-speed operational amplifiers [4]. In this paper, a couple of the most commonly used topologies are briefly reviewed.

In a traditional folded-cascode amplifier which is shown in Fig. 3, the widest bandwidth is achievable while the slew rate is limited to the amount of the tail current available to charge or discharge the total capacitance on the high-impedance node C_t. Since the slew rate is I_0/C_t, in order to obtain higher slew rates, either the supply current should be increased or the total capacitance C_t should be decreased.

In many high-speed circuits, the amount of C_t is limited to the sum of the junction capacitances set by the process and size of the transistors used in the circuit. In this type of amplifier, the unity-gain bandwidth is $0.159/RC_t$. To increase the slew rate without disturbing the bandwidth, input stage transconductance should be reduced by increasing the value of R. This will result into higher input noise, more input offset voltage, and lower open-loop gain [5].

Current-feedback amplifiers have been around for many years. These types of amplifiers generally provide excellent slew rate; close-loop bandwidth is independent of noise gain and depends on the feedback resistor.

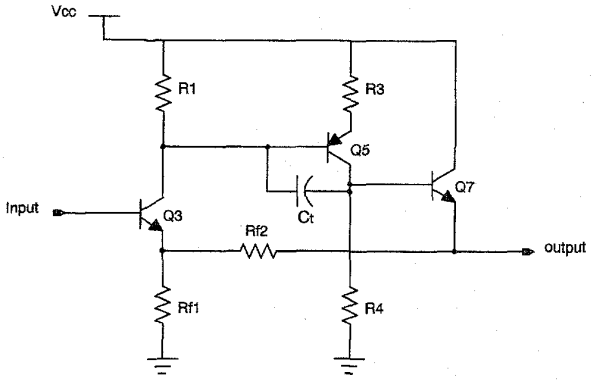


Fig. 5. Half-circuit series-shunt equivalent circuit of a current-feedback amplifier.

Fig. 4 shows a simplified schematic diagram of a current-feedback amplifier. Here, the input stage is a unity-gain buffer forcing the inverting input to follow the noninverting input. Any voltage imbalance at the inputs of this buffer causes the current flow in or out of the inverting input. These currents are mirrored internally to charge and discharge the total compensation capacitor. The amount of current depends on the feedback resistor $Rf2$ which couples the output of the amplifier to its inverting input.

Fig. 5 shows the half-circuit series-shunt equivalent circuit of a current-feedback amplifier. After opening the feedback loop and taking into account its loading effect on the emitters of Q3 and Q7, the following equation for the closed-loop gain can be derived [6]

$$A_{\mathrm{cl}} = \left(1 + \frac{Rf2}{Rf1}\right) X \left(1 + J\frac{\omega}{\omega_p}\right)^{-1} \tag{5}$$

where

$$\omega_p = (Rf2XC_t)^{-1}. \tag{6}$$

Equation (6) clearly shows that the closed-loop pole which determines the -3 dB bandwidth of the amplifier is set by the total capacitance C_t and feedback resistor $Rf2$ and is independent of the closed-loop gain.

In the current-feedback amplifier, any large signal input step creates momentarily a large error voltage across the feedback resistor. The current available to charge and discharge the compensation capacitor is proportional to this differential input voltage and inversely proportional to the value of the feedback resistor. This might imply an unlimited slew rate; however in real life a variety of second-order effects limit the slew rate. Current-feedback amplifiers generally suffer from higher noise, high input offset current, less precision, poor CMRR, poor low-level settling, and thermal feedback errors [7].

IV. Circuit Design on VIP3 Amplifier

Fig. 6 shows the simplified schematic diagram of the low-power, high-speed voltage-feedback amplifier fabricated on VIP3 process. The modified class AB input stage is fully symmetrical and has a similar slewing characteristic to the

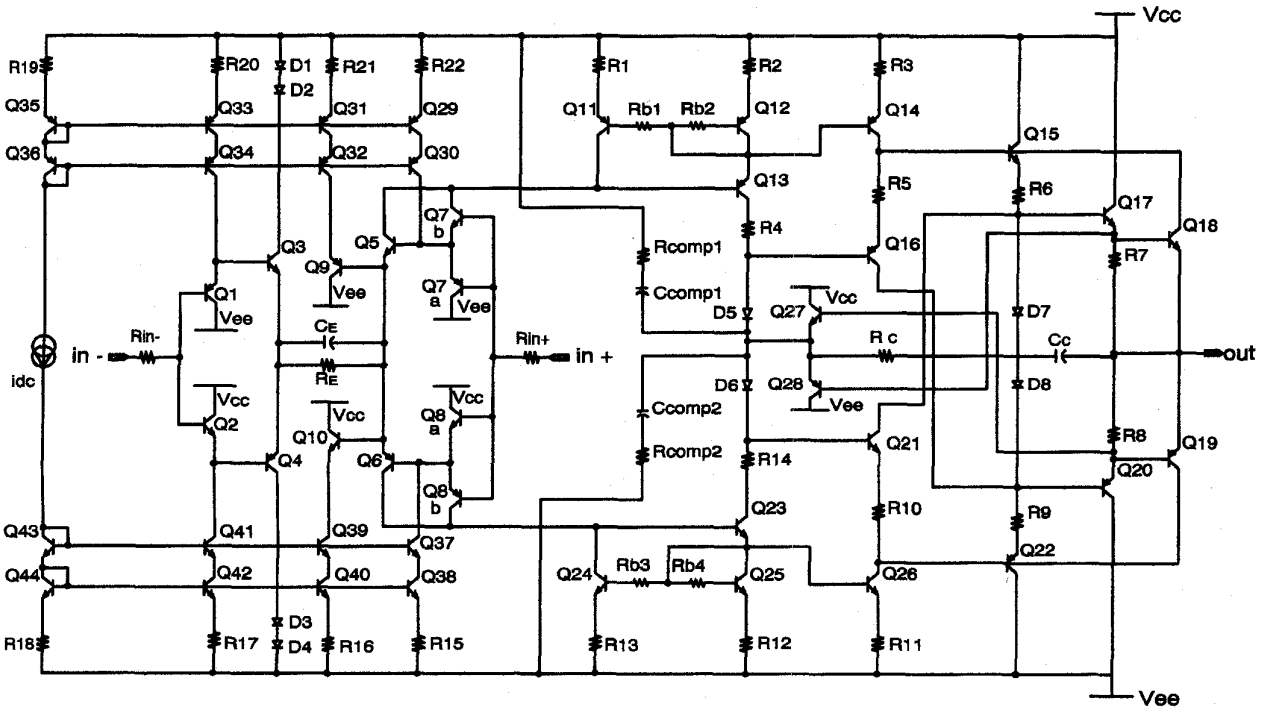


Fig. 6. Simplified schematic diagram of low-power, high-speed, voltage-feedback amplifier.

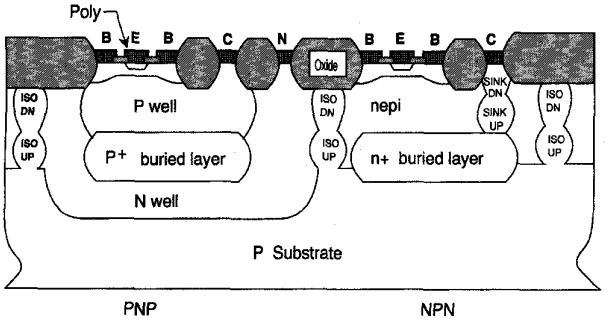


Fig. 7. Cross-sectional view of the VIP3 complementary poly-emitter process.

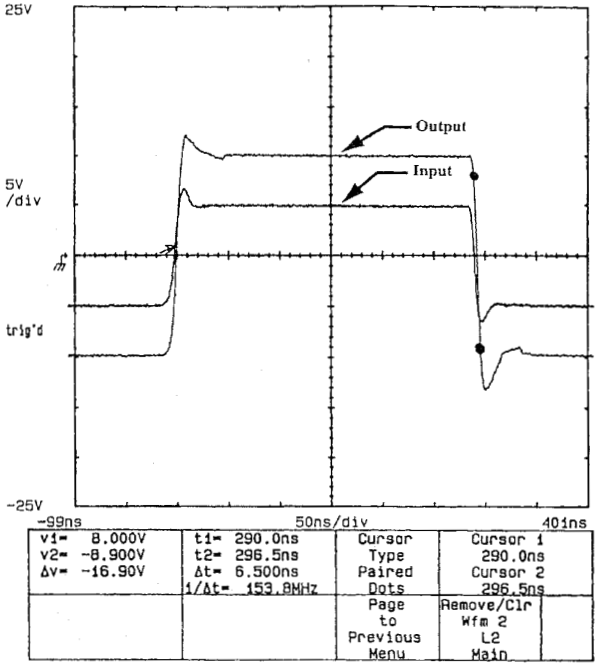
current-feedback amplifier. Here, Q5–Q8 form the equivalent of the current-feedback input buffer, R_E the equivalent of a feedback resistor, and Q1–Q4 buffer the inverting input. The transconductance of the input stage is inversely proportional to the degeneration resistor R_E. The quiescent current of the input stage is set by the cascoded mirror Q29–Q34 in the top side-mirror and Q37–Q42 in the bottom-side mirror. The capacitor CE in parallel with R_E creates a high-frequency zero that increases the g_m, extends the bandwidth, and improves the phase margin.

In the design of this amplifier different current mirrors were tried. However, the modified Wilson current mirror with extra base resistors delivered the best ac response. The extra low-ohm base resistors reduce the peaking of the mirror at higher frequencies. Q11–Q13 together with $Rb1$–$Rb2$ form the top-side mirror, and Q23–Q25 with $Rb3$–$Rb4$ are used in the bottom-side mirror.

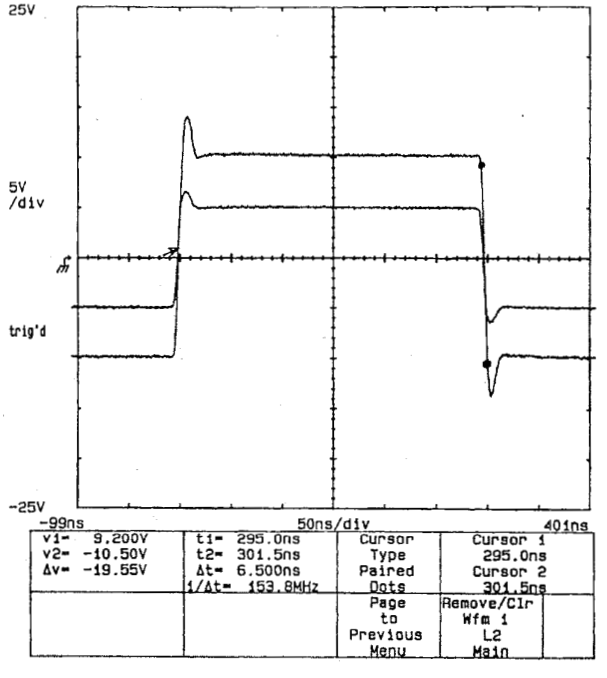
Addition of transistors Q9–Q10 to the input stage compensate for NPN, PNP beta mismatch and center the offset voltage considerably. Slew-enhancement transistors Q7b and Q8b improve the transient response of the amplifier significantly. These transistors are normally off; however, if the input is driven with a fast differential pulse, they provide extra base current for the bases of Q5 and Q6 during the positive slew and negative slew respectively. Notice that the collector currents of these transistors are mirrored back to the high-impedance point where they charge and discharge the compensation capacitor faster during large signal slew.

The somewhat complex output stage is very linear and provides 100 mA of current into the load. In Fig. 6, Q14–Q28 comprise the triple-buffered output stage. Collectors of Q16 and Q21 are bootstrapped to minimize the parasitic capacitance effect and improve the phase delay of this stage. The base-collector of these transistors are reverse biased by two diode drops; however, from the ac point of view, the rate of change of voltage between base-collector junction is zero, and therefore there is no current flowing in the parasitic junction capacitance.

Emitter resistors R5–R6 and R9–R10 play an essential role in minimizing the effect of temperature upon overall performance of the amplifier and improving the stability of the emitter followers while damping the follower peaking at higher frequencies. These resistors also improve the gain margin at the expense of a small amount of bandwidth. Q18 and Q19 are short circuit protection transistors. Q27–Q28 clamp the high-impedance node to the output. These transistors are off under normal operating conditions.

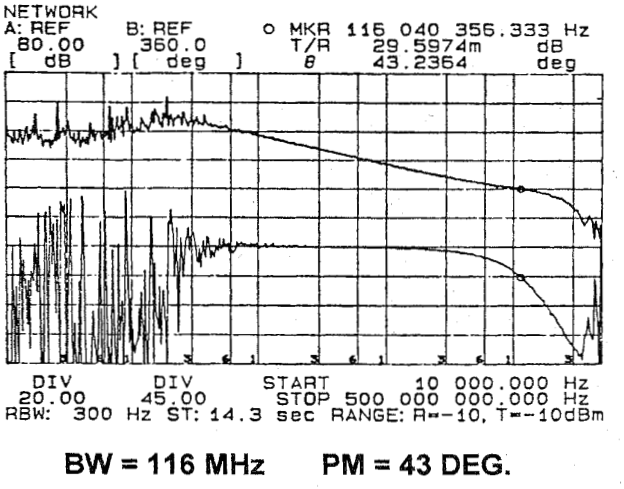


(a)

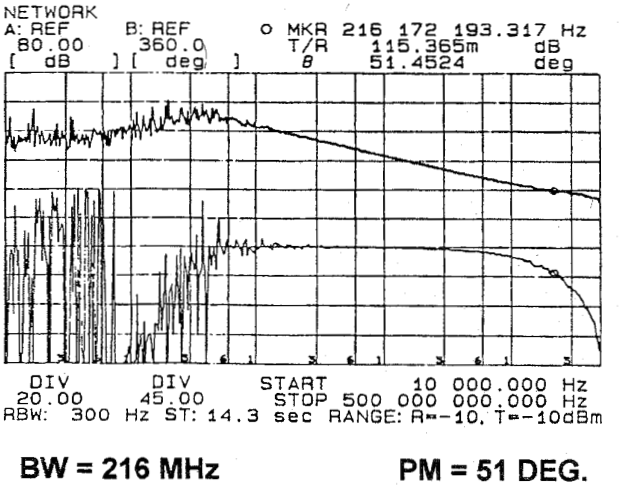


(b)

Fig. 8. Large signal pulse-response of (a) low-current amplifier and (b) medium-current amplifier.



(a)



(b)

Fig. 9. Open-loop gain and phase of (a) low-current amplifier and (b) medium-current amplifier.

The series R_c-C_c network across the output stage is completely bootstrapped and does not have significant effect at lower frequencies. At higher frequencies, R_c-C_c bypasses the output stage, and this improves the bandwidth. When driving capacitive load, this network is not bootstrapped completely, and it begins to interact with the load impedance creating a voltage difference between the high-impedance node and the output. This effectively reflects part of the capacitive load to the high-impedance node, therefore improving the phase margin by reducing the bandwidth and enhancing stability. By proper choice of R_c-C_c network, the amplifier can drive infinite capacitive load.

V. Process Considerations

These low-power, high-speed op-amps were fabricated on a recently-developed 40 V poly-emitter complementary bipolar technology called VIP3. The technology uses deep junction isolation, twin buried layer, N-type epitaxial layer, combined with single-poly non-self-aligned emitter/base transistor

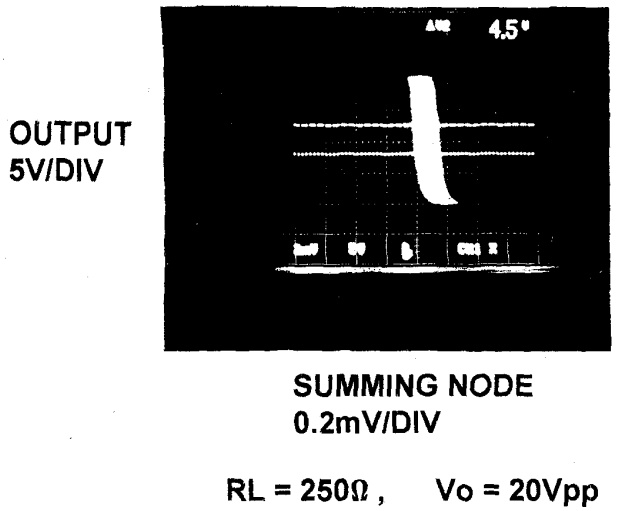


Fig. 10. Oscilloscope photograph of open-loop gain linearity of low-current amplifier.

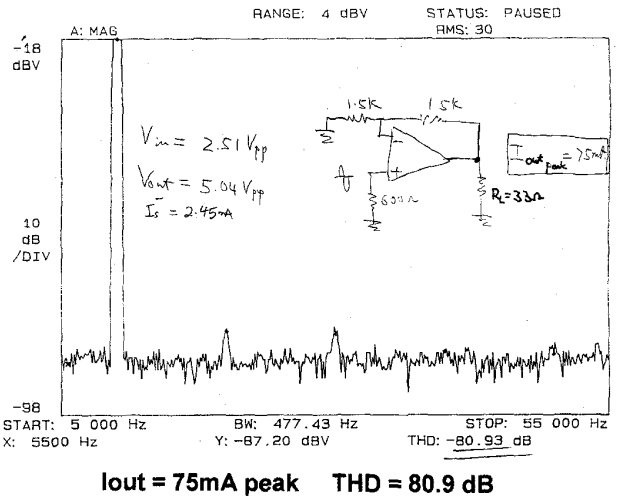


Fig. 11. THD of low-current amplifier at 10 KHz with 75 mA output peak current.

TABLE I
TYPICAL MEASURED PERFORMANCE DATA

PARAMETER	LOW CURRENT	MEDIUM CURRENT
SUPPLY CURRENT	2.5mA	6.5mA
GAIN	90dB	85dB
INPUT BIAS CURRENT	0.7uA	1.8uA
OFFSET VOLTAGE	100uv	250uv
CMRR	104dB	100dB
PSRR	81dB	82dB
OUTPUT SWING	26.5Vpp	26.5Vpp
UNITY GBW	110MHz	200MHz
PHASE MARGIN	45 degrees	45 degrees
SETTLING TIME 0.1%	30ns	25ns
SLEW RATE	2500V/us	3000V/us
LINEARITY RL = 250Ω	0.001%	0.0007%

structure with minimum feature size of 2 μm. The process also offers n and p type poly-silicon resistors and poly-silicon/LTO/metal capacitor. A cross-sectional view of NPN and PNP devices is shown in Fig. 7.

The process has a standard p-substrate and the usual $n+$ buried-layer of the NPN transistors. In addition, an n-well is diffused into the substrate to hold the PNP transistor and isolate it from the substrate. Aluminum, because of its very high diffusivity, is used in conjunction with boron to form the deep PNP collector/p-well and isolation region. The intrinsic bases are implanted prior to poly-silicon deposition through a pad oxide and the emitter and extrinsic base contacts are diffused from the poly-silicon electrodes.

VI. Experimental Results

As mentioned earlier in the text, two amplifiers have been fabricated on the VIP3 process and the dimensions of the die are 51 mils by 76 mils. In the layout of these amplifiers, the n-well tubs of the signal path transistors are bootstrapped to minimize the effect of the n-well-to-collector capacitances. The offset voltage of the medium-current amplifier is trimmable via metal fuses. The two amplifiers have been fully characterized and the typical measured performance data is shown in Table I. In Fig. 8(a) and (b), the large signal pulse response of both amplifiers are shown. The open-loop gain and phase of the parts are depicted in Fig. 9(a) and (b). Open-loop gain linearity of the low-current amplifier was measured for an output swing of 20 V_{pp} into 250 ohms load. Scope photo of the result is shown in Fig. 10. This measurement proved that the linearity is better than 0.001% under that load condition. In another application circuit, the THD of the low-power amplifier was measured at 10 KHz for an output current of 75 mA into the load. Fig. 11 shows the result of measurement and THD is about 81 dB.

VII. Conclusion

Two wide-band, low-power, voltage feedback amplifiers have been designed and fabricated on a low-cost 40 V poly-emitter, junction-isolated, complementary process. Since the design and process development were concurrent, a dynamic approach was taken toward the circuit design, and many different simple and complex test circuits were stepped into one wafer to fully characterize the process. The modified class AB input stage used in these wide-band amplifiers enhances the slew rate significantly without increasing the supply current. The output stage can provide 100 mA of load current with very low quiescent current and minimum amount of phase delay. The parasitic capacitances on the signal path have been bootstrapped to minimize their effect and improve the bandwidth. Both amplifiers are operational from $+/-2.75$ V to 18 V supply range with excellent PSRR and CMRR.

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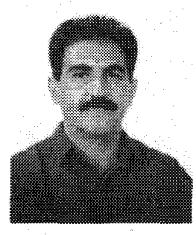

Farhood Moraveji was born in Arak, Iran, in 1955. He received the B.S. degree in electrical engineering from the University of Shiraz, Iran, in 1979 and the M.S. degree in electrical engineering from the University of Santa Clara, CA, in 1987.

From 1979 to 1983 he was with the Pars Toshiba Company where he worked on the design of RF and video circuits for TV and VTR. He joined the Linear Design Group at National Semiconductor Corporation, Santa Clara, CA, in 1987. There, he has designed temperature sensor, a very high-speed, high-precision sample-and-hold amplifier. In the last few years he has designed several high-speed, low-power operational amplifiers. He has published many papers in the IEEE journals and holds five patents. His research interests are in the area of wide-band, low-power bipolar, CMOS and BICMOS, analog IC design.