DEVELOPMENT OF A DOLBY S-TYPE IC USING NEW MASTER SLICE METHOD

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1.Abstract

An audio signal processing IC for the Dolby S-type consumer audio noise reduction IC has been developed using a new bipolar master slice process with high flexibility.

1.Introduction

Dolby S-type is a newly developed audio noise reduction system introduced by Dolby Laboratories in 1989 for compact cassette products. The system is based on the Dolby SR (Spectral Recording) system introduced in 1986 for professional format recording, and features excellent dynamic range improvement, low noise modulation and tolerance to record/playback path level and frequency response error.

We have developed a new bipolar IC for Dolby S-type using a unique design method. We had to develop the IC quickly in parallel with the system development, since it was impossible to introduce the S-type to consumer products without an IC development. We have developed the IC using a new bipolar M/S (master slice) process, which has very short TAT (turn around time) and is very flexible for system modifications and parameter adjustment. The method was very useful, and offers a new analog IC design style.

2.S-type system and IC design

The S-type processor, shown in figure 1, is composed of high and low level signal processing stages as in Dolby C-type. While the C-type processor has only two SB (sliding band) compressors the S-type processor is more complex in that it has an additional three FB (fixed band) compressors for a total of five compressor stages. The number of compressor stages is a good relative measure of complexity since the majority of IC elements are dedicated to these stages.

Referring to figure 1, note that the signal flow can be thought of as being the sum of a passive main path with that of two side paths. It is a fundamental principle of S-type that all dynamic signal processing take place in the side paths. Since the contribution of the side path decreases with increasing level (due to signal compression), the output signal at high levels is basically that which would be obtained by passing the signal through the passive main path alone. This circuit topology places less emphasis on the audio performance of the side path thereby simplifying its design.

Figure 2 shows the block diagram of a HF (high frequency) stage. On the diagram HLS and LLS mean high level stage and low level stage respectively. The HF stage is comprised of two

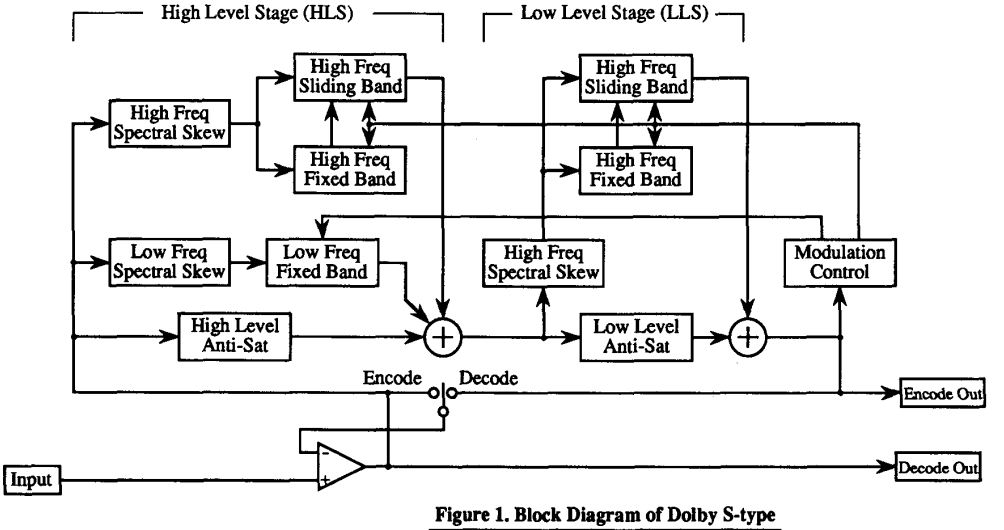

Figure 1. Block Diagram of Dolby S-type

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compressors known as the HF/FB(high frequency fixed band) and the HF/SB (high frequency sliding band). The audio signal is taken from the node labeled "Output" and is a combination of the fixed and sliding band outputs. If the transfer functions of the HF/FB and HF/SB are labeled HF(s) and HS(s) respectively, the output VOUT can be described as

$$V_{OUT}(s) = HF(s) + HS(s) - HF(s) \cdot HS(s) \quad (1)$$

The variable resistance elements are controlled by a DC signal which is proportional to the steady state magnitude of the compressor output signal. The sliding band can be thought of as a variable high pass filter whose corner frequency rises with increasing signal level or frequency. The fixed band is a variable attenuator whose attenuation increases with increasing signal level in the band defined by the input filter. In the no signal or quiescent condition, the variable high pass filter and variable attenuator have unity gain.

The control paths (dotted lines) basically frequency-weight the signal then rectify and smooth it to produce the DC control signal. Each control path has a non-linear element to provide the desired relationship between the control voltage and the subsequent variable resistance value. The O/S (overshoot suppression) signals are not smoothed and can quickly change the control voltage to control overshoots during transient signal conditions. Modulation control signals (MC1, MC2, and MC3) oppose the control signal and reduce its value under certain signal conditions. The parking and control limit circuits set the minimum and maximum value for the control voltage. This will provide a defined limit for circuit operation in the event of extreme signal conditions.

When the IC design was begun, a working circuit had been built using standard discrete components but some details regarding desired performance were not yet finalized. It was decided that the S-type system should be defined as being easily built using existing bipolar IC technology (previous IC's were defined by discrete circuits which were difficult to accomplish with bipolar technology). This approach required some flexibility in the IC and the system design such that the goal of integratability would not compromise system performance and vice-versa.

3.New master slice system

As shown in figure 3, we have a unique bipolar M/S (master slice) system, on which 15 and 19 independent circuits, for a 1st generation and a 2nd generation respectively, can be integrated. A batch of wafers is run periodically 2 to 3 times a month. IC development time and cost were reduced drastically by using the M/S system.

Table 1 shows outline of the typical M/S chips (standard L size chip). Other size chips or a chip having special elements like a power transistor are also obtained.

The 1st generation M/S chip had traditional bipolar analog M/S element arrangement, therefore the element density was relatively low compared with a chip by full custom layout . It was mainly used as an IC development tool instead of a bread board, since the TAT was very short and the development cost was very low.

A newly developed 2nd generation M/S chip achieved high element density. Advantages of the 2nd generation M/S chip are that it has:

1.Poly-silicon resistor

2.Element arrangement like a channel-less gate array.

The chip features

1.High element density
(more than 2000 elements on a 4.4 x 3.1mm chip)

2.Flexible resistance and capacitance (type 2).

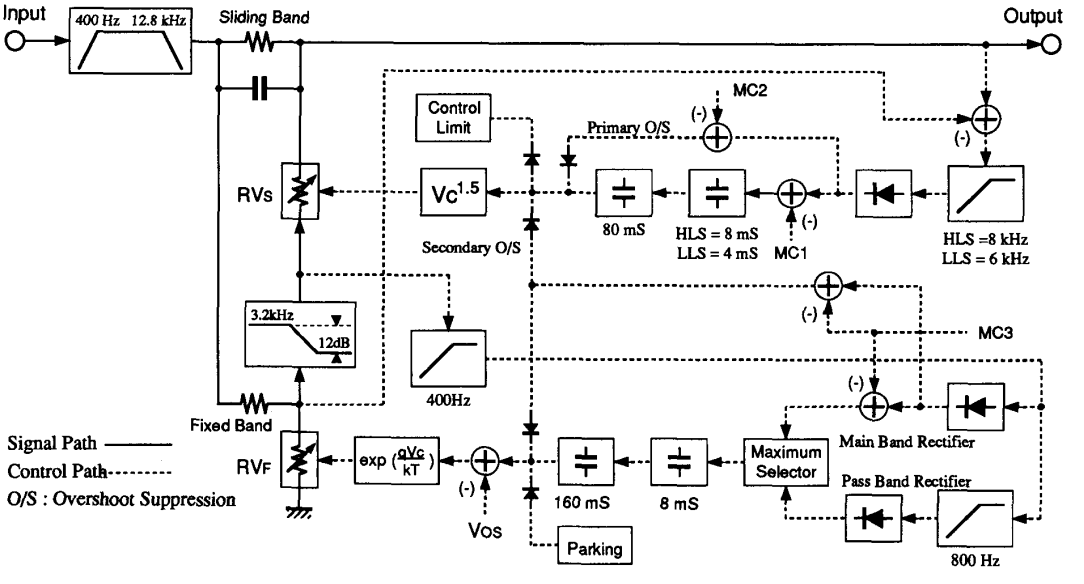

Figure 2. Block Diagram of High Frequency Stage

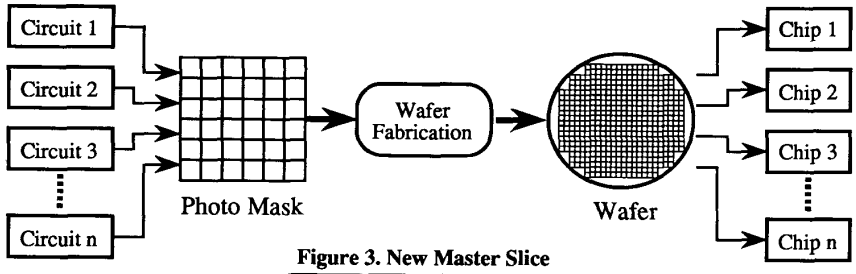

Figure 3. New Master Slice

The 2nd generation M/S accepts 2 kinds of design, type 1 and type 2, on a common wafer. Type 1 is a standard M/S having fixed values of resistance and capacitance. Type 2 accepts flexible component value, however, pattern layout has to be completed a week earlier than type 1. Average period from pattern layout to sample of the type 1 is 5 weeks for a 1000 element circuit.

Element density of the 2nd generation M/S was improved approximately 3 times compared to the 1st generation. If a circuit topology and scale are matched well with the element arrangement of the chip, then the IC chip size using the 2nd generation chip will be comparable with a custom layout chip, and will be competitive even for consumer products. The 1 chip S-type IC is one of the best example of this.

The M/S system offers a new analog IC design style. In analog IC design, it takes more time to find a problem than to fix it. One of the reasons is that it is difficult to evaluate the total function and characteristics of a large chip using a typical analog simulator like SPICE. The M/S chip offers a way which shows total chip function and performance quickly and easily. If it is quick and easy to provide an actual device, even though it may take several sample revisions, the correct result can be achieved more quickly by this method. The method is effective especially in an IC for a system in which details are not certain and an IC in which a computer simulation is not effective.

	1st generation	2nd generation	
		Type 1	Type 2
Process	Lateral PNP or Vertical PNP		
Chip Size	4.4 x 3.1 mm (L size chip)		
Pin	48 (L size chip)		
Resistor	Diffusion	Poly-Silicon	
Resistance	8/12K or 2/3K	8K or 2K	Free
Capacitance	1P/2P/4P 10P/15P/20P	2P/20P	>2P >20P
Mask	3	4	8
Effective Maximum Element Count	700 to 1000 elements	2000 to 2800 elements	

Table 1. Outline of Master Slice

4.Development of the S-type IC

One chip Dolby S-type was designed using 3 development phases.

Phase 1 : Main events in phase 1 were translation from discrete and general purpose IC based topology to IC based topology and definition of the system. 2 chips with IC-based circuits of key functional blocks were developed using the 1st generation M/S chips. These chips were used to build prototype processors which were used to define the system definition.

Phase2 : We developed an S-type IC set with 3 chips using the 1st generation M/S chips. Purposes of the IC set were system introduction to the Dolby licensees and determination of the final system parameters. It was also a bread board of the final one chip IC. Since most of the system parameters had to be determined by external components, the IC set had many pins and a high external component count, and the IC set was not suitable for use in consumer products.

Phase 3 : As the final target of the project, we have developed a one-chip S-type IC for use in consumer products using the 2nd generation M/S chip.

5.Computer Model

In order to accurately define the S-type process, a computer model was developed. This model calculates the steady-state response of the S-type process to sine wave input signals. The model was developed by writing equations which represented the transfer functions of various audio and control path blocks. The definition of S-type was altered and refined by examining the results from this model. From this process, key parameters were defined which determined processor performance.

During phase 1, the main use of the model was to determined the non-linear transfer function in the compressor control paths. This was an important prerequisite to further IC development since it was difficult to change the transfer function externally while linear circuit gains or time constants and some topology changes were easily done.

An exponential law was chosen for the fixed band. It had the desired characteristics of a smooth onset of compression followed by a compression effect which increased with increasing control voltage. The transition between these two regions was varied by using the offset term, V_{OS} (see figure 2).

Errors due to the temperature dependence of this law were minimized by proper selection of the zero temperature coefficient current.

A power law of 1.5 was chosen for the sliding band. It provides a smooth onset of compression and a fixed maximum compression ratio which does not change with increasing control voltage.

During phase 2, attempts were made to predict or confirm IC circuit performance using results from the model. A computer controlled measurement system was employed to gather and compare measured versus predicted results. At this stage however, the circuit still defined the required performance. After the performance requirements were met, the circuit was analyzed to extract the model parameters. These parameters were further altered where necessary to allow for circuit design using standard consumer component values. The resulting model now defines the steady-state response of the S-type processor.

In phase 3, parameter defining equations were derived in terms of the IC circuit defining equations using SPICE. This allowed direct calculation of desired IC element values. As a final step, small corrections were made to the IC design to account for non-ideal IC circuit performance. The model was used to check phase 3 IC performance and was very valuable as a tool for pinpointing IC design or performance errors.

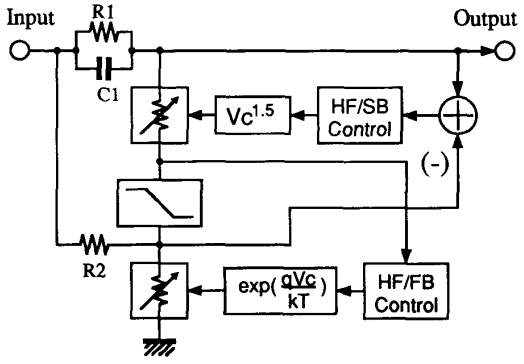

Figure 4. Original Topology of Variable Filter

6.Circuit Design

Subjects on the one-chip IC design (phase 3) were

1.IC-based circuit topology

2.Temperature coefficient zero (TCZ) design.

Figure 4 shows an original topology of a variable filter which is a combination of a sliding band filter and a fixed band attenuator in a HF (high frequency) stage side chain. The circuit was converted to a new topology using VCRs (voltage controlled resistor) and a VIC (voltage to current converter) with current outputs as shown in figure 5. Figure 6 shows a VCR with a current output. A VIC can be thought of as a variation which is rejected a feedback path from the VCR. The VCR has differential input of a high impedance input and a variable impedance input (VCR In). A current mode signal processing using the VCR and the VIC has several advantages.

1.The summing amplifiers in the main path become voltage followers for the main path signal. It eliminates a gain error due to mismatching of a resistor ratio, and makes simple an anti-saturation network.

2.Dynamic offset (due to buffer amplifier input bias current) is reduced since the buffer amplifier is no longer connected to the variable impedance input.

3.It is simple to realize TCZ design, since a required dependency to KR, which is a ratio of an actual resistance and a designed resistance, can be provided easily by adding a temperature coefficient to the current source IY in figure 6.

To achieve the TCZ design, a voltage reference having 3 outputs of VRI, VRE and VRX is used. As shown in following equations, VRI is a fixed voltage source, VRE is a voltage source proportional to a poly-silicon resistance, and VRX is a voltage source inversely proportional to a poly-silicon resistance.

A simplified schematic of the voltage reference is shown in figure 7. In most of the functional blocks bias currents are generated by VRI, which is the sum of the band-gap voltage (1.2V) and 2•VBE.

$$VRI = 1.2 + 2 \cdot V_{BE} \ (V) \qquad (2)$$

The terminal IREF which is band-gap voltage of 1.2V is

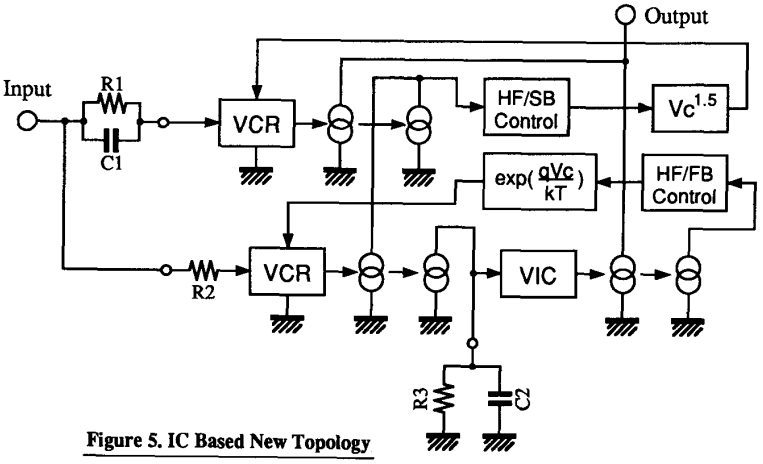

Figure 5. IC Based New Topology

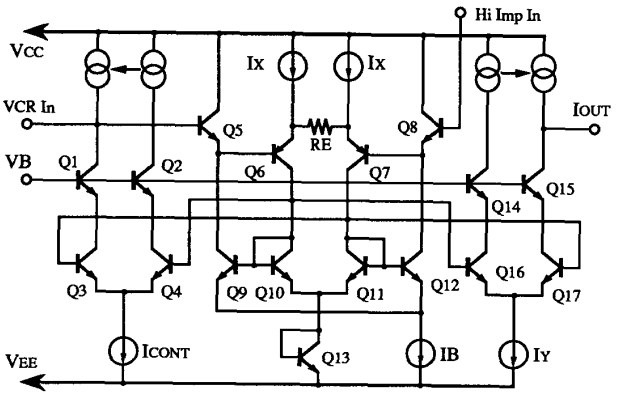

Figure 6. VCR (Voltage Controlled Resistor)

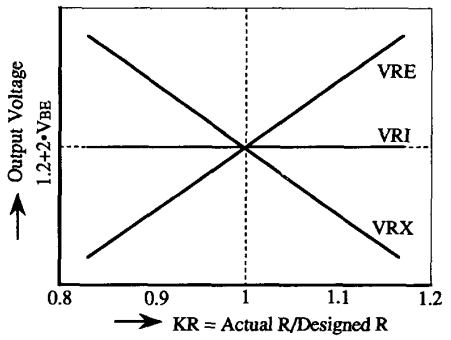

Figure 8. Reference Voltage

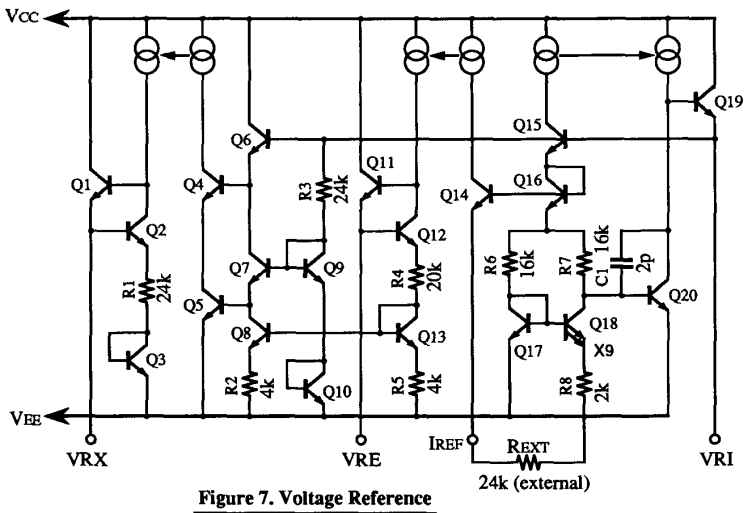

Figure 7. Voltage Reference

connected to an external resistor REXT. A current flowing through REXT is a reference current IREF, which is given as

$$I_{REF} = 1.2/R_{EXT} = 50\ (\mu A) \quad (3)$$

A factor KR is introduced as follows

$$KR = \text{Actual resistance/Designed resistance} \quad (4)$$

Since the actual resistances of R4 and R5 are multiplied by KR to the designed resistances, VRE becomes

$$V_{RE} = 1.2\cdot(R4+R5)/R_{EXT} + 2\cdot V_{BE} = 1.2\cdot KR + 2\cdot V_{BE}\ (V) \quad (5)$$

Collector currents of Q8 and Q10, $I_{C(Q8)}$ and $I_{C(Q10)}$ are given as follows

$$I_{C(Q8)} (=I_{C(Q7)}) = I_{REF} = 50\ (\mu A) \quad (6)$$
$$I_{C(Q10)} (=I_{C(Q9)}) = 1.2/R3 = 50/KR\ (\mu A) \quad (7)$$

The sum of VBE of Q5 and Q7 is equal to the sum of VBE of Q9 and Q10, therefore $I_{C(Q5)}$ is given as

$$I_{C(Q5)} = I_{C(Q9)}\cdot I_{C(Q10)}/I_{C(Q7)} = 50/(KR)^2\ (\mu A) \quad (8)$$

And a voltage of VRX becomes

$$V_{RX} = I_{C(Q5)}\cdot R1 + 2\cdot V_{BE} = 1.2/KR + 2\cdot V_{BE} \quad (9)$$

The relationship between the output voltages and the factor KR is shown in figure 8.

Figure 9 shows a level detector in the HF/FB (high frequency fixed band). A control voltage which controls a VCR should not depend on the factor KR, or system parameters in the level detector will depend on temperature and the poly-silicon resistance.

Idet is an input current of the level detector from the current output of the VCR, and is converted to a voltage by Ri1. A1 generates separately positive half and negative half current frequency weighted by an impedance Zm. The current i1 is a full wave rectified version of current im flowing through the

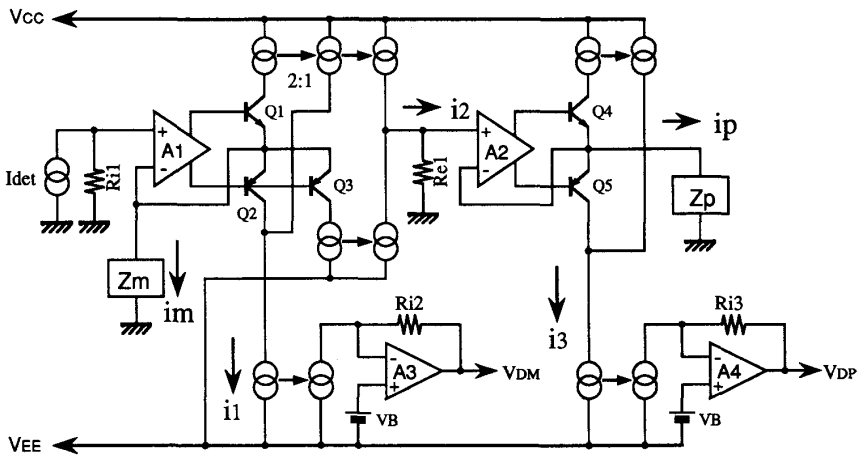

Figure 9. HF/FB Level Detector

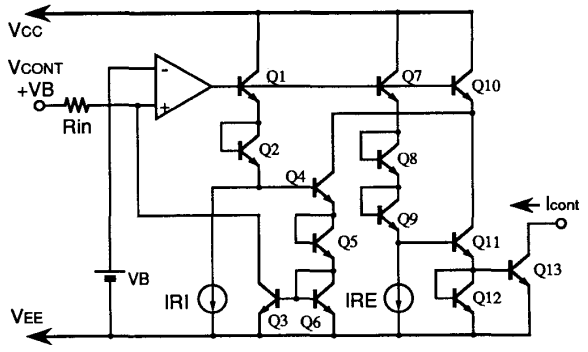

Figure 10. HF/FB Control Current Generator

Items	Specification	Unit
Type	CXA1417 S/Q	
Package	Shrink DIP 48 Pin QFP 48 Pin	
Supply Voltage	±4.5 to ±6.5 9 to 13	Volts
Supply Current	11.0 (no signal)	mA
Encode Error for Computer Model	within ±0.3 (Average)	dB
THD	0.03 (1kHz +10dB)	%
S/N	65 (typ. CCIR/ARM)	dB

Table 2. Outline of S-type IC

impedance Zm. The current i2 is half of im, which is converted to a voltage again by Re1. The voltage drop of Re1 generates the current ip, which is frequency-weighted by an impedance Zp. The current i3 is a full-wave rectified version of ip.

Main band and pass band detector outputs VDM and VDP are obtained from i1 and i3 respectively by current to voltage conversion with A3, A4, Ri2 and Ri3.

Gains of the detectors are given as

$$V_{DM}/Idet = k1 \cdot Ri1 \cdot Ri2/Zm \quad (10)$$

$$V_{DP}/Idet = k2 \cdot Ri1 \cdot Re1 \cdot Ri3/(Zm \cdot Zp) \quad (11)$$

where k1 and k2 are constants.

Resistors Ri1, Ri2 and Ri3 are internal poly-silicon resistors, and impedances Zm and Zp are external components. The condition in which the outputs of VDM and VDP do not depend on KR is given by the following two conditions

(1) Idet is proportional to square of 1/KR

(2) Re1 is an external resistor.

The condition (1) can be easily satisfied by combination of the VCR and the reference voltage source.

Figure 10 shows a control current generator with a power law of 1.5 as another example of TCZ design. Bias currents IRI and IRE are generated by VRI and VRE respectively, and are given as follows

$$IRI = 25/KR\ (\mu A) \quad (12)$$

$$IRE = 25\ (\mu A) \quad (13)$$

Collector currents of each transistor are given as

$$I_{C(Q1)} = I_{C(Q2)} = IRI \quad (14)$$

$$I_{C(Q3)} = I_{C(Q4)} = I_{C(Q5)} = I_{C(Q6)} = V_{CONT}/Rin \quad (15)$$

$$I_{C(Q7)} = I_{C(Q8)} = I_{C(Q9)} = IRE \quad (16)$$

$$I_{C(Q11)} = I_{C(Q12)} = I_{C(Q13)} = I_{CONT} \quad (17)$$

Since the total of the base-emitter voltages of Q1, Q2, Q4, Q5 and Q6 are equal to the total of the base-emitter voltages of Q7, Q8 Q9, Q11 and Q12, the following equation is introduced

$$IRI^2 \cdot (V_{CONT}/R_{IN})^3 = IRE^3 \cdot I_{CONT}^2 \quad (18)$$

$$I_{CONT} = IRI \cdot [V_{CONT}/(Rin \cdot IRE)]^{1.5} \quad (19)$$

The resistor Rin is an internal poly-silicon resistor, and the actual resistance is expressed KR•Rin0, where Rin0 is a designed resistance. By equations (12), (13) and (19) I_{CONT} is given finally as follows

$$I_{CONT} = 25 \cdot [V_{CONT}/(Rin0 \cdot IRE)]^{1.5}/KR \quad (20)$$

where V_{CONT} and Rin0 are in mV and kΩ respectively.

The gain of the fixed band stage is defined by the ratio of the impedances between the VCR and an internal resistor, therefore I_{CONT} should be inversely proportional to KR.

7.Outline of the IC

In the phase 3 development, 6 revisions were made before the final design was completed. During the revisions, correction of careless errors, rejection of parasitic effects, optimization of the VCR, pinpoint adjustment of the encode characteristics and so on were made step by step over a period of 10 months.

If we had chosen full custom design instead of the M/S method, then at least 2 revisions of a full mask set, 2 times the development time and several times the development cost would have been required. The M/S was developed timely for the S-type development, and the IC has shown the best application of the M/S.

The IC-based circuit and system design has resulted in very accurate encode characteristics. Difference between average encode characteristics of the IC and that of the computer model was about 0.3dB maximum.

Table 2 shows an outline of the IC. The IC functions as an S-type encoder, and an external operational amplifier is required to provide a decode function. Next generation Dolby B/C type IC will provide interface functions for S-type, and full functions of B/C/S type will be easily obtained by these devices in the future.

8.Conclusion

A new IC has been developed to implement the Dolby S-type noise reduction process. The IC was developed using the new M/S process. This method has several advantages over full custom IC design including : lower cost, fast TAT, more design flexibility, and quick assessment and correction of design problems.

The advantages of the new M/S method were particularly useful in the design of the S-type IC. This is because the system design changed to accommodated integration and performance requirements and SPICE evaluation was difficult. The resulting IC is a very high performance, low cost, single package which should find good acceptance among manufacturers and consumers.

9.Acknowledgment

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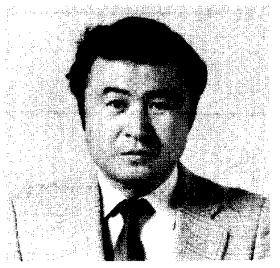
Biographies



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