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Integrated Smart Solenoid Driver with Current Tracking

Aleksander Sešek, Janez Trontelj

Faculty of Electrical Engineering, Laboratory for Microelectronics, University of Ljubljana, Tržaska 25, 1000 Ljubljana, Slovenia

***Abstract*— Solenoid drivers use magnetic force generated by current flowing through the coil, which causes armature movement in the coil. Due to the armature movement, inductance changes and the current level needed for the armature positioning also changes. Special pulse width modulation current driving is needed for the inductive loads to achieve desired response and low power consumption. The current consumption issue is especially important in automotive applications. In typical applications the current value is switched between two fixed levels. Initially a high "pull in" current value is applied to provoke the armature motion, followed by the low constant "hold in" current value to maintain a constant magnetic field and to hold the armature in the final position. This principle does not take in the consideration temperature and other variations due to ageing of the moving section, etc. In the paper a new concept with current tracking during the PWM "ON" phase is presented, focusing on the current measuring principle. The track record, called coil "signature," provides data for smart current driving, which is also described in the paper together with simulation results, main layout considerations, and some measurements.**

***Keywords*— solenoid driver, current control, pulse width modulation, solenoid signature**

I. Introduction

Solenoids are used for many applications, i.e. fluid dispenser, valve, magnetic switch, etc. For solenoid driving mainly pulse-width-modulation (PWM) signals are used [1, 2, 3], and rarely is direct current (DC) driving applied [4]. The PWM signal from the central processing unit (CPU) and its duty cycle determine the value of the current through the solenoid coil, which causes the armature movement.

Due to the tendency to minimize power consumption, especially in the automotive industry [1, 3, 4, 5], many solutions were proposed [6, 7, 8]. A high current is needed to move the armature into the coil, or when the solenoid goes in the "ON" state, but after the movement inductance of the solenoid is changed the current can be reduced. Knowing the exact position of the armature is important for determining the right moment to change the current value.

The armature position is also defined by the change of the solenoid inductivity; the method is based on decay time measuring when applying the reference current [9] and when the reference current is turned off. The time difference gives the information of the armature position. An advanced approach with two reference currents is used in some applications [2, 10] for "OFF" and "ON" state of the solenoid, decay times are measured, and their ratio calculated. From the ratio, the state of the armature can be defined. An electric model for an ABS solenoid driver was presented [1], with good physical modelling of the solenoid valve, and several modelling technique descriptions. The model is built on the prediction of correct operation of the solenoid valve with a no error handling solution and with no online armature position tracking.

As the solenoid current value directly influences the automotive battery discharging and therefore the battery charge, smart driving is important to achieve optimum battery performance. One of the solutions [11], proposes smart solenoid driving with online solenoid voltage adjustment. The main problem of such a solution is the lack of the solenoid armature position information. In case of the resistance change due to the ageing or some other deficit, the current would be still delivered to solenoid and no reaction with e.g. error message or turning off the device would happen. In the paper the method for the solenoid current measurement is proposed, without an expensive shunt resistor, but with voltage drop sensing on the driving transistor channel [12]. Error in the armature movement is registered online and the driver reacts accordingly to the information stored in the memory or according to the central process unit (CPU) instructions. In the paper block diagram of the circuit, the principle of operation, measurement technique, and main layout guidelines are discussed.

II. Principle Of Operation

The function of the solenoid current level versus time Is(t), during the "ON" phase, provides the information about the coil resistance and inductance.

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The coil current values and its curve shape is used in the algorithm which adapts the target driving current for optimal operation with minimal thermal losses and minimized power consumption.

For the precise study of inductance change due to the armature movement, measurements were taken with a commercial solenoid. The schematic, shown in Fig. 1 presents the proposed solenoid driver architecture – application-specific integrated circuit (ASIC).

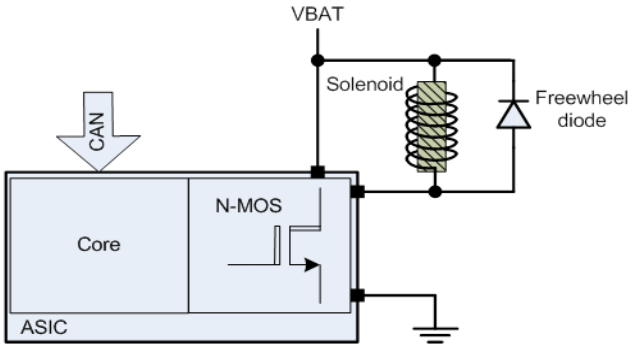

Fig. 1. Architecture of solenoid driver ASIC

The main part of the schematics is N-MOS block, which consists of multiple PWM-driven N-MOS transistors. The request for activation of the solenoid comes via the data bus from the central processing unit. The core reacts according to data stored in the memory. Required current values and other parameters such as solenoid driver current values are stored in the solenoid test phase in the memory. The coil current value is proportional to the main parameters as the duty cycle of the PWM signal, battery supply voltage, and solenoid temperature. But, there are also other parameters which can change and influence solenoid operation, such as the solenoid return spring ageing and environmental changes (dirt and moisture). The exact solenoid movement tracking is important to prevent false operation, and so safety loss or unnecessarily high power consumption.

III. Structure Of Solenoid Driver

The proposed solenoid driver ASIC consists of four main blocks – the Reference Current generator, PWM generator, R-block, and P-block. Additional blocks such as the Timer/clock, Control block, and Signal processing are necessary for monitoring the result and correct timing. The structure of the driver ASIC is shown in Fig. 2.

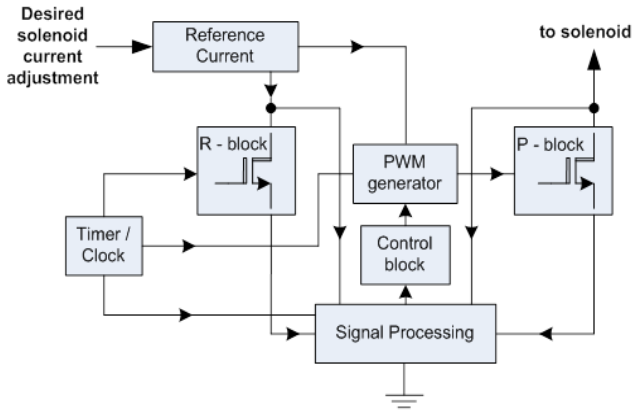

Fig. 2. Block diagram of the solenoid driver ASIC

Initially, the output current adjustment is done in the Reference current block, which sets the reference current and transistor area in R / P - blocks. As the mirroring ratio remains the same regardless of the current level setting, also the current density remains constant, and so mirroring error is minimized. The reference current can be set in various ranges depending on the application (solenoid properties). The initial value of the PWM frequency is set to 4 kHz and can be adjusted as well.

The driver starts with a 50% duty cycle PWM and operates in a closed loop due to the result of the comparison between the reference and measured power transistor currents.

The current through the solenoid is driven by the PWM signal. The current through the N-MOS driving transistor flows only during N-MOS "ON" phase, therefore the values are sampled in this phase. The average coil current depends on the duty cycle. As supply voltage, temperature, etc., changes during operation, the ASIC core reacts by the duty cycle adjustment to maintain the required average coil current value.

For precise and real time current adaptation, measuring must be done online during operation, and the current value – the PWM width changed accordingly. This value can be obtained by measuring voltage drop on external resistor [9], or as proposed in this paper, by measuring the current value directly in the transistor block. Therefore, the N-MOS block is divided into two parts, as shown in Fig. 2. The schematic of both blocks merged together is shown in Fig. 3.

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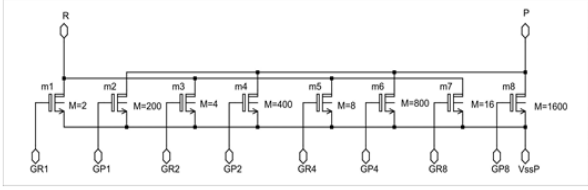

Fig. 3. Block diagram of the solenoid driver ASIC

In the Fig. 3, two groups of the transistors are shown (R-block and P-block). The first group is reference transistors and are connected between **R** and **VssP** pins. They are controlled by inputs named *GRx*. The second group consists of power transistors and are connected to the **P** pin and **VssP**. The power transistors are controlled by inputs *GPx*. The schematic is quite simple and includes geometry factors M. The main advance of this block is in layout realization. The transistors are merged in schematics to reflect the importance of the correct positioning in the layout, where an interdigital and centroid layout is a must.

IV. Reference And Solenoid Current

During the "ON" phase both reference and power blocks are active. Current flows through reference transistors controlled by *GR* inputs. The reference current value is set according to solenoid resistance and the target power current. The current ratio between the reference and power blocks is R : P = M. The main and most important issue is to provide an equal current density through the reference and power transistors to achieve good matching conditions. If this is fulfilled, the following equations can be written:

$$j_P = j_R \quad (1)$$

$$A_P = M * A_R \quad (2)$$

$$I_P = M * I_R \quad (3)$$

Where in (1) $\mathbf{j_P}$ and $\mathbf{j_R}$ are power and reference current densities, in (2) $\mathbf{A_P}$ and $\mathbf{A_R}$ are areas of power and reference transistors, and in (3) $\mathbf{I_P}$ and $\mathbf{I_R}$ are currents through power and reference transistors. The power current can be controlled by observing the voltage drop on the power transistor, the voltage drop on the reference transistor, and adjusts regarding their ratio with PWM width change, and so the power current value. In this process a careful and precise layout is crucial.

In Tab. I the reference current adjusting bits and their influence on solenoid current are shown.

It can be noticed in Tab. I, that the M factor is kept constant, therefore the current densities are constant, but the reference current changes from 1.6mA to 24mA, and the solenoid current from 160mA to 2.4A, respectively.

Table I
Reference And Power (Solenoid) Current Ratio With Adjusting Bit Change

No.	Adjusting Bits				Iref	Isol	Transistor Ratio
	3	2	1	0	[mA]	[mA]	R : P = M
1	0	0	0	0	0	0	-
2	0	0	0	1	1.6	160	1:100
3	0	0	1	0	3.2	320	2:200
4	0	0	1	1	4.8	480	3:300
5	0	1	0	0	6.4	640	4:400
6	0	1	0	1	8	800	5:500
7	0	1	1	0	9.6	960	6:600
8	0	1	1	1	11.2	1120	7:700
9	1	0	0	0	12.8	1280	8:800
10	1	0	0	1	14.4	1440	9:900
11	1	0	1	0	16	1600	10:1000
12	1	0	1	1	17.6	1760	11:1100
13	1	1	0	0	19.2	1920	12:1200
14	1	1	0	1	20.8	2080	13:1300
15	1	1	1	0	22.4	2240	14:1400
16	1	1	1	1	24.0	2400	15:1500

The key issue at the mirroring principle, is the V_{DS} voltage of the reference and power transistors must be kept equal to achieve good current matching.

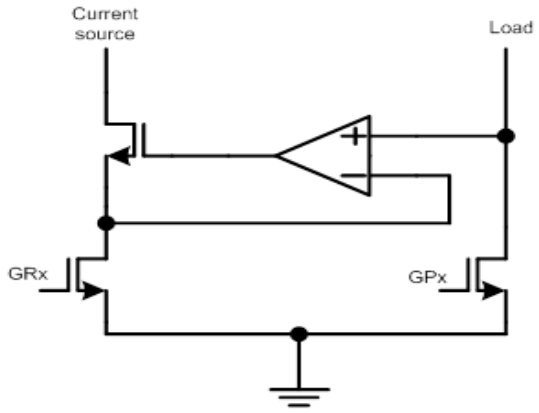

Fig. 4. Circuit schematic for VDS equalization

Therefore, a special circuit was added to measure and be equal. A simplified schematic to achieve it is shown in Fig. 4.

The most advanced solenoid drivers apply two levels of current for operation [6, 8, 9]. The initial current level is the so called "pull-in" current which is needed to pull-in the armature.

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This current has higher values, but it is needed only for a short time, until the armature does not reach its final position. The second current is the "hold-in" current, which has a lower value and is only used for holding the armature in its final position. The ASIC core or external CPU must decide, how long the pull-in current needs to flow, which means a wide PWM, and when it must change to a hold-in current – with a narrow PWM. Normally this is done with timers or in some advanced solutions [6], by measuring the current indirectly, as voltage drop on the resistor. The main problem of all methods and realizations is that there is no information of the actual position of the armature.

The smart driver solution presented in the paper considers the shape of the current curve through the coil and initially memorizes the "virgin" curves of the current during the setup mode, called the coil "signature" [10, 12, 13]. In normal operation the driver compares the virgin curves of the current with the actual current shape during the armature transition.

V. Solenoid Signature And Sampling

A sampling circuit stores one reference transistor voltage drop sample and two power transistor voltage drop samples. This is sufficient for the average voltage calculation and basic signature capture-detection of the angle of rising current.

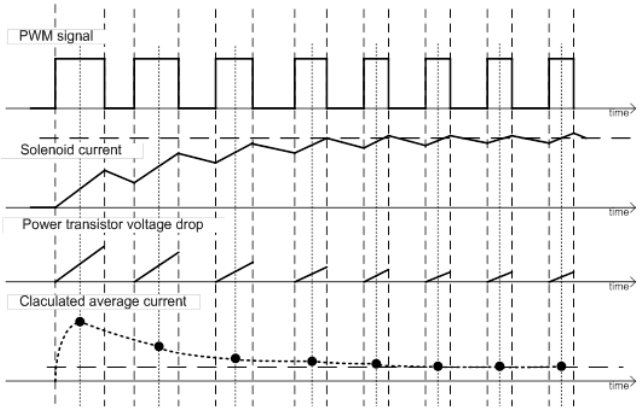

Fig. 5. Solenoid "pull-in" current transient

If necessary, more samples can be used. In Fig. 5a typical startup of the proposed solenoid driver is presented.

Trace 1 presents a PWM signal which controls the power gate, on the second trace preset value of the solenoid current (dashed line), and the actual solenoid current is shown. On the power transistor voltage drop, proportional to solenoid, the current appears and is shown on the third trace.

They are sampled at the beginning and end of the "ON" phase and the average is calculated and presented on fourth trace. The average value of the reference transistor voltage drop (dotted line) converges to the constant value of the reference transistor voltage (dashed line). With data gathered from this measurement, prediction of the future behavior can be done, and error in the armature movement can be detected. Each solenoid type has its unique parameters which reflect in its signature – in this case the signature is the unique average current change within the armature movement.

For sampling and information storing a microcontroller can also be used, in that case the detailed signature can be captured. From the stored data, a precise current average value can be calculated, position of the solenoid armature in real time and its movement trajectory. The unique signature shows a nonlinear current curve in the PWM "ON" phase. This also brings new facts about solenoids and other inductive loads.

VI. ASIC Simulation Results

The transient response time and magnitude of the solenoid current depends on the PWM duty cycle, resistance, and inductance of the solenoid. Fig. 6 presents signals for solenoid with 8Ω resistance and 1mH inductance. For operation, a so-called 'freewheel' diode is connected parallel to solenoid (shown in Fig. 1), to allow current flow during the PWM "OFF" mode.

On the first trace solenoid current, which settles around 1.28A is presented. The second trace shows the result of two sampling points –point **A** at the beginning of the solenoid "ON" time and point **B** at the end of the solenoid "ON" time. Then the average is calculated using a simple analog circuit, and is presented as a *V(Iavg)* signal on the middle trace.

The sampled reference transistor voltage drop is constant, at the end average and reference voltage are almost equal. The third trace shows the outputs of the digital control block. The bottom trace shows the 4kHz PWM signal starting at the 50% duty cycle and ending at 87%.

The PWM duty cycle is generated by comparison of the resulting average voltage to the reference. The resulting average voltage is the analog equivalence of the control block state. The PWM duty cycle depends on result of the calculation of the embedded algorithm which is described in the next section, where the reference transistor voltage drop and power transistor voltage drop sampling are explained.

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In Fig. 7 one of the PWM phases is shown. In the top trace nonlinear current of the solenoid is presented. This unique solenoid current curve can be sampled, and the whole movement of the armature can be stored in ASIC memory.

Later, it can be compared to the new armature transition, when the solenoid is activated again and checked for anomalies – errors online. If all samples from beginning of armature movement to the armature end position are stored, the exact armature position can be easily determined.

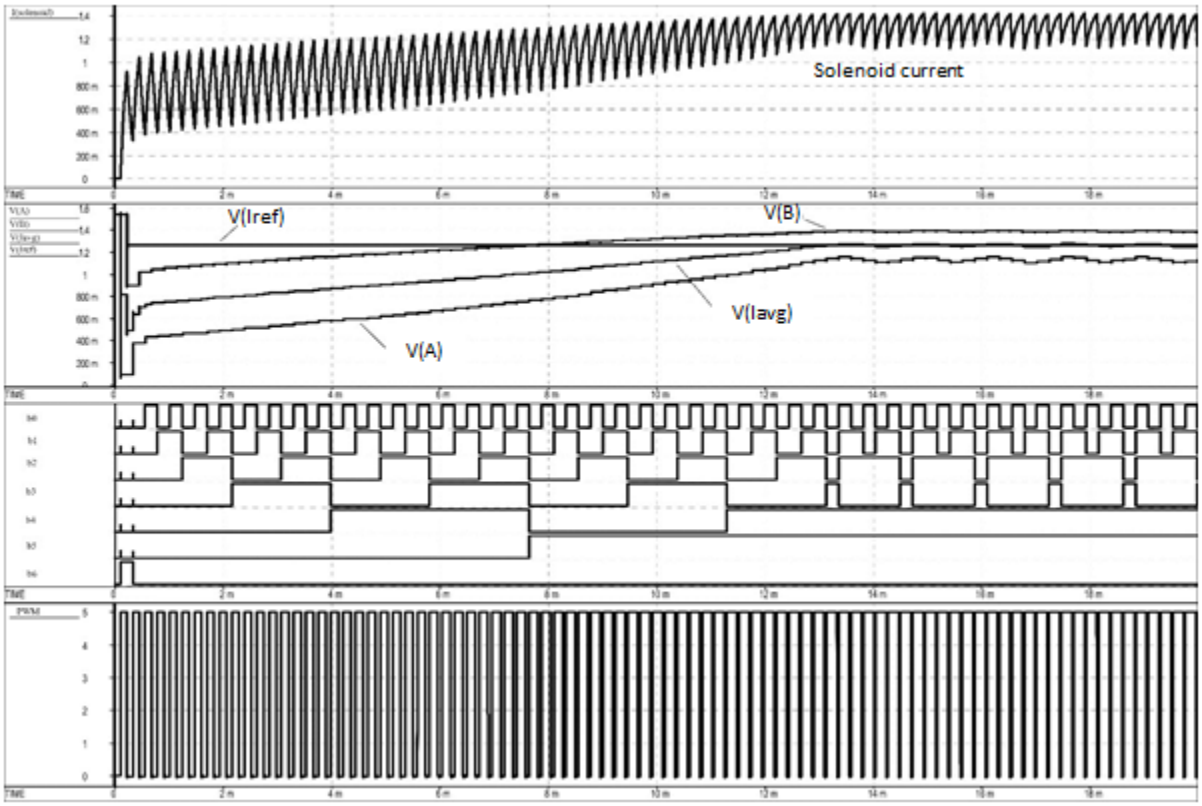

Fig. 6. Simulation result of the ASIC operation

The second trace presents three sampling points *sp1*, *sp2*, and *srv* used for the main sampling and then delayed signals *sp1d*, *sp2d*, and *srvd* for data storing. At the beginning of the PWM "ON" state, sampling signals *sp1* and *sp1d* are active. At the *sp1* moment, the power transistor voltage drop is sampled and the resulting voltage **A** is stored on the capacitor **c1** when *sp1d* is high. A similar operation follows when the *sp2* occurs at the end of PWM "ON" state. The power transistor voltage drop is sampled again, and when *sp2d* is high voltage value is stored on **c2** as voltage **B**. The reference transistor voltage drop is sampled in the middle of the PWM "OFF" state to minimize the influence of transients.

Two sample signals *srv* and *srvd* sample and store the reference voltage value **R**. Later on, the analogue subcircuit calculates the average voltage value of solenoid current from stored voltages **A** and **B**, which is used for comparison with reference voltage **R**. The embedded algorithm in the ASIC ensures closed loop operation, which includes the PWM signal duty cycle control, to reach minimal difference. The minimal difference or power current error is determined by reference current adjustment step and mismatch error of the current mirroring principle. Therefore, again the precise layout is very important.

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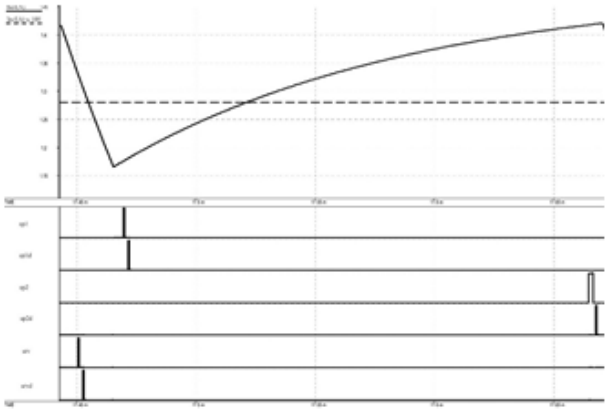

Fig. 7. Magnetizing curve of the solenoid and sampling signals

VII. Optimized Layout

In the layout, each parasitic voltage drop, caused by current flowing through supply metal lines, influences the final precision and matching between the power and reference transistor. So, power lines must be designed carefully as shown in Fig. 8.

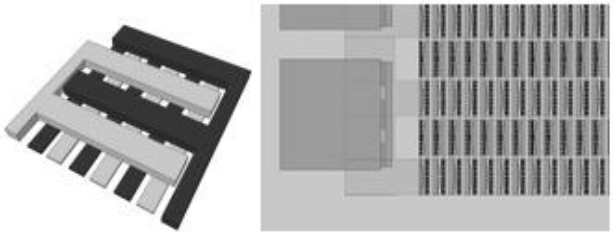

Fig. 8. Metal lines - schematics and layout

The left side of the Fig. 8 presents ground connections with grey lines and black lines – positive battery connections. Together they present a power mesh which evenly distributes current and so minimizes parasitic voltage drops and improves matching. On the right side, the layout of the power mesh is presented. On the left side of the layout ground pads can also be seen. The figure presents only part of the power transistor block. The N-MOS block is presented in Fig. 9. The power transistor block and its transistors are distributed in two parts, separated with the middle part where the reference transistors are positioned. Therefore, power and reference transistors have the same conditions, which also minimize mismatching error.

In the layout, on the left side are ground **VssP** pads, and on the right side are power **P** connections. On the top – is reference pad **R** in the middle.

At layout generation a special technique was used. Total area of this block is only 825µm x 1355µm, which is nearby half of the area needed if a standard layout would be applied. As the transistor block is horizontally divided in two symmetrical parts, in the vertical direction there are multiple transistors distributed as shown in the distribution of transistor map on the right side of Fig.9.

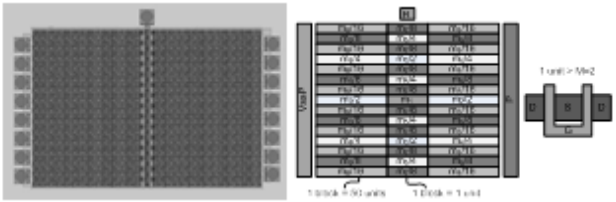

Fig. 9. Layout of N-MOS block and distribution of transistors map

Units and block are marked as in Fig. 3 with same transistor names. Transistors are distributed regarding current mirroring and area, to achieve constant current density. So, this distribution is very complex and good power distribution and matching was achieved, and also *rds* ON resistance is minimized.

VIII. Measurement Results

An integrated circuit was fabricated and characterization of proposed current measuring principle in the solenoid driver. The layout of the circuit is presented in Fig. 9. The solenoid current is driven with a 4kHz PWM signal, and its value was observed only during the PWM "ON" phase. The first measurement shows the influence of the supply voltage influence on the PWM duty cycle. The oscillograph with the change of duty cycle for constant solenoid current is shown in Fig. 10.

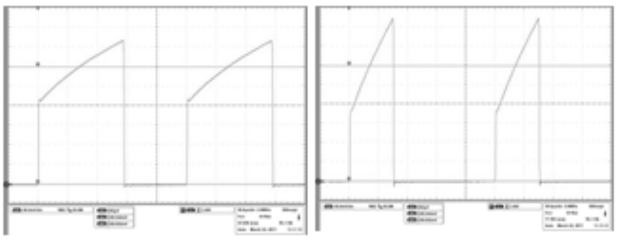

Fig. 10. Duty cycle change due to supply voltage change

The left oscillograph in Fig. 10 presents solenoid driving transistor current at the minimal operation supply voltage with a 60% duty cycle. When the supply voltage is doubled the duty cycle drops to 30% to maintain the same solenoid current value, shown on the right oscillograph.

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As the solenoid uses copper winding, its resistance changes approximately 30% per 100°C or in the required temperature range from -40°C to 120°C for +48% of the value at -40°C. ASIC core regulations cover a complete range of the solenoid resistance variations and the regulation algorithm is complex, as also supply voltage, temperature etc., can vary during operation. The ASIC or microcontroller reacts to the mentioned variations by the duty cycle ratio, and maintains the constant coil current value independently.

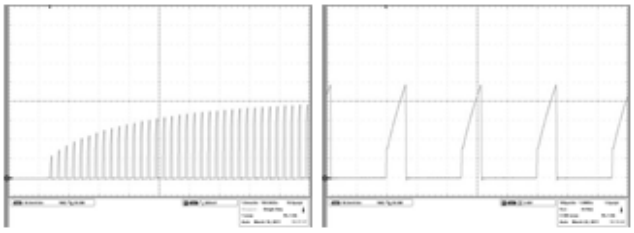

Fig. 11. Solenoid start and normal operation

Fig. 11 presents driving transistor current pulses. On the left oscillograph, startup of the solenoid can be observed, with a transient needed for solenoid core magnetizing. On the right oscillograph normal operation after current stabilization is shown. The current has close to linear curve during "ON" phase; its angle depends on the supply voltage and solenoid inductance.

IX. Coil Signature Measurement

The coil signature can be obtained by observing the slopes of the current through the coil when the armature moves into the solenoid coil. At the beginning, the curve has the highest slope when the armature is outside the coil, and at the end when armature is fully inside, curve has the lowest slope. The angle change is the result of coil inductance change, depending on the percentage of the inserted armature. If the slope is calculated at every PWM pulse, the information of the armature position can be obtained. The solenoid current shape at different armature positions is presented in Fig. 12.

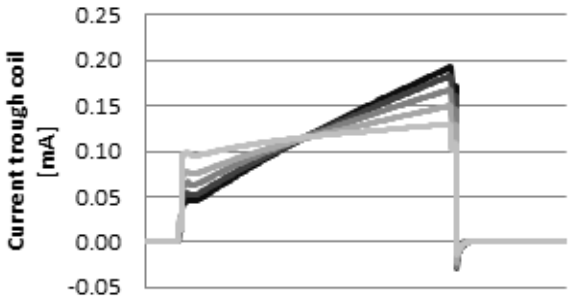

Fig. 12. Measured solenoid current shape and value at different armature position

The curves of the certain armature position are coded with different color gradient – dark stands for the initial armature position outside of the coil, and bright for the final armature position inside of the coil. Each gradient step shown presents approximately 20% of armature position change toward the solenoid's final position.

As measurements were done at each repetitive PWM signal with no omitted period, the nonlinearity of angle change can be noticed (as changes of angle is not equidistant). From this and several different "signatures" the obstacles on the armature route are detected, or in marginal cases malfunction or error detected.

X. Conclusions

In the paper a novel principle for solenoid driver was presented with a new feature called "solenoid signature." A basic block diagram of fabricated ASIC, together with some simulation results, principle description, and measurement results were given. The results confirm the usability of the proposed algorithm, but it also leaves the system open to other solutions with microcontroller usage, but still using the proposed principle. To summarize – as a novelty capturing the value of current in at least two points and storing the values in the memory as part of "signature" of a specific solenoid were presented. If this is done for the complete "pull-in" phase at the first use of the solenoid, the data presents a "virgin signature," where from all necessary information about armature movement and position can be calculated with a comparison of the stored data with online data during normal solenoid operation.

The proposed signature capture brings new opportunities of solenoid usage, and for smart & safe operation of the solenoid systems in automotive and other safety critical applications.

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