

Comparison of Intrinsic Energy Losses in Unipolar Power Switches

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Abstract—We explore the intrinsic loss in power switches seen when they undergo charging and discharging of their output capacitance. The intrinsic loss occurs even if switching is carried out at zero current and no on-state current is conducted, and accidental turn-on is avoided. The intrinsic loss cannot be eliminated by using soft-switching schemes and essentially sets an upper limit for the switching speed of the soft-switching converters.

This work measures and compares the intrinsic energy losses in the popular commercial unipolar power switches including Si superjunction MOSFETs, GaN cascode, SiC cascode, and SiC MOSFETs. The intrinsic loss mechanisms of these devices are also discussed. A simple experiment setup is proposed and used to measure the intrinsic energy losses. The experimental results show that the SiC cascode has the lowest intrinsic energy loss.

Keywords—superjunction; cascode; MOSFET; SiC; GaN; energy loss; soft switching converter

I. INTRODUCTION

Power switches are key components of power converters and basically determine the overall performance of the converter, such as efficiency, switching speed, power density, as well as cost. The most important parameters of a power switch are the conduction loss and switching loss. For unipolar switches such as MOSFET and JFET, the conduction losses stem from the finite on-resistance of the switch. The conduction loss can be reduced by increasing the size of the power chips or by paralleling more power chips. Switching loss is caused by the finite switching speed of the device leading to a crossover of the switch voltage and current during switching transients. Soft switching techniques have been developed to avoid the crossover of the switch voltage and current during switching transients, which can substantially reduce or even completely eliminate the switching losses of the power switches. The basic concept of the soft switching techniques is to turn on the switch when the switch voltage is zero (ZVS), and turn off the switch when the switch current is zero (ZCS). Soft switching converters require more complex circuit topologies and gate drive controls, but can achieve very high efficiencies at very high switching speeds. Soft switching techniques are essential for realizing next generation power converters targeting for high switching frequency ($>1\text{MHz}$) and high power density ($>150\text{W/in}^2$) [1].

Recent efforts [2,3] have clarified that power switches have a third type of energy loss that is called “intrinsic energy loss” in this paper. The intrinsic energy loss is caused by the internal structure of the switch and occurs during the voltage charge-discharge cycle, even when this is done at zero current. The intrinsic energy loss is usually much smaller than switching energy losses and conduction loss and, therefore, is neglected in the design of hard switched modern power converters. However, this intrinsic energy loss cannot be eliminated or reduced with soft-switching approaches and become increasingly important as the switching frequency increases. The intrinsic energy loss of these power switches will eventually set an upper limit for the switching speed of the next generation high-frequency power converters.

The advent of wide bandgap power devices provides more choices of high-performance power switches. At present, there are four types of power switches on the market suitable for high-frequency and high-power density power conversion applications. They are Si Superjunction MOSFET, GaN cascode or GaN enhancement HEMT, SiC cascode and SiC MOSFET. Even though it is very important for high-frequency power conversion applications, the intrinsic energy loss is not presently stated in the device datasheets. The intrinsic losses of Si superjunction MOSFET and GaN cascodes have been reported [2, 3]. But no experimental results have been published about the intrinsic losses of SiC power switches. The purpose of this work is to measure and compare the intrinsic losses of the commercial available power switches and provide helpful information on selecting power switches for next generation power converters.

II. EXPERIMENTAL SETUP

Fig. 1 shows the experimental setup proposed for measuring the intrinsic loss of a power switch. This is a resistive load switching circuit with a high-side switch. R_L is the load resistor. The device under test (DUT) is kept in off-state by shorting the gate and source terminals.

When the switch is turned on, the output capacitance C_{oss} of the DUT is charged to the DC bus voltage through the switch, and the resistors R_1 and R_s . When the switch is turned-off, the C_{oss} of the DUT is discharged to the ground potential through the resistor R_s , the diode D_1 , and the load resistor R_L . To make the charging and discharging paths have the same resistance, R_1 is chosen to be the same as R_L , and R_1 is bypassed by the diode D_1 during discharging period.

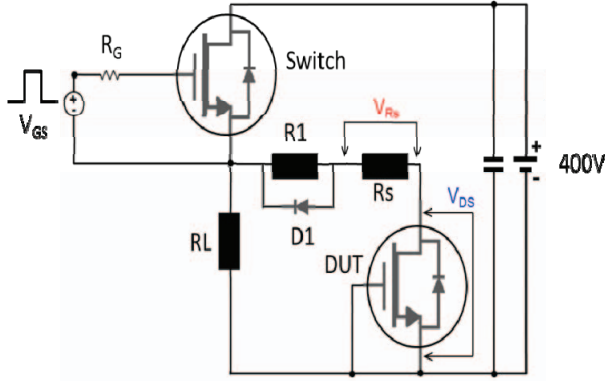


Fig. 1: Experimental setup for measuring the intrinsic loss of a power switch.

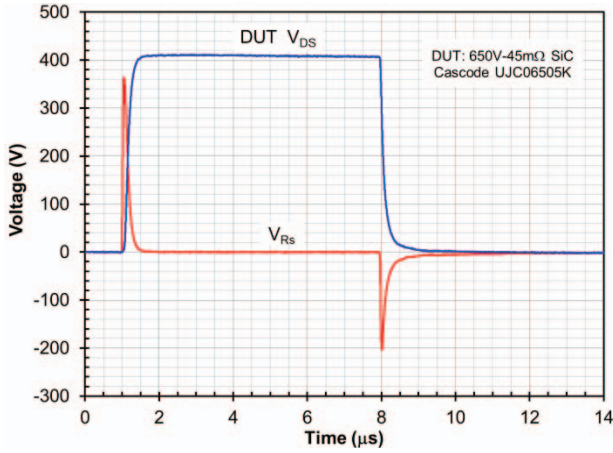


Fig. 2: Measured waveforms of the DUT drain voltage and the voltage across R_s .

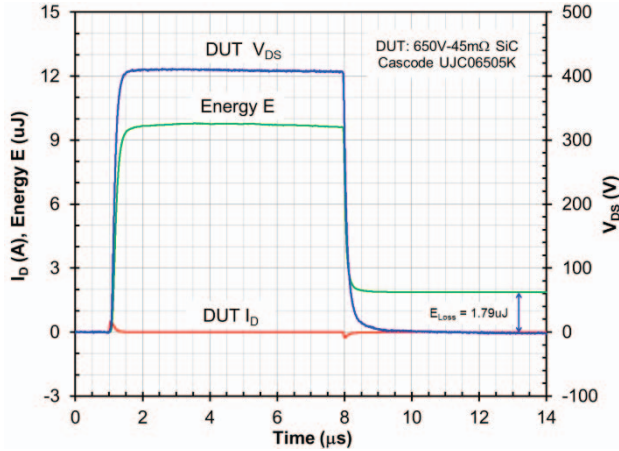


Fig. 3: Energy and DUT current waveforms obtained from the voltage waveforms in FIG. 2.

The drain current I_D of the DUT during the charging and discharging processes is monitored using the current sensing resistor R_s . The voltage across R_s (V_{RS}) is measured with a differential voltage probe. Then, the DUT current I_D is given by the following equation:

$$I_D = V_{RS} / R_s \quad (1)$$

The drain voltage V_{DS} of the DUT during the charging and discharging processes is measured with a single-ended voltage probe. A single pulse is used for the measurement. The pulse width should be wide enough to allow the charging process to finish. All experiments are performed at room temperature with a DC bus voltage up to 400V.

Fig. 2 shows an example of the measured voltage waveforms for a 650V-45mΩ SiC cascode (UJC06505K). The charging process starts at $t = 1\mu s$. During the charging process, a positive voltage pulse is observed across the current sensing resistor R_s , indicating a displacement current flowing through the DUT from the drain terminal to the source terminal to charge the C_{OSS} of the DUT. Once the charging process ends at $t = 1.6\mu s$, the drain voltage V_{DS} of the DUT reaches the DC bus voltage and the voltage V_{RS} of the current sensing resistor R_s becomes zero.

The discharging process starts at $t = 8\mu s$. During the discharging process, a negative voltage pulse is observed across the current sensing resistor R_s , indicating a displacement current flowing through the DUT from the source terminal to the drain terminal to discharge the C_{OSS} of the DUT. Once the discharging process ends at $t = 12\mu s$, the drain voltage V_{DS} of the DUT reaches the ground potential and the voltage V_{RS} of the current sensing resistor R_s becomes zero.

Fig. 3 shows the energy and current waveforms obtained from the voltage waveforms in Fig. 2. The DUT drain current I_D is calculated with the equation (1). The energy E is computed by integrating the product of V_{DS} and I_D over the time. It is seen that, after a full cycle of charging and discharging of the C_{OSS} of the DUT, the energy is not zero but a positive value of 1.79μJ, indicating a power loss.

It is seen from Fig. 2 that the drain-source voltage V_{DS} of the DUT is always positive, meaning the built-in body diode is never conducting during the whole switching event. Therefore, there is no diode conduction loss involved in the experiment. In addition, the leakage current of the DUT is less than 2μA at 400V, thus, the leakage current related energy loss is less than 0.0057μJ, which is much smaller than the energy loss shown in Fig. 3. Therefore, the energy loss shown in Fig. 3 is the device structure related intrinsic loss. With this approach, the intrinsic losses of the commercial available 650V class power switches are measured and presented in the next section.

III. EXPERIMENTAL RESULTS

Table 1 lists the commercial 650V-class unipolar power switches investigated in the work. The devices are divided into three groups: Si superjunction MOSFET (SJ-MOSFET), Cascode, and SiC MOSFET. The typical on-resistances of the devices from the datasheets are included in the Table 1. It is seen that these devices have different on-resistances. In order to make comparisons, the measured intrinsic energy loss E_i is normalized to the typical on-resistance $R_{on,typ}$ of the device as follows:

$$FOM_{Ei} = E_i \times R_{on,typ} \quad (2)$$

Where, FOM_{Ei} is the normalized intrinsic energy loss which can be used as a Figure-of-Merit for benchmarking the intrinsic losses.

TABLE I. COMMERCIAL 650V CLASS POWER SWITCHES EVALUATED IN THIS WORK

Part #	Descriptions	Voltage Rating	$R_{on,typ}$ @ RT
<i>Si Superjunction MOSFETs</i>			
IPW65R045C7	CoolMOS C7 series	650V	40mΩ
FCH041N65F	SuperFET II FRFET	650V	36mΩ
IXFK80N65X2	X2-Class HiPerFET	650V	33mΩ (measured)
STW62N65M5	MDmesh M5	650V	41mΩ
<i>Wide Bandgap Cascodes</i>			
UJC06505K	SiC Cascode	650V	34mΩ
TPH3205WS	GaN cascode	650V	52mΩ
<i>SiC MOSFETs</i>			
C3M0065090D	New C3M technology	900V	65mΩ
SCT2120AF		650V	120mΩ

A. Si Superjunction MOSFETs

Fig. 4 presents the measured normalized intrinsic energy losses FOM_{Ei} and fitted trend lines of the Si superjunction MOSFETs as a function of the DC bus voltage. FCH041N65F and IXFK80N65X2 have about the same FOM_{Ei} for the DC bus voltages up to 250V. After 250V, the FOM_{Ei} of IXFK80N65X2 increases faster than that of FCH041N65F. The FOM_{Ei} of IPW65R045C7 increases almost linearly for the DC bus voltages up to 250V and tends to saturate after 250V. STW62N65M5 shows the largest intrinsic energy loss, which increases quickly as the DC bus voltages is elevated to 200V and tends to saturate after 200V.

The physical mechanism of the intrinsic energy losses of Si SJ-MOSFETs has been discussed in [4]. It is believed that the free carriers (electrons or holes) isolated in the depleted drift region cause the intrinsic energy loss in SJ-MOSFETs. Fig. 5 shows the TCAD simulated space-charge distribution in the drift region of a Si superjunction PN diode under a reverse bias. Because the doping concentrations in the p-columns and n-columns are not uniform, there exist isolated un-depleted regions in the p-columns that contain free holes, and isolated un-depleted regions in the n-columns that contain free electrons. These isolated regions are surrounded by the high resistance depleted regions. When the reverse bias is further increased, some of the free carriers in the isolated un-depleted regions must be removed in order to widen the depletion regions to support higher voltage. The removed free carriers must go through the high-resistance depleted region and generate Joule heat, resulting in energy losses.

To reduce the intrinsic loss in SJ-MOSFETs, the doping concentrations in the n-columns and p-columns must be made uniform to avoid isolated up-depleted regions. The popular techniques used to create p and n columns are multiple-epitaxy and trench-filling methods. The trench-filling MOSFET, in general, has more uniform doping concentrations in the n-columns and p-columns than the multiple-epitaxy MOSFET, and therefore has low intrinsic energy loss.

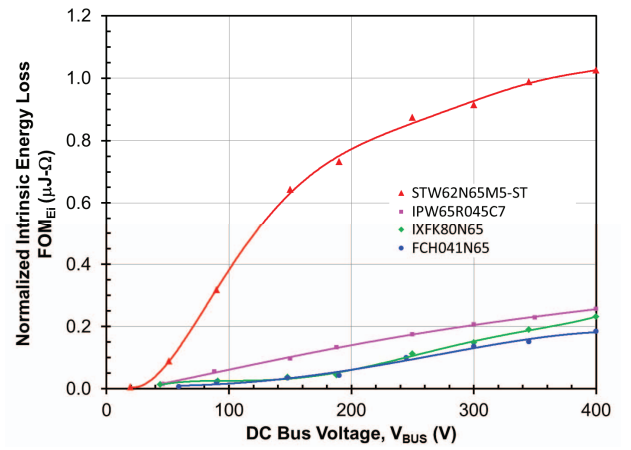


Fig. 4: Measured intrinsic energy losses and fitted trend lines of the Si superjunction MOSFETs at different DC bus voltages.

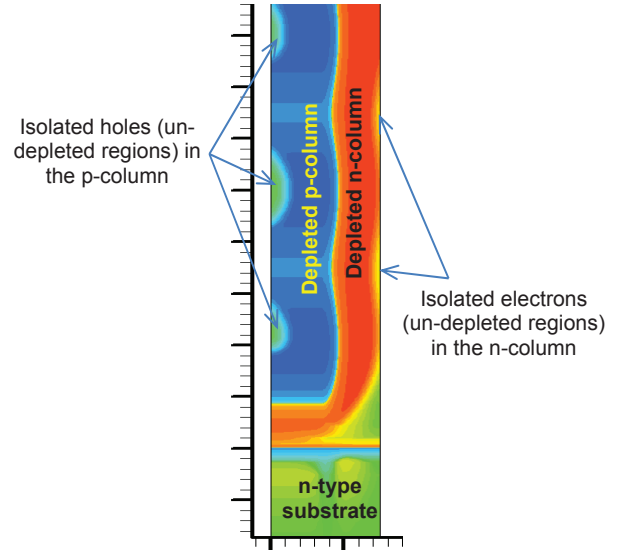


Fig. 5: TCAD simulated space charge distribution of a Si superjunction PN diode under a reverse bias.

B. Wide Bandgap Cascodes

Fig. 6 shows the measured normalized intrinsic energy losses FOM_{Ei} and fitted trend lines of the SiC cascode UJC06505K and GaN cascode TPH3205WS as a function of the DC bus voltage. Both cascodes have similar energy loss at the DC bus voltage less than 100V. When the DC bus voltage is greater than 100V, the energy losses of both cascodes increase, but the energy loss of the GaN cascode increases much faster than that of the SiC cascode. At $V_{BUS} = 400V$, the energy loss of the GaN cascode is more than 4X that of the SiC cascode.

Two different mechanisms are probably responsible for the intrinsic energy loss of the GaN cascode [3]. One is the avalanche loss during turn-off transition when the low-voltage Si MOSFET is driven into avalanche. The other is the early turn-on loss during turn-on transition when the drain voltage of the low-voltage Si MOSFET is decreased to the threshold

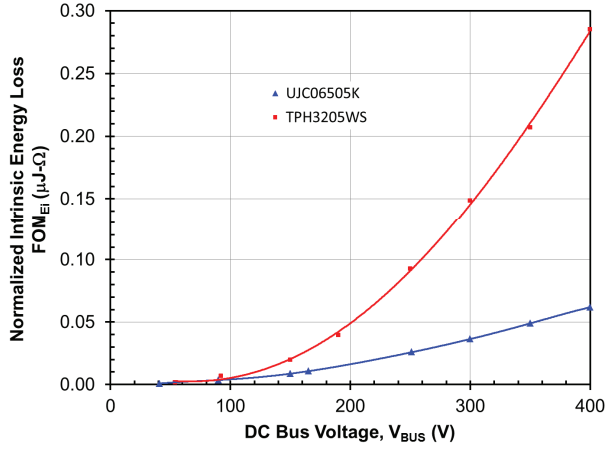


Fig. 6: Measured intrinsic energy losses and fitted trend lines of the SiC cascode UJC06505K and GaN cascode TPH3205WS at different DC bus voltages.

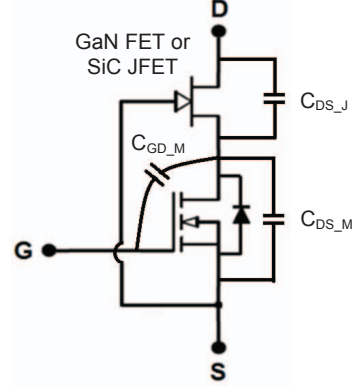


Fig. 7: Circuit schematic of a GaN or SiC cascode.

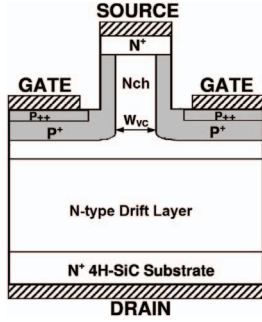


Fig. 8: Cell structure of the SiC JFET with a trench-and-implanted vertical channel.

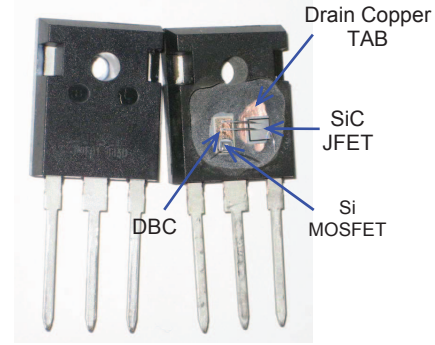


Fig. 9: Internal layout of the SiC co-packaged side-by-side cascode.

voltage of the GaN FET and the GaN FET is still supporting the high voltage. Both loss mechanisms are mainly caused by the charge balancing or voltage dividing effect between the drain-source capacitance C_{DS_J} of the GaN FET and the output capacitance C_{OSS} ($C_{GD_M} + C_{DS_M}$) of the Si MOSFET, as illustrated in Fig. 7.

In the SiC cascode UJC06505K, the SiC JFET used has a negligible drain-source capacitance because of its trench-and-implanted vertical channel structure as shown in Fig. 8. However, the TO-247 package of the cascode introduces a small capacitance between the drain and source terminals of the JFET because UJC06505K is a co-packaged side-by-side cascode as shown in Fig. 9. A DBC attached to the package drain tab is used to hold the Si MOSFET chip. The top surface of the DBC is connected to the source terminal of the JFET through wire-bonding and the bottom surface of the DBC is connected to the drain terminal of the JFET through the package drain tab. Therefore, the capacitance of the DBC will become the C_{DS_J} of the JFET. The capacitance of the DBC is very small and is not likely to cause the avalanche breakdown of the Si MOSFET during off-state or during turn-off transition. However, the early turn-on of the JFET during the turn-on transition is still possible depending on the threshold voltage and leakage current of the JFET.

C. SiC MOSFETs

Fig. 10 shows the measured normalized intrinsic energy losses FOM_{Ei} and fitted trend lines of the SiC MOSFETs SCT2120AF and C3M0065090D as a function of the DC bus voltage. It is seen that SiC MOSFETs also have an intrinsic energy loss. The intrinsic energy losses of SCT2120AF and C3M0065090D have similar trend and similar value even though these two SiC MOSFETs are from different manufacturers. The physical mechanisms of the intrinsic energy loss of SiC MOSFETs have not been reported so far. More experimental and theoretical work is needed in order to understand the physical mechanisms of the intrinsic energy loss in SiC MOSFETs.

D. Comparisons

Fig. 11 presents the measured normalized intrinsic energy losses of all of the power switches tested in this work. The DC bus voltage is 400V. It is seen that the SiC cascode has the lowest intrinsic energy loss, showing that the SiC cascode is the best potential power switch for use in the next generation high-frequency high-efficiency power conversion applications.

The GaN cascode has the second largest intrinsic loss, which may limit its applications in the ultra-high frequency

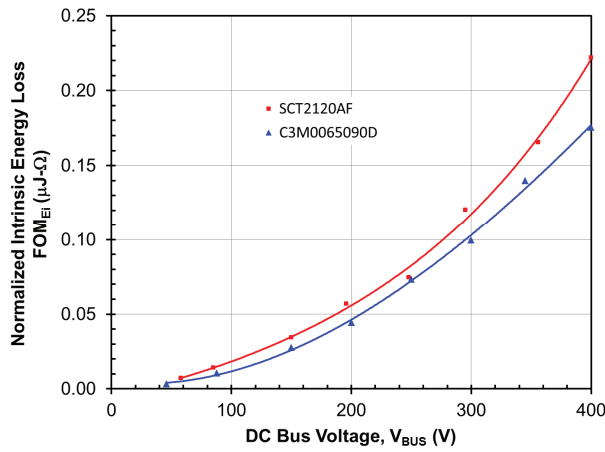


Fig. 10: Measured intrinsic energy losses and fitted trend lines of the SiC MOSFETs SCT2120AF and C3M0065090D at different DC bus voltages.

(>1MHz) power converters without further modifications. The GaN cascode has the same circuit topology as the SiC cascode. However, the GaN FET has a large drain-source capacitance, which forms a capacitive divider with the low voltage MOSFET[3], and leads avalanche energy loss in the low-voltage Si MOSFET. This is avoided in the SiC JFET cascode with a trench-and-implanted vertical channel, making it the ideal FET structure for constructing a cascode.

The Si superjunction MOSFET STW62N65M5 exhibits an extremely high intrinsic energy loss. Two samples of STW62N65M5 are tested and show the similar results, ruling out the possibilities of experimental error or bad devices.

IV. SUMMARY

This work proposes a simple experimental setup for evaluating the intrinsic energy loss of the power switches. The intrinsic losses of the commercial available 650V class power switches, including SiC cascode, GaN cascode, SiC MOSFETs, and Si superjunction MOSFETs, have been measured and compared. The measured results provide helpful

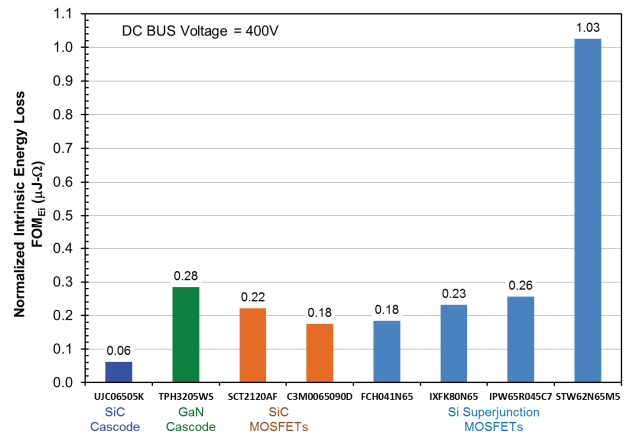


Fig. 11: Comparisons of the measured intrinsic energy losses of the commercial available 650V class power switches at a DC bus voltage of 400V at RT.

information for selecting power switches for high-frequency soft switching power converters.

The SiC cascode has the lowest intrinsic energy loss, showing great potential for next generation high-frequency and high-efficiency power conversion applications.

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