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FEEDFORWARD COMPENSATION OF THE AMPLIFIER OUTPUT STAGE FOR IMPROVED STABILITY WITH CAPACITIVE LOADS

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The stability margin of an audio power amplifier is reduced by a pole in the loop-gain transfer function caused by shunt capacitance in the loudspeaker load. The problem is most severe in amplifiers with output stages that have a high output impedance before feedback. Because MOSFET devices can have an output impedance that is much higher than BJT devices, amplifiers with MOSFET output stages are particularly susceptible to load induced oscillations. A feedforward frequency compensation technique is described which bypasses the pole in the output stage caused by the load capacitance for improved stability of the amplifier.

I. INTRODUCTION

Stability from oscillations is an important consideration in negative feedback amplifier design. Early researchers called the oscillation phenomenon "singing" [1], probably because oscillations in early vacuum tube amplifiers occurred at audible frequencies. Contemporary solid state amplifiers tend to oscillate at much higher frequencies. Even though these frequencies cannot be heard, the effects can be destructive. In particular, the failure of expensive power output transistors can occur.

The term "frequency compensation" refers to the design process used to prevent oscillations in amplifiers. The most commonly used methods are dominant pole lag compensation, reduction of the transconductance of the input subtracting stage, and lead compensation. The first two set the gain-bandwidth product and the slew rate of the amplifier [2]. The third is normally applied in the feedback network to correct for phase lag in the output stage. Because this lag is a function of the load impedance, lead compensation can be unreliable if the load impedance changes.

An amplifier can be stable when tested with a resistive load but can oscillate when the load presents a shunt capacitance. A shunt capacitance is present in all loudspeaker loads. Part of the capacitance is due to the interconnecting cable between the amplifier and the loudspeaker. For example, long cable runs in metal conduits are often encountered in public address systems which present a large load capacitance to the amplifier. Also, some special marketed loudspeaker cables use a geometry that can exhibit large shunt capacitance.

An amplifier can oscillate with a capacitive load when it is stable with a resistive load because the capacitance causes the addition of a pole to the loop-gain transfer function making the total phase shift in the loop large enough to satisfy the conditions for oscillations. To suppress this problem, a load isolating circuit that consists of an inductor or a parallel resistor and an inductor in series with the amplifier output is often used. The inductor can be expensive component, and it can decrease the amplifier damping factor.

This paper describes a feedforward compensation circuit which bypasses the output stage in an amplifier loop-gain transfer function at high frequencies. This decreases the effect of a pole in the output stage caused by a shunt load capacitance. The method can be particularly effective with output devices which have a relatively high output impedance, such as power MOS field-effect transistors. The higher the output impedance of the output stage devices, the lower the pole frequency will be with a given load capacitance, and the more susceptible the amplifier will be to oscillations.

II. THE FEEDFORWARD COMPENSATION CIRCUIT

Figure 1 illustrates the block diagram of an amplifier having an input stage and a power output stage, the latter having a gain k. A feedback network samples the high-frequency voltage from the input stage and the low-frequency voltage from the output stage. Because the high-frequency feedback is taken before the output stage, it follows that the high-frequency effects of load capacitance at the output of the amplifier will be isolated from the feedback input to the input stage. The network is said to be of the feedforward type because it takes the high-frequency signal from a point forward of the output node in the loop-gain transfer function.

If i_- is neglected, the node voltage equation at the v_4 node in Figure 1 is

$$v_4\left[\frac{1}{R_4}+\frac{1}{R_2+R_1\|(1/C_1s)}+\frac{1}{R_3+(1/C_2s)}\right]=v_2\left[\frac{1}{R_3+(1/C_2s)}\right]$$
$$+\,v_3\left[\frac{1}{R_1+R_2\|(1/C_1s)}\times\frac{(1/C_1s)}{R_2+(1/C_1s)}\right] \tag{1}$$

where the symbol $\|$ has been used to indicate the parallel combination of impedances. By superposition, v_4/v_2 can be solved for by setting $v_3 = 0$ in (1) and v_4/v_3 can be solved for by setting $v_2 = 0$. The following transfer functions are obtained:

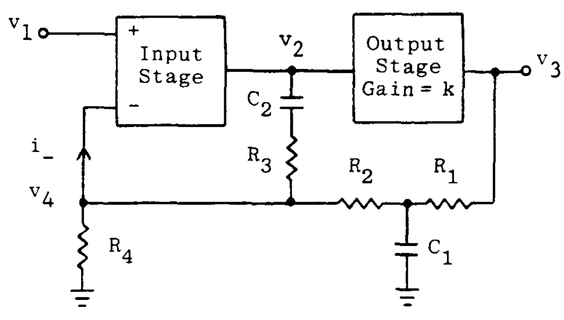

Figure 1. Block diagram of a feedback amplifier showing an input subtracting stage, an output stage having a gain k, and the feedforward feedback network.

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$$\frac{v_4}{v_2} = \frac{\dfrac{\tau_1 s}{1+\tau_1 s}}{\dfrac{R_3}{R_4} + \dfrac{R_3}{R_1+R_2}\,\dfrac{1+\tau_2 s}{1+\tau_3 s} + \dfrac{\tau_1 s}{1+\tau_1 s}} \tag{2}$$

$$\frac{v_4}{v_3} = \frac{\dfrac{R_3}{R_1+R_2}\,\dfrac{1}{1+\tau_3 s}}{\dfrac{R_3}{R_4} + \dfrac{R_3}{R_1+R_2}\,\dfrac{1+\tau_2 s}{1+\tau_3 s} + \dfrac{\tau_1 s}{1+\tau_1 s}} \tag{3}$$

where $\tau_1 = R_3C_2$, $\tau_2 = R_1C_1$, and $\tau_3 = R_1 \| R_2 C_1$.

For the feedback ratio to be the same at low and high frequencies, the following condition will be imposed:

$$\frac{1}{k}\frac{v_4}{v_2} + \frac{v_4}{v_3} = \frac{1}{1 + \dfrac{R_1+R_2}{R_4}} \tag{4}$$

Substitution of (2) and (3) into (4) yields after algebraic simplification

$$\frac{1}{1 + \dfrac{R_1+R_2}{R_4}\left[\dfrac{1 + \dfrac{R_4}{R_2}\dfrac{\tau_3 s}{1+\tau_3 s} + \left(1-\dfrac{1}{k}\right)\dfrac{R_4}{R_3}\dfrac{\tau_1 s}{1+\tau_1 s}}{\dfrac{1}{1+\tau_3 s} + \dfrac{1}{k}\dfrac{\tau_4 s}{1+\tau_1 s}}\right]}$$

$$= \frac{1}{1 + \dfrac{R_1+R_2}{R_4}} \tag{5}$$

where $\tau_4 = (R_1+R_2)C_2$. This can hold only if

$$1 + \frac{R_4}{R_2}\frac{\tau_3 s}{1+\tau_3 s} + \left(1-\frac{1}{k}\right)\frac{R_4}{R_3}\frac{\tau_1 s}{1+\tau_1 s} = \frac{1}{1+\tau_3 s} + \frac{1}{k}\frac{\tau_4 s}{1+\tau_1 s} \tag{6}$$

which yields the conditions

$$\tau_3 = \tau_1 \tag{7}$$

$$1 + \frac{R_4}{R_2} + \left(1-\frac{1}{k}\right)\frac{R_4}{R_3} = \frac{1}{k}\frac{R_1+R_2}{R_3} \tag{8}$$

In the audio band, the amplifier gain is set by R_1, R_2 and R_4. If the gain before feedback is large, the equation for this gain is

$$\frac{v_3}{v_1} = 1 + \frac{R_1+R_2}{R_4} \tag{9}$$

It thus follows that once R_1, R_2, and R_4 are selected for a desired gain, (8) can be used to solve for R_3. C_1 and C_2 can be solved for by specifying the break frequency between the two feedback paths.

When the condition of (7) is used in (3), it can be shown that (3) reduces to

$$\frac{v_4}{v_3} = \frac{1}{1 + \dfrac{R_1+R_2}{R_4}} \times \frac{1}{1 + \tau_5 s} \tag{10}$$

where τ_5 is the time constant given by

$$\tau_5 = \frac{R_1R_2R_4}{R_1+R_2+R_4}\,\frac{1}{R_2 \| R_3 \| R_4}\,C_1 \tag{11}$$

A specification of τ_5 in (11) can be used to determine C_1 and (7) can be used to solve for C_2.

III. EXAMPLE IMPLEMENTATION OF THE FEEDFORWARD CIRCUIT

The circuit in Figure 2 will be used to illustrate the feedforward technique. Transistors Q_1 through Q_4 implement complementary differential amplifiers which form the input subtracting stage. These drive the complementary common-emitter stages Q_5 and Q_6. The collector outputs of Q_5 and Q_6 are separated by a bias source which is represented in the circuit by a battery. It is common to use an active circuit such as a V-BE multiplier to implement this in an actual circuit.

The output stage consists of transistors Q_7, Q_8, M_1, and M_2. Q_7 and Q_8 are operated as complementary emitter followers to provide a low source impedance to drive the gate capacitance of M_1 and M_2. The latter are MOSFET devices which are operated as complementary source followers. MOSFET output devices have been selected over BJT devices because they exhibit a higher output impedance. This makes the circuit more susceptible to oscillations induced by a load capacitance. Both a load resistor and a load capacitor are shown connected to the output of the amplifier. The feedback network consists of resistors R_1 through R_4 and capacitors C_1 and C_2. It samples both the voltage input to and the voltage output from the output stage.

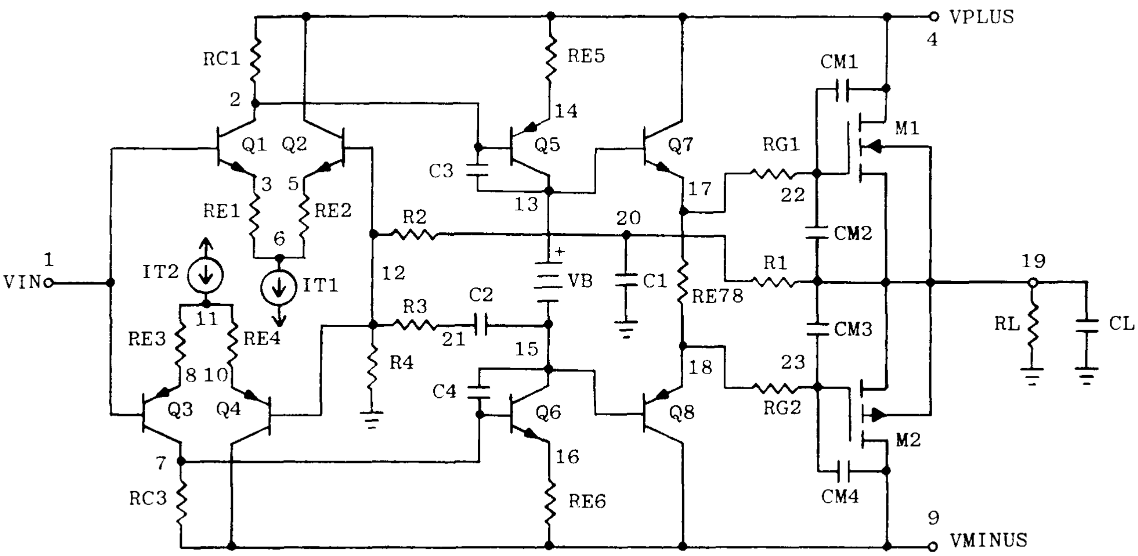

Figure 2. Circuit diagram of the example amplifier design used for the computer simulation of the feedforward compensation method. SPICE nodes are shown numbered from 1 to 21. The feedback network consists of resistors R1, R2, and R3, and capacitors C1 and C2.

Bias currents for the transistors are 1 mA for Q_1 through Q_4, 4 mA for Q_5 and Q_6, 5 mA for Q_7 and Q_8, and 100 mA for M_1 and M_2. Appendix A gives the SPICE code used to simulate the circuit. Values and model parameters of all circuit elements are given in this table. Model parameters for Q_1 through Q_8 are typical for BJT devices used in similar stages of contemporary amplifiers. Model parameters for M_1 and M_2 simulate typical power MOSFET devices described in [3]. The gate-to-source and gate-to-drain capacitances of M_1 and M_2 are modeled as external capacitors. These are labeled CM_1 through CM_4 on the circuit diagram.

With an 8 Ω resistive load, simulation data and calculations indicate that the amplifier has a gain-bandwidth product of just over 8 MHz and a slew rate of about 34 V/μsec. With power supply voltages of ± 50 V, the amplifier should be capable of putting out approximately 100 watts of average sine-wave power into an 8 Ω load with small-signal and large-signal bandwidths of 400 KHz and 135 KHz, respectively.

The feedback network was designed to give the amplifier a closed-loop gain of 21. The break frequency in the feedforward compensation was chosen to be 100 KHz, a frequeny well above the audio band. To calculate the feedback network element values, the low frequency gain k of the output stage was required. A SPICE simulation gave k = 0.805. The feedback network element values are given in Appendix A.

With a resistive load of 8 Ω, a SPICE simulation was used to calculate the gain magnitude and phase as a function of frequency both with and without the feedforward network. The upper half-power cutoff frequency in each case was 380 KHz with a phase margin that was close to 45°. To conserve space, the results of these calculations are not shown here.

With the feedforward compensation disabled, the effect of a 0.33 μF capacitor in parallel with the 8 Ω load is shown in Figure 3. The figure shows the calculated magnitude and phase of the output voltage (V(19) and VP(19)) and 21 times the feedback voltage (21*V(12) and VP(12)) for an input signal of 1 V AC. The gain below 10 KHz was constant and is not shown in order to give better resolution in the high-frequency range. The capacitor causes the addition of a 249 KHz pole in the amplifier output stage, a frequency below the unity loop-gain frequency of 380 KHz. This pole causes the magnitude response to show a gain peak just above 300 KHz where the gain increases from the low-frequency value of 21 to a value just below 60. This gain peak would cause severe ringing with a square-wave input to the amplifier. The phase response shows that the phase is approaching -180° at the peak gain frequency. Thus the amplifier is close to being unstable. Increasing the load capacitance makes the gain peak increase rapidly while the phase becomes -180°. The amplifier would become a continuous oscillator when this occurs.

From Figure 3, it can be seen that there is little difference between the magnitude and phase of the output voltage and the magnitude and phase of 21 times the feedback voltage. This is to be expected because the feedback network is purely resistive. The gain peaking in the magnitude plots is a result of the phase of the feedback signal passing through the value -180° near the upper cutoff frequency. The feedforward compensation eliminates the gain peaking by reducing the phase lag in the feedback signal at the upper cutoff frequency.

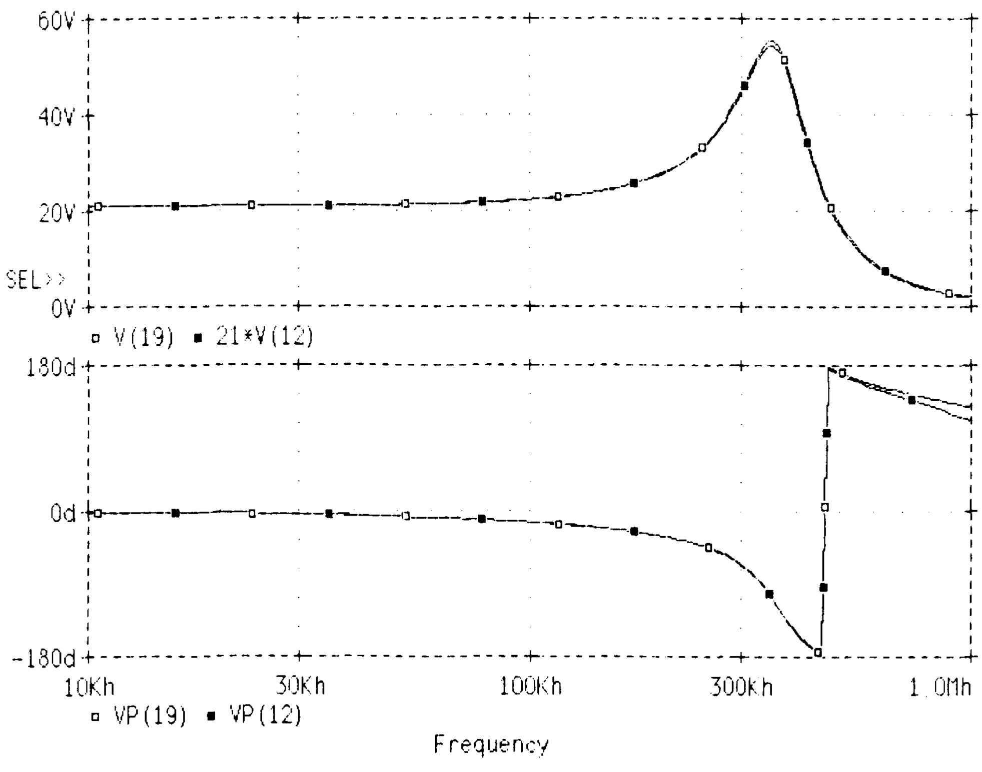

Figure 3. Magnitude (upper figure) and phase (lower figure) versus frequency of the amplifier gain without the feedforward compensation. Calculations made with a 1 V AC generator driving the input so that the calculated voltage is the gain. The load impedance is an 8 Ω resistor in parallel with a 0.33 μF capacitor. V(19) and VP(19) are the calculated magnitude and phase, respectively, of the amplifier output voltage. 21*V(12) is the calculated magnitude of 21 times the feedback voltage, where 21 is the amplifier closed-loop gain. VP(12) is the calculated phase of the feedback voltage.

Figure 4 shows the effect of the feedforward compensation on the frequency response of the amplifier with the 0.33 μF load capacitance. It can be seen that the large gain peak above 300 KHz has been reduced to a much smaller peak just above 100 KHz. Also, the magnitude and phase of the feedback signal are much better behaved compared to the curves of Figure 4. Thus the amplifier with the capacitove load is much more stable with the feedforward compensation.

Of interest is the effect of the feedforward compensation on the amplifier ouput impedance. To investigate this, the input signal was set to zero, the load resistor and capacitor were removed, and the output node of the amplifier was driven by a 1 V AC current source. The calculated output voltage is the output impedance of the amplifier. Figure 5 shows the magnitude of the output impedance versus frequency with and without the feedforward compensation. In each case, the low-frequency impedance is approximately 9 mΩ. With the feedforward compensation it begins to rise at about 300 Hz. Without the feedforward compensation it begins to rise at about 1.5 KHz.

Because the output impedance of a feedback amplifier becomes inductive above its dominant pole fre-

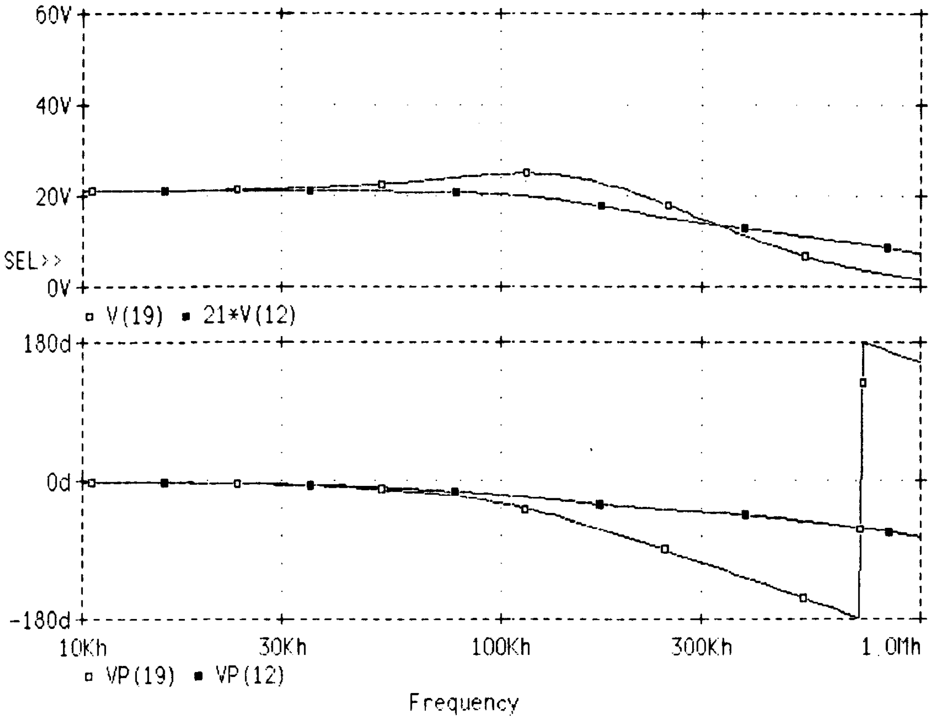

Figure 4. Magnitude (upper figure) and phase (lower figure) versus frequency of the amplifier gain with the feedforward compensation. The load impedance is an 8 Ω resistor in parallel with a 0.33 μF capacitor. V(19) and VP(19) are the calculated magnitude and phase, respectively, of the amplifier output voltage. 21*V(12) is the calculated magnitude of 21 times the feedback voltage, where 21 is the amplifier closed-loop gain. VP(12) is the calculated phase of the feedback voltage.

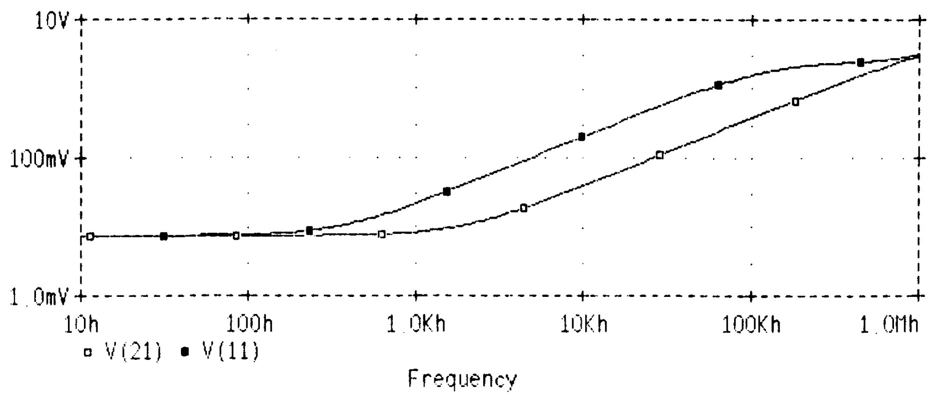

Figure 5. Magnitude of the output impedance of the amplifier versus frequency. Calculations made with a 1 A AC generator driving the output node so that the output impedance is equal to the calculated voltage. V(21) is the calculated impedance without the feedforward compensation. V(11) is the calculated impedance with the feedforward compensation.

quency [4], a SPICE simulation was performed to determine if the feedforward compensation changed the dominant pole. The output impedance was calculated with the feedforward network removed but with R_3 and C_2 connected from node 13 in Figure 2 to ground. The calculated impedance was identical to that for the amplifier without the feedforward compensation. Thus the loading effect of R_3 and C_2 was not significant. It was concluded that the change in output impedance was caused by positive shunt-shunt feedback from the v_3 node to the v_2 node in Figure 2. This positive feedback could be minimized by choosing the v_2 node to be a lower impedance point in the circuit, e.g. C_2 could be connected to the emitter of Q_7 (node 17) rather then to its base.

It is believed that the increase in output impedance caused by the feedforward compensation in the present example is not significant enough to cause a change in performance of an amplifier with a typical loudspeaker load. Because the low-frequency output impedance is not changed, the damping factor at the lower cutoff frequency of a woofer would not be affected. In the present example, the predicted output inductance with and without the feedforward network is 4.8 μH and 0.95 μH, respectively. Both of these values are negligible compared to the inductance of any loudspeaker load.

IV. CONCLUSIONS

Feedback amplifier stability can be improved if the output stage is bypassed in the loop-gain transfer function at frequencies above the audio band. This removes a possible pole from the transfer function caused by the output stage when driving a load capacitance. The method of bypassing the output stage at high frequencies is a feedforward compensation technique. It can cause an increase in the output impedance of the amplifier that is insiginificant for most applications. This effect can be minimized if the feedforward network is connected to a low-impedance point in the circuit.

Above the break frequency in the feedforward compensation, distortion components produced by the output stage will not be fed back with full amplitude. This reduces the amount of negative feedback for reduction of distortion components generated in the output stage. If the break frequency in the feedforward compensation is well above the audio band, in-band distortion components will be reduced by the full amount of available feedback.

V. APPENDIX A

All computer simulations were made with the PSPICE Software Circuit Simulator. A listing of the code used for calculating the curves of Figure 3 is given in the following. The asterisk in the first column of the third line of code caused this line not to be read for the calculations of Figure 3. The SPICE nodes used for the simulation are labeled in Figure 2. The value given for the parameter KP in the .MODEL statements for M1 and M2 was doubled for the simulations to correct for an apparent error in the PSPICE code.

```
FEEDFORWARD SIMULATION
VIN 1 0 AC 1V
*IIN 0 19 AC 1A
VPLUS 4 0 DC 50V
VMINUS 9 0 DC -50V
IT1 6 9 DC 2MA
IT2 4 11 DC 2MA
VBIAS 13 15 DC 2.81V
RE1 3 6 300
RE2 5 6 300
RE3 8 11 300
RE4 10 11 300
RC1 2 4 1.8K
RC3 7 9 1.8K
RE5 14 4 300
RE6 16 9 300
RE78 17 18 430
RG1 17 22 220
RG2 18 23 220
CM1 4 22 30PF
CM2 22 19 600PF
CM3 19 23 900PF
CM4 23 9 30PF
RL 19 0 8
CL 19 0 0.33UF
R1 19 20 11K
R2 20 12 11K
R3 21 12 25.08K
R4 12 0 1.1K
C1 20 0 265.6PF
C2 13 21 58.25PF
C3 2 13 10PF
C4 7 15 10PF
Q1 2 1 3 T1
Q2 4 12 5 T1
Q3 7 1 8 T2
Q4 9 12 10 T2
Q5 13 2 14 T3
Q6 15 7 16 T4
Q7 4 13 17 T4
Q8 9 15 18 T3
M1 4 22 19 19 T5
M2 9 23 19 19 T6
.MODEL T1 NPN IS=1.26E-14
+RB=200 BF=150 VA=200
+CJC=10PF TF=5.8E-10
.MODEL T2 PNP IS=1.26E-14
+RB=200 BF=150 VA=200
+CJC=20PF TF=7.3E-10
.MODEL T3 PNP IS=8.7E-14
+RB=200 BF=100 VA=150
+CJC=34PF TF=4.4E-9
.MODEL T4 NPN IS=8.7E-14
+RB=200 BR=100 VA=150
+CJC=19PF TF=3.1E-9
.MODEL T5 NMOS VTO=0.0
+KP=0.1667V
.MODEL T6 PMOS VTO=0.0
+KP=0.1667V
.OP
.AC DEC 80 10K 1MEG
.PROBE
.END
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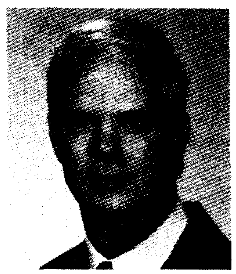

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