Operational Amplifier Stability
Part 9 of 15: Capacitive Load Stability: Output Pin Compensation

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Part 9 of this series is the fifth verse of our familiar electrical engineering tune, "There must be six ways to leave your capacitive load stable." The six ways are: Riso, High Gain & CF, Noise Gain, Noise Gain & CF, Output Pin Compensation, and Riso w/Dual Feedback. In Part 9, here, we cover Output Pin Compensation. This stability technique is NOT the same as an output op amp *snubber* network, which is often used on the output of power operational amplifiers (with all-npn output stages) to stop undesired, high-frequency oscillations when driving capacitive loads. Details of the use of the snubber network will be discussed in a later part of this article series.

Sometimes, in the real world, we do not always have access to the –input and/or +input of the op amp to allow us to use other compensation tricks in our analog tool box. Here we will derive the Output Pin Compensation technique for both emitter-follower output op amps and also CMOS RRO op amps. The emitter-follower application will entail a reference output on a unique 4 - 20 mA building block integrated circuit. The CMOS RRO application involves a difference amplifier used in the feedback for a power supply. Both of these definition-by-example cases are real-world applications where we will conclude our only stability option is Output Pin Compensation. In addition to first-order analysis and TINA Spice simulation, real-world implementation has been completed with as-predicted results.

Bipolar Emitter-Follower: Output Pin Compensation

Our bipolar emitter-follower Output Pin Compensation case is shown in Fig. 9.1. The XTR115/XT116 is a two-wire, 4 - 20 mA IC that can translate an input voltage change into an analog 4 - 20 mA signal. Since the 4 - 20 mA transmitter is intended to drive long wires, it needs a wide operating voltage range of 7.5 V to 36 V. Additionally, the XTR115/XTR116 has a sub-regulator to provide 5 V to power sensor conditioning circuitry and a precision reference of 2.5 V (XTR115) or 4.096 V (XTR116).

The 4 - 20 mA signal range is a well-established industrial standard intended to transmit analog signals over long distances (over 1 mile or 1.6 km) in noisy environments, such as factories, where 50 Hz or 60 Hz large voltage noise is prevalent. Since the standard is a current controlled transmission, it is immune to voltage noise coupling into its two wires. Power and signal are transmitted over the same two wires. Since the useable analog signal range is defined as 4 - 20 mA, up to 4 mA is allowed to power the signal conditioning circuitry and excite a sensor at the transmitter end of the two wires. Power is provided by the receiver which also receives the analog 4 - 20 mA signal, which has been scaled to correspond to a sensor's measurement of real-world parameters such as pressure from a bridge pressure sensor. At the receiver end, the 4 - 20 mA signal is often converted to a voltage (1 V to 5 V) across a resistor (250 Ω) to be read by an ADC.

Often times in such a 4 - 20 mA sensor transmitter a microcontroller is used to read and apply linearization constants to the real-world sensor. The microcontroller must be low power to allow some current to excite the sensor since our total conditioning circuit current budget must be less than 4 mA. The MSP430F2003 provides a low-voltage, low-quiescent current microcontroller and has an on-board ADC to read the bridge changes. After the microcontroller applies its linearization constants it talks to

the DAC8832, a low-power DAC to create the required analog input voltage to the XTR115/XTR1116. The DAC8832 is buffered by a zero-drift, low-power, single-supply op amp, OPA333. Since we have an absolute system we can power everything from the accurate VREF pin of the XTR115/XTR116. We choose the XTR115 (2.5-V VREF) since the MSP430F2003 can only operate from 1.8 V to 3.3 V. Now the on-board ADC of the MSP430F2003, as well as the DAC8832, will use the precision 2.5-V reference of the XTR115. Our total, typical conditioning circuit quiescent current is 562 µA, which leaves up to 3.4 mA to excite our bridge sensor. Our only challenge now is that we need to add many local bypass capacitors for good, high-frequency bypass near the many ICs powered from the VREF pin of the XTR115. Will the XTR115 VREF pin be stable?

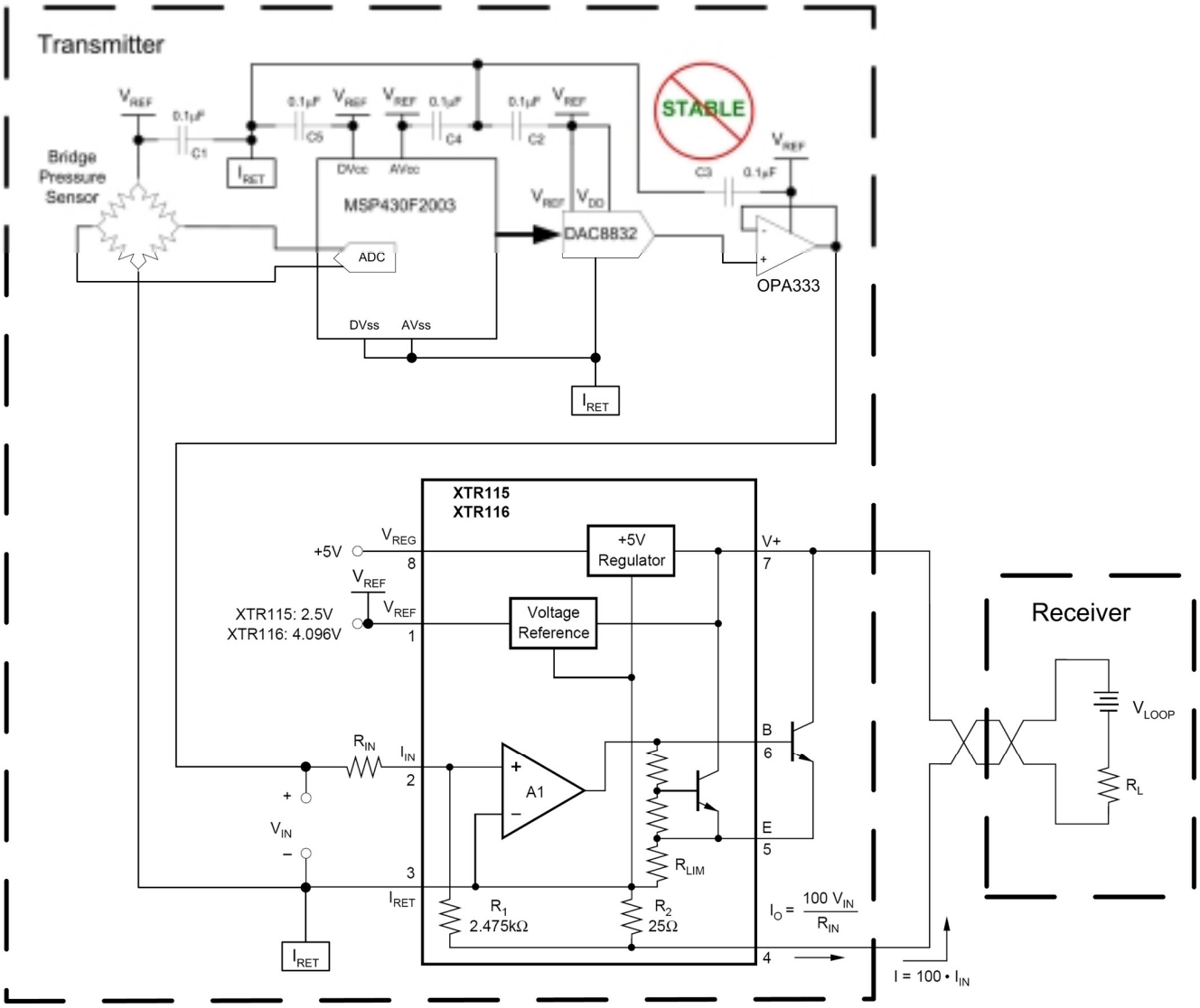


Fig. 9.1: 4 - 20-mA Bridge Sensor Application

In Fig. 9.2 we detail the key specifications for the ICs used in our 4 - 20 mA bridge sensor conditioner application.

XTR115/XTR116
2-Wire 4-20mA Current Loop Transmitter

Parameter	Specification
Supply Voltage Range	7.5V to 36V
Quiescent Current	240uA typical
SubRegulator	5V
VREF for Sensor Excitation	2.5V (XTR115), 4.096V (XTR116)
VREF Accuracy	+/-0.05% typical
VREF Drift	+/-20ppm/C typical
VREF PSR	+/-1ppm/V (V+ = 7.5V to 36V)
VREF vs Load	+/-100ppm/mA (IREF = 0mA to 2.5mA)
VREF Noise	10uVpp typical (0.1Hz to 10Hz)
Span Error	0.05% typical
NonLinearity Error	0.003% typical
Package	SO-8

DAC8832
16-Bit, Ultra-Low Power, Voltage-Output, Digital-to-Analog Converter

Parameter	Specification
Resolution	16 Bit
Supply	2.5V to 5.5V
Quiescent Current	5uA typical
Linearity Error	+/-0.5LSB typical
Differential Linearity Error	+/-0.5 typical
Gain Error	+/-+/-1LSB typical
Gain Drift	+/-0.1ppm/C typical
Zero Code Error	+/-0.25LSB typical
Zero Code Drift	+/-0.05ppm/C
Package	QFN-14

OPA333
1.8V, microPower CMOS Operational Amplifier, Zero-Drift Series

Parameter	Specification
Supply Voltage	1.8V to 5.5V
Quiescent Current	17uA typical
Offset Voltage	2uV typical
Offset Drift	0.02uV/C typical
Input Bias Current	+/-70pA typical
Input Voltage Noise	1.1uVpp (0.1Hz to 10Hz)
Input Voltage Range	(V-)-0.1V to (V+)+0.1V
Gain-Bandwidth Product	350kHz
Slew Rate	0.16V/us
Voltage Output Swing from Rail	30mV typical (RL=10k)
Package	SOT23-5, SC70-5, SO-8, DFN-8

MSP430F2003
1.8V, microPower CMOS Operational Amplifier, Zero-Drift Series

Parameter	Specification
Supply Voltage	1.8V to 3.6V
Quiescent Current	300uA typical (Active Mode, 1MHz)
Architecture	16-bit RISC
A/D Converter	16-Bit Sigma-Delta
Watchdog Timer	
Flash	1k Byte + 256 Byte
RAM	128 Byte
Port 1	8 I/O
Port 2	Xtal or 2 I/O
Interface	Universal Serial (SPI, I2C), Port 1
Clock	Internal, External 32kHz crystal
Package	TSSOP-14, DIP-14, QFN-16

Fig. 9.2: Key Specifications For 4 - 20-mA Conditioning Circuit ICs

The XTR115 VREF pin is the output of an emitter-follower output topology as shown in Fig. 9.3.

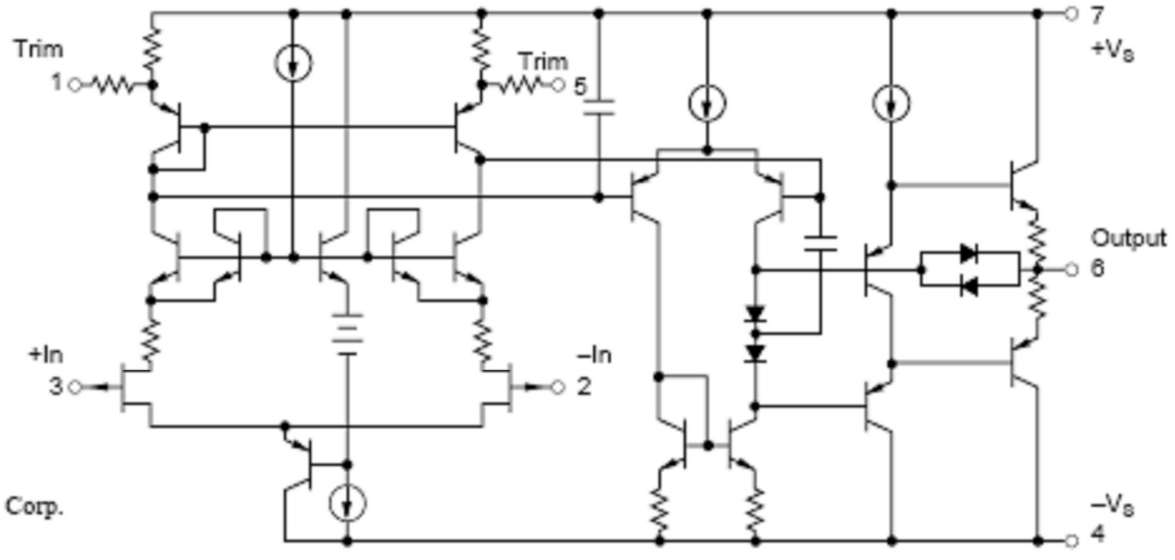


Fig. 9.3: XTR115 VREF Pin: Emitter-Follower Output Op Amp

Fig. 9.4 shows the equivalent circuit of the XTR115 VREF pin. VREF is a buffered 1.25-V bandgap reference which is amplified by x2 to yield the XTR115 2.5V reference output. The emitter-follower output stage has an Ro of 4.7 kΩ. This information, along with values for RF and RI and the Aol curve of U1, were obtained from the factory as it is not given in the data sheet. Our total capacitive load, CL, is seen to be 500 nF. Ro will interact with CL to form a second pole, fpu1, in the modified Aol curve for the XTR115 VREF op amp. Note that we have no access to the –input or +input of U1 since it is internal to the XTR115. This leaves us with only one pin to compensate the amplifier for stability (the output pin: VREF). Also note that we want the VREF pin to remain extremely accurate, and so putting any resistance in series with this pin before CL is not an acceptable solution.

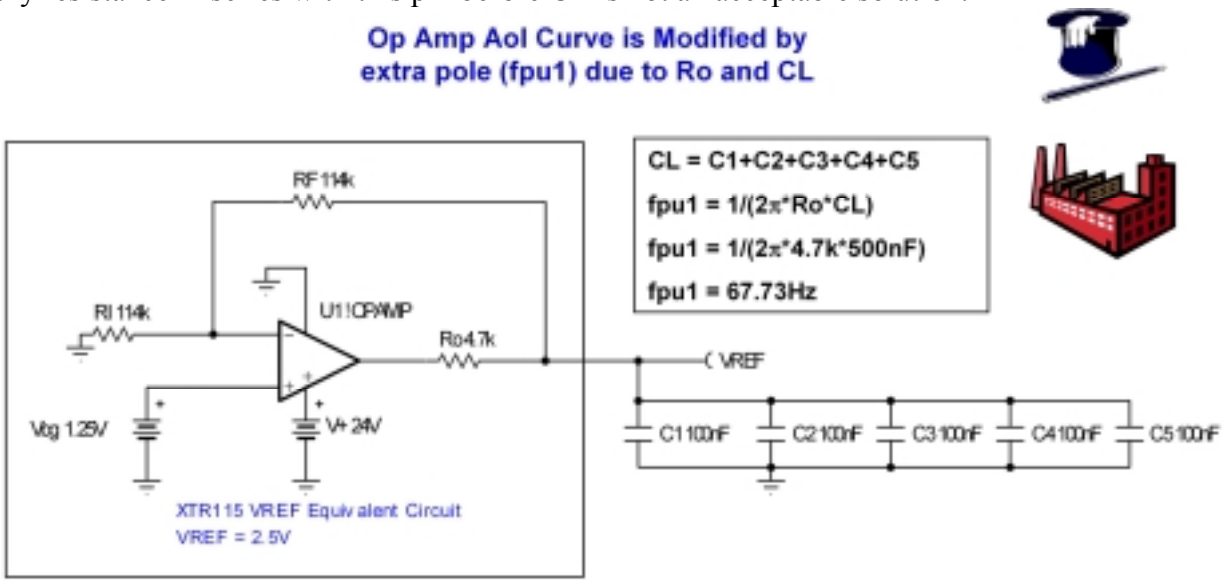


Fig. 9.4: XTR115 VREF Pin: Capacitive Load, Equivalent Schematic

We will use the TINA Spice circuit of Figure 9.5 to examine the Aol curve of the op amp and the modified Aol curve due to CL. We use our Spice AC analysis trick by using LT, short at DC and an open at AC frequencies of interest, and CT, open at DC and a short at AC frequencies of interest.

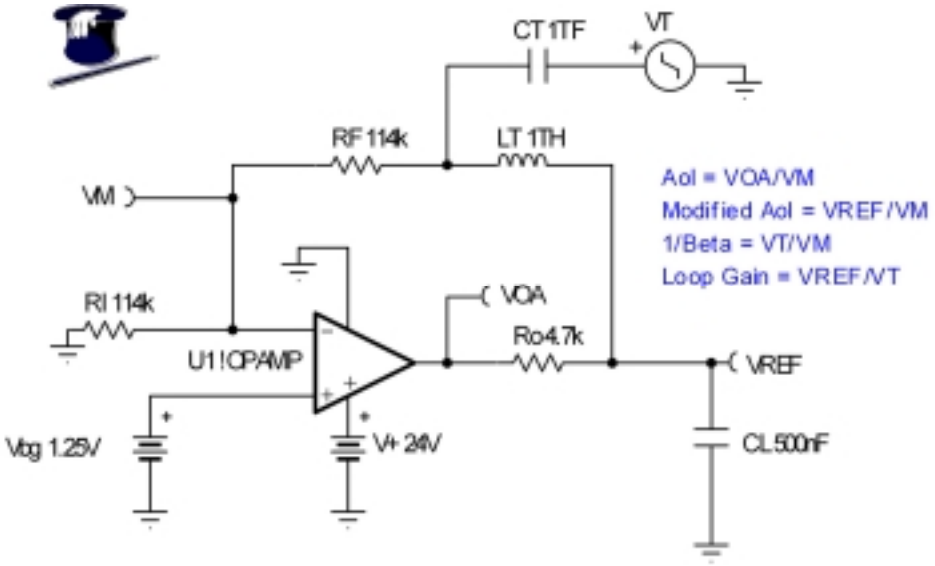


Fig. 9.5: Ac Stability Check: Original Circuit

Fig. 9.6 shows the op amp Aol curve and the modified Aol curve due to CL. At fcl1, we see a 40 dB/decade rate-of-closure which is unstable by our first-order stability criteria. Our predicted fpu1 due to CL was 67.73 Hz which from inspection looks to be correct in this plot.

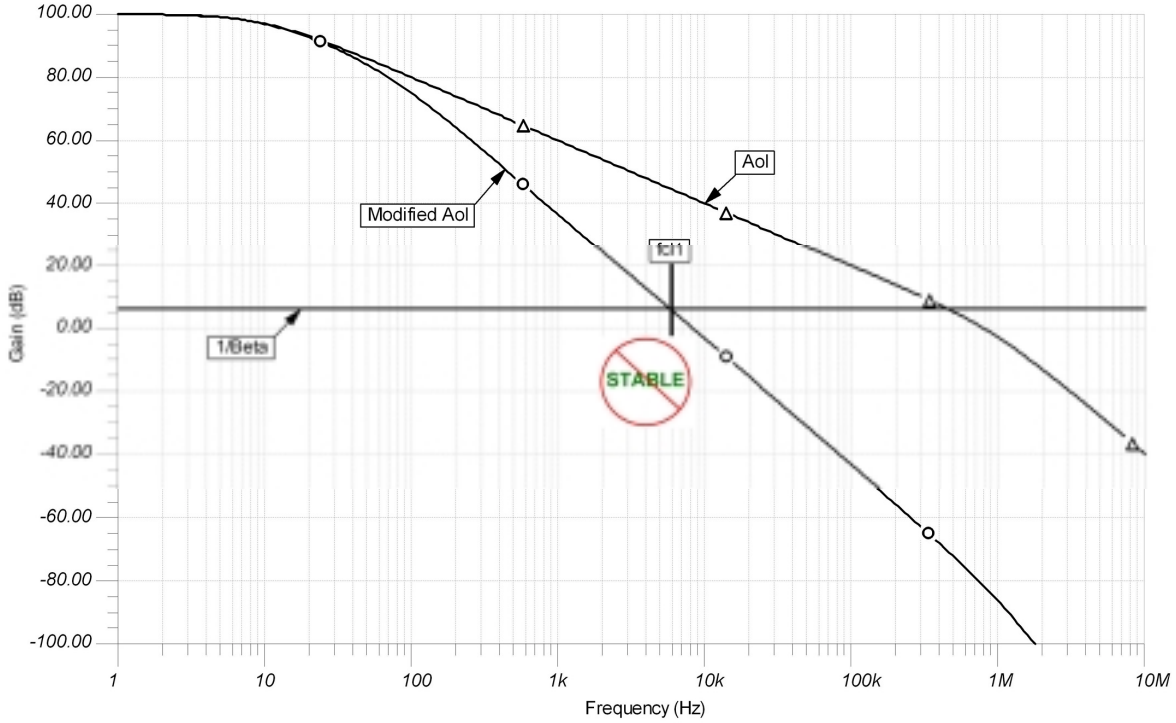


Fig. 9.6: Aol And Modified Aol: Original Circuit

A loop-gain plot in Fig. 9.7 confirms our concerns with phase margin almost zero (0.442°!) at fcl1.

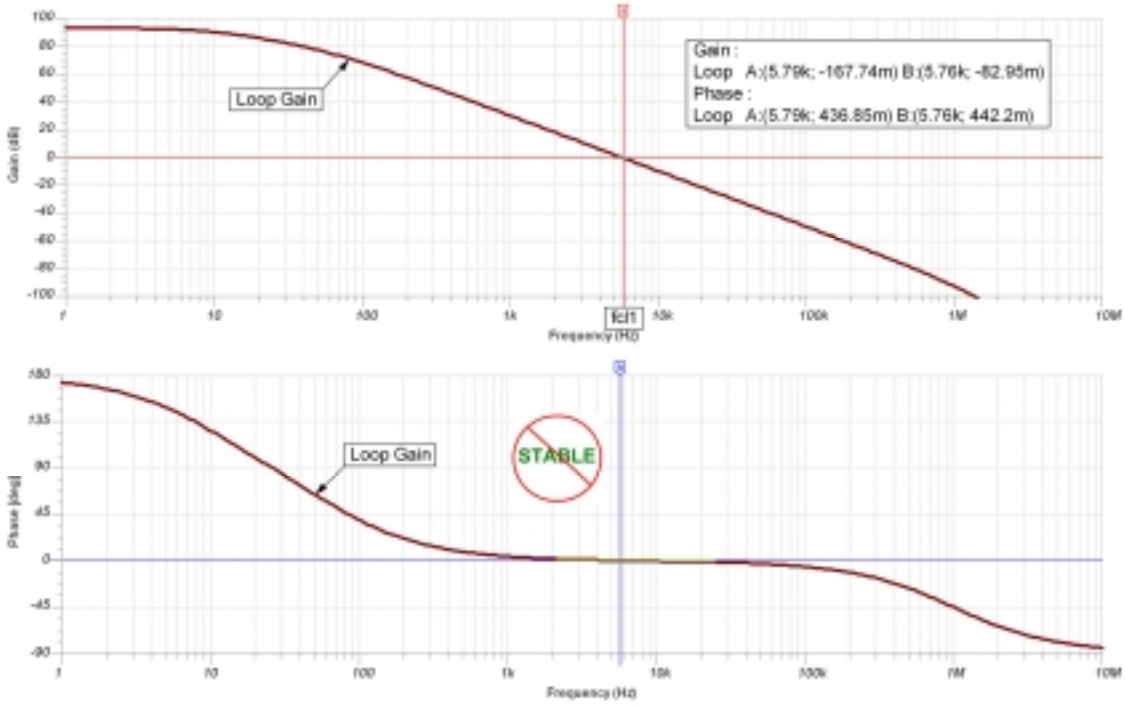


Fig. 9.7: Loop-Gain Plot: Original Circuit

In Figure 9.8 we do a transient stability test by injecting a small square wave into our closed loop circuit with CL of 500 nF attached.

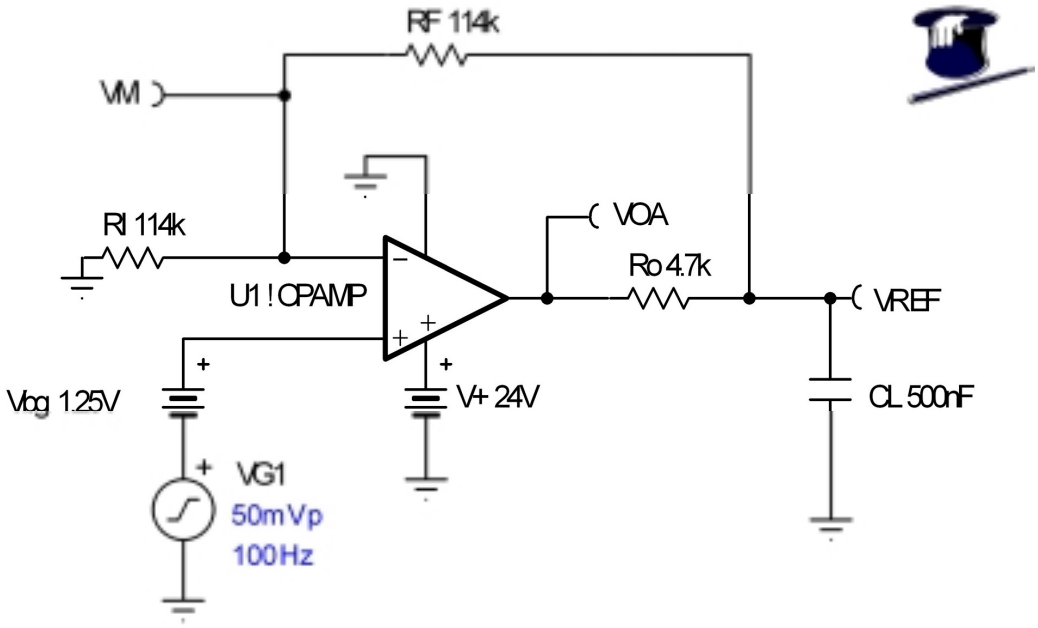


Fig. 9.8: Transient Stability Test: Original Circuit

Our transient stability plots in Figure 9.9 indicate, again, that our circuit is not stable. Our op amp output never settles in response to a small step change. Note that VOA is transitioning about 2.5 V, indicating that our dc levels are correct for this circuit.

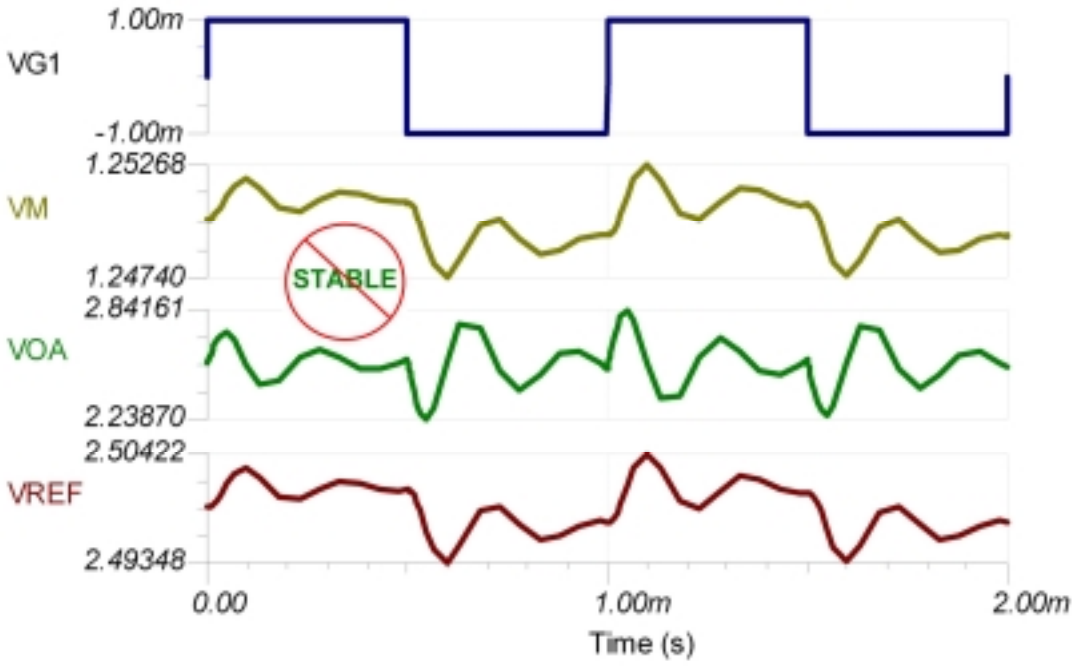


Fig. 9.9: Transient Stability Plots: Original Circuit

In Fig. 9.10 we identify the technique for Output Pin Compensation for bipolar emitter-follower output amps. First we modify the op amp's original Aol curve with fpu1, the pole due to Ro and CL (see Curve 1). Once this curve is created, we plot a second curve (Curve 2) which starts where the Curve 1 intersects 0 dB. From this starting point we plot back at -20 dB/decade to a point which is one decade above fp1 (the op amp Aol low frequency pole) where we change the slope to -40 dB/decade. At fp1 frequency we change the slope back to –20 dB/decade until we intersect the dc Aol value of the op amp. This proposed modified Aol curve (Curve 2) meets all of our rule-of-thumb criteria by keeping poles and zeros within one decade of each other to keep loop gain phase from dipping below 45° within the loop-gain bandwidth. Our proposed modified Aol curve (Curve 2) will also meet our first-order stability criteria of 20 dB/decade rate-of-closure at fcl2.

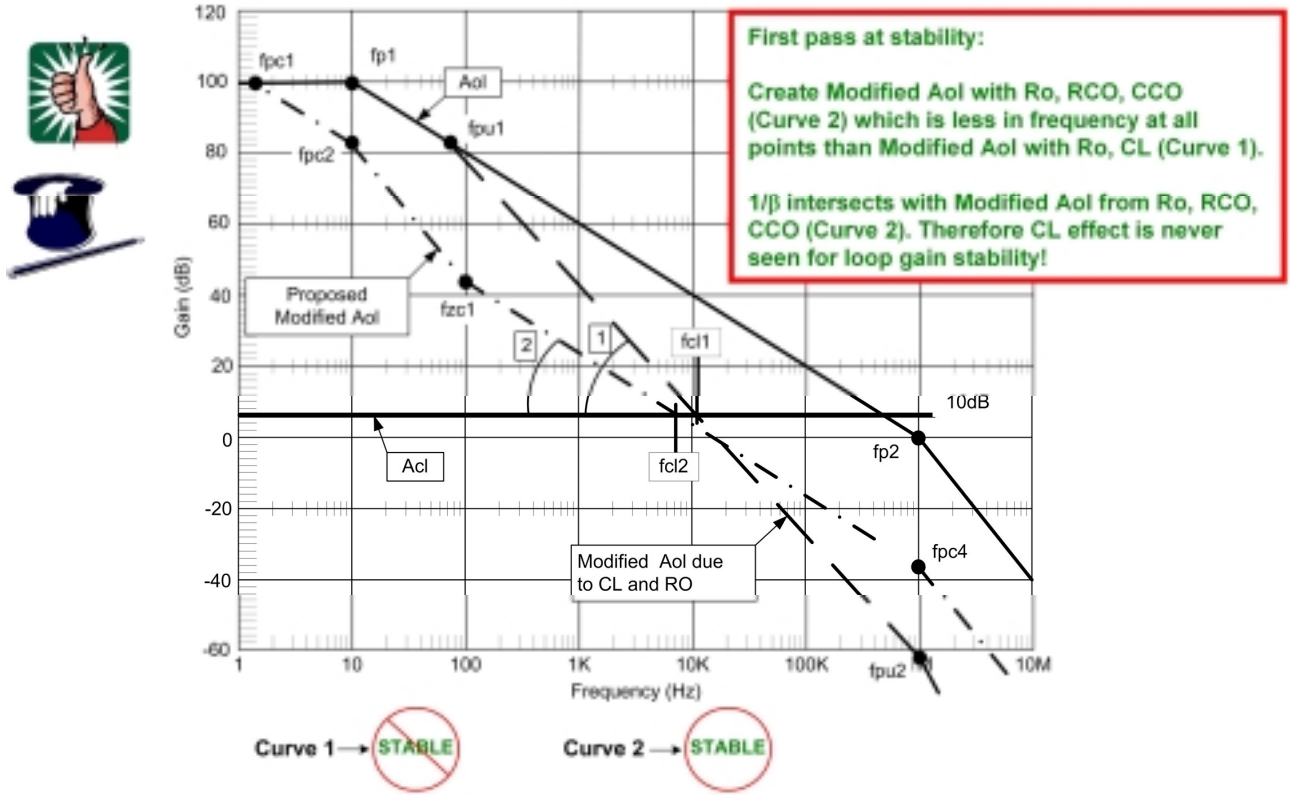


Fig. 9.10: Output Pin Compensation: Bipolar Emitter-Follower

Fig. 9.11 shows how we will get our proposed modified Aol curve by using RCO and CCO. There will be an additional pole we will have to also consider since, at some high frequency, CCO will become a short and CL and RCO will form an additional high-frequency pole. If this pole occurs beyond fcl2, we will still be okay.

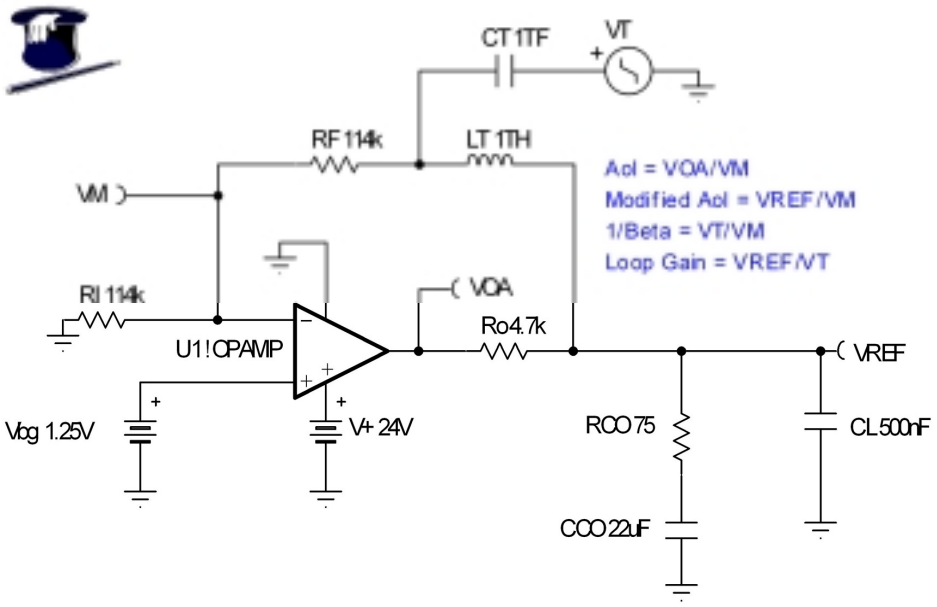


Fig. 9.11: Ac Stability Check: Output Pin Compensation

Since we know Ro and CL we can use the formulae in Fig. 9.12, in conjunction with our proposed modified Aol curve in Fig. 9.10 (Curve 2), to compute our compensation components RCO and CCO along with the extra high-frequency pole formed by RCO and CL.

Ro = 4.7kΩ, RCO = 75Ω, CCO = 22μF, CL = 500nF

fpc1 = 1/[2π*(Ro+RCO)*CCO]

fpc1 = 1/[2π*(4.7kΩ+75Ω)*22μF] = 1.5Hz

fpc2 = fp1 = 10Hz
(Low frequency pole from op amp Aol curve)

fzc1 = 1/(2π*RCO*CCO)

fzc1 = 1/(2π*75Ω*22μF) = 96.5Hz

fpc3 = 1/[2π*(Ro//RCO)*CL]
fpc3 = 1/{2π*[(Ro*RCO)/(Ro+RCO)]*CL}

If: RCO < 10*Ro and CCO > 10*CL
Then: fpc3 ~ 1/[2π*RCO*CL]
fpc3 ~ 1/[2π*75Ω*500nF] = 4.2kHz

fpc4 = fp2 = 1MHz
(High frequency pole from op amp Aol curve)

Fig. 9.12: Output Pin Compensation Formulae: Bipolar Emitter-Follower

In Fig. 9.13 we plot our predicted curves using Output Pin Compensation. Since our closed-loop op amp inside the XTR115 runs at a gain of x2 (6 dB), the closed-loop VREF/VIN curve will remain flat until it intersects with our modified Aol at fcl2, where it will then follow the modified Aol curve on down since loop gain has gone to zero.

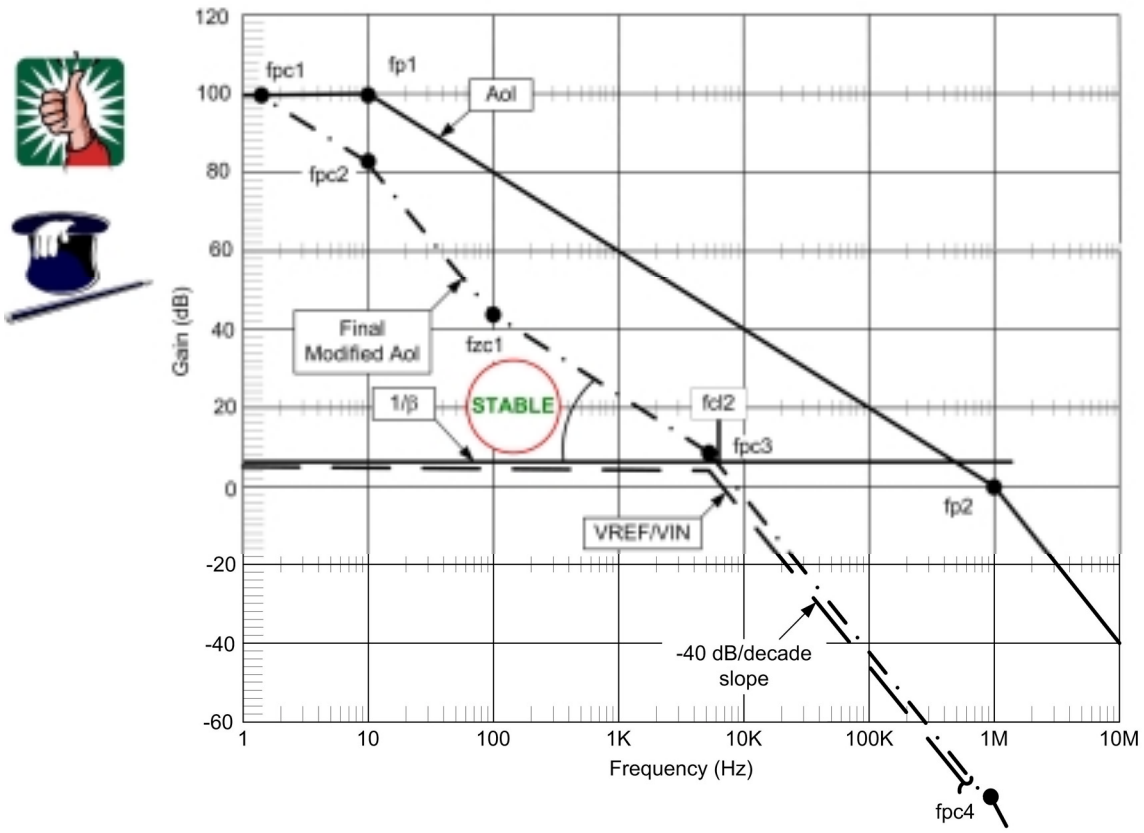


Fig. 9.13: Final Predicted Curves: Output Pin Compensation

Fig. 9.14 is the result of our ac stability analysis TINA Spice simulation using the circuit of Fig. 9.11. At fcl2 it looks like 20 dB/decade rate-of-closure, but we should look at a phase plot for more detail.

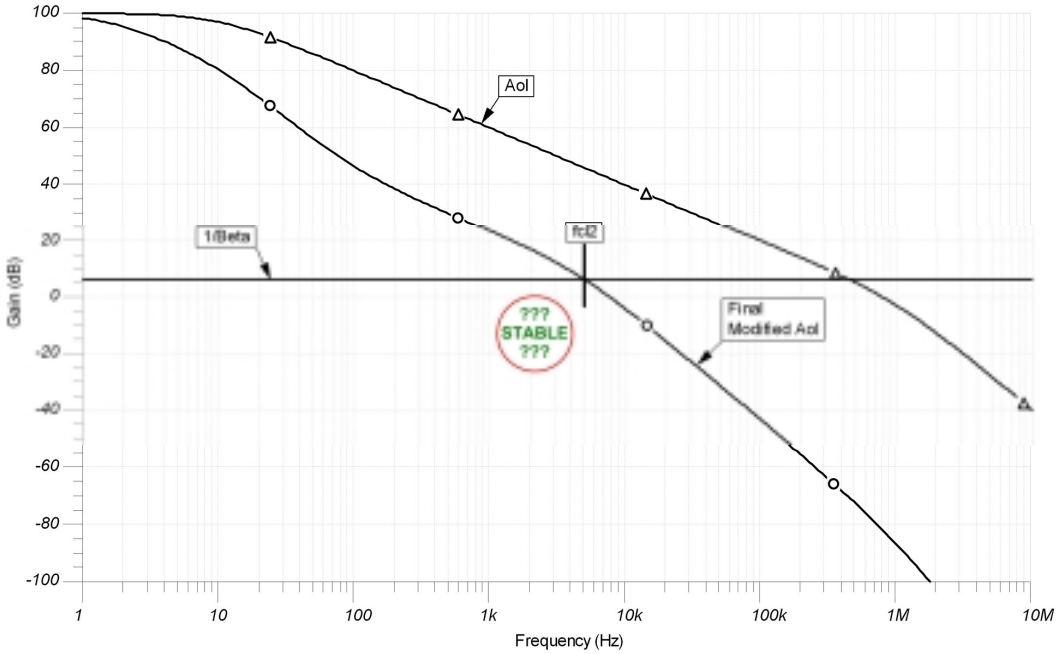


Fig. 9.14: Aol And Modified Aol: Output Pin Compensation

Our loop gain plot shown in Figure 9.15 confirms that our Output Pin Compensation will yield a stable circuit. At fcl2 we have a 40 degree phase margin with phase not dipping much below 45 degrees inside the loop gain bandwidth. If we wanted to we could adjust Output Pin Compensation values slightly to gain more phase margin at fcl2.

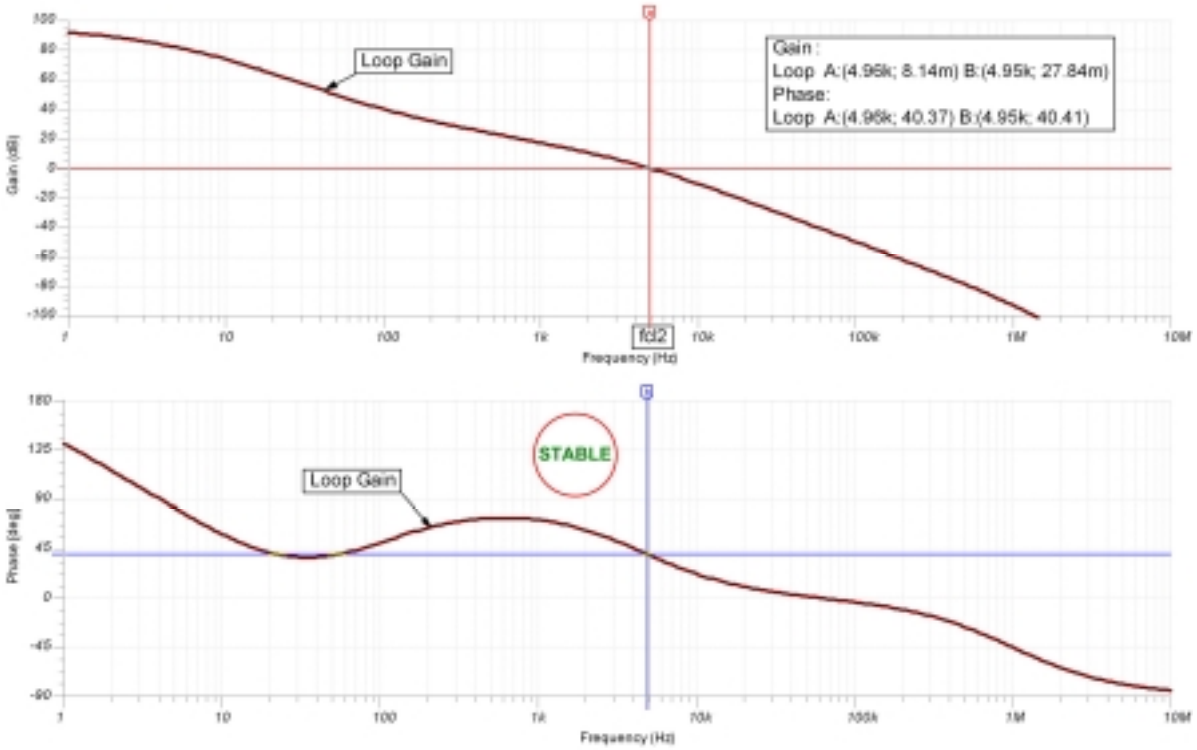


Fig. 9.15: Loop Gain: Output Pin Compensation

The circuit in Fig. 9.16 uses our transient stability test to check our final circuit using Output Pin Compensation.

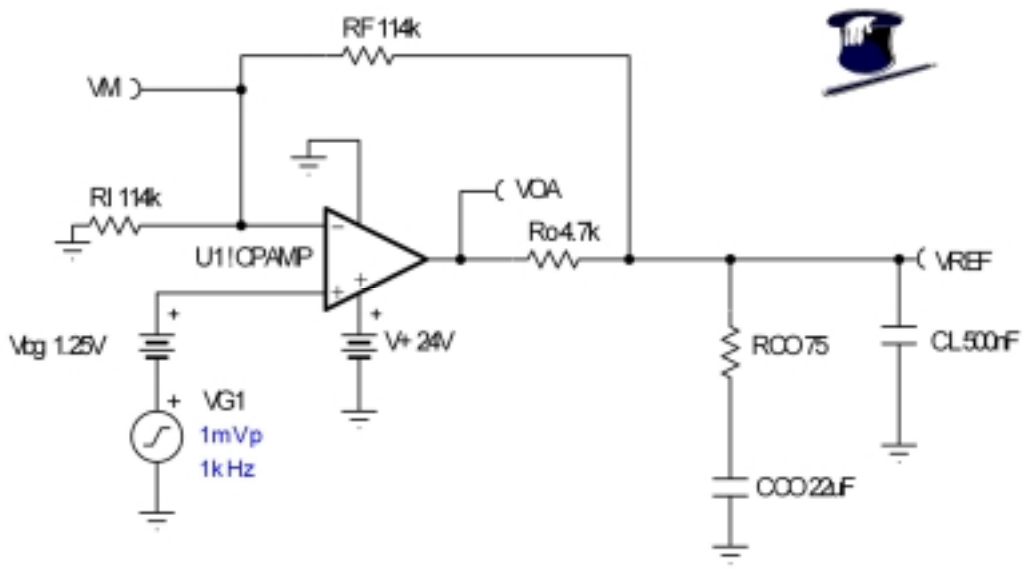


Fig. 9.16: Transient Stability Test: Output Pin Compensation

Our transient stability test results in Fig. 9.17 confirm our loop-gain check that our Output Pin Compensation produced a stable circuit. A small overshoot and one undershoot with no excessive ringing looks close to a typical 45° phase margin compensated circuit.

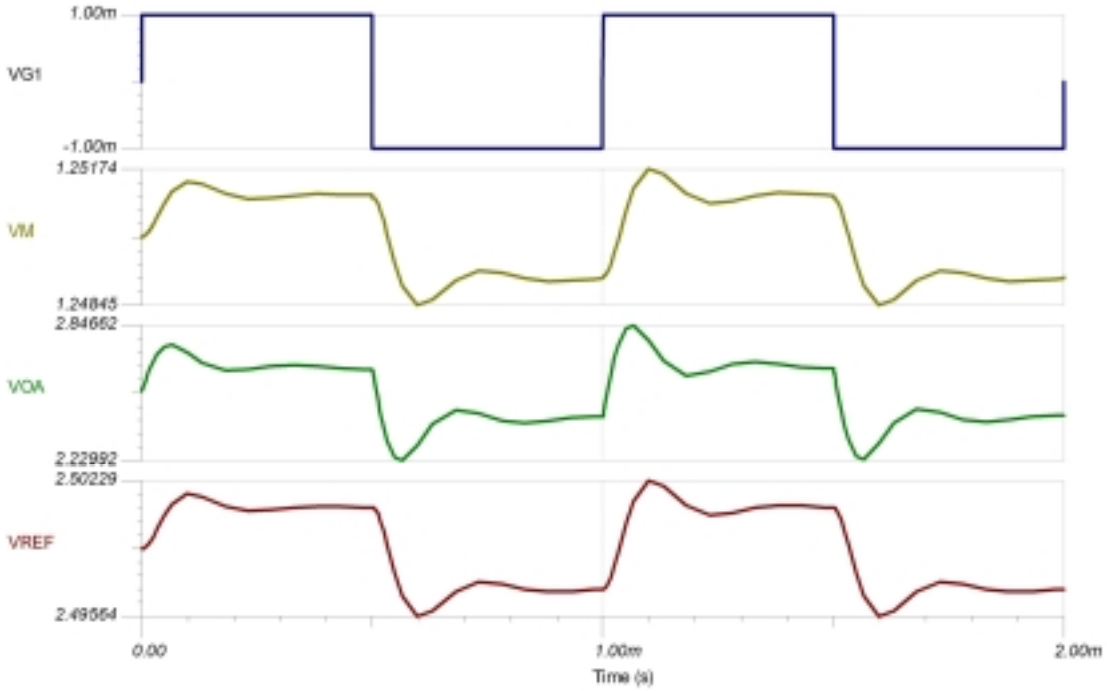


Fig. 17: Transient Stability Plot: Output Pin Compensation

The TINA Spice circuit in Fig. 9.18 allows us to see if our final VREF/VIN closed-loop ac response is as we predicted in Fig. 9.13.

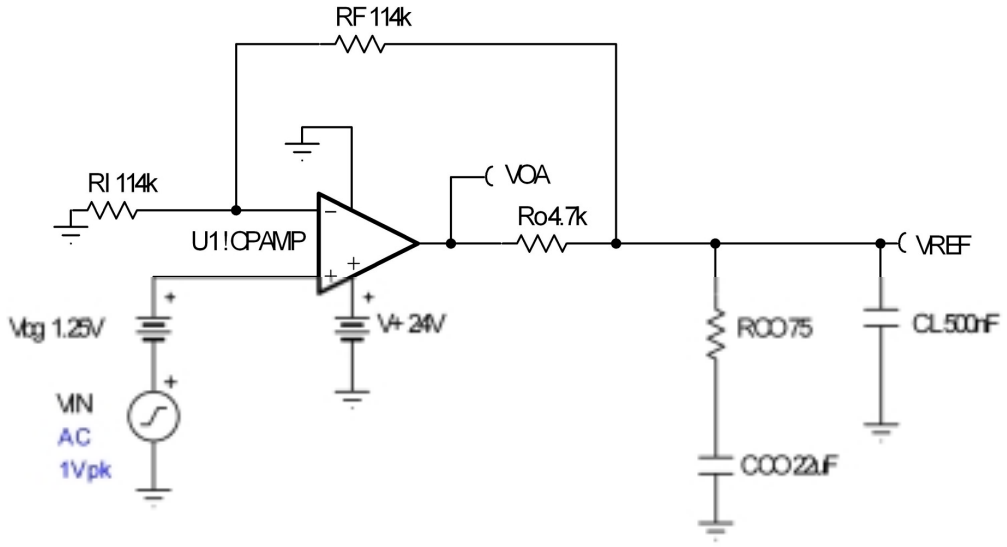


Fig. 9.18: VREF/VIN Ac Circuit: Output Pin Compensation

From Fig, 9.13 we estimate fcl2 to be at around 5 kHz and thus expect a sharp roll-off at this point for VREF/VIN. In Fig. 9.19 we see the closed-loop ac response is as predicted. There is a slight peaking which, for this application, causes no concern but if we desired to reduce it we would need to go through one more pass of our Compensation and increase the phase margin at fcl2 to greater than 40°.

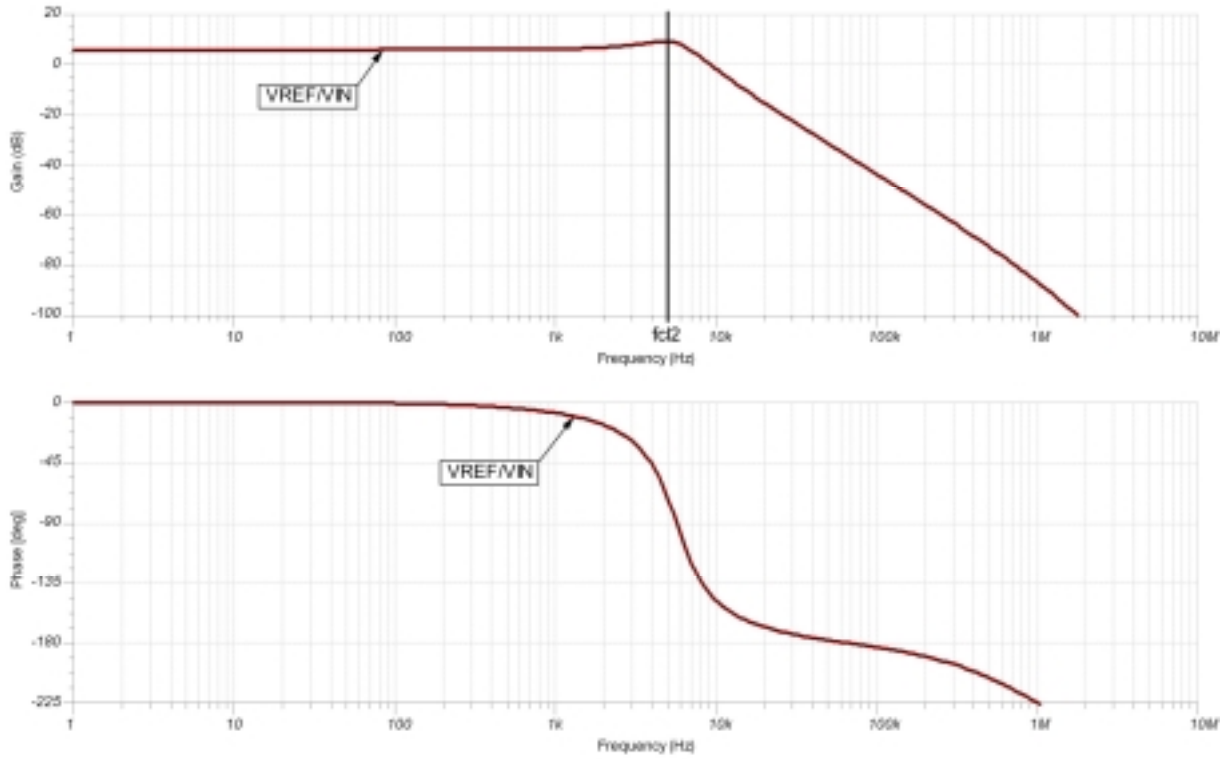


Fig. 9.19: VREF/VIN Ac Response: Output Pin Compensation

CMOS RRO: Output Pin Compensation

Our CMOS RRO Output Pin Compensation case is shown in Fig. 9.20. This real-world power supply application uses an OPA569 power op amp as a programmable power supply. For accurate power supply voltage across the load a difference amplifier, INA152, is used to monitor the voltage differentially across the load.

The closed-loop system then will correct for any losses due to wire drops in either the positive or negative connection from the programmable power supply to the load. The current limit on the OPA569 is set for 2 A. In our actual application this power supply has flexible configurations, and as a result can end up with up 10 nF of capacitance on the output of the difference amplifier.

Is this going to result in a stable operation of our programmable power supply?

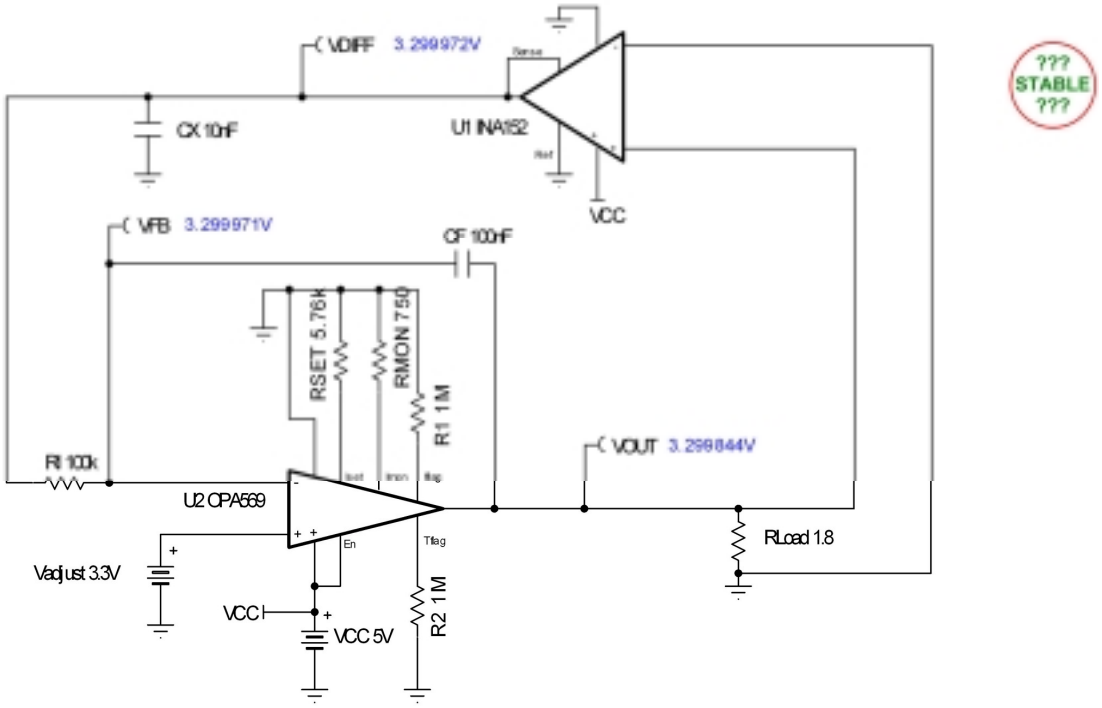


Figure 9.20: Programmable Power Supply Application

In Fig. 9.21 are the key specifications for the ICs used in our programmable power supply application.

INA152

Single Supply Difference Amplifier

Parameter	Specification
Supply Voltage	2.7V to 20V
Quiescent Current	500uA typical
Offset Voltage	+/-250uV typical
Offset Drift	+/-3uV/C typical
Input Impedance Differential	80k typical
Input Impedance Differential	80k typical
Common Mode Rejection	94dB typical
Output Voltage Noise	2.4uVpp (0.1Hz to 10Hz)
Output Voltage noise	10nV/rt-Hz (10kHz)
Input Voltage Range	2(V-) to 2(V+)-2V
Bandwidth	800kHz
Slew Rate	0.4V/us
Gain	1V/V typical
Gain Error	+/-0.01% typical
Gain Drift	+/-1ppm/C typical
NonLinearity	+/-0.002%FS
Voltage Output Swing from Rail	20mV typical (RL=10k)
Package	MSOP-8

OPA569

Rail-to-Rail I/O, 2A Power Amplifier

Parameter	Specification
Thermal Protection	Shutdown at +150C
Adjustable Current Limit	+/-0.2A to +/-2.2A
Current Limit Warning Flag	Normal = V+, Current Limit = V-
Temperature Warning Flag	Low = >+147C, High =<+130C
Shutdown w/Output Disable	>(V-)+2.5V = enabled, <(V-)+0.8 = disabled
Current Monitor Pin	Imonitor = Iout/450
Supply Voltage	2.7V to 5.5V
Quiescent Current	9mA typical, 0.01mA in Shutdown
Offset Voltage	+/-0.5mV typical
Offset Drift	+/-1.3uV/C typical
Input Bias Current	+/-1pA typical
Input Voltage Noise	8uVpp (0.1Hz to 10Hz)
Input Voltage noise	12nV/rt-Hz (1kHz)
Input Voltage Range	(V-)-0.1V to (V+)+0.1V
Gain-Bandwidth Product	1.2MHz
Slew Rate	1.2V/us
Voltage Output Swing from Rail	150mV typical (Iout=+/-2A)
Package	SO-20 Power Pad

Fig. 9.21: Key Specifications For Programmable Power Supply ICs

The INA152 difference amplifier we use for feedback is a CMOS RRO topology (see Fig.9.22).

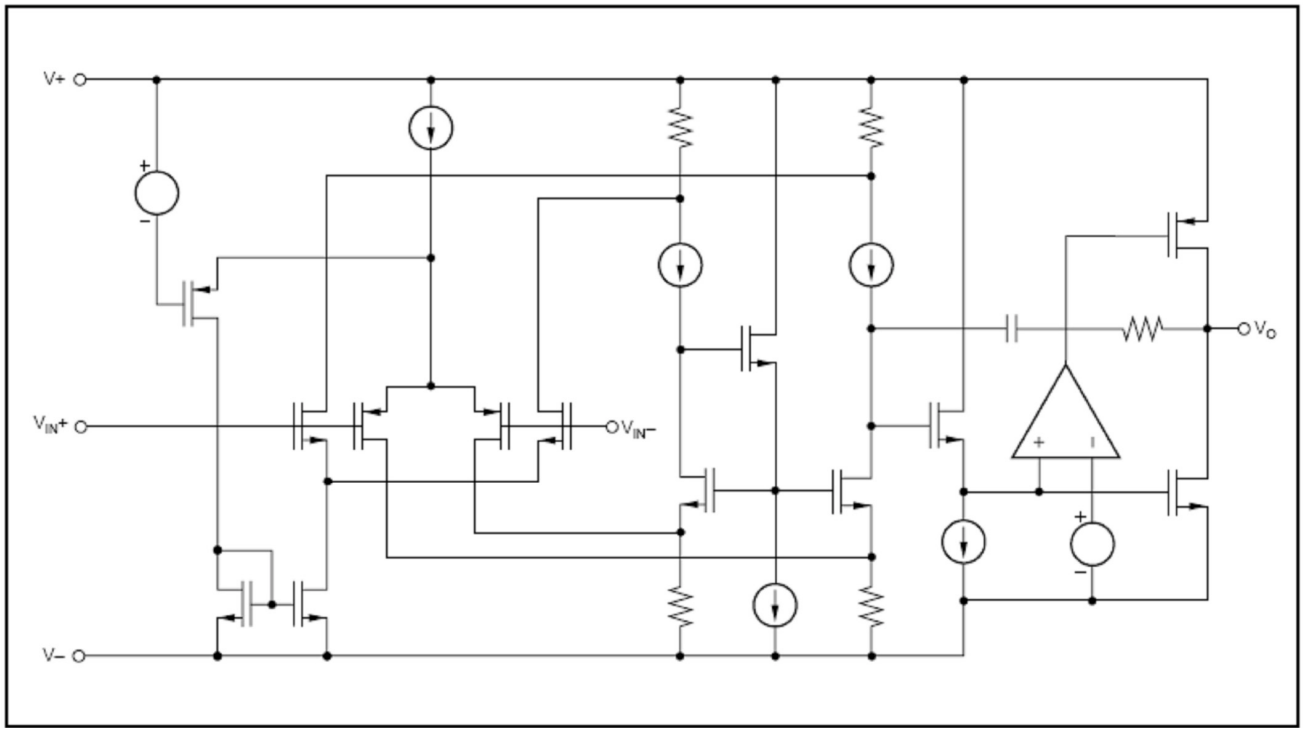


Fig. 9.22: INA152 Difference Amplifier: CMOS RRO

We use the TINA Spice circuit in Fig. 9.23 to check for stability of our programmable power supply. Our dc output is set by Vadjust to be 3.3 V and a small transient square wave will be applied to look for overshoot and ringing.

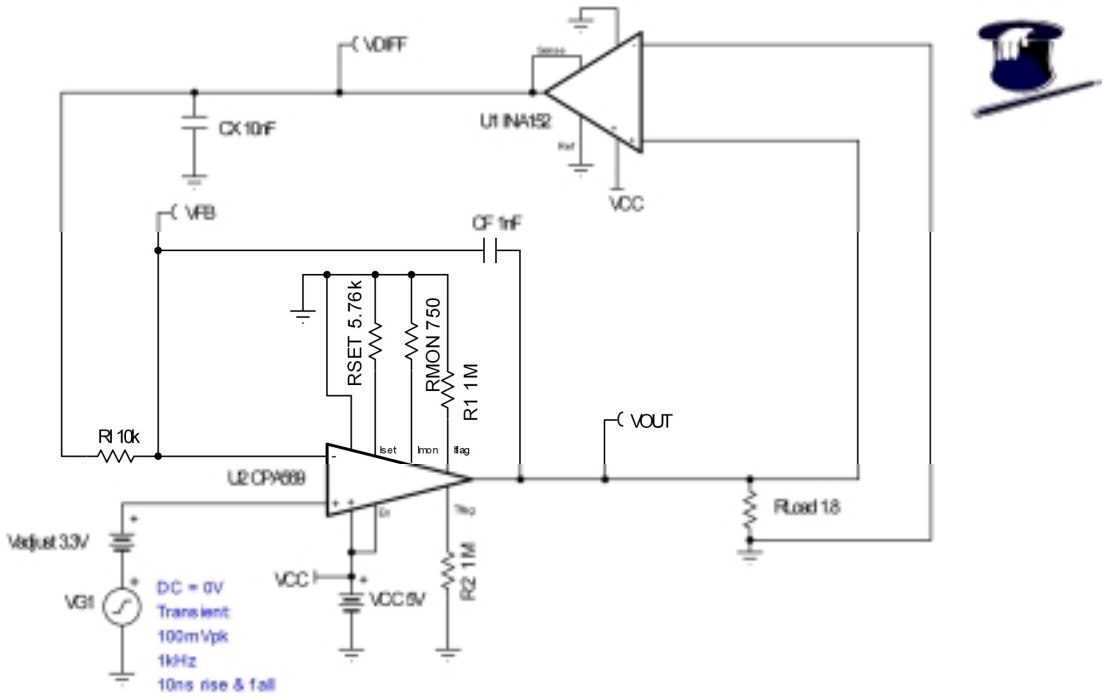


Fig. 9.23: Transient Stability Test: Original Circuit

In Fig. 9.24 the results of our transient stability test are clearly undesirable. This is not a circuit we want to go to production without some additional stability compensation.

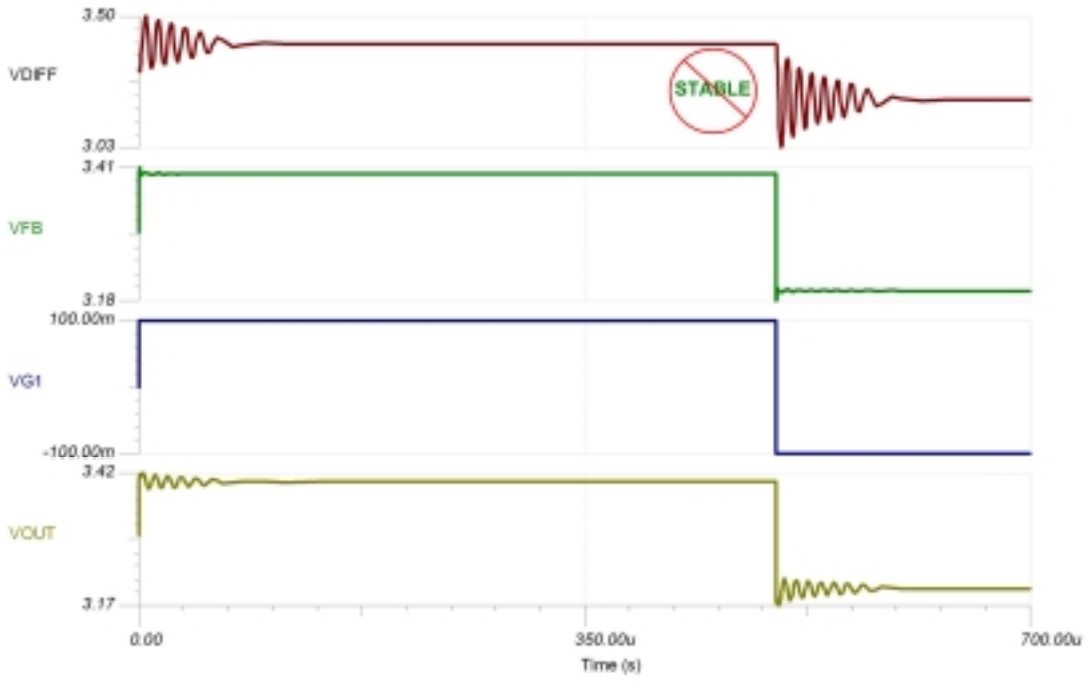


Fig.9.24: Transient Stability Plot: Original Circuit

The TINA Spice circuit in Fig. 9.25 is used to see if the instability in our original circuit is due to the CX load on the output of the INA152. We will use a transient stability test for a quick check.

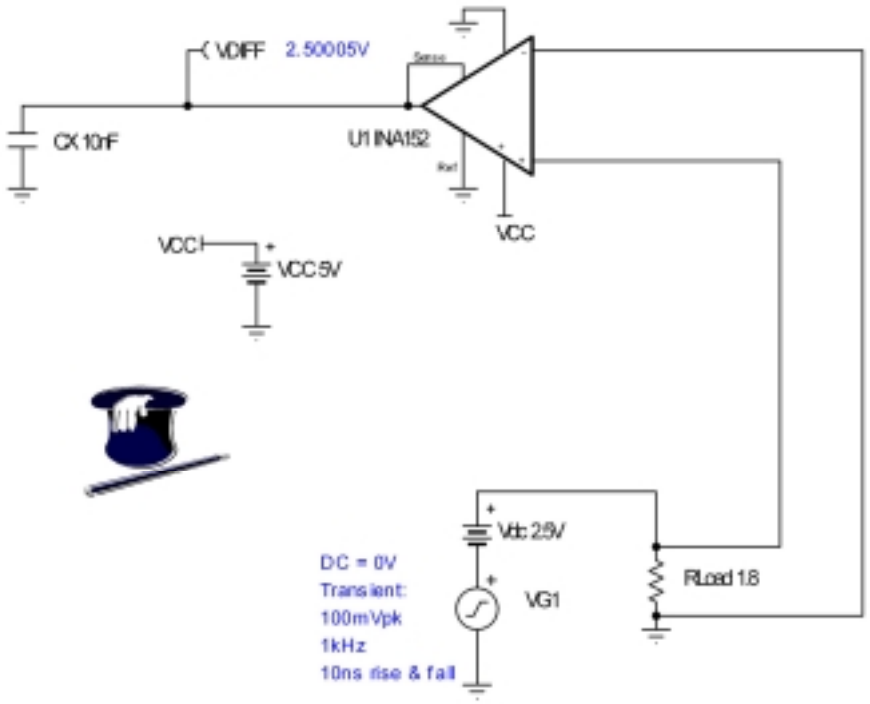


Fig. 9.25: Difference Amplifier Feedback: Original Circuit

Fig. 9.26 confirms our theory of CX causing instability on the difference amplifier INA152.

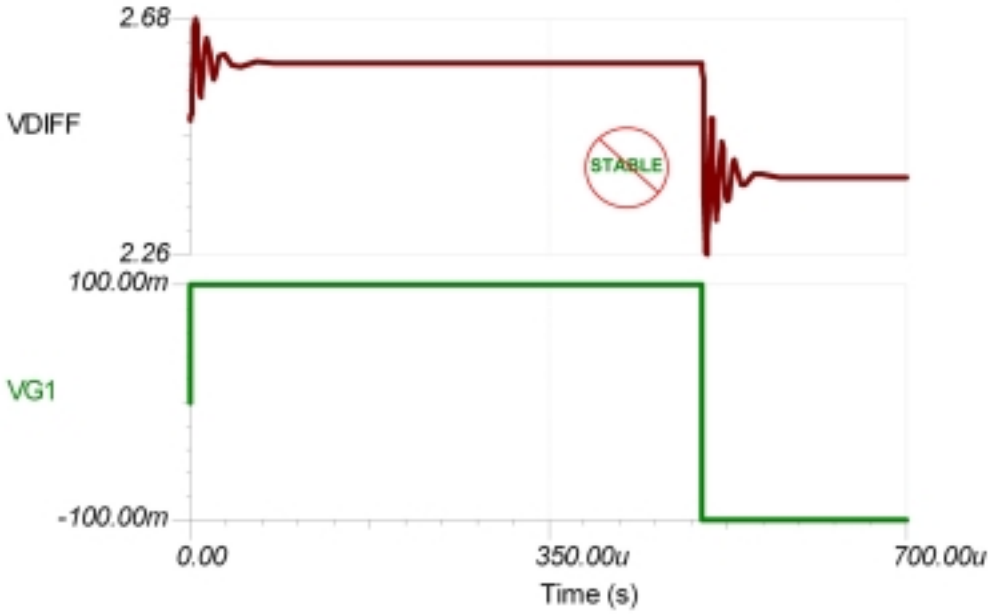


Fig. 9.26: Transient Plots: Difference Amp Feedback, Original Circuit

The difference amplifier consists of an op amp and four precision ratio-matched resistors. This presents us with a challenge for analysis since we do not have direct access to the –input or +input of the internal op amp. In Fig. 9.27 we see the equivalent circuit for the difference amplifier and a clever way we can measure the Aol. We will use LT to break open the feedback for any ac frequencies of

interest and still retain an accurate dc operating point (LT is short for dc, open for ac frequencies of interest). By connecting the Ref pin of the INA152 to the VIN+ pin we create a non-inverting input amplifier. By placing LT between Sense and VOA we will essentially be driving the op amp open loop at any ac frequency of interest. VM, the internal node for the INA152 op amp will be at zero for ac frequencies of interest. VP will simply be VG1 and we easily can measure Aol = VOA/VG1. Note that we scale the dc operating point by setting VdcBias to 1.25 V to yield 2.5 V on VOA for dc.

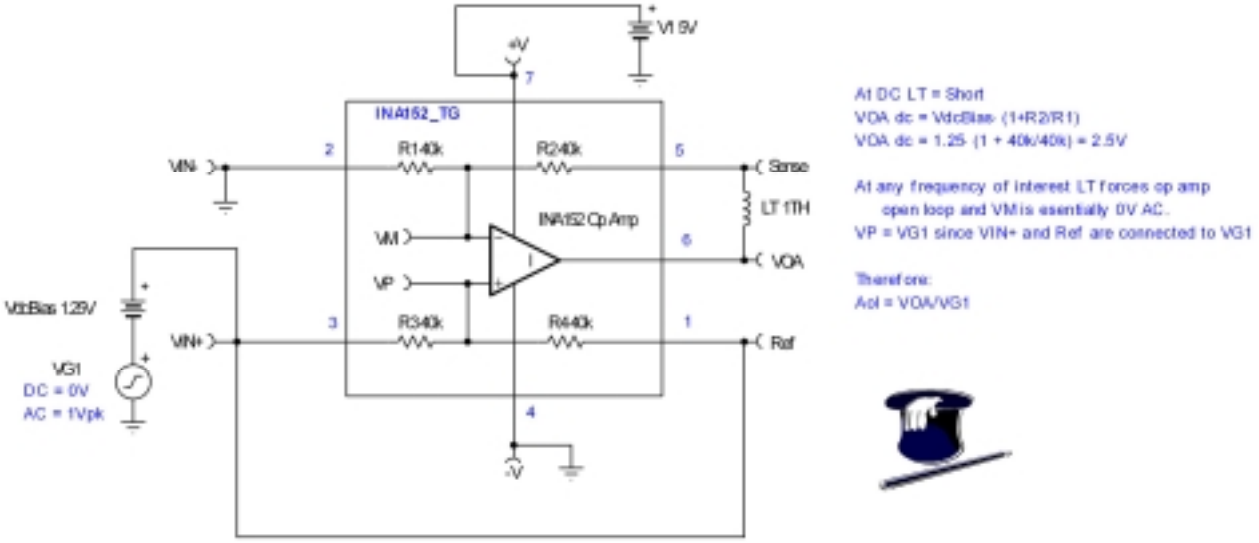


Figure 9.27: INA152 Aol Test Circuit Concept

We translate our INA152 Aol Test Circuit Concept of Figure 9.27 into a TINA Spice circuit here (see Fig. 9.28. We know that the TINA Spice macro-model for the INA152 is a Bill Sands [Consultant, *Analog & RF Models,* http://www.home.earthlink.net/%7Ewksands/] macro-model and, thus, will accurately match the real silicon.

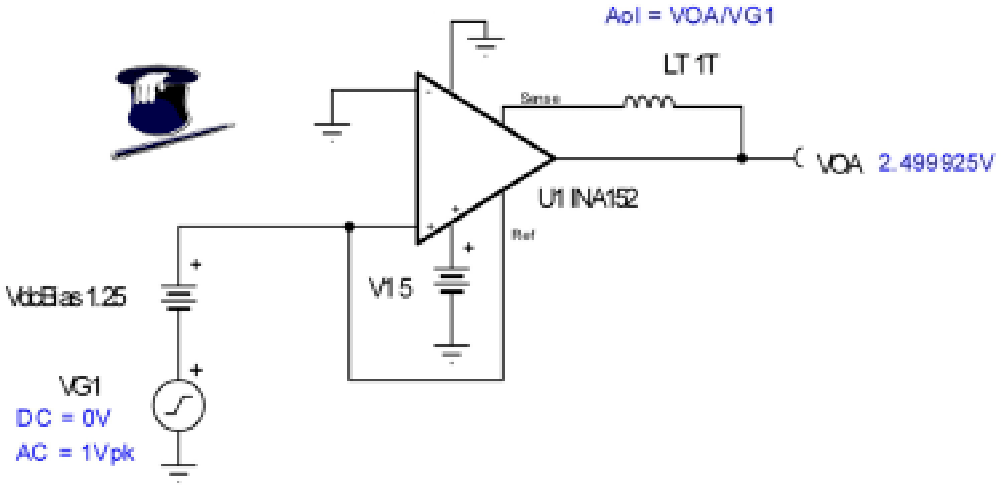


Fig. 9.28: TINA Spice INA152 Aol Test Circuit

Fig. 9.29 gives us the detailed Aol curve for the INA152 from our TINA Spice simulation. Note that there is a second pole in the Aol curve at about 1 MHz with some higher-order poles beyond that based on the Aol phase curve which, beyond 1 MHz, shows a slope steeper than –45°/decade.

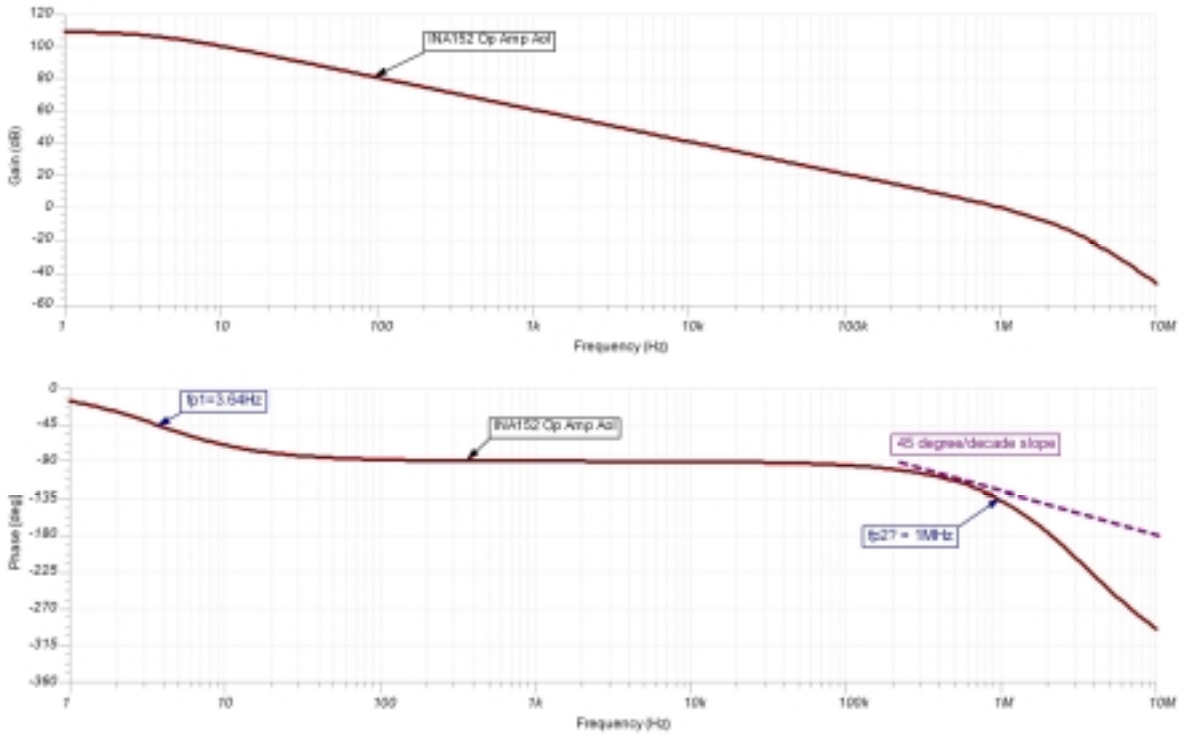


Fig. 9.29: INA152 Aol TINA Spice Results

Since we know the INA152 is a CMOS RRO difference amplifier, in addition to the Aol curve, we will need Zo to attempt any analytical stability analysis. In Fig. 9.30 we develop a Zo Test Circuit Concept. Similar to our Aol Test Circuit of Fig. 9.28, we can force the internal op amp of the INA152 to be open loop for any ac frequencies of interest through the use of LT and the circuit connections as shown. Now we will drive the output with an ac current source, set to 1 Apk, and measure Zo directly by the voltage at VOA.

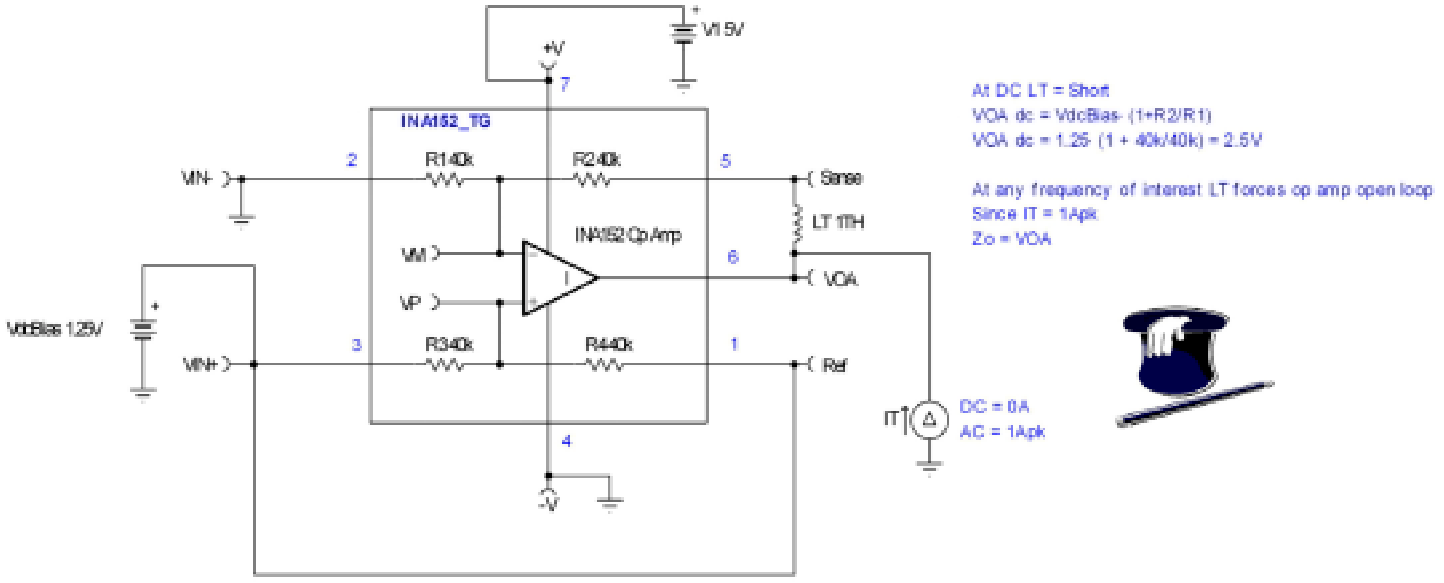


Fig. 9.30: INA152 Zo Test Circuit Concept

In Fig. 9.31 we build our TINA Spice INA152 Zo Test Circuit. A quick dc analysis confirms we are at the proper dc operating point for the INA152. It is always a good idea to perform a dc analysis before running an ac one in Spice to confirm that the circuit is not saturated at either supply rail -- causing an erroneous ac analysis results.

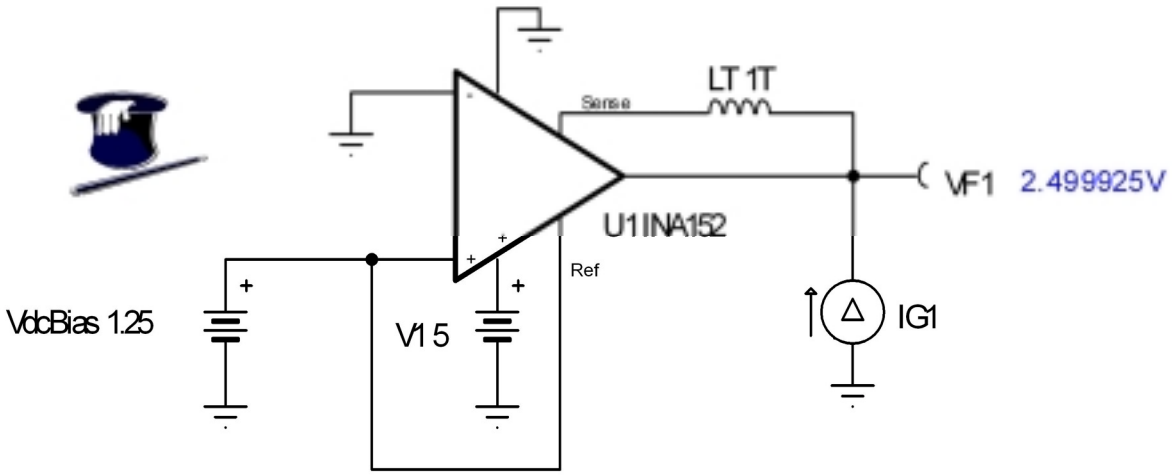


Fig. 9.31: INA152 Zo TINA Test Circuit

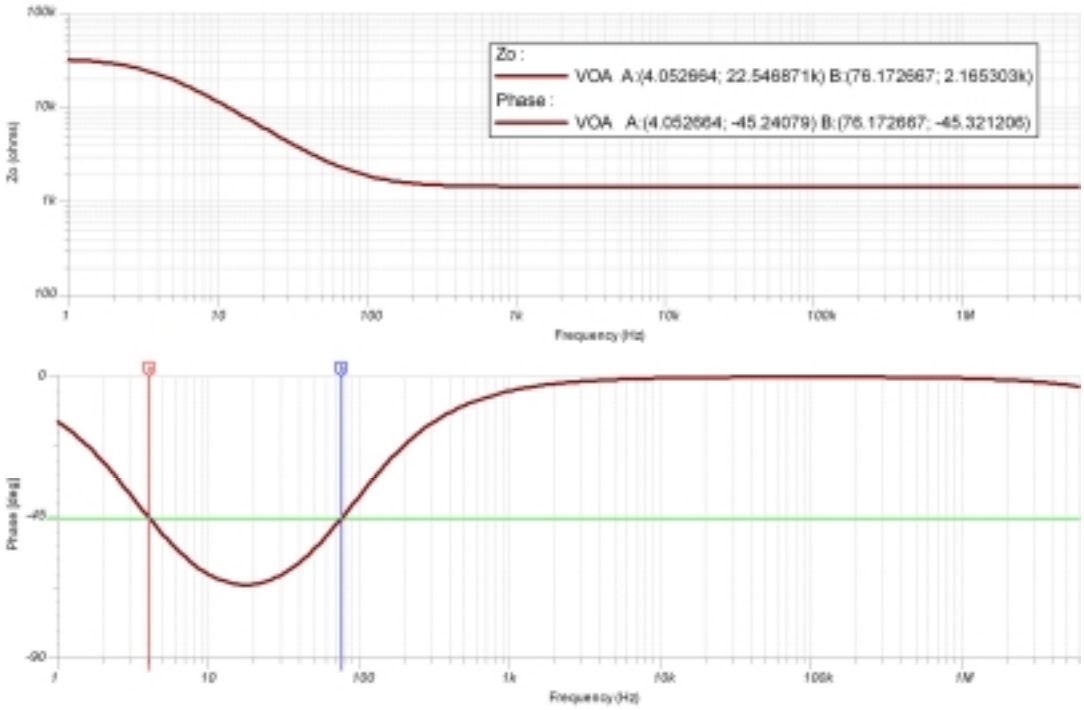


Fig. 9.32: INA152 TINA Zo Curves

The results of our TINA Zo test in Fig. 9.32 show a typical CMOS RRO response for Zo. We see a zero at fz = 76.17 Hz and a pole at fp = 4.05 Hz.

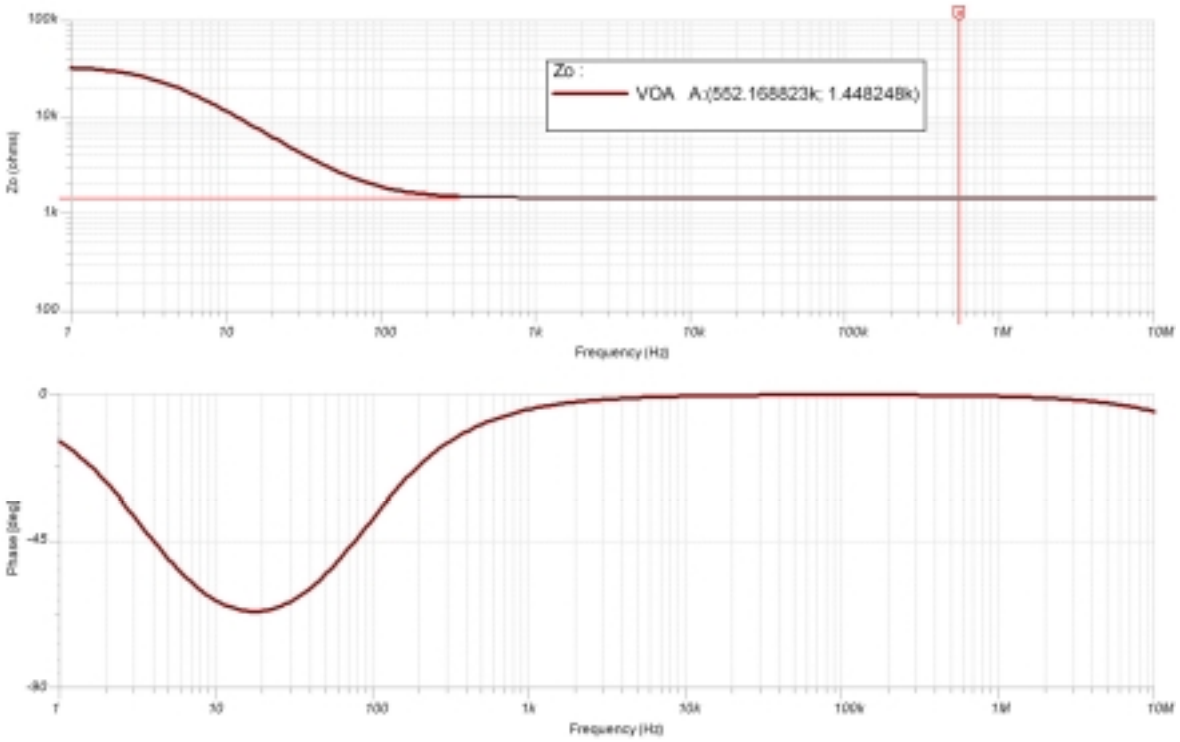


Fig. 9.33: INA152 Tina Ro Measurement

In Fig. 9.33 we measure Ro from our Zo curves created by TINA Spice. Ro = 1.45 kΩ.

From our measured Zo plots we know Ro, fz, and fp. This information allows us to build our equivalent Zo model for the INA152 (see Fig. 9.34).

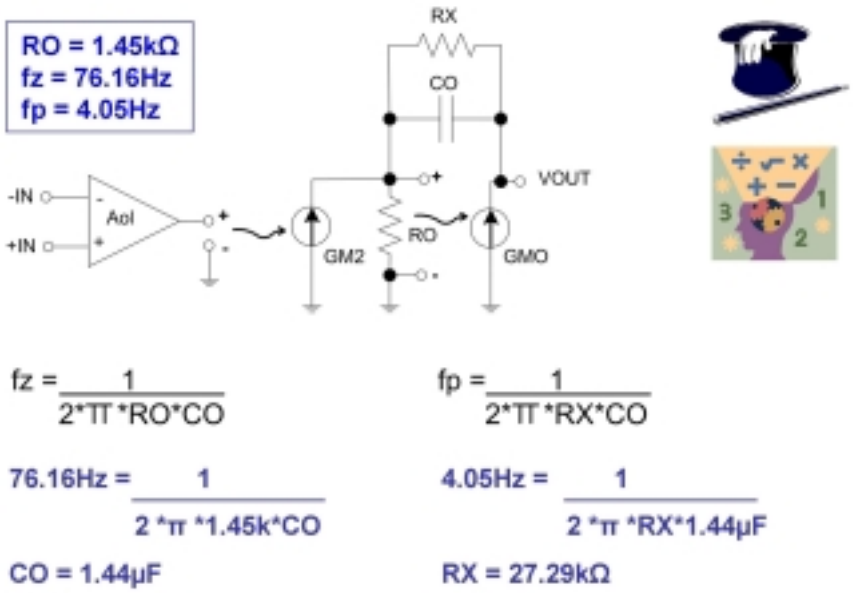
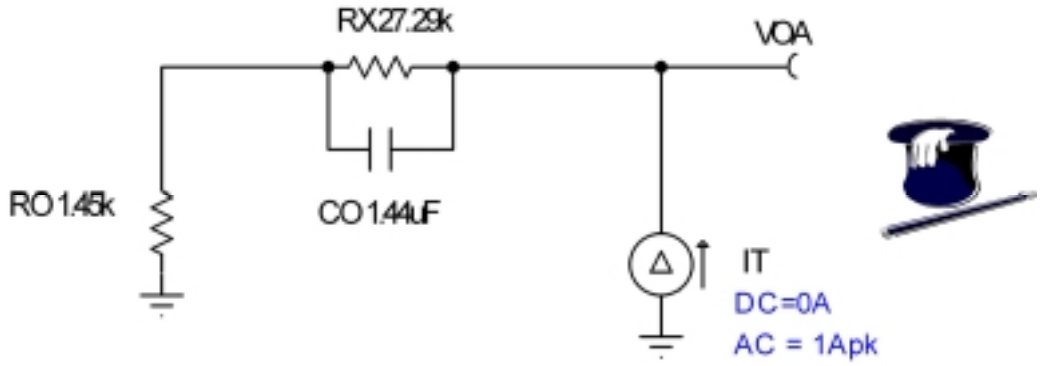


Fig. 9.34: INA152 Zo Model

We can use our TINA Spice simulator to quickly check the accuracy of our equivalent Zo model against the actual INA152 Zo. The equivalent Zo model results are shown in Fig. 9.36 with a comparison shown in Fig. 9.35. We see that our equivalent Zo model is close enough to proceed with our stability analysis.



Zo	fz	fp
INA152 Measured	76.16Hz	4.05Hz
Equivalent Model	71.2Hz	4.56Hz

Fig. 9.35: Zo Equivalent Model Vs INA152 Zo

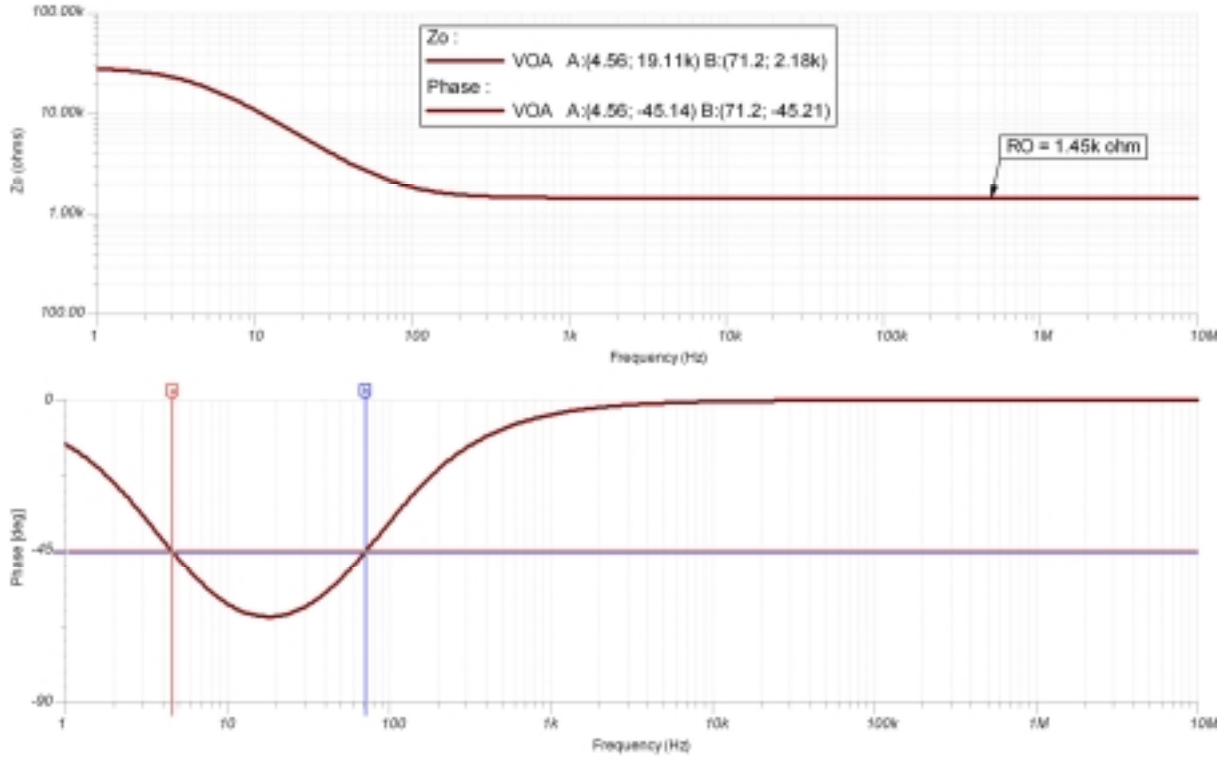
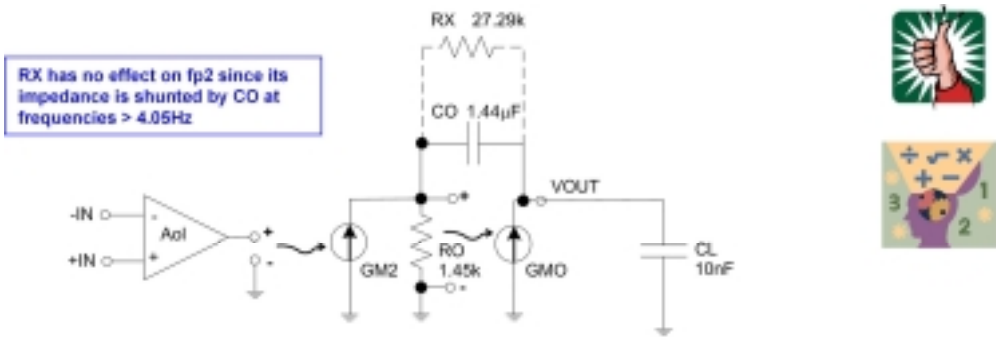


Fig. 9.36: TINA Plots: Equivalent ZO Model for INA152

We can now analyze the effect of load capacitance, CL, on the output of the INA152 using our Zo equivalent model. We see an additional pole in the Aol curve at 10.98 kHz as shown in Fig. 9.37.



$$fp2 = \frac{1}{2*TT*Ceq*RO} \qquad fp2 = \frac{1}{2*TT*10nF*1.45k} = 10.98kHz$$

where: $Ceq = \frac{CO * CL}{CO + CL}$

CL<1.44µF CL dominates: Ceq ≈ CL

CL>1.44µF CO dominates: Ceq ≈ CO

remember:

1) capacitors in series are like resistors in parallel
2) XC = 1/sC
3) XCeq = 1/sCO +1/sCL
4) Ceq = 1/XCeq

Fig. 9.37: Computing The Pole (fp2) Due To Zo And CL

In Fig. 9.38 we add the CL of 10 nF to our equivalent Zo model for the INA152.

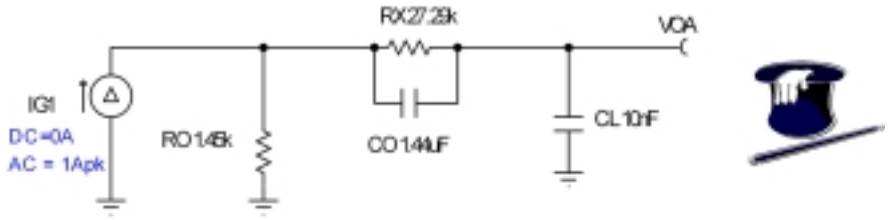


Fig. 9.38: TINA Circuit For Analysis Of fp2

From Fig. 9.39 we see the simulation results place fp2 at 11.01 kHz, which is close enough to our predicted 10.98 kHz to proceed forward.

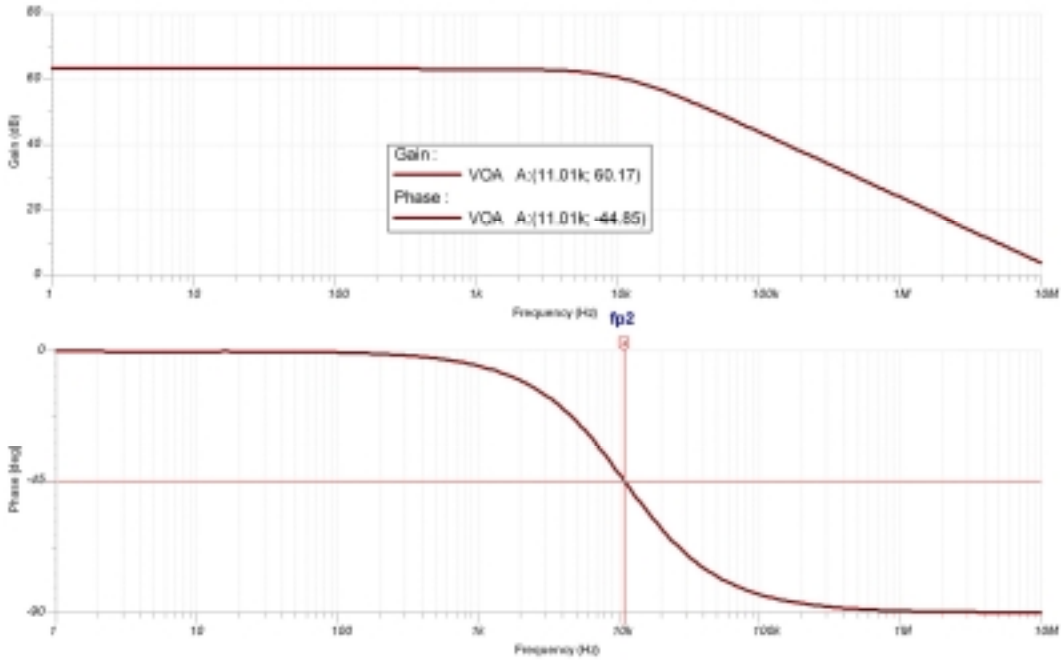


Fig. 9.39: fp2 Plot For Zo And CL = 10 nF

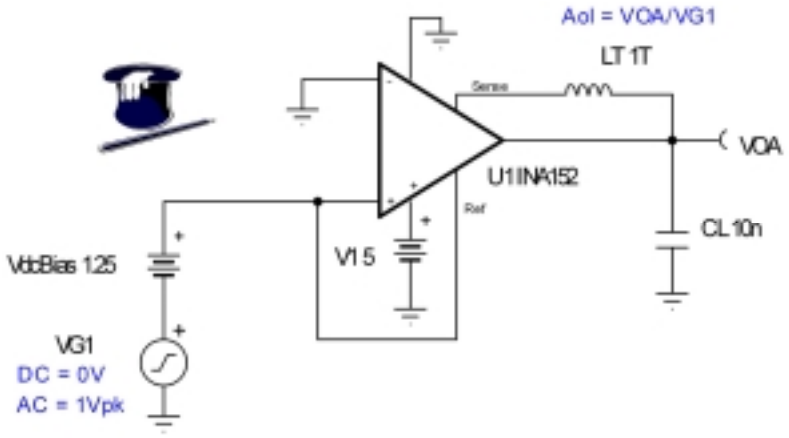


Fig. 9.40: TINA Circuit For Modified Aol Curve With CL = 10 nF

Now we can run a TINA simulation the actual INA152 with CL = 10 nF and compare it to our predicted response using the circuit of Fig. 9.40.

The TINA simulation results in Fig. 9.41 show a low frequency pole due to the INA152 op amp original Aol at 3.4 Hz (fp1) and a second pole due to Zo and CL = 10 nF at fp2 = 11.02 kHz. Remember, we predicted fp2 = 10.9 kHz by first-order analysis and fp2 = 11.01 kHz by equivalent Zo model simulated with CL = 10 nF.

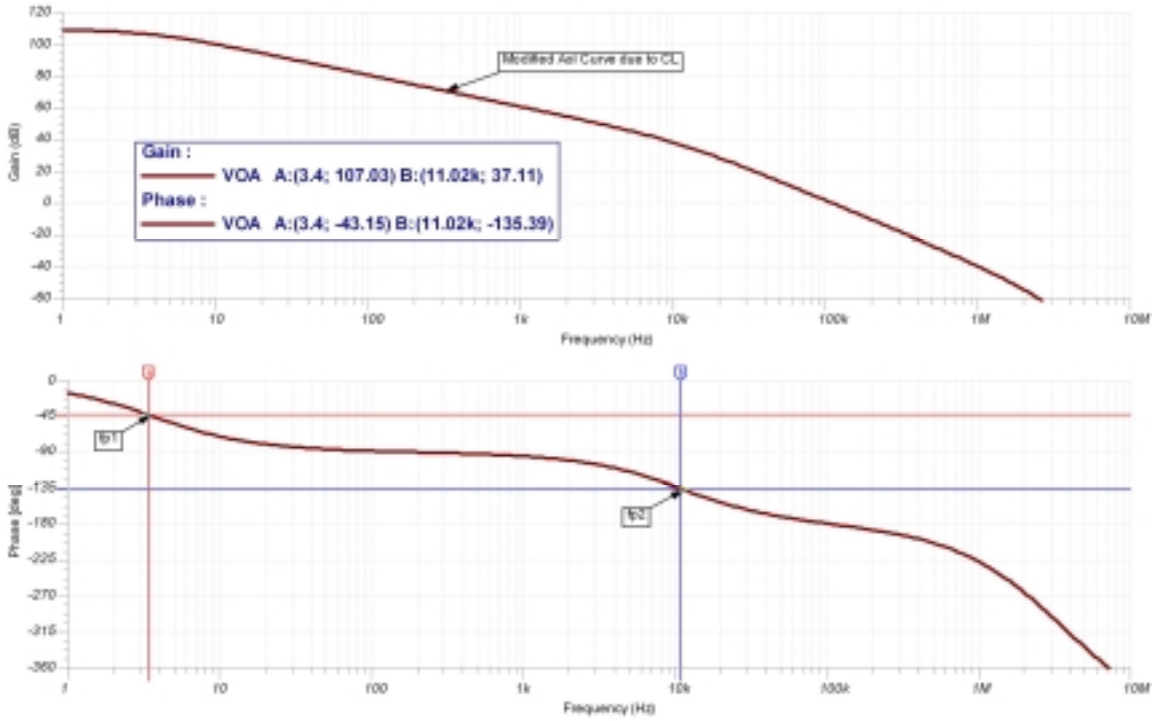


Fig. 9.41: TINA Plots For Modified Aol Curve With CL = 10 nF

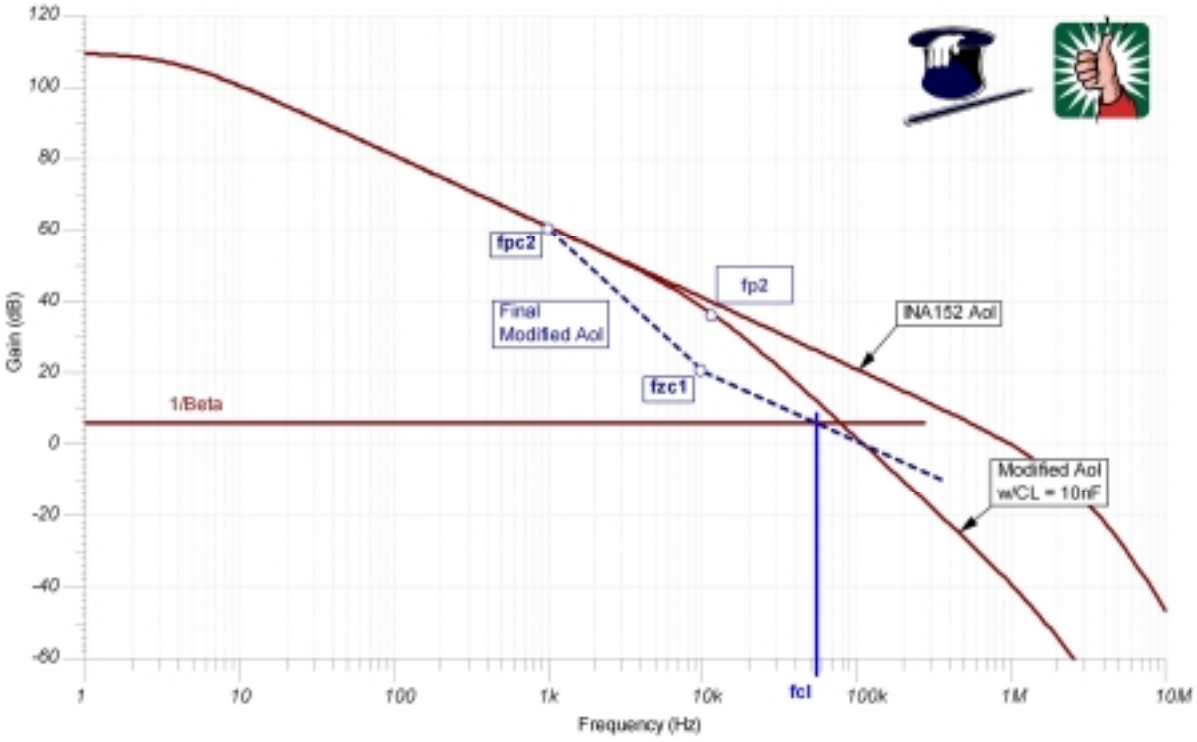
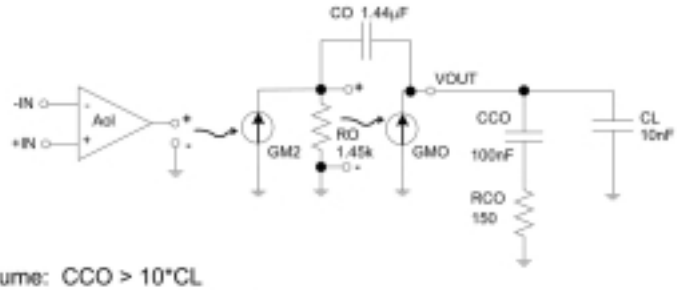


Fig. 9.42: Output Pin Compensation: CMOS RRO

In Fig. 9.42 we identify the technique for Output Pin Compensation for CMOS RRO op amps. The graphical part of this technique will be similar to that for bipolar emitter-follower op amps. First we

modify the op amp's original Aol curve with fp2, the pole due to Zo and CL (Fig. 9.41). Once this curve (modified Aol with CL = 10 nF) is created we plot a second curve (final modified Aol) which starts where the modified Aol with CL = 10 nF curve intersects 0dB. From this starting point we plot back at –20 dB/decade to a point which is one decade less than the zero dB intersection of the modified Aol curve with CL = 10 nF (100 kHz).Here at fzc1 we change the slope to –40 dB/decade. At fpc2 we intersect the original INA152 Aol curve. This proposed final modified Aol curve meets all of our rule-of-thumb criteria by keeping poles and zeros within one decade of each other to keep loop-gain phase from dipping below 45° within the loop-gain bandwidth. Our proposed final modified Aol curve also meets our first-order stability criteria of 20 dB/decade rate-of-closure at fcl.

Fig. 9.43 details the formulae based on Zo and the desired final modified Aol curve. In addition, we notice another high-frequency pole due to RCO interacting with CL when CCO becomes a short.



Assume: CCO > 10*CL
Set: fpc2 = 1kHz, fzc1 = 10kHz

$$fpc2 = \frac{1}{2*\pi*Ceqo*RO} \qquad fpc2 = \frac{1}{2*\pi*CCO*1.45k} = 1kHz$$

CCO = 109.76nF → use 100nF

where: $Ceqo = \frac{CCO * CL}{CCO + CL}$

CCO < 1.44µF CCO dominates: Ceqo ≈ CCO

$$fzc1 = \frac{1}{2*\pi*Ceqo*RCO} \qquad fzc1 = \frac{1}{2*\pi*100nF*RCO} = 10kHz$$

RCO = 159.15Ω → use 150Ω

where: $Ceqo = \frac{CCO * CL}{CCO + CL}$

CCO < 1.44µF CCO dominates: Ceqo ≈ CCO

At High Frequency CCO becomes a short
Another pole, fpc3 is formed by RCO and CL

$$fpc3 = \frac{1}{2*\pi*CL*RCO} \qquad fpc3 = \frac{1}{2*\pi*10nF*150} = 106kHz$$

Fig. 9.43: Output Pin Compensation Formulae: CMOS RRO

In Fig. 9.44 we build a TINA Spice circuit to confirm our formulae, which predict effects on the Aol curve due to Zo, CCO, RCO, and CL.

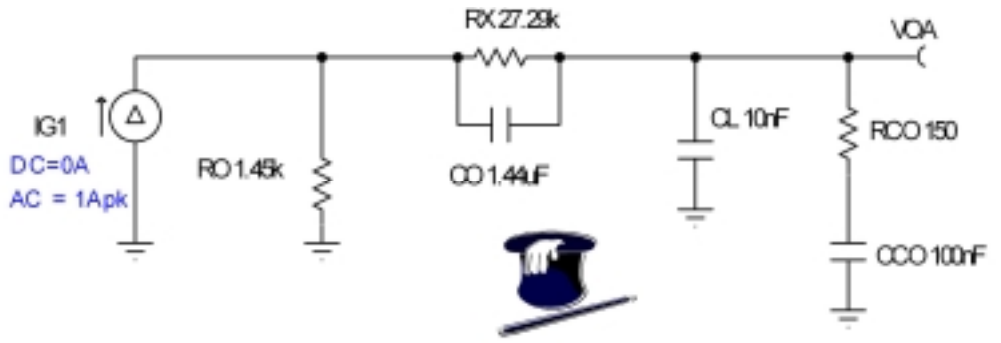


Fig. 9.44: TINA Circuit For Modified Aol Effects By Zo, CCO, RCO, CL

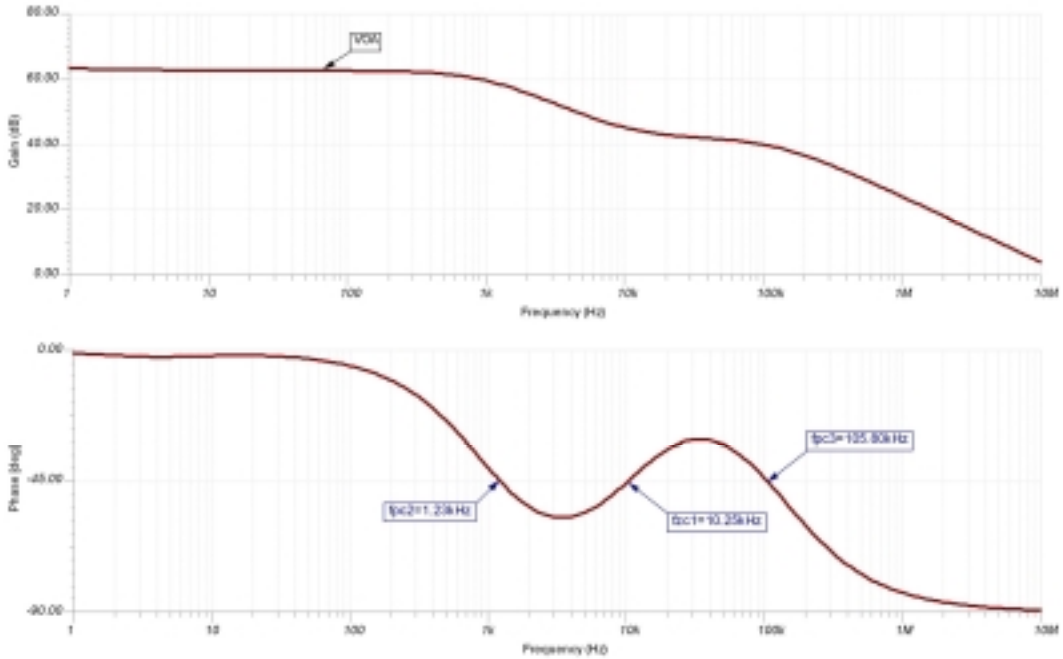


Fig. 9.45: Modified Aol Effects By Zo, CCO, RCO, CL

In Fig. 9.45 we see the results of simulation to check our formulae for Aol modification due to Zo, CCO, RCO, and CL. Predicted fpc2 = 1 kHz, actual fpc2 = 1.23 kHz. Predicted fzc2 = 10 kHz, actual fzc2 = 10.25 kHz. Predicted fpc3 = 106 kHz, actual fpc3=105.80 kHz. Based on our equivalent Zo model our predictions match close enough to the simulated results.

Based on our analysis of Fig. 9.43 and simulation confirmation we can create a final modified Aol prediction as shown in Fig. 9.46. The final closed-loop response, Vout/Vin, is predicted to be flat until loop gain goes to zero at fcl upon which it is expected to follow the modified Aol curve as shown.

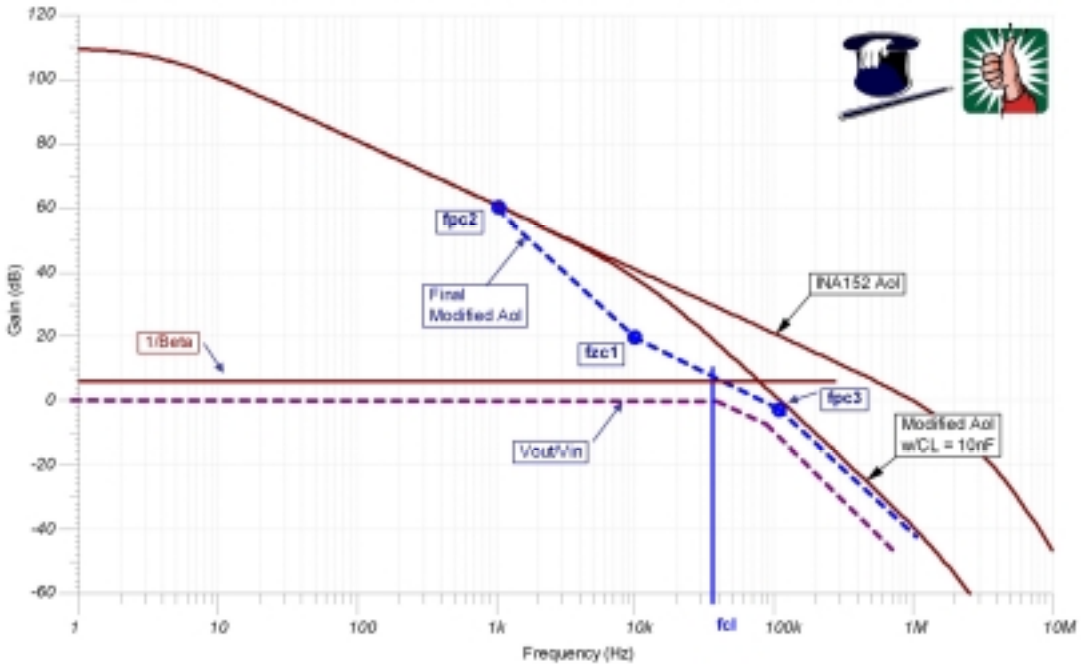


Fig. 9.46: Final Modified Aol Predictions

Our ac stability test circuit using our final Output Pin Compensation is shown in Fig. 9.47. The result will be a modified Aol curve due to the Output Pin Compensation and CL.

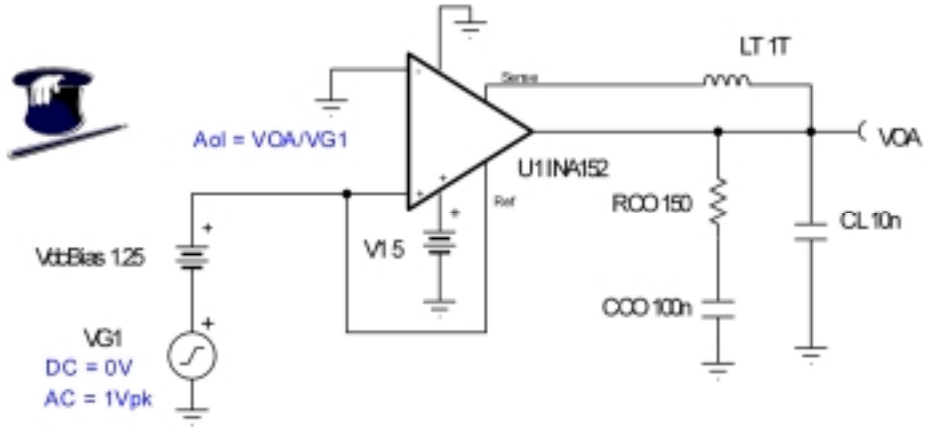


Fig. 9.47: Ac Stability Circuit: Output Pin Compensation

The results of our final modified Aol using the Output Pin Compensation technique are shown in this Fig. 9.48 and match our first-order predictions from Fig. 9.46.

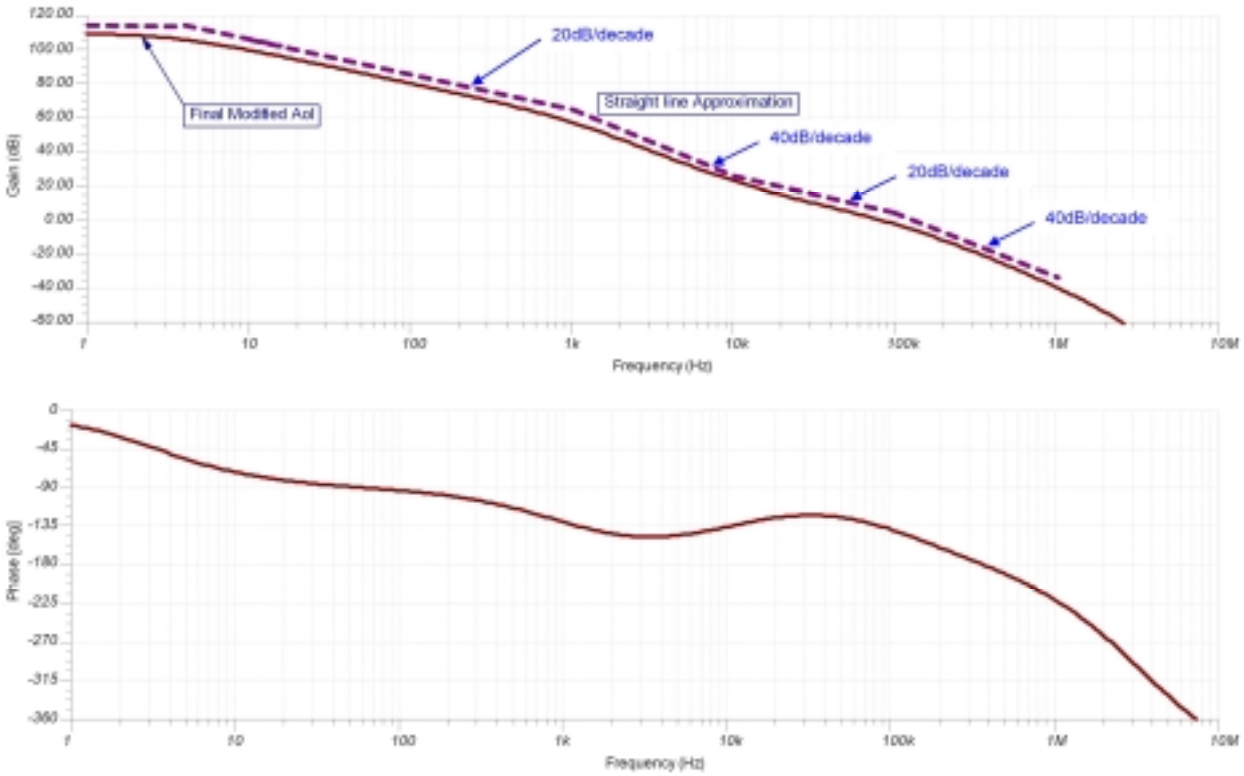


Fig. 9.48: Ac Stability Plots: Output Pin Compensation

We will use the circuit of Fig. 9. 49 to run a transient stability test with our final Output Pin Compensation in place.

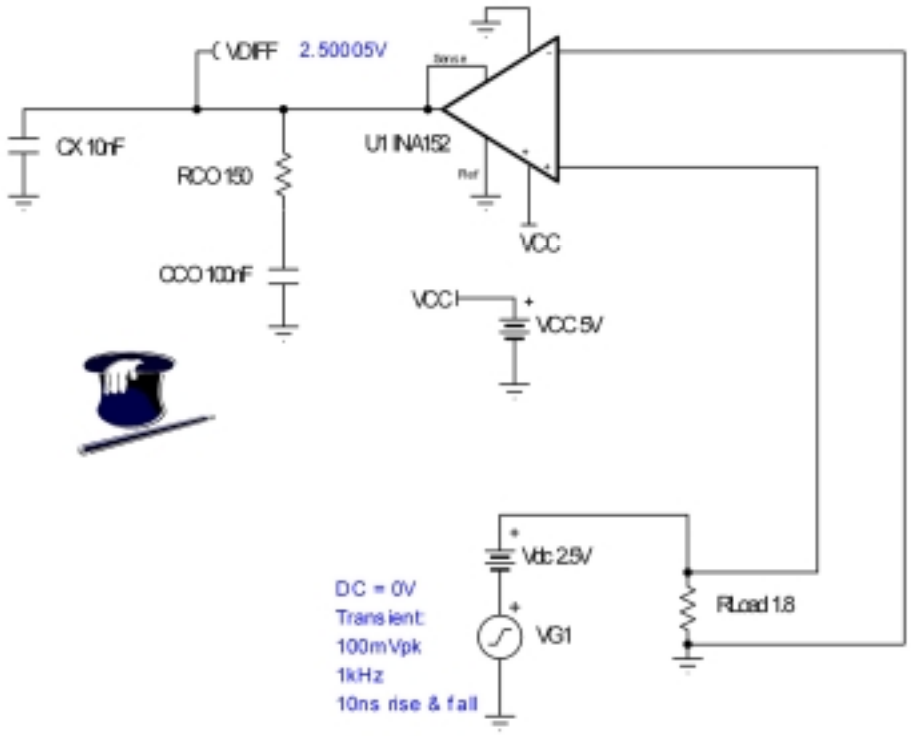


Fig. 9.49: Transient Stability Test: Output Pin Compensation

Our transient stability results (Fig. 9.50) assure us that we have properly chosen the right compensation values for the Output Pin Compensation technique on this CMOS RRO difference amplifier.

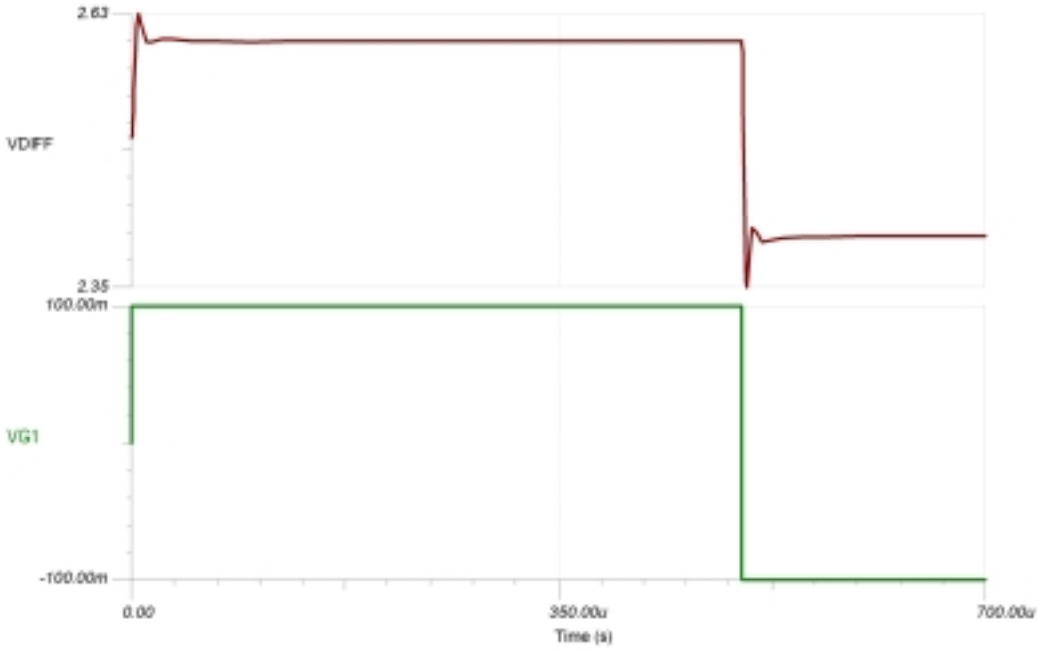


Fig. 9.50: Transient Stability Results: Output pin Compensation

TINA circuit of Fig. 9.51 enables confirmation of predicted Vout/Vin transfer function of Fig. 9.46.

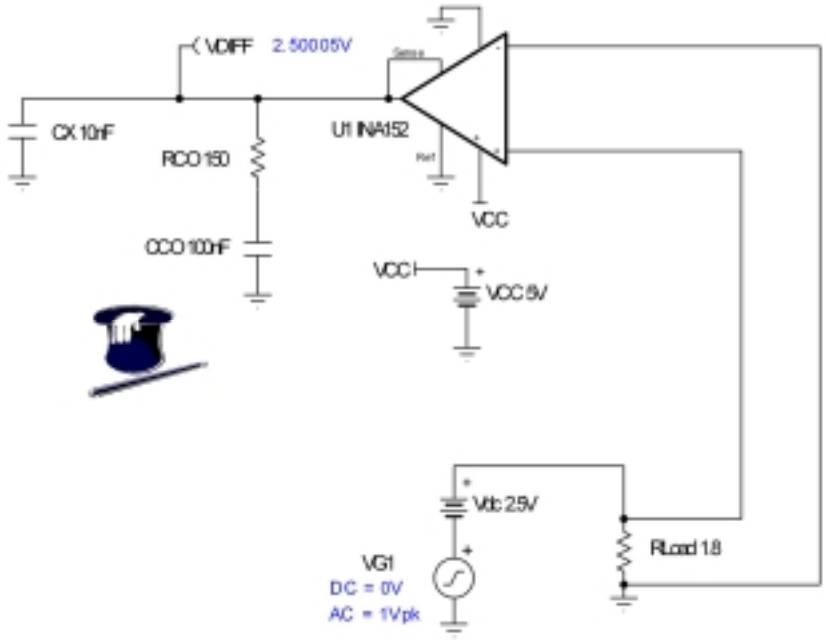


Fig. 9.51: Vout/Vin Ac Response Circuit: Output Pin Compensation

In Fig. 9.52 we see the Vout/Vin ac closed-loop response for our INA152 circuit compensated by the Output Pin Compensation technique. A comparison with Fig. 9.46 shows predicted response matching the simulated results with a roll-off in the closed-loop response plot beginning just above 35 kHz.

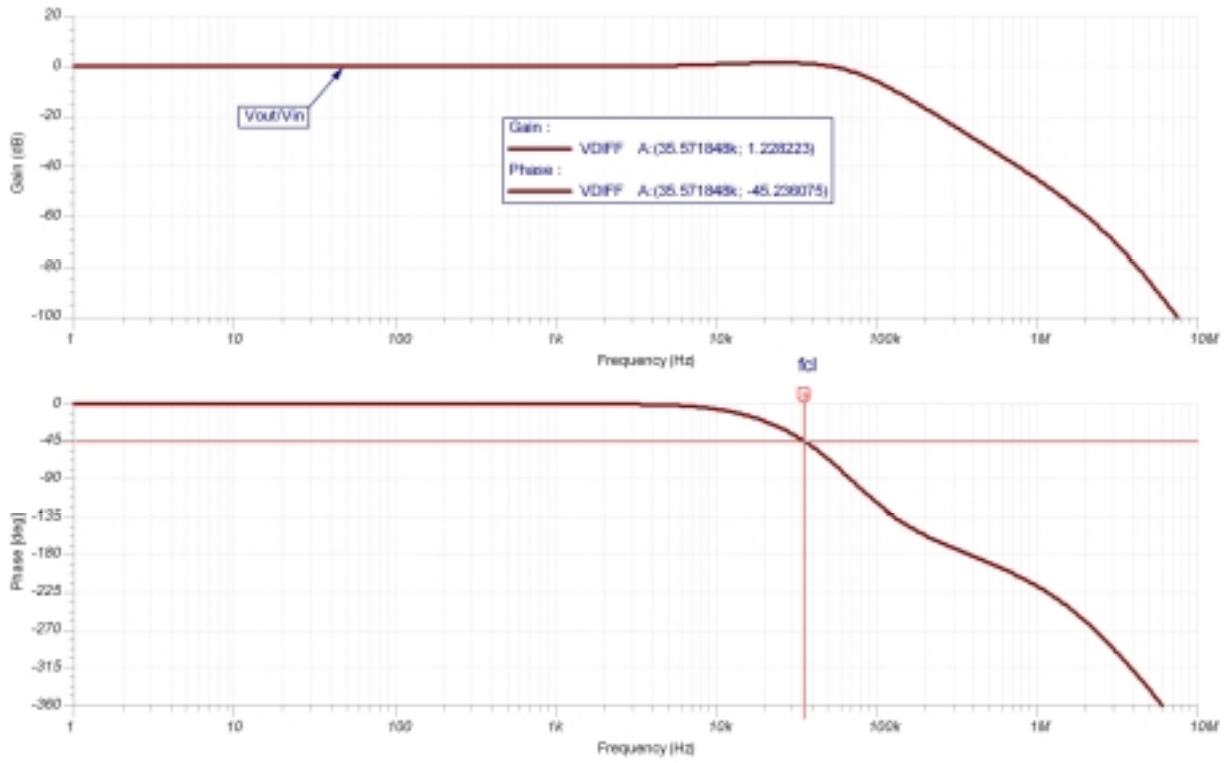


Fig. 9.52: Vout/Vin Ac Response: Output Pin Compensation

In Figure 9.53 we return to our original CMOS RRO application and add the Output Pin Compensation on the INA152, and close the entire loop to check for stability using our transient stability test.

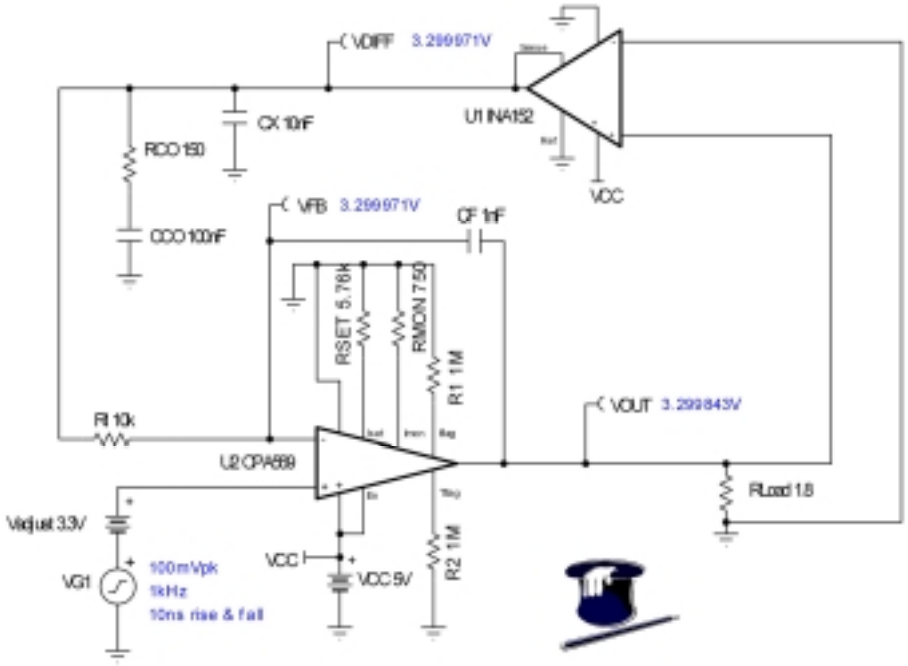


Fig. 9.53: Programmable Power Supply: Output Pin Compensation

Fig. 9.54 confirms that by fixing the capacitive load instability on the output of the INA152 through Output Pin Compensation we were able to create a stable programmable power supply.

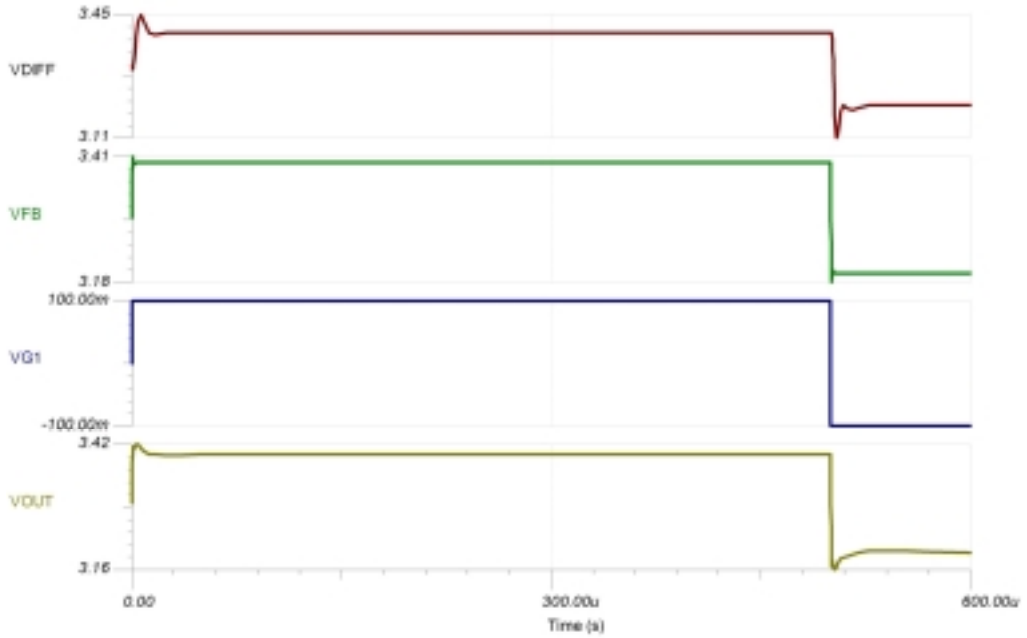


Fig. 9.54: Programmable Power Supply: Transient Stability With Output Pin Compensation

A Word About Tantalum Capacitors

When capacitor values exceed about 1 µF, many times Tantalum capacitors are used for their larger values of capacitance in a relatively small size. Tantalum capacitors are not just pure capacitance. They also have an ESR or resistive component along with smaller parasitic inductances and resistances (Fig. 9.55). The most dominant component after their capacitance is their ESR. When using the Output Pin Compensation technique for stability ensure ESR < RCO/10 to guarantee that RCO is the dominant resistance to set the zero in the modified Aol curve.

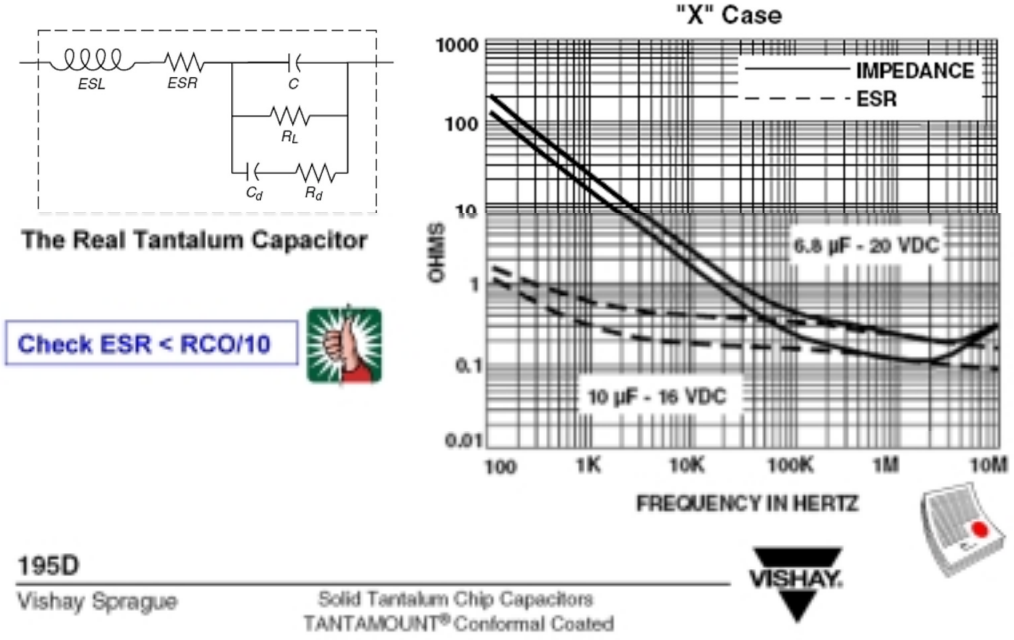


Fig. 9.55: A Word About Tantalum Capacitors And Output Pin Compensation

About the Author

After earning a BSEE from the University of Arizona in 1981, Tim Green has worked as an analog and mixed-signal board/system level design engineer for over 24 years, including brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems and CCD cameras. Tim's recent experience includes analog & mixed-signal semiconductor strategic marketing. Currently he is the Linear Applications Engineering Manager for Texas Instruments, Tucson, AZ.