Operational Amplifier Stability
Part 5 of 15: Real-World Design Of A Single Supply Buffer Circuit

by Tim Green
Strategic Development Engineer, Burr-Brown Products from Texas Instruments

This part of the series focuses on a "real-world" application where our tricks and rules-of-thumb learned up until now will pay off in helping us easily stabilize an otherwise complicated circuit. We will design a universal single-supply buffer amplifier (to buffer a 2.1 V to 4.1 V reference) capable of operating linearly from a single 5-V supply, providing high output current (> 13mA) and swinging to within 0.4 V of the rail over an operating temperature range of -40°C to +125°C. Although this circuit may be used for many applications, a brief history of what spurred this design is presented and why no off-the-shelf circuit could be found to do the job. The synthesis techniques used here to develop the component networks to provide a stable circuit will prove useful for many op amp applications.

Background

A common application of the Wheatstone Bridge Sensor in the real world is pressure measurement. Many of these pressure sensors have a dominant second order nonlinearity with applied pressure as shown in Fig. 5.1.

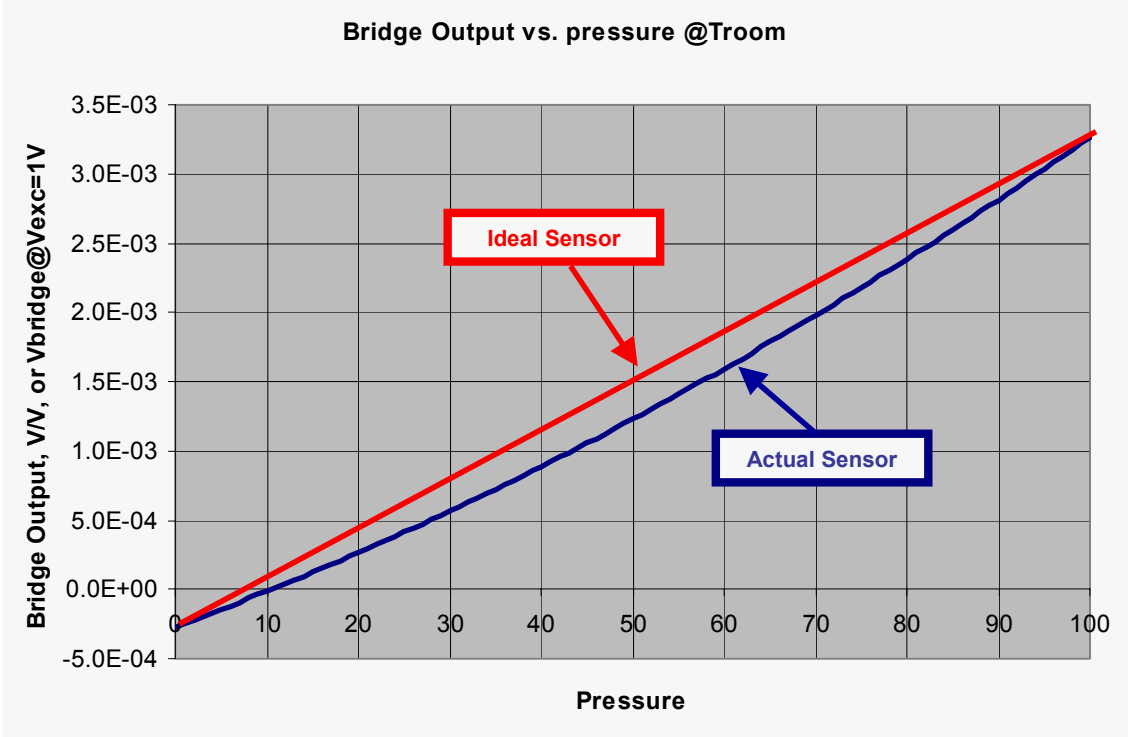


Fig. 5.1: Typical Real World Sensor Output Vs Applied Pressure

In addition to the nonlinearity with applied pressure many pressure sensors have nonlinearities of their span and offset over temperature. A modern way to calibrate these errors out is to build the electronics in with the pressure sensor and to then digitally calibrate the electronics and pressure sensor together as a module over temperature. One type of IC suited for this is the Burr-Brown Products' PGA309 from

Texas Instruments (see Fig. 5.2). This voltage output, digitally-calibrated sensor signal-conditioning IC contains an analog sensor linearization circuit which uses a portion of the output voltage fed back to the sensor voltage excitation pin to linearize a second-order nonlinearity with a 20:1 improvement. The VEXC pin will adjust its voltage with applied pressure to the sensor. One limitation with this circuitry is that pin VEXC is limited to a maximum current output of 5 mA over temperature. Herein lies our dilemma: how to excite sensors when their impedance requires more than 5 mA.

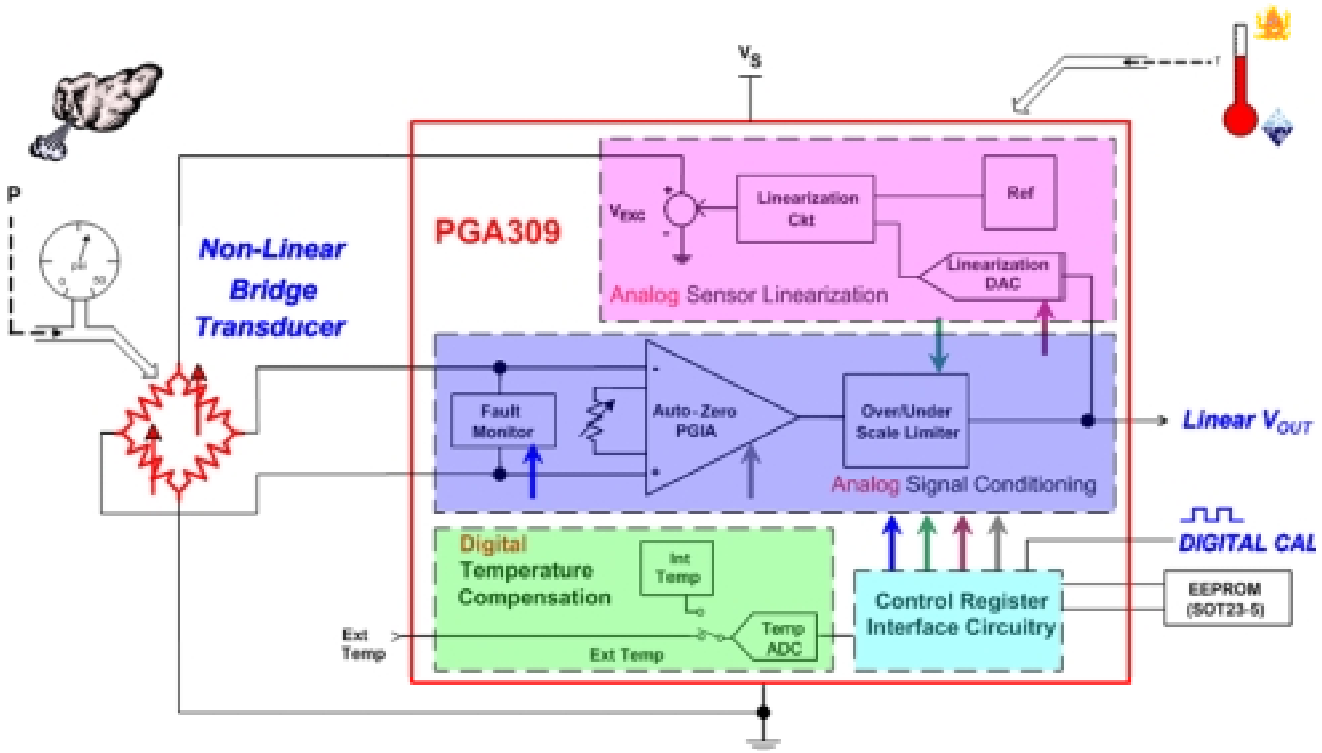


Fig. 5.2: Modern, Digitally-Calibrated Sensor Signal Conditioner

Design Requirements

The key design requirements are detailed in Fig. 5.3.

Requirements:

- Single Supply (4.5V< V_S < 5.5V)
- Unity Gain Buffer
- V_{IN} = 2.1V to 4.1V
- RL = 300Ω to 820Ω
- $I_{OUT\ MAX}$ = 13.6mA → (4.1V / 300Ω)
- Small Signal Bandwidth 100kHz
- Large Signal Slew Rate 1V/µs
- -40°C < Operating Temperature < +125°C
- No crossover distortion in CM range of Op Amp Input

Fig. 5.3: Single-Supply, High-Current Buffer Requirements

We wish to operate from a 5-V supply with a 10% tolerance. We will need a unity-gain buffer since we do not want to introduce any error in the linearization loop circuitry of the PGA309. Since the PGA309 has a wide programmability range for the VEXC pin we will need to accommodate a voltage range of 2.1 V to 4.1 V. Our minimum sensor resistance is 300Ω, so for a maximum output of 4.1 V we need to provide at least 13.6 mA. The PGA309 Linearization Circuit loop has about a 35 kHz bandwidth. Because of the way the loop gets closed we will need our buffer to have a bandwidth at least equal to or greater than the Linearization Loop Circuit. We will choose a 100 kHz small-signal closed loop bandwidth as our target. A 1 V/μs slew rate for large-signal response will be sufficient for the sensor applications we are interested in. The design must operate reliably over the temperature range of -40°C to +125°C. Since we do not want to add any extra errors in the final application due to our buffer we will need a circuit which does not exhibit any crossover distortion within the common mode input range of the op amp. This issue we will look at briefly since it is a problem for almost all CMOS single supply Rail-to-Rail Input (RRI) op amps.

The traditional approach for RRI op amps uses n-channel and p-channel MOSFETs in parallel to achieve swing beyond the rails. The problem is that there is a transition zone where both pairs of transistors are on (see Fig. 5.4). The PSR, CMR, offset voltage, and offset drift are abnormal in this region. The modern approach uses a patent-pending, low-noise charge pump to eliminate the need for the parallel MOSFETs used in the traditional approach, and the transition zone where the offset is disturbed is eliminated. The OPA363 and OPA364 have linear offset over the entire common-mode range. The typical curves shown are for a 1.8-V supply and the changes and nonlinearities of V_{OS} with common-mode voltage get worse as the supply voltage increases to +5 V. So, for best linearity with common-mode input voltage we will use the OPA364.

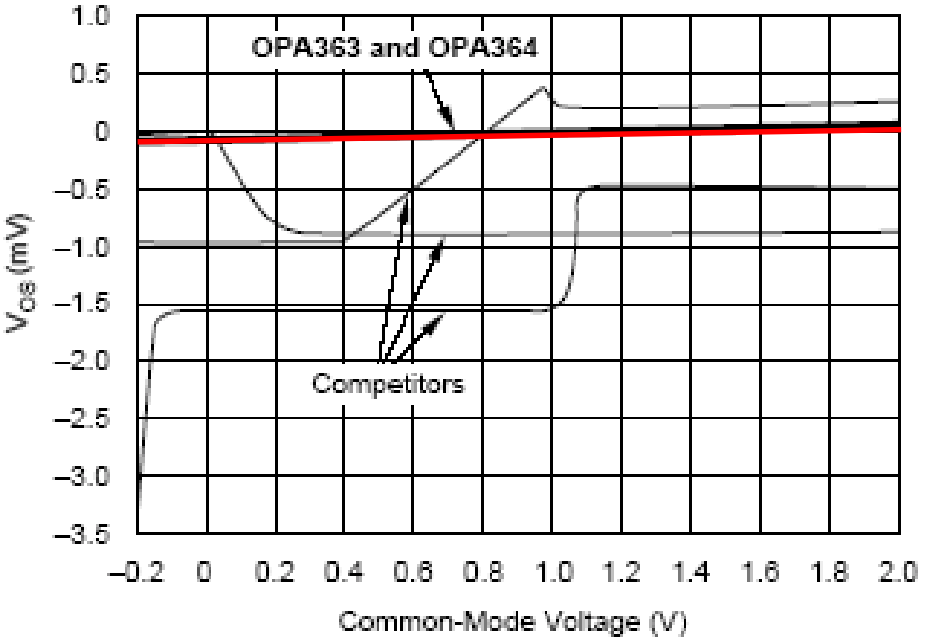


Fig. 5.4: Single-Supply, RRI Op Amp V_{OS} Vs Common-Mode Input

Some key specifications for the OPA364 are shown in Fig. 5.5.

OPA364 RRIO Op Amp

Supply: 1.8V to 5.5V
Temp Range: -40C to +125C
Common Mode Voltage Range:
(V-)-0.1V to (V+)+0.1V
Slew Rate: 5V/µs
Gain Bandwidth: 7MHz

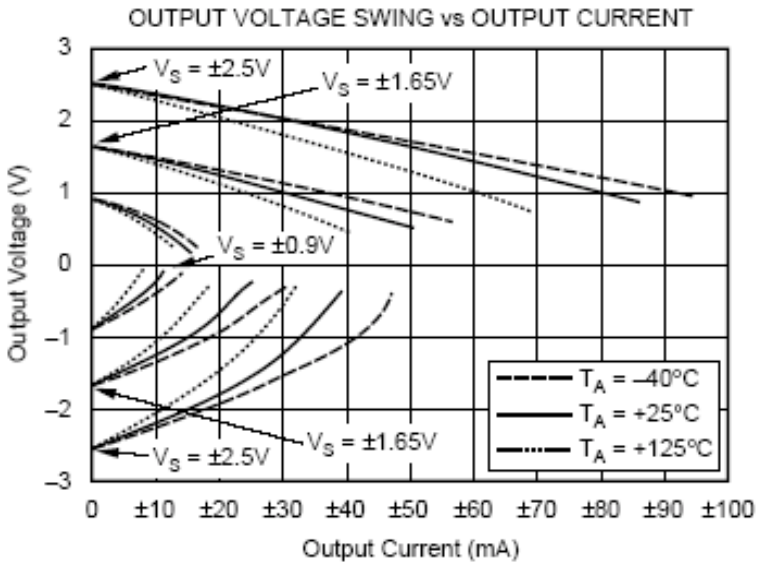


Fig. 5.5: OPA364 Key Specifications

Design Topology

Since we know we have very little voltage headroom to work with let's use a bipolar transistor instead of a MOSFET since the V_{be} of a bipolar should be around 0.65 V whereas a MOSFET gate-source voltage might be 2 V or more. We will not be able to make it using an emitter-follower configuration (see Fig. 5.6) since we run out of voltage headroom at any temperature with the worst case at -40°C.

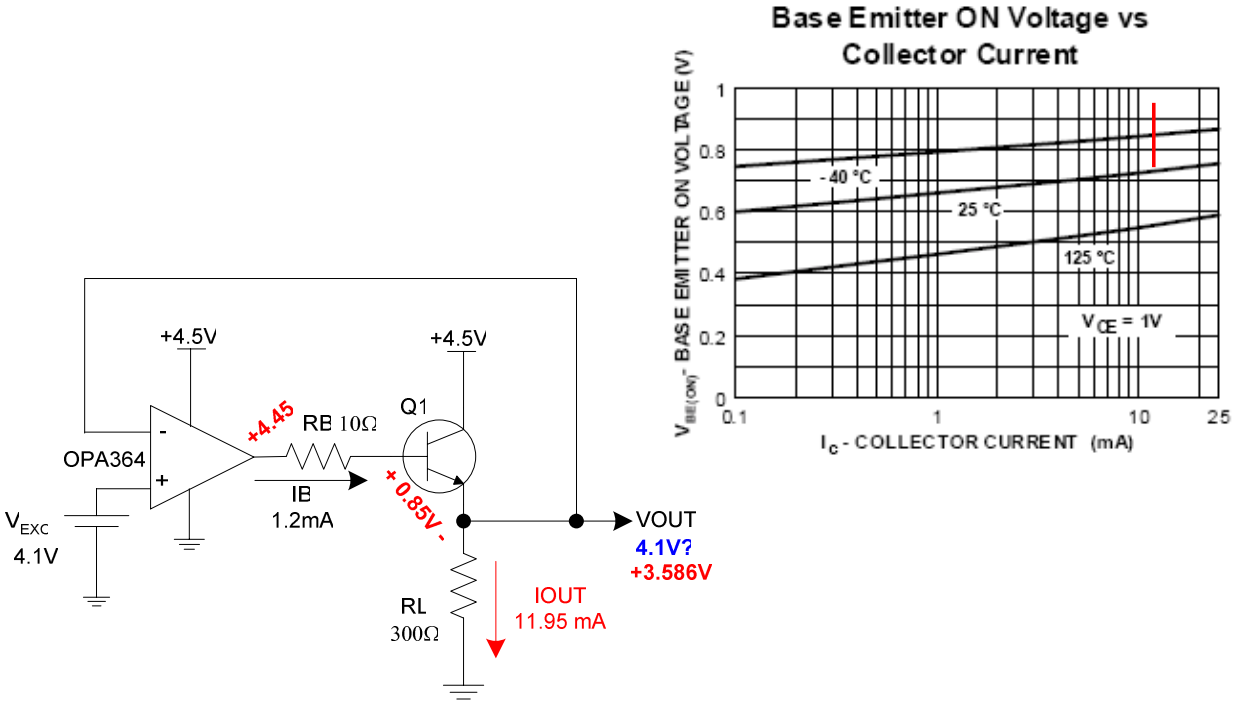
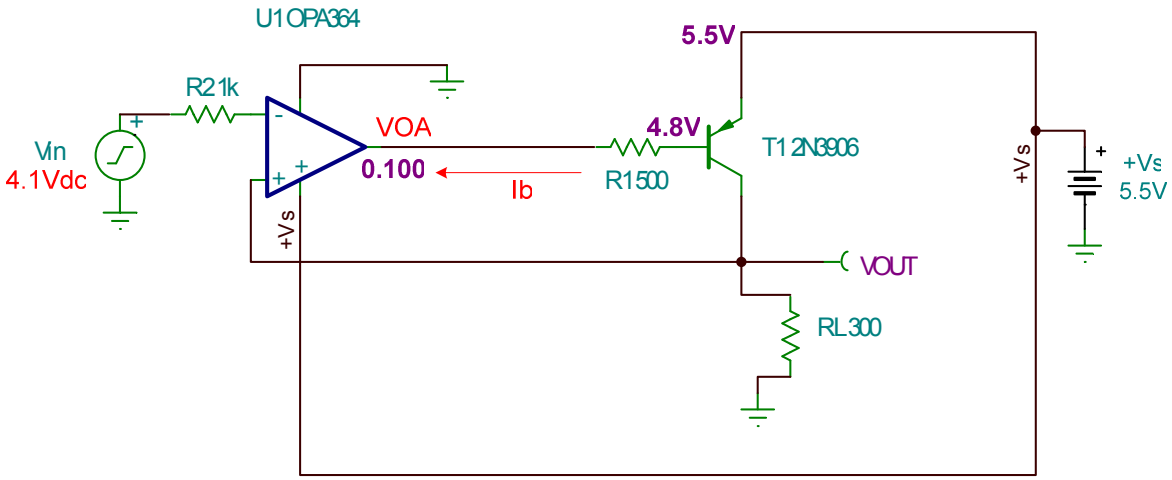


Fig. 5.6: Use Emitter Follower? – Easy to Stabilize!

Let's keep the bipolar transistor since we still have so little voltage headroom to work with, but let's change the transistor to a pnp (see Fig 5.7). As we look at this topology it seems a little bit strange. At first glance we might say it looks like positive feedback is used and oscillation is imminent! However, on closer inspection we see that we actually get a phase inversion of 180° through T1. Intuitively we see that as the output of U1 goes low, more base current is driven through T1's base and this causes more current to flow in T1's collector and through the load RL. This then causes VOUT to increase. So a decrease in the output of U1 causes an increase in VOUT. Because of this inversion our topology will use the minus input of U1 as its input and the plus input of U1 as the feedback point.



Choose PNP transitor for close swing to the rail and high current
Requires feedback into OP Amp +input due to phase inversion through transistor
Choose OPA364 for no CM crossover distortion

Assume VOA min = 0.1V
Choose R1 to limit the maximum Ib into OPA364 Output
Ib max = 4.7V / 500 oms = 9.4mA: a reasonable value
R1 also provides "isolation" between VOA and T1 base
R1 will also allow us a potential place for stability networks to be added

Fig. 5.7: Basic Buffer Amplifier Topology

We will add R1 as a means of limiting the maximum dc current the OPA364 needs to handle during startup or transient conditions. R1 will also isolate the output of the op amp from the parasitic capacitances of transistor T1 and provide one place to easily add stability networks in if we need them.

A few key parameters we will need regarding T1, a 2N3906 PNP transistor, are detailed in Fig. 5.8.

ON CHARACTERISTICS

h_{FE}	DC Current Gain *	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	60 80 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.25 0.4	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V

Fig. 5.8: T1, 2N3906, Key Parameters

1/β Analysis

A stability analysis of our buffer circuit will start by computing the dc 1/β term (see Fig. 5.9). Assume that T1 has a current gain of h_{fe} = 200. Our 300-Ω load requires 13.67 mA at 4.1 V out from our buffer circuit implying that the base current in T1 needs to be 68.35 µA. Assume a 0.7-V V_{be} drop on T1 and we see that VOA will need to be 4.2658 V to provide the necessary base current in T1. This implies that a 0.0342-V change at the output of the OPA364 will cause 13.67 mA to flow in RL so we can calculate a voltage related β term for this circuit, which is computed to be 119.88. For dc 1/β this implies a -41.5 dB value. For most op amp circuits 1/β is normally a positive number but the techniques we have developed are still valid and will allow us to analyze this topology. By adding gain in the feedback path of the op amp circuit we are creating a negative 1/β value. We know there are parasitic capacitances in the transistor T1 which we guess would add some high-frequency poles in the feedback path and therefore zeros in the 1/β plot. However, it is not readily apparent from the data sheet of the device, or after a long discussion with a veteran IC designer how to easily determine how these capacitances reflect in our loop analysis. So we will get the manufacturer's SPICE transistor model and use Tina SPICE to show us where they are located.

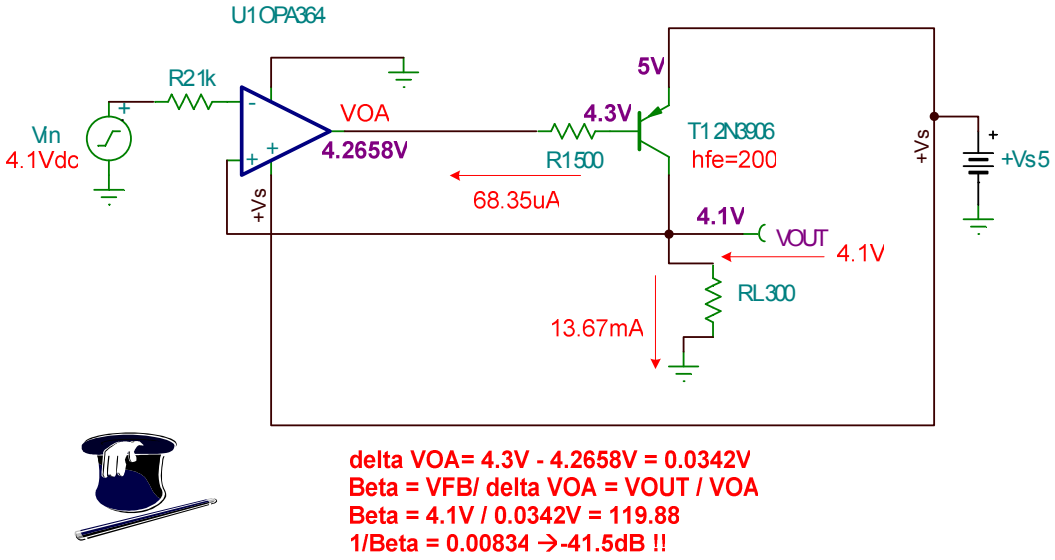


Fig. 5.9: What Is Dc 1/β?

Our Tina SPICE circuit to find the suspected high-frequency pole in our buffer circuit is shown in Fig. 5.10. Note that we apply a dc voltage, V1, such that transistor T1 is biased near its real-world operating point. This ensures we obtain the proper ac analysis results.

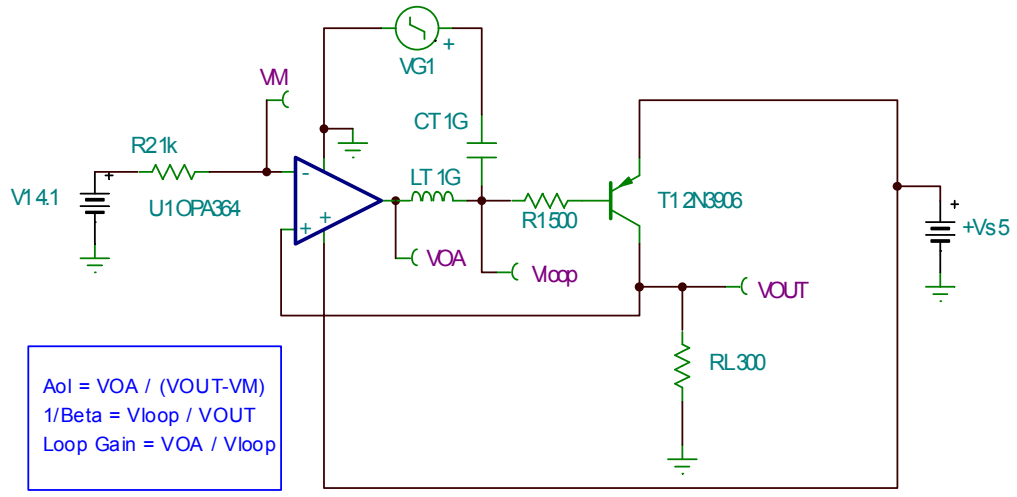


Fig. 5.10: "Where Is The High-Frequency Pole?" Circuit

The results of our simulation for finding the high-frequency pole are shown in Fig. 5.11. We notice that the dc 1/β for RL = 300 Ω is -30.89dB: we had predicted with our first order analysis -41.5dB. The simulated results, as with the real-world results, will depend upon the actual transistor used. For RL = 820 Ω simulation shows dc 1/β to be -39.6 dB. We do expect β increase (1/β to decrease) as the load increases. VOUT remains constant but as the load increases IOUT reduces and therefore both the base current and ΔVOA become less. This means VOUT/ΔVOA increase as does β while 1/β reduces (more negative dB magnitude!). We see the high-frequency pole is at about 736 kHz. For ease of our first-order analysis we will use dc 1/β to be -40 dB and the high-frequency pole to be 1 MHz. From our first order rate-of-closure criteria for stability we see that our current buffer circuit IS NOT STABLE (40 dB/decade rate-of-closure at fcl)!!

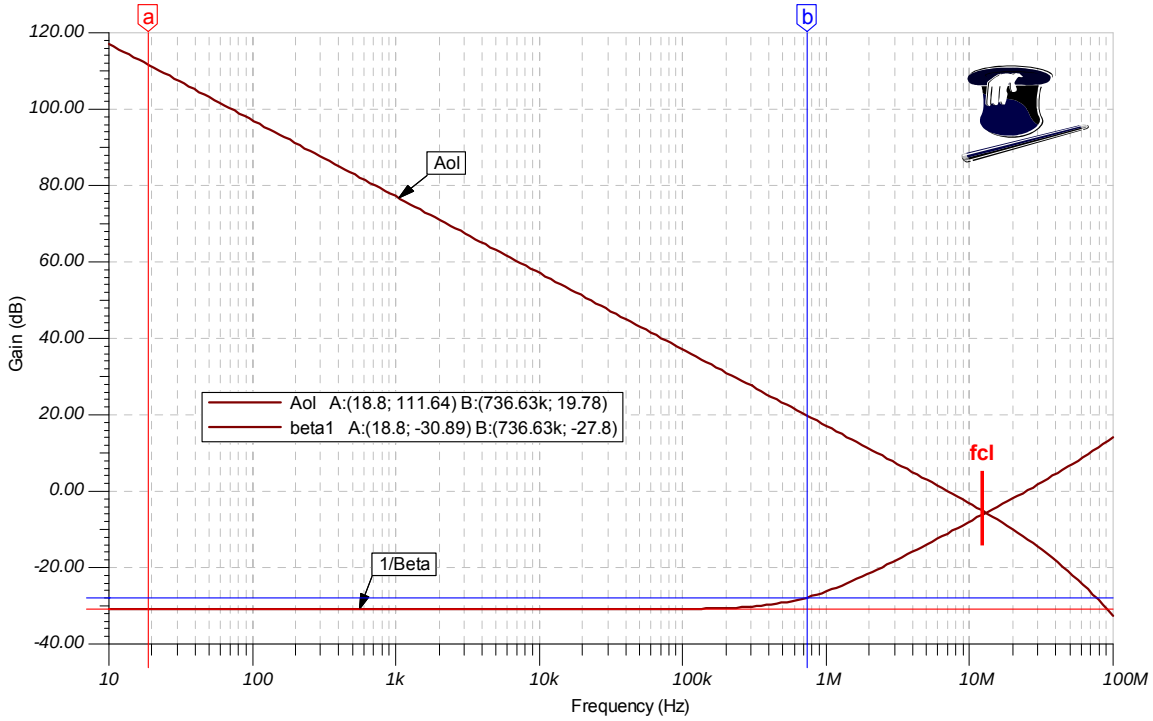


Fig. 5.11: Found The High-Frequency Pole!

As a quick check on our unstable prediction we run a Tina Transient analysis, similar to our real world stability test, on our existing buffer circuit as shown in Fig. 5.12 and find it is more than happy to oscillate as shown in Fig. 5.13!

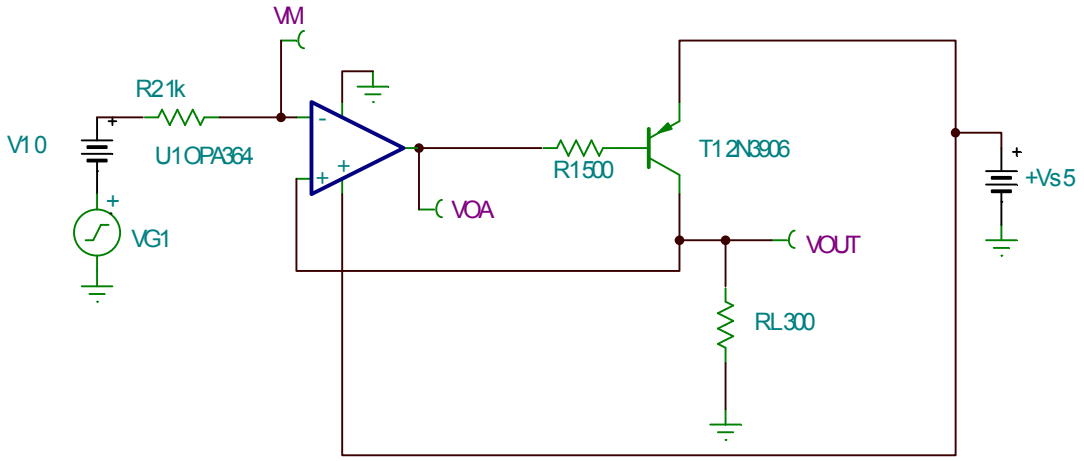


Fig. 5.12: Transient Analysis Circuit: Buffer Topology Without Compensation

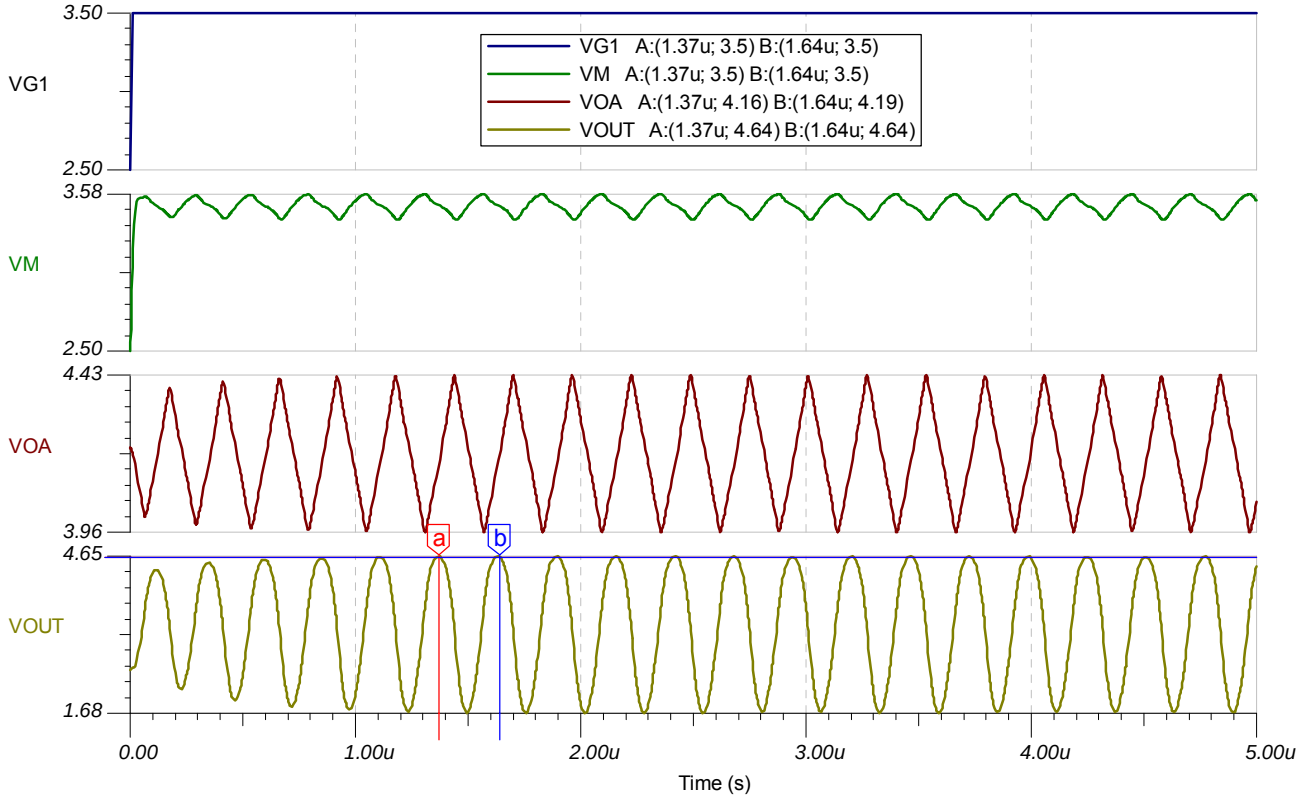


Fig. 5.13: Transient Analysis Results: Buffer Topology Without Compensation

Our buffer topology without compensation was built in the lab and the results of a 100-Hz square-wave excitation are shown in Fig. 5.14. Now we have "closed the loop" by predicting an unstable circuit from first-order analysis, then Tina SPICE simulation, and finally proving in the real world that the circuit is, as predicted, UNSTABLE. The exact frequency of oscillation is not identical to our SPICE simulation since a substitute transistor was used for T1 and if a 2N3906 was available in the lab it would not have had the exact parameters that the 2N3906 SPICE model had.

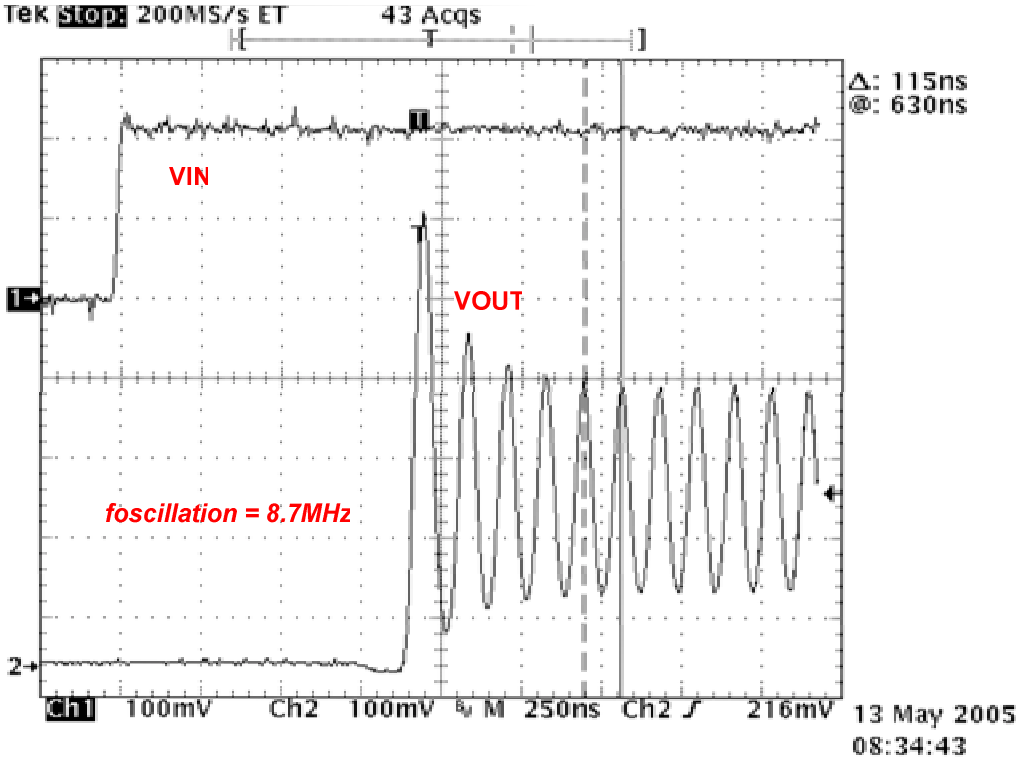


Fig. 5.14: "Real-World" Transient Instability: Buffer Topology Without Compensation

Proceeding with our stability analysis requires the Aol data sheet curve for the OPA364 (Fig. 5.15).

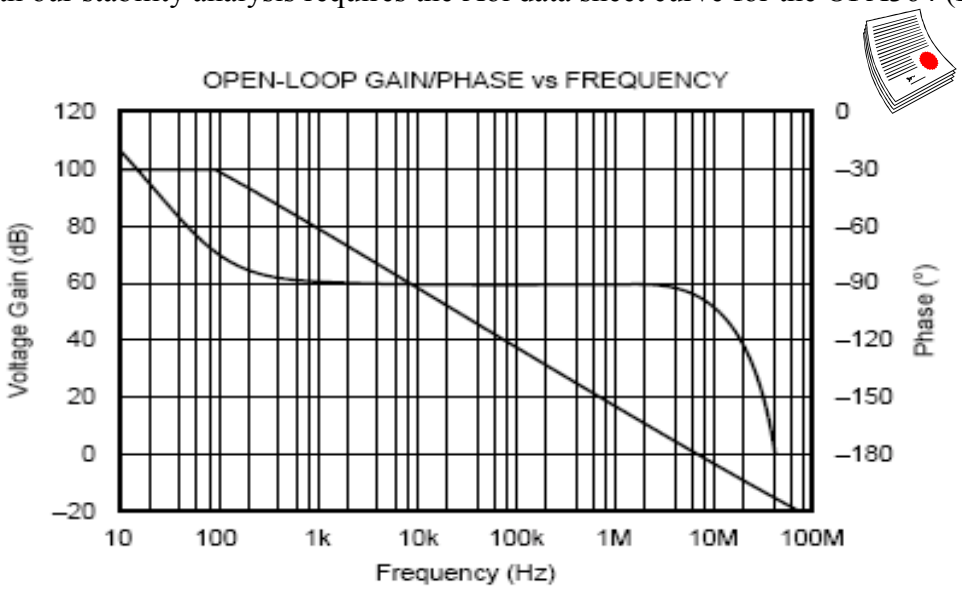


Fig. 5.15: OPA364 Data Sheet Aol Curve

From the data sheet curve we analyze (see Fig. 5.16) we analyze our buffer topology without Compensation and propose a solution using two feedback paths. The curve labeled "1/Beta w/no compensation" is the result of our dc Beta analysis and our Tina SPICE run to find the high-frequency pole. Now using our decade rules-of-thumb let's modify FB#1 which is the existing feedback of our buffer circuit. We observe that we want to get a 20 dB/decade rate-of-closure at fcl. It is a long way to go from -40 dB to 0 dB so we will take it a decade in magnitude at a time which will step us also up in frequency. Once we hit 1 MHz in the FB#1 plot we will need to add in the high-frequency pole due to the transistor capacitive parasitics (from the 1/Beta w/no compensation Curve). We have done all we can to FB#1 but notice it intersects with Aol at a 40 dB/decade rate-of-closure. Now we add a second feedback path, FB#2. If we can add it into our buffer circuit we see that it will dominate at frequencies above 1 MHz and the net 1/βplot intersects the Aol curve at a 20 dB/decade rate-of-closure!!

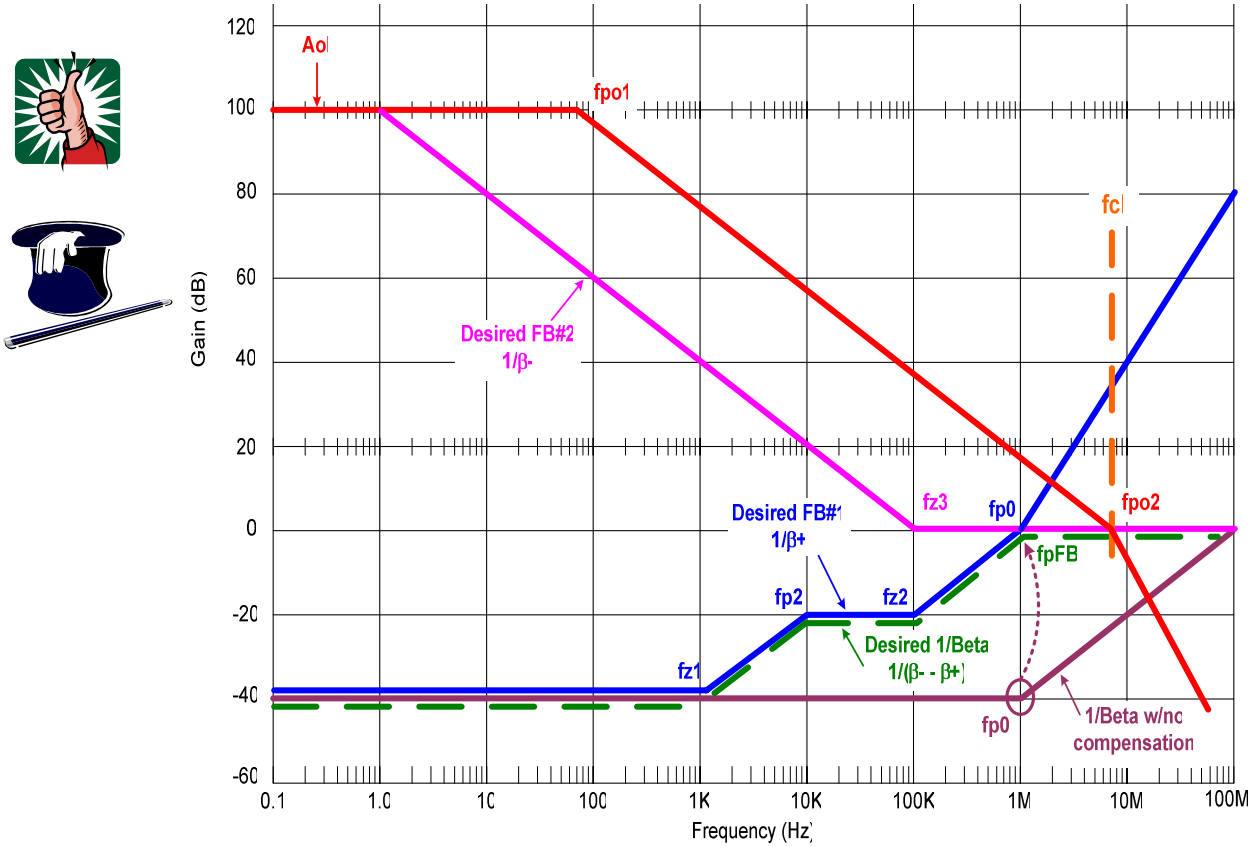


Fig. 5.16: First-Order Analysis: Aol & 1/β Plots

It may be easier for us to synthesize our desired 1/β plots into components if we convert them to β plots. That way as we "walk around" our buffer circuit in the feedback loop it may be easier to see where to add the desired poles and zeros. As shown in Fig. 5.17 we use our knowledge of the reciprocal nature of β and 1/β to plot β curves easily. In FB#2 we will need to add fZ3. In FB#1 we will need to add fz1, fp2, fz2. fp0 already exists due to the parasitic capacitances of the transistor T1.

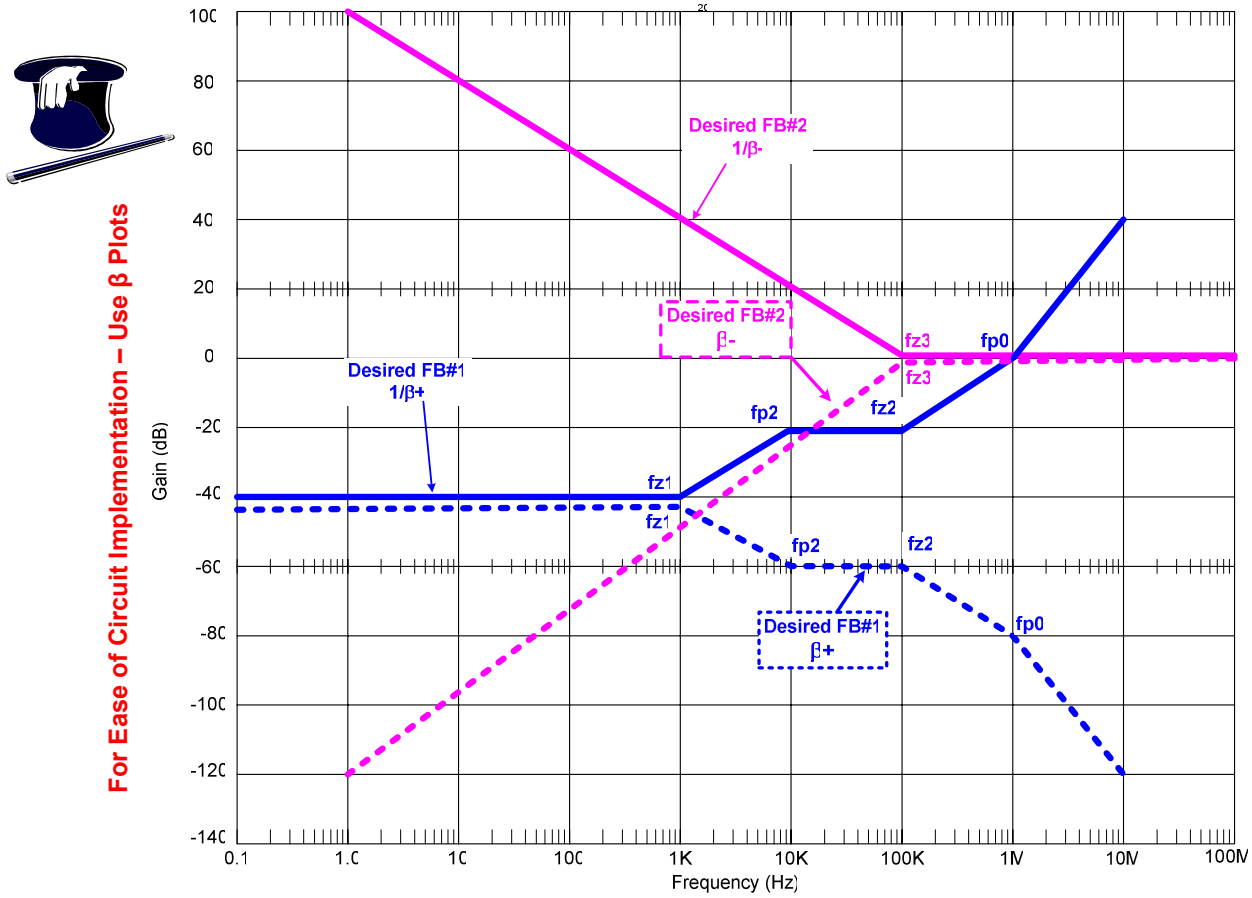
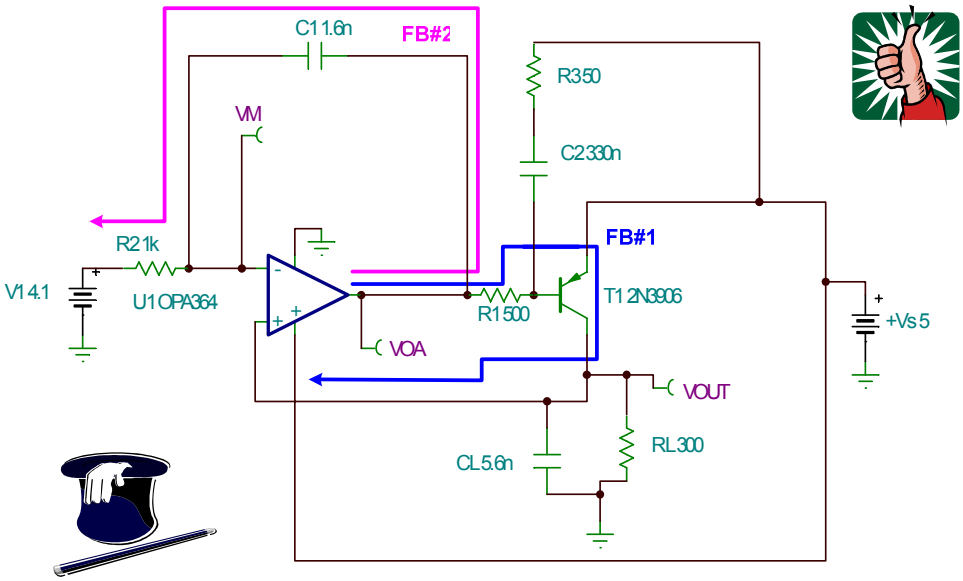


Fig. 5.17: Plot β+ from 1/β+ and β- from 1/β-

We look around FB#1 (Fig. 5.18) to see where we can easily add fz1, fp2, fz2. Since fz1 is a pole from a β+ view we can easily put it in by adding C2 and using it with the existing R1. fp2, a zero in our β+ view, can be added with R3 in series with C2. And fz2, a pole in the β+ view, is added with capacitor, CL, in parallel with the load resistor RL. CL will actually serve a great dual role: as well as helping to provide stability for our loop it will act as a local high-frequency bypass for the resistive bridge load, represented here by RL. FB#2 requires us to add fz3, a pole in the β- view. This is accomplished by adding a feedback capacitor, C1, and an input resistor, R2. For completeness we should consider if we need to include the effects of R_O, the op amp open loop output resistance in our computations for β and 1/β. R_O for the OPA364 is 160 Ω. With regards to FB#2 VOA is the midpoint between R_O and the input to the base of T1 which looks like a large impedance. With regards to FB#1 the R_O is in series with R1, 500 Ω, and is not therefore major error contribution for our first-order analysis and we can neglect its effects, checking if we are close through the use of our Tina SPICE simulation.



FB#1 (1/β+):
fz1 = 1 / (2 ·Π· R1·C2)
fz1 = 1kHz
(Pole in β+ Plot)

fp2 = 1 / (2 ·Π· R3·C2)
fp2 = 10kHz
(Zero in β+ Plot)

fz2 = 1 / (2 ·Π· RL·CL)
fz2 = 100kHz
(Pole in β+ Plot)

FB#2 (1/β-):
fz3 = 1 / (2 ·Π· R2·C1)
fz3 = 100kHz
(Pole in β- Plot)

From our Loop Stability Tricks and Rules-Of-Thumb:

Look at FB#1 (1/β+) and FB#2 (1/β-) and add poles and zeros where our desired 1/β breakpoints are. Often this is easier to do from a β+ and β- plot.

Remember a smaller V_{FB} → Smaller β → Larger 1/β

Fig. 5.18: Synthesizing Poles and Zeros for Stability

Side Note On CMOS Amplifiers & Aol

As the load on a CMOS amplifier output increases (lower load resistance) the dc portion of its Aol curve lower in value. For an OPA364 circuit (Fig. 5.19) we see a load on VOUT of 2 MΩ. In the resultant Tina SPICE simulation for Aol with this load (see Fig. 5.20) we notice that the dc Aol value extends to about 118 dB at 10 Hz which does not match the data sheet Aol curve (Fig. 5.15).

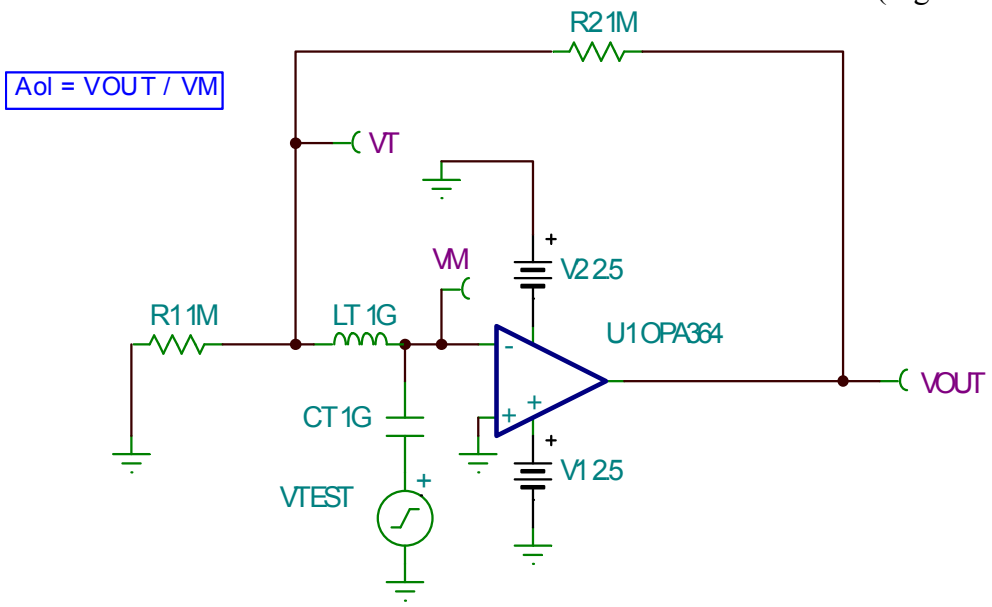


Fig. 5.19: OPA364 Aol Test Circuit With Load Of 2 MΩ

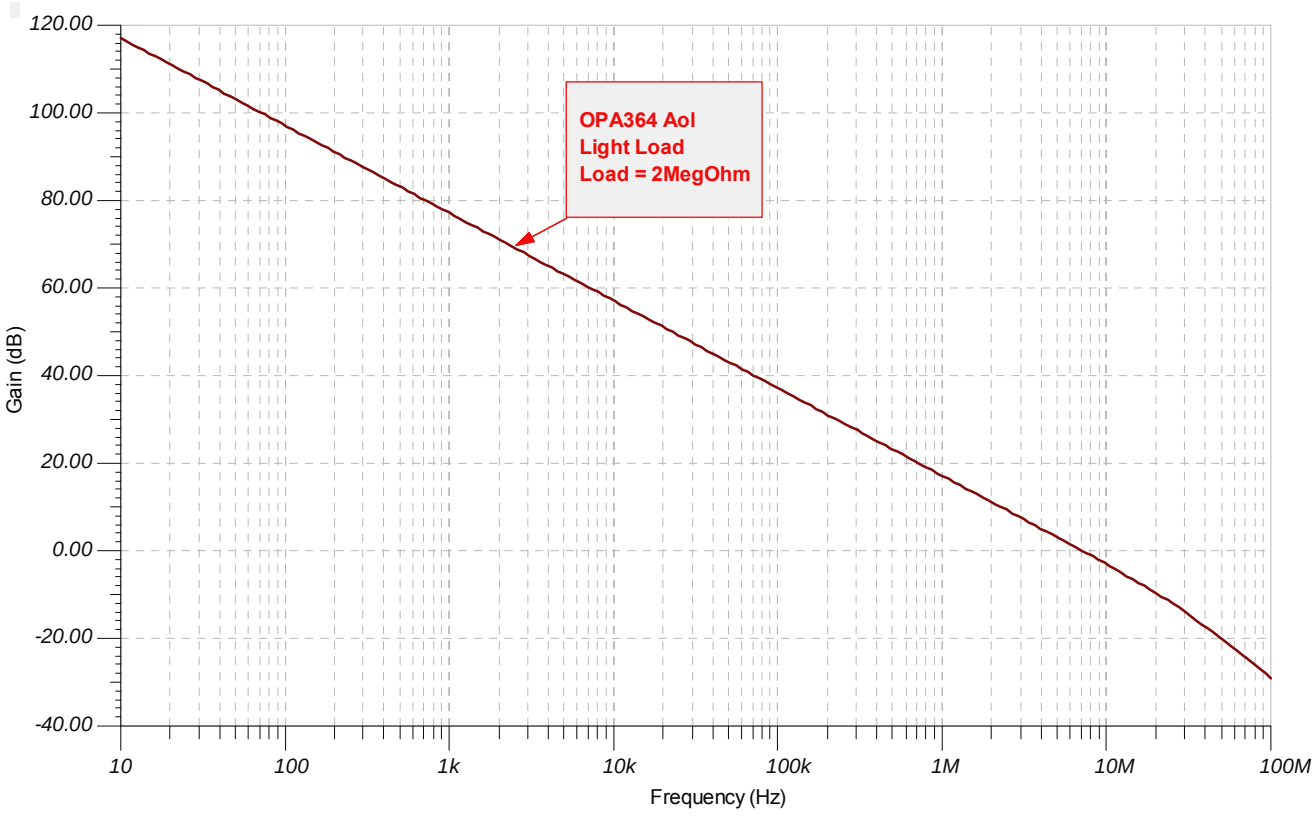


Fig. 5.20: OPA364 Aol With Load Of 2 MΩ

The circuit shown in Fig. 5.21 loads the output of the OPA364 with 10 kΩ. This is the load specified in the Aol Curve from the OPA364 data sheet and the results of our Tina SPICE simulation (see Fig. 5.22) agree and, therefore, our unloaded OPA364 Aol Curve in the analysis of our single-supply buffer is also accurate. This OPA364 SPICE model accurately models what the CMOS amplifier does in the real world with respect to Aol changes at low frequency with change in output loading.

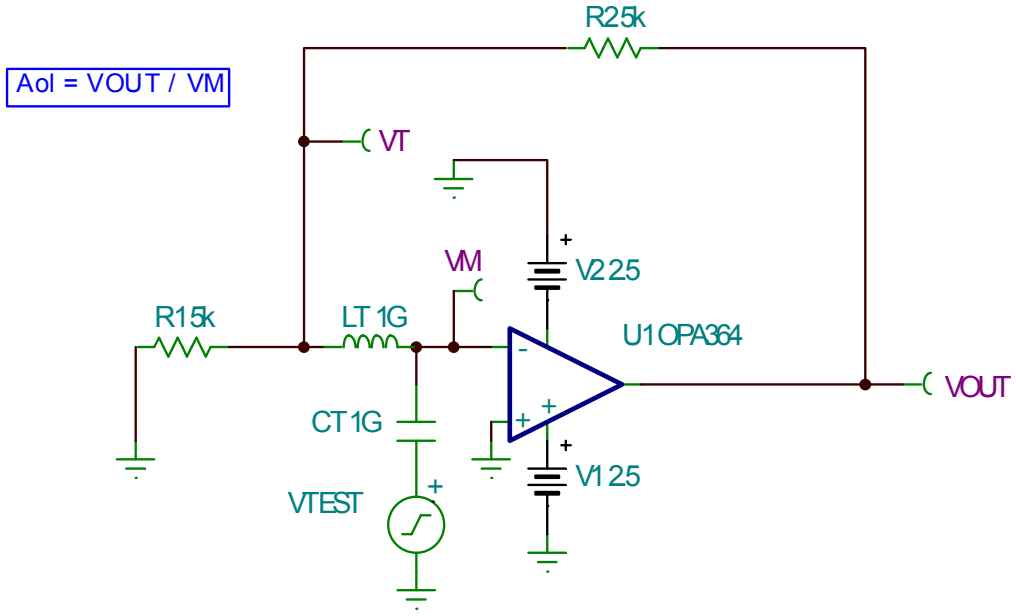


Fig. 5.21: OPA364 Aol Test Circuit With Load Of 10 kΩ (Data Sheet Aol Curve)

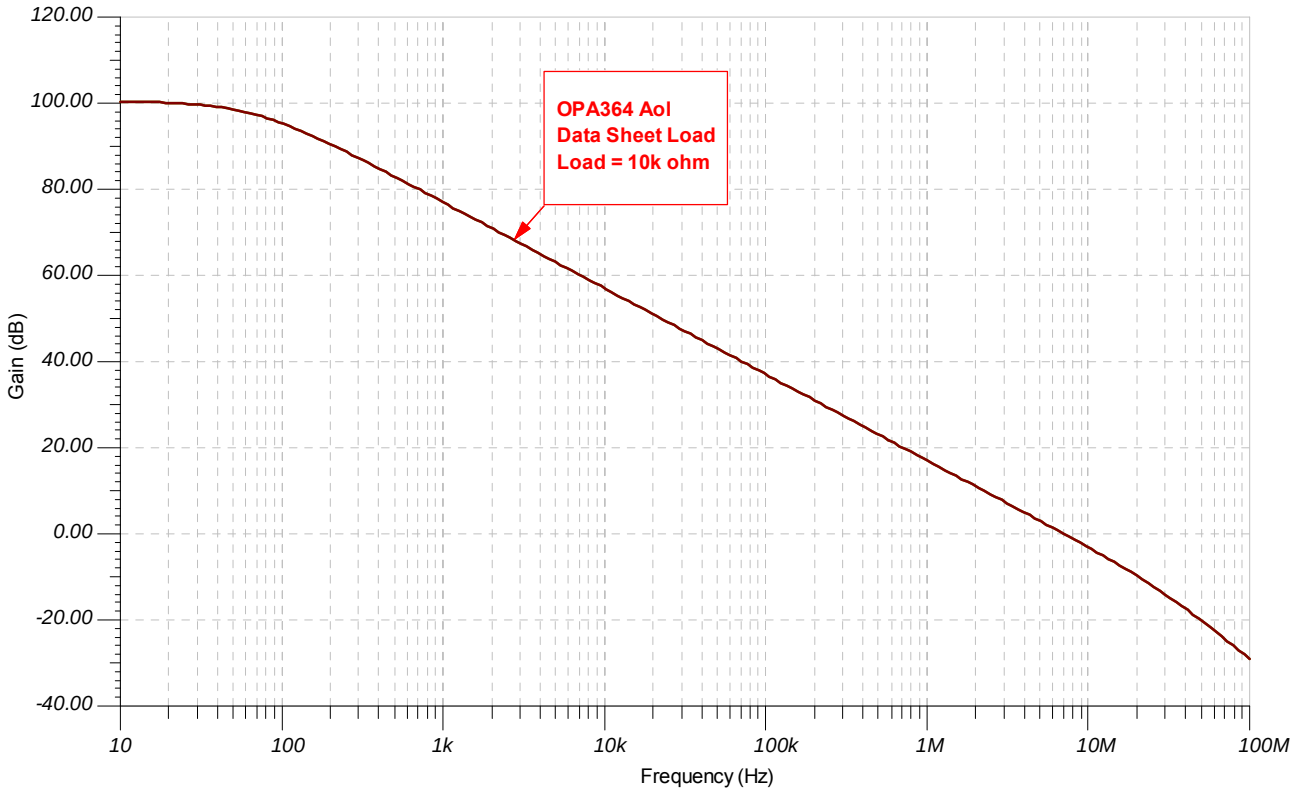


Fig. 5.22: OPA364 Aol With Load Of 10 kΩ (Data Sheet Aol Curve)

Final Buffer Analysis:

Now we perform a Tina SPICE analysis of our compensated buffer amplifier circuit (Fig. 5.23).

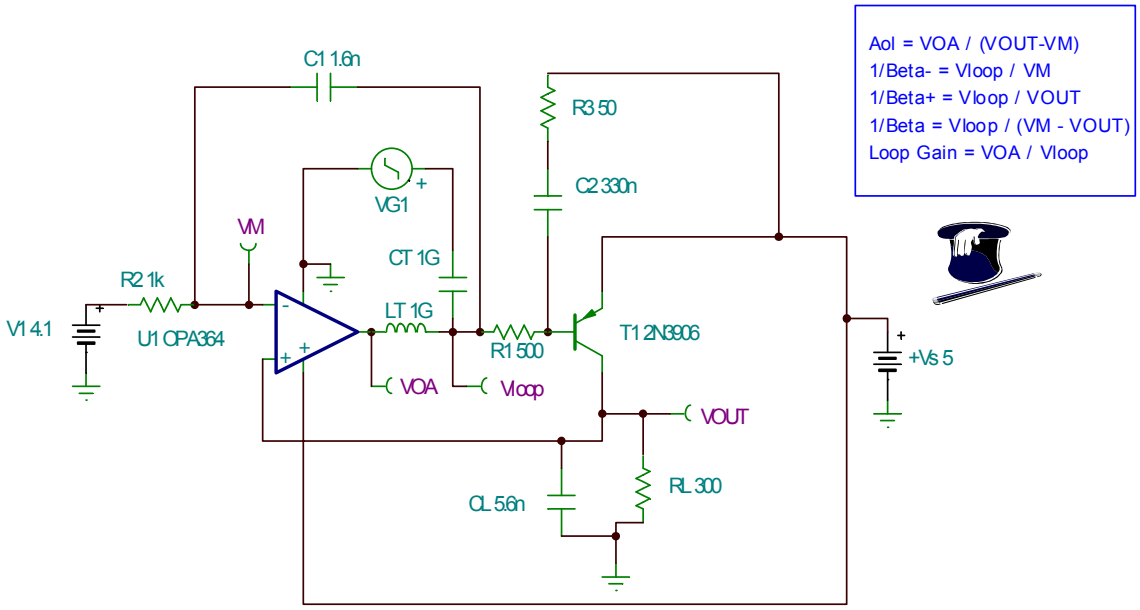


Fig. 5.23: Complete AC Analysis Circuit

Our 1/β plot (Fig. 5.24) is as predicted, the lower in gain between 1/β+ and 1/β- at any given frequency; our first-order analysis in these Tina SPICE simulation curves match what we predicted!

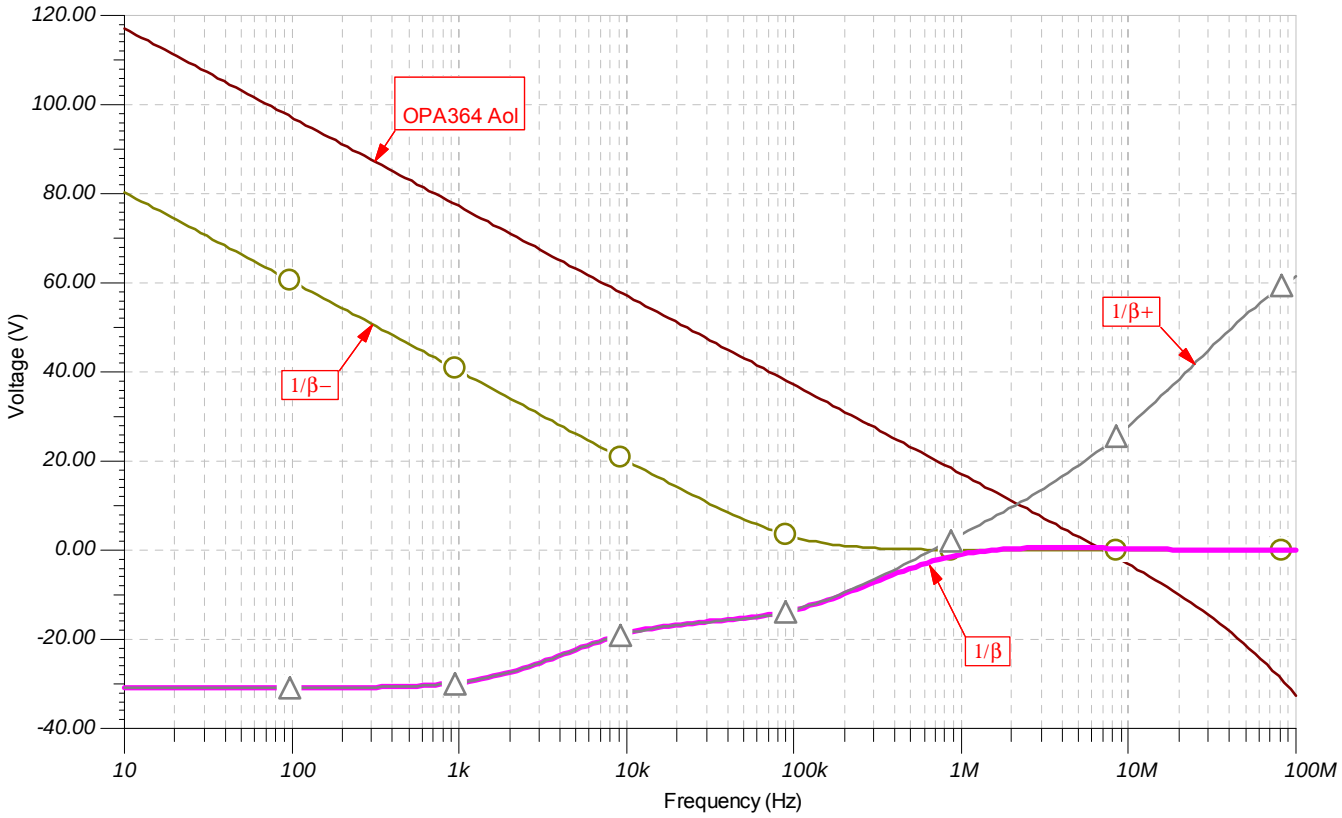


Fig. 5.24: Aol, 1/β+, 1/β-, and 1/β Plots

So for a detailed look at our stability picture we will use loop gain magnitude and phase plots (see Fig. 5.25) from our Tina SPICE simulation to accurately see how we did on synthesizing a stable unity-gain buffer. Our goals included keeping phase margin above 45° at frequencies less than fcl: we did well, with a little dip below 45° at 300 kHz with increasing phase margin from there on out in frequency.

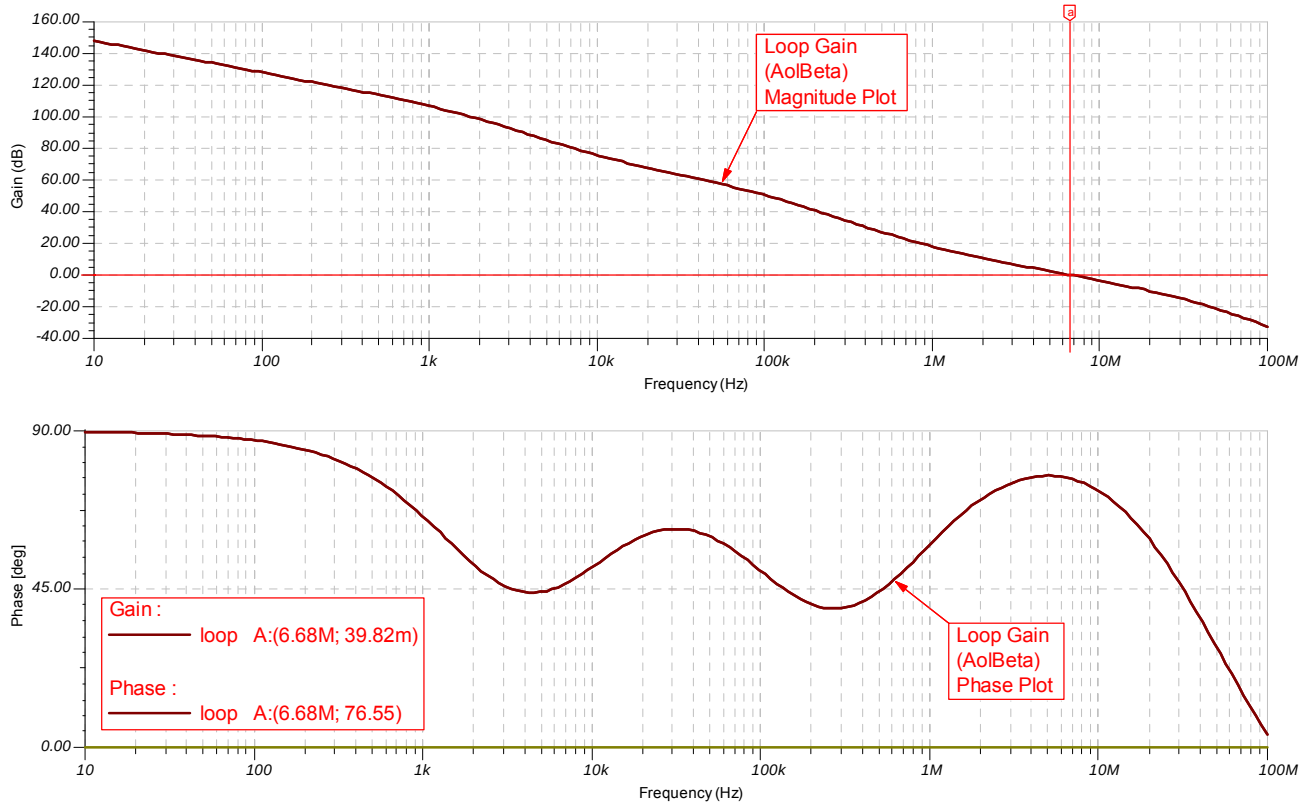


Fig. 5.25: Loop Gain (Aolβ) Magnitude & Phase Plots

The circuit (Fig. 5.26) predicts and simulates the ac closed-loop transfer function of VOUT/VIN.

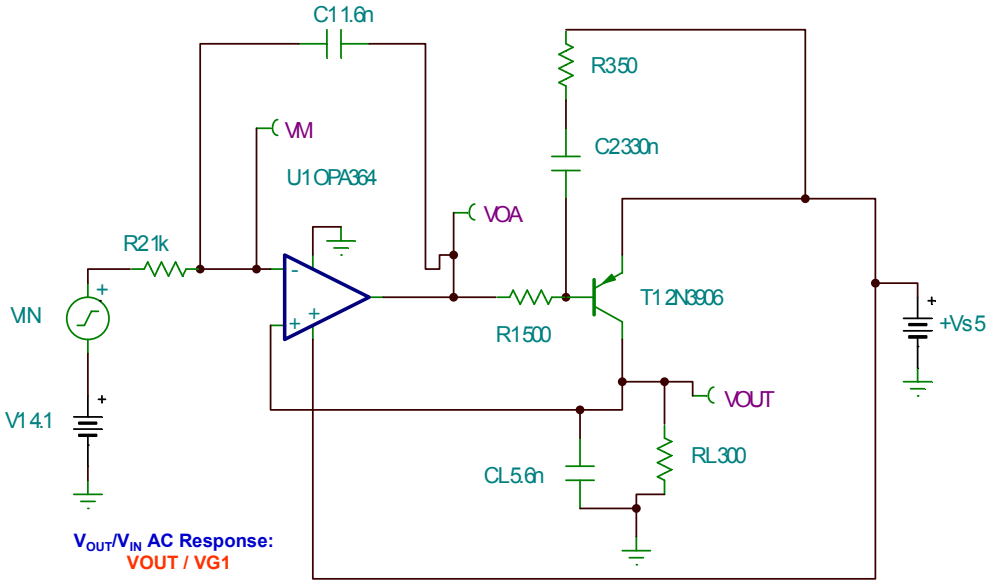


Fig. 5.26: VOUT/VIN AC Response Circuit

To our first-order analysis plots of Aol, 1/β+, 1/β -, and 1/β we will add a predicted VOUT/VIN curve for closed loop ac response (see Fig. 5.27). From dc to fpx U1, the OPA364, acts as an error amplifier with an integrator function such that it forces VOUT to match VIN. At fpx the integrator is forced to a gain of 1 since XC1/R2 = 1. From fpx to fpy VOUT/VIN continues down at -20 dB/decade due to XC1/R2. At fpy VOUT/VIN follows the Aol curve on down since there is no loop gain (AolB) left to correct for errors.

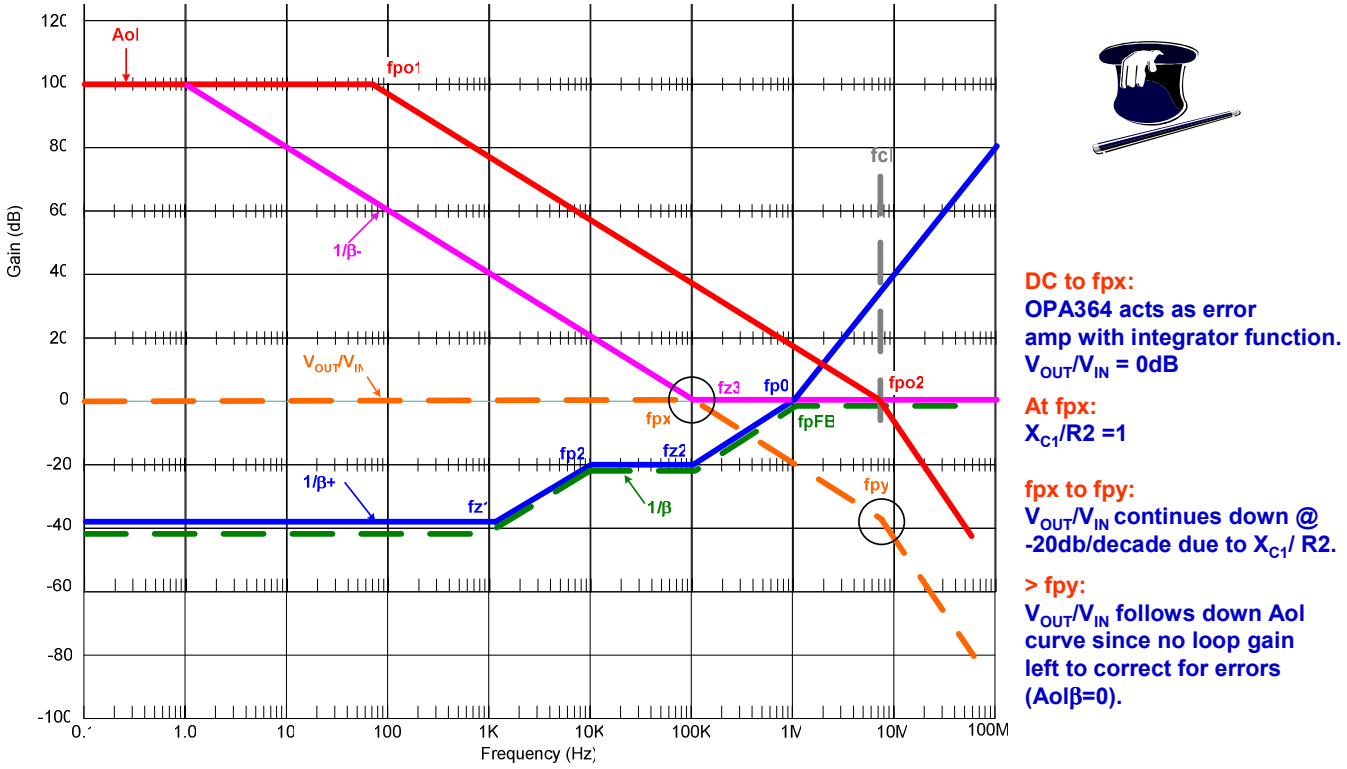


Fig. 5.27: First Order VOUT / VIN Analysis

The Tina SPICE simulation results for VOUT/VIN are shown in Fig. 5.28 and are shown to be as we predicted from our first-order analysis. We also note the we have achieved our initial goal of a 100-kHz small-signal bandwidth for our buffer amplifier circuit.

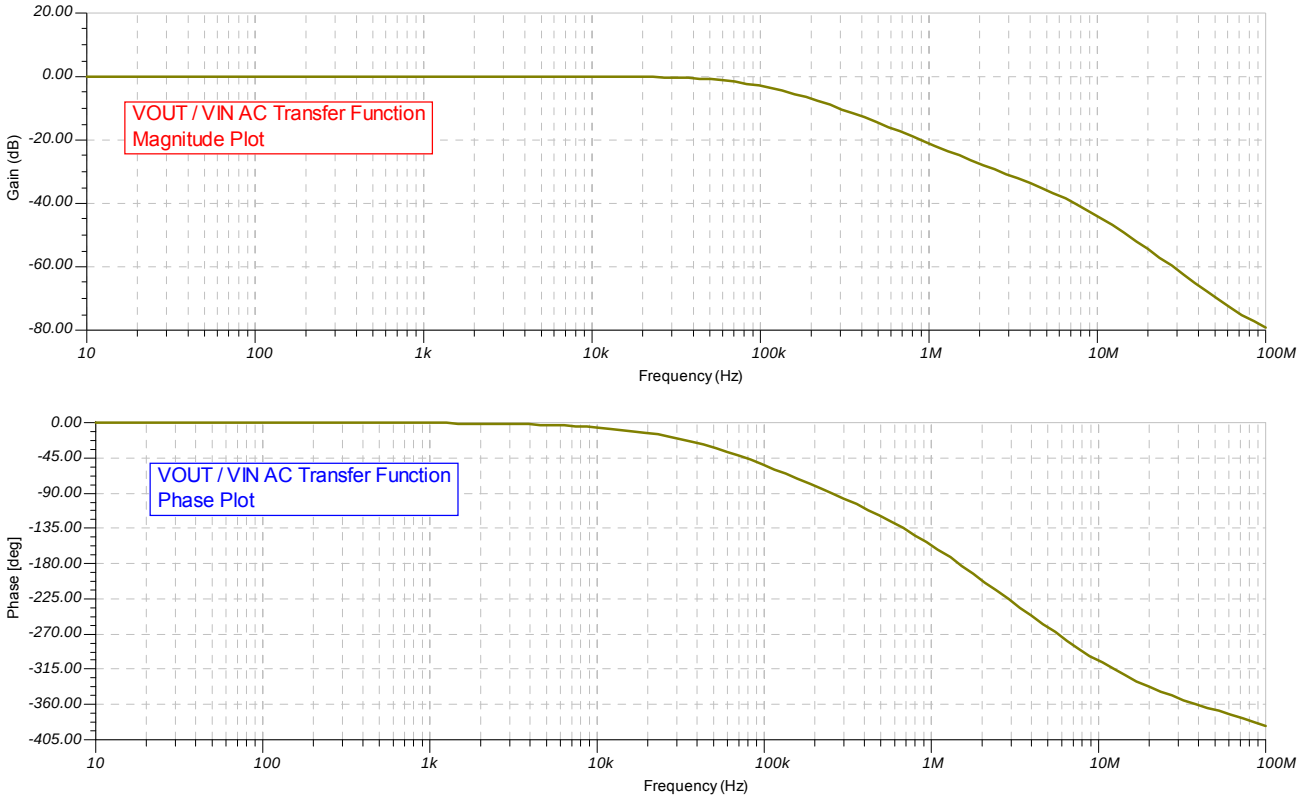


Fig. 5.28: VOUT/VIN SPICE Simulation Results

Now let's run a transient analysis test in Tina SPICE to look for overshoot and ringing based on our real-world stability test. The circuit for this is shown in Fig. 5.29.

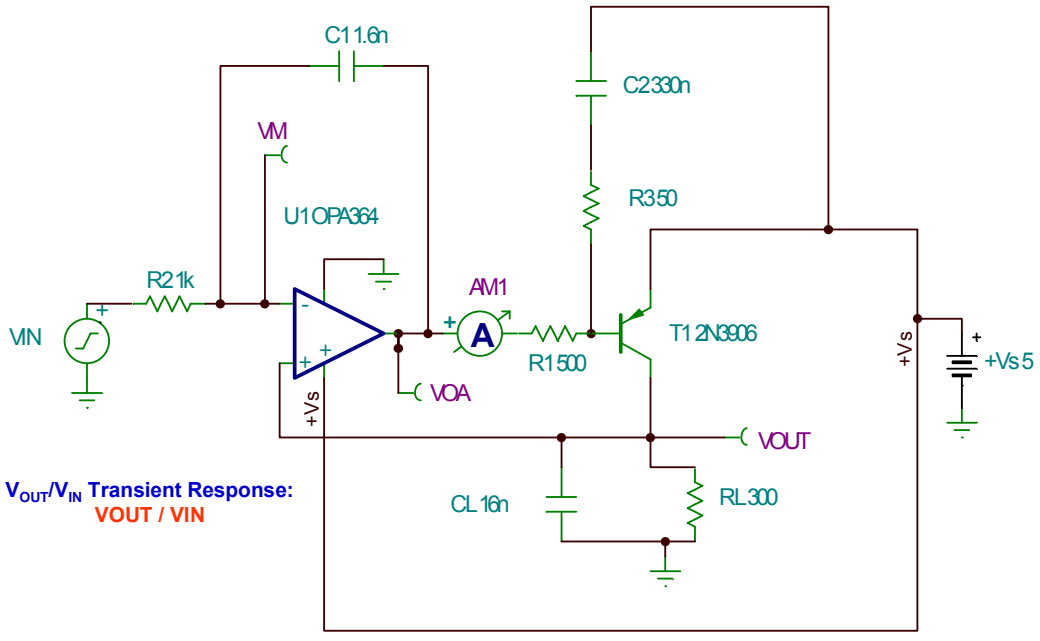


Fig. 5.29: Transient Stability Test Circuit

The results from our Tina SPICE Transient Analysis (Fig. 5.30) show that VOUT exhibits no excessive overshoot or ringing which is what we would predict from our loop stability analysis. In addition we monitored the current into and out of the OPA364 for these rapid step changes of 200 mV from 4 V to 4.2 V and back again. There are no excessive current spikes and we can expect a well-behaved, robust, stable, real-world, unity gain, buffer amplifier circuit now.

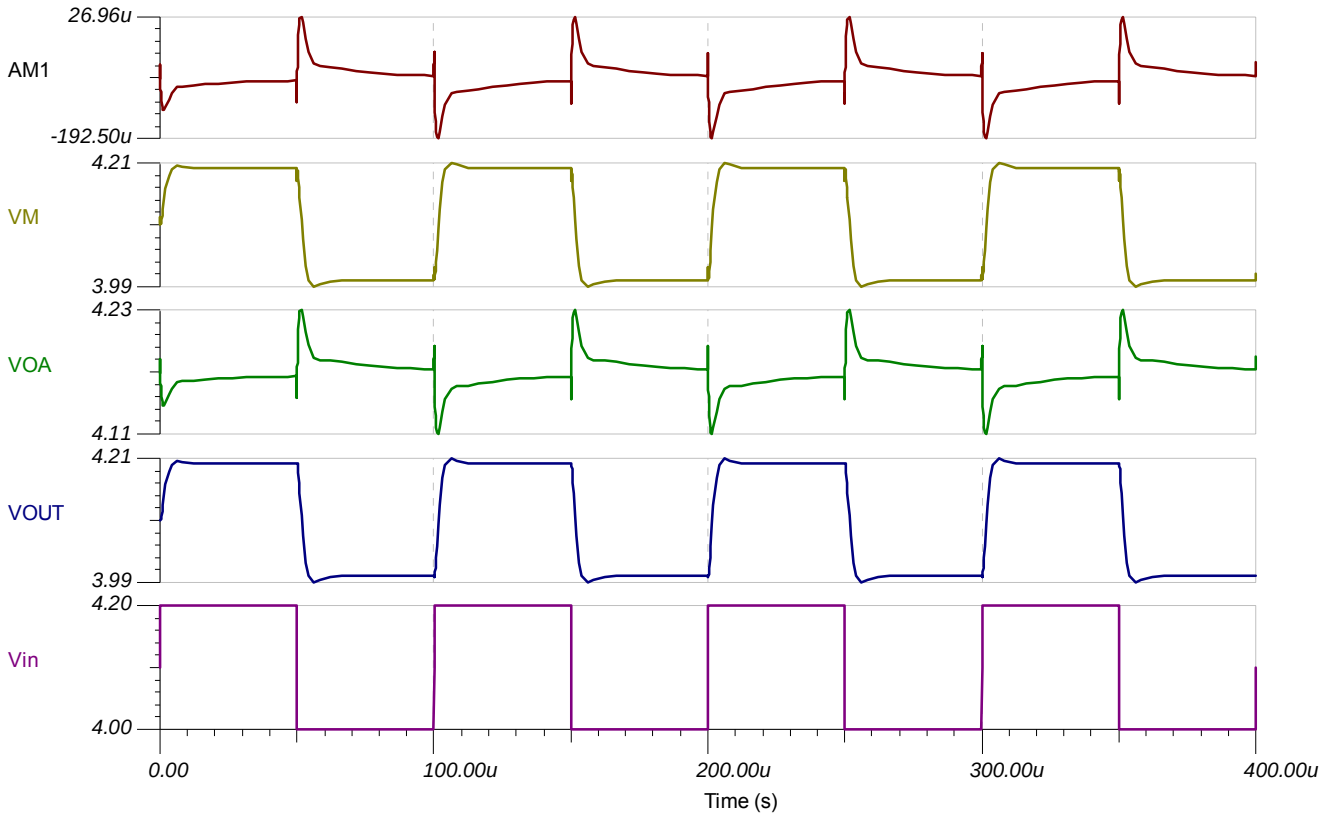


Fig. 5.30: Transient Stability Test SPICE Results

But wait that's not all. We added the stability networks to our real-world lab circuit and ran a transient stability test on it with the results shown in Fig. 5.31. Sweet success! We have proven our buffer amplifier circuit is stable from first-order analysis to Tina SPICE simulation and finally to the real-world stability test. Our analytical and synthesis techniques have been proven to work effectively resulting in a stable, reliable, single supply, high-current buffer amplifier circuit.

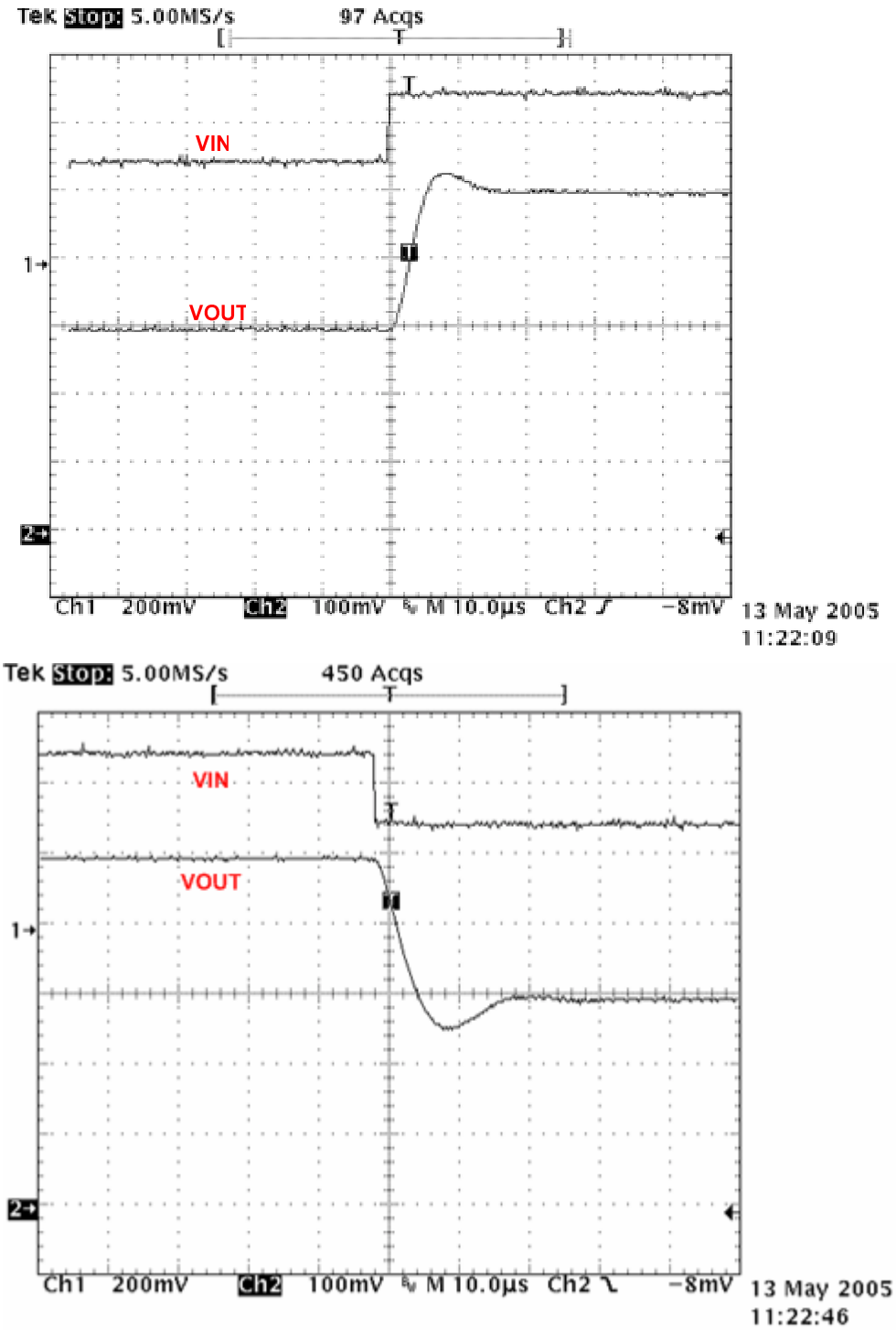


Fig. 5.31: "Real-World" Transient Stability Test Results: Buffer Topology With Compensation

About The Author

After earning a BSEE from the University of Arizona, Tim Green has worked as an analog and mixed-signal board/system level design engineer for over 23 years, including brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, and CCD cameras. Tim's recent experience includes analog & mixed-signal semiconductor strategic marketing. He is currently a Strategic Development Engineer at Burr-Brown, a division of Texas Instruments, in Tucson, AZ and focuses on instrumentation amplifiers and digitally-programmable analog conditioning ICs. He can be contacted at green_tim@ti.com