Operational Amplifier Stability
Part 8 of 15: Capacitive Load Stability: Noise Gain & CF

by Tim Green
Linear Applications Engineering Manager, Burr-Brown Products from Texas Instruments

Part 6 of this series was the beginning of a new Electrical Engineering tune "There must be six ways to leave your capacitive load stable." The six ways are Riso, high gain & CF, noise gain, noise gain & CF; output pin compensation, and Riso with dual feedback. Part 6 covered Riso, high gain & CF, and noise gain. Part 7 re-investigated Z_O, small signal ac output impedance, for both the bipolar emitter-follower and CMOS RRO op amps. Now in Part 8 we will return our focus studying noise gain & CF.

Our investigation will make use of familiar tools from our stability analysis tool kit (Z_O analysis, modified Aol curve creation, first order analysis & synthesis, Tina SPICE loop stability simulation, Tina SPICE transient simulation, and Tina SPICE Vout/Vin ac transfer function analysis). The noise gain & CF techniques presented have been confirmed to work as predicted in real-world, actually-built circuits at some time over the last 24 years. However, due to resources each circuit specifically presented here has not been built, but rather is left to the reader as an exercise on the application of each technique to his/her own individual application (ie analyze, synthesize, simulate, build and test).

Noise gain & CF compensation will be split into two different cases: noise gain & CF inverting and noise gain & CF non-inverting. As the names imply the difference will be if the op amp circuit configuration is either inverting or non-inverting, respectively.

Op Amp For Noise Gain & CF Capacitive Load Stability Analysis

OPA348
1MHz, 45uA, CMOS, RRIO Operational Amplifier

Input Specs	
Offset Voltage	5mV max
Offset Drift	4uV/C
Input Voltage Range	(V-)-0.2V to (V+)+0.2V
Common-Mode Rejection Ratio	82dB typ
Input Bias Current	10pA max
Noise	
Input Voltage Noise	10uVpp, f=0.1Hz to 10Hz
Input Voltage Noise Density	35nV/rt-Hz @1kHz
Input Current Noise Density	4fA/rt-Hz
Output Specs	
Vsat @ Iout = 27uA	25mV max
Vsat @ Iout = 540uA	125mV max
Vsat @ Iout = 5mA	1V max
Iout Short Circuit	10mA

AC Specs	
Open Loop Gain, RL = 100k	108dB typ
Open Loop Gain, RL = 5k	98dB typ
Gain Bandwidth Product	1 MHz
Slew Rate	0.5V/us
Overload Recovery Time	1.6us
Total Harmonic Distortion + Noise	0.0023%, f=1kHz
Setling Time, 0.01%	
Supply Specs	
Specified Voltage Range	2.5V to 5.5V
Quiescent Current	65uA max
Over Temperature	75uA max
Temperature & Package	
Operating Range	-40C to +125C
Package options	SOT23-5, SO-8, SC70-5

Fig. 8.1: Typical CMOS RRIO Op Amp, Noise Gain & CF Inverting

Our op amp of choice for noise gain & CF capacitive load analysis will be a CMOS RRIO op amp with the specifications detailed in Fig. 8.1. The OPA348 is a low quiescent current (65 µA) op amp optimized for single supply operation (2.7 V to 5.5 V) with beyond rail-to-rail input (greater than 0.2 V beyond either supply) and rail-to-rail output (Vsat = 25 mV @ Iout = 27 µA). The OPA348 will also provide output current of 5 mA at a saturation voltage of 1 V max. Since this is a CMOS RRO op amp we will need to know its open-loop output impedance to create a modified Aol curve for our loop stability synthesis.

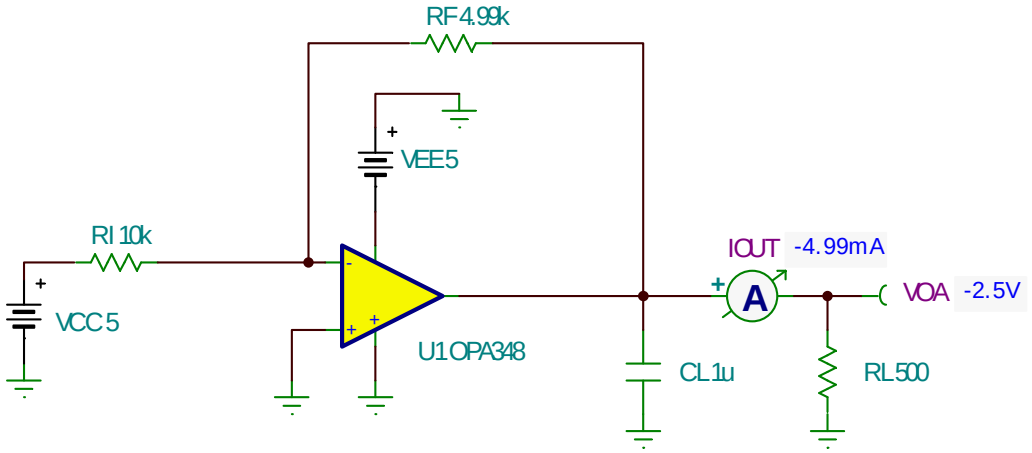


Fig. 8.2: One-Half Supply Negative Reference

A very common application (Fig. 8.2) where the noise gain & CF compensation will be used is in applications involving a low-voltage supply where a reference voltage is created at ½ of the supply voltage. For good response to ac load transients on the output of this type of a reference a capacitor is usually placed directly at the output. This "charge bucket" provides an immediate reserve for high-frequency load transients while the op amp accurately recharges the capacitor and keeps the overall dc voltage to its programmed level. Noise gain & CF inverting analysis will use the circuit where the op amp is powered from -5 V and ground. The input signal is +5 V through a gain of -½ to create a resultant -2.5 V reference output. We will design for a 500-Ω load implying a -5 mA load current.

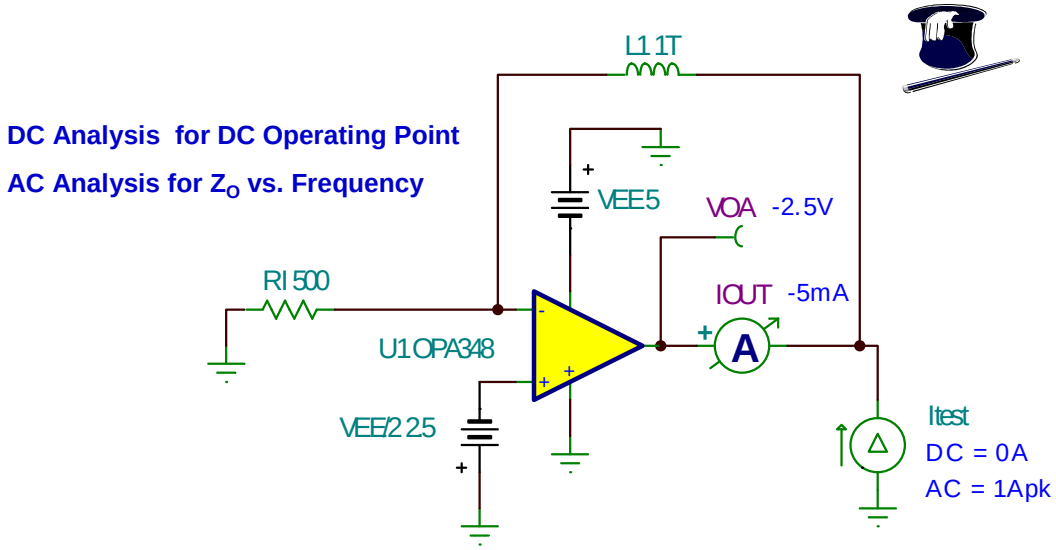


Fig. 8.3: Z_O Test Circuit

In order to predict what effect our capacitive load has on our Aol curve we need to first find out what Z_O is for our given dc load of -5mA. We will use the techniques and model for CMOS RRO Z_O presented in "Part 7 of 15: When Does R_O Become Z_O?" In Fig. 8.3 L1 is a 1 TH inductor and RI sets the load current through the output of U1. For ac L1 is a short and an open for any ac frequencies of interest. By driving U1 output with a 1 Apk ac current generator, which is swept over frequency, VOA becomes directly Z_O.

The results of our Tina SPICE analysis ac analysis are shown in Fig. 8.4. We see that for a -5 mA dc load that Z_O contains an R_O component of 42.43 Ω and has a zero at fz = 1.76 kHz.

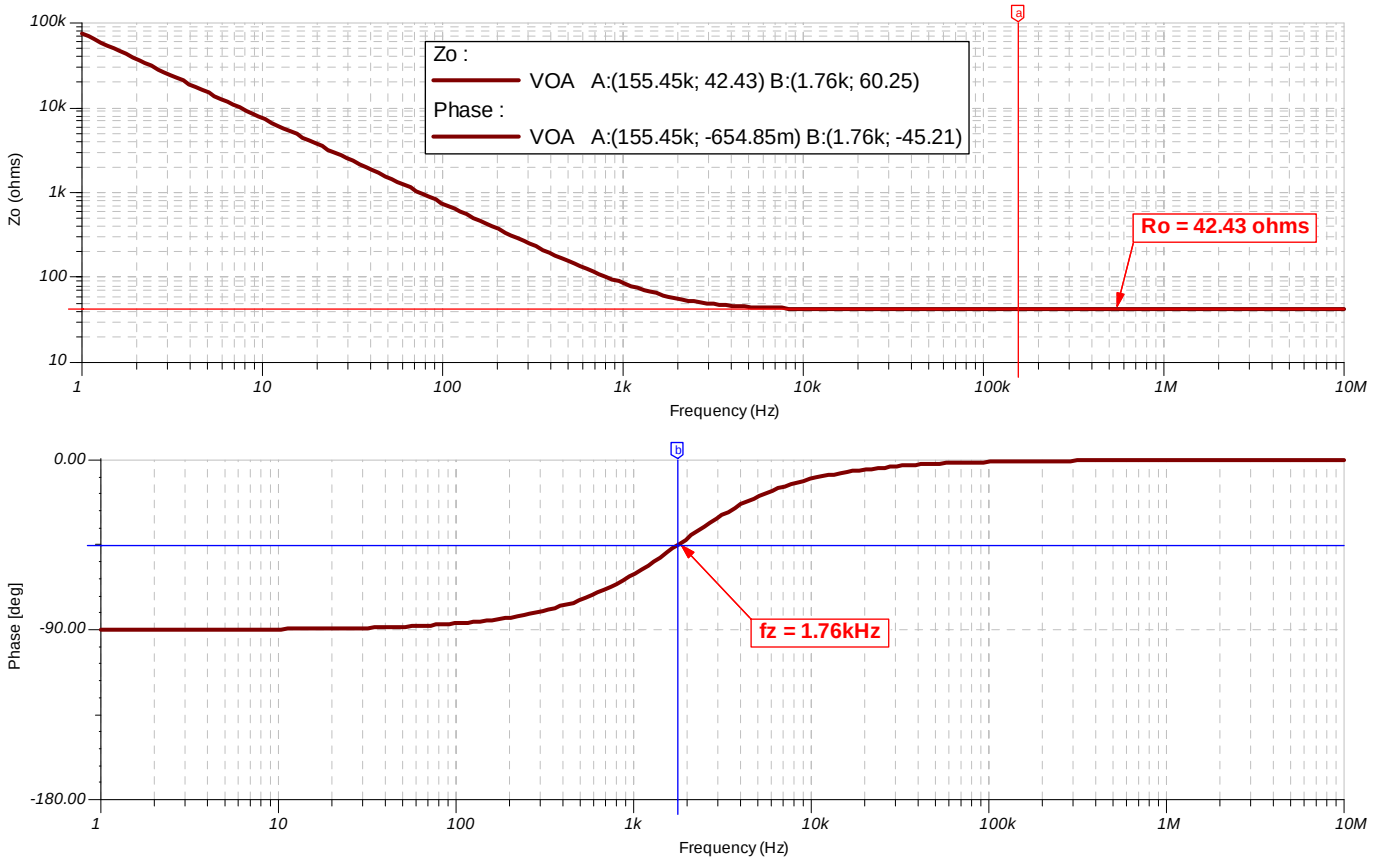
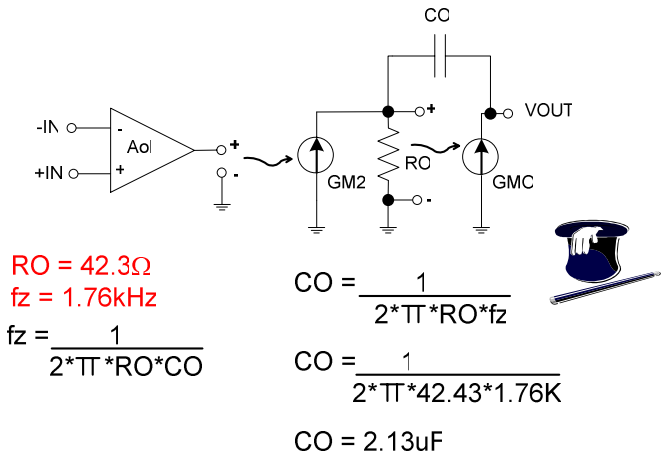


Fig. 8.4: Z_O Tina SPICE Plots



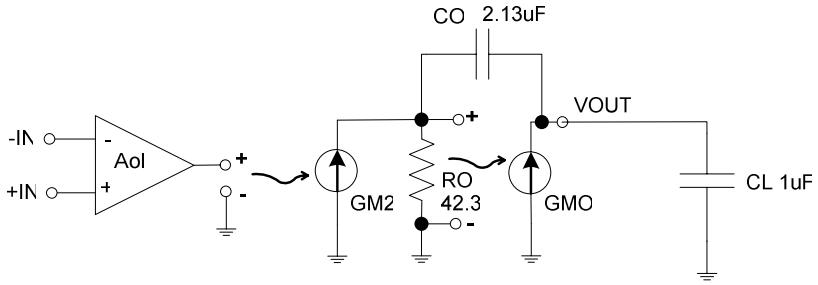
Output is two GM (current gain) Stages
Output is *Current Source* GMO (ideal current source has infinite impedance)

Output Impedance (Z_O) is dominated by R_O at High Frequencies
Z_O will look capacitive at Low and Medium Frequencies

Fig. 8.5: OPA348 Z_O Model

We build our CMOS RRO model in Fig. 8.5. Given our measured results for R_O and fz we can quickly calculate CO and complete our Z_O model for the OPA348 at a dc load current of -5 mA.

We are going to use superposition to create our predicted modified Aol curve due our capacitive load, CL. We begin in Fig. 8.6 by looking at the effect of CL without the effect of RL. Using our Z_O model we calculate fp2, the pole in our modified Aol curve due to the effects of Z_O and CL.



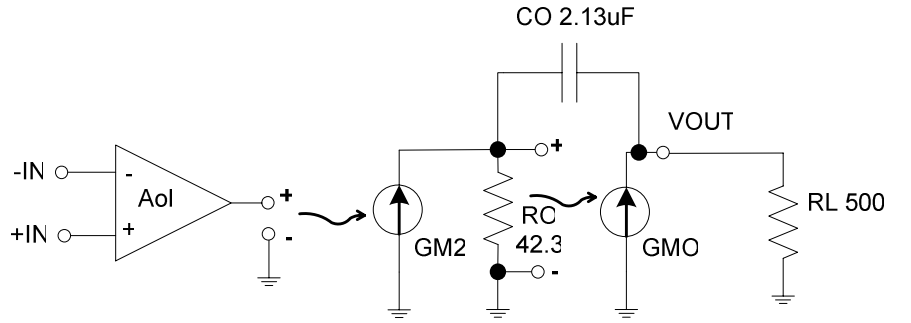
$$fp2 = \frac{1}{2*\Pi T*Ceq*RO} \qquad fp2 = \frac{1}{2*\Pi T*0.68uF*42.3} = 5.53kHz$$

where: $Ceq = \frac{CO * CL}{CO + CL}$ $\qquad Ceq = \frac{2.13uF*1uF}{2.13uF+1uF} = 0.68uF$

remember:
1) capacitors in series are like resistors in parallel
2) XC = 1/sC
3) XCeq = 1/sCO +1/sCL
4) Ceq = 1/XCeq

Fig. 8.6: Modified Aol due to CL

In Fig. 8.7 we will look separately at the effect of RL and Z_O on the Aol Curve. f_{HP} is our predicted pole in the modified Aol curve



$$f_{HP} = \frac{1}{2*\pi*CO*RL}$$

Low Frequency Aol affected by RL
Due to CO & RL High Pass Function
Assume RL >10*RO

$$f_{HP} = \frac{1}{2*\pi*2.13uF*500} = 149.44Hz$$

Fig. 8.7: Modified Aol due to RL

To use the results of our superposition calculations to create our modified Aol curve we will need to have the unloaded Aol curve for the OPA348. We can get this from the manufacturer's data sheet or in this case measure it on our Tina SPICE macro-model for the OPA348 since we have inside knowledge that it matches the data sheet extremely accurately. Our unloaded Aol test circuit is in Fig. 8.8. Note how we create a dc operating point that matches our application without loading down the output of the op amp by using high value resistors. If SPICE analysis is done with the op amp in a saturated dc condition at the output (either positive or negative saturation) the Aol curve will not be correct since the MOSFET models used inside of the op amp macromodel will not be in a linear region of operation.

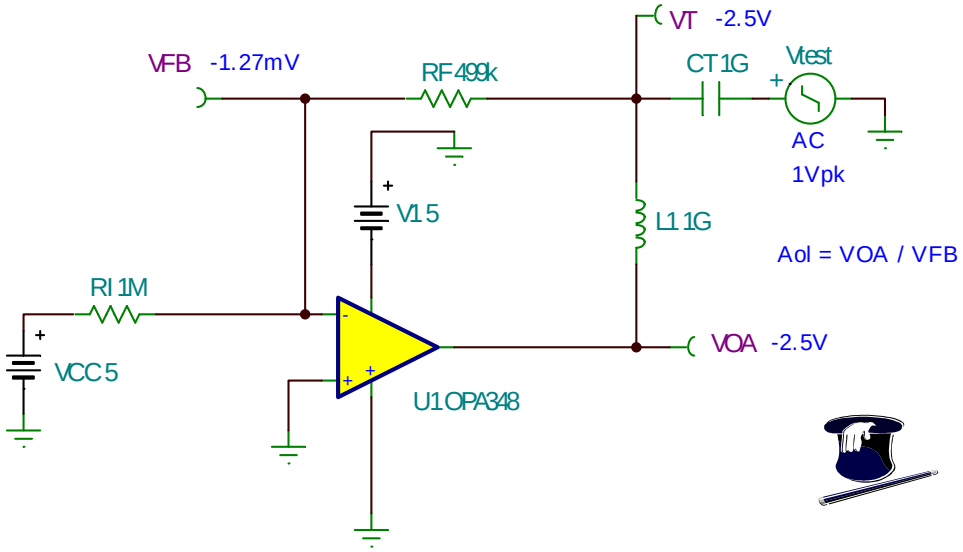


Fig. 8.8: Unloaded Aol Test Circuit

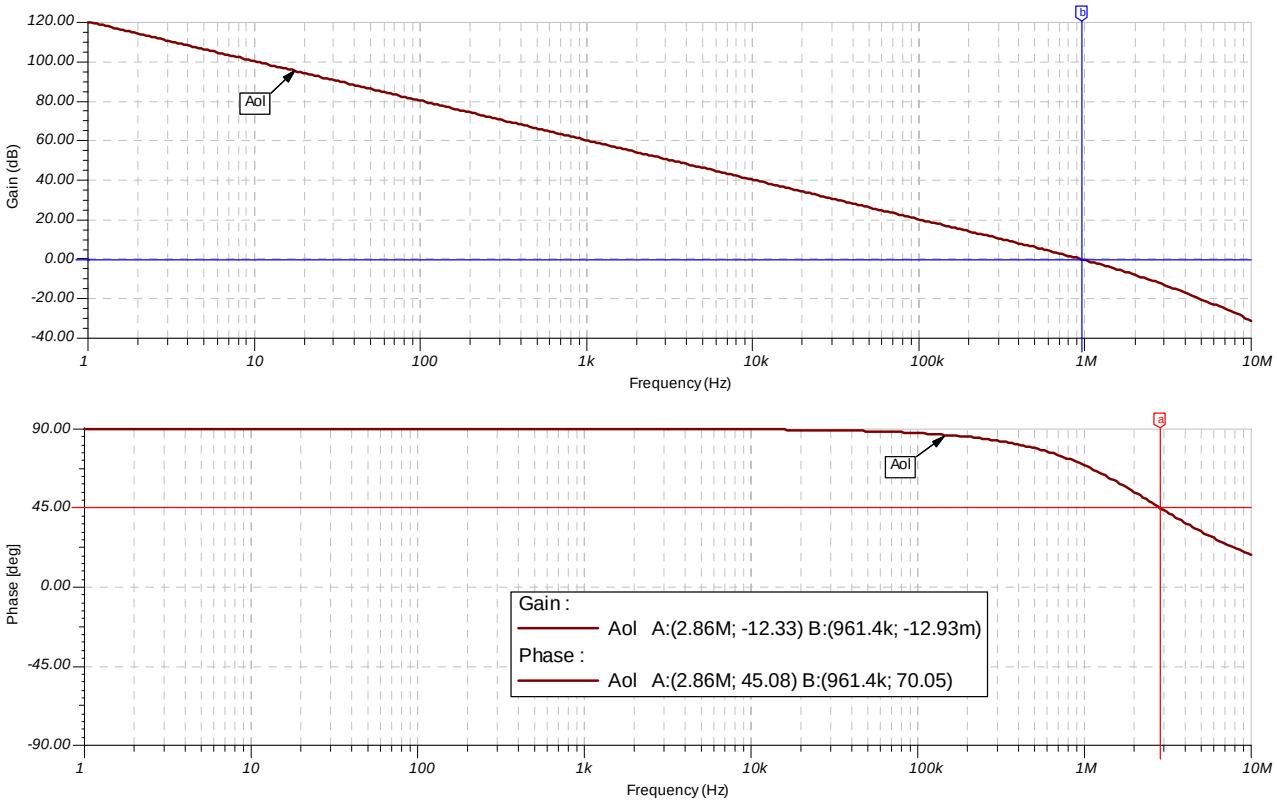


Fig. 8.9: Unloaded Aol Curve

Now, in Fig. 8.10, we can finally combine all of our superposition analysis components to form our predicted modified Aol curve. On our unloaded Aol curve we plot the effects of Z_O, CL, and RL. Since the unloaded Aol curve passes through our Z_O model it is "amplified" or "multiplied" by the Z_O model.

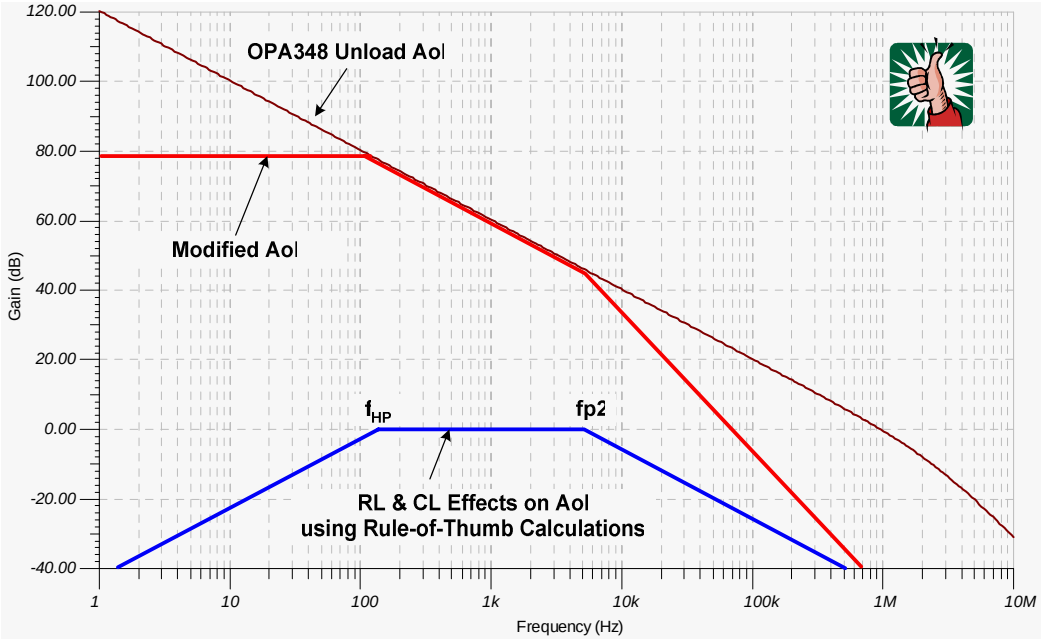
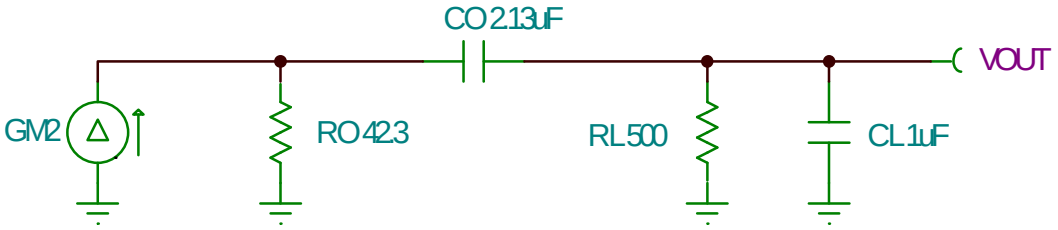


Fig. 8.10: Predicted Modified Aol Model

Remember multiplication in linear math simply becomes addition on a Bode plot. Our predicted modified Aol curve shows about 80 dB from dc to f_{HP} (149Hz) and then rolls off at -20 dB/decade until fp2 (5.53 kHz) where it changes to -40 dB/decade.

Before we look at the actual modified Aol curve versus our predicted modified Aol curve let us see, from a filter perspective, how far off our superposition technique is. Our net circuit with both RL and CL is shown in Fig. 8.11. An ac Tina SPICE analysis was done with the results in Fig. 8.12. Results of our superposition rule-of-thumb analysis are shown as well as the actual frequency response from SPICE. Notice that our frequency prediction for fp2 is close to the actual but our prediction for f_{HP} is off a bit. f_{HP} was computed with CO and RL. By adding CL into the picture we expect that this would cause f_{HP} to happen at a lower frequency since CL will reduce the net impedance across RL as frequency changes. If CL <CO ÷ 10, CO would have dominated and CL would not have been a significant factor. However, as a quick check for the shape of the curve and relative breakpoints we can use our simplified calculation techniques using superposition, cognizant that we expect a lower actual value in frequency for f_{HP}.



	f_{HP}	fp2
Rule-of-Thumb Frequency	**149.44Hz**	**5.53kHz**
Actual Frequency	**94.1Hz**	**5.99kHz**

If CL < CO/10 then Rule-of-Thumb Frequency would have been much closer to Actual Frequency for f_{HP}.

Rule-of-Thumb close enough for sanity check on Tina SPICE Modified Aol Curve analysis.

Fig. 8.11: f_{HP} & fp2 Actual Frequencies Test Circuit

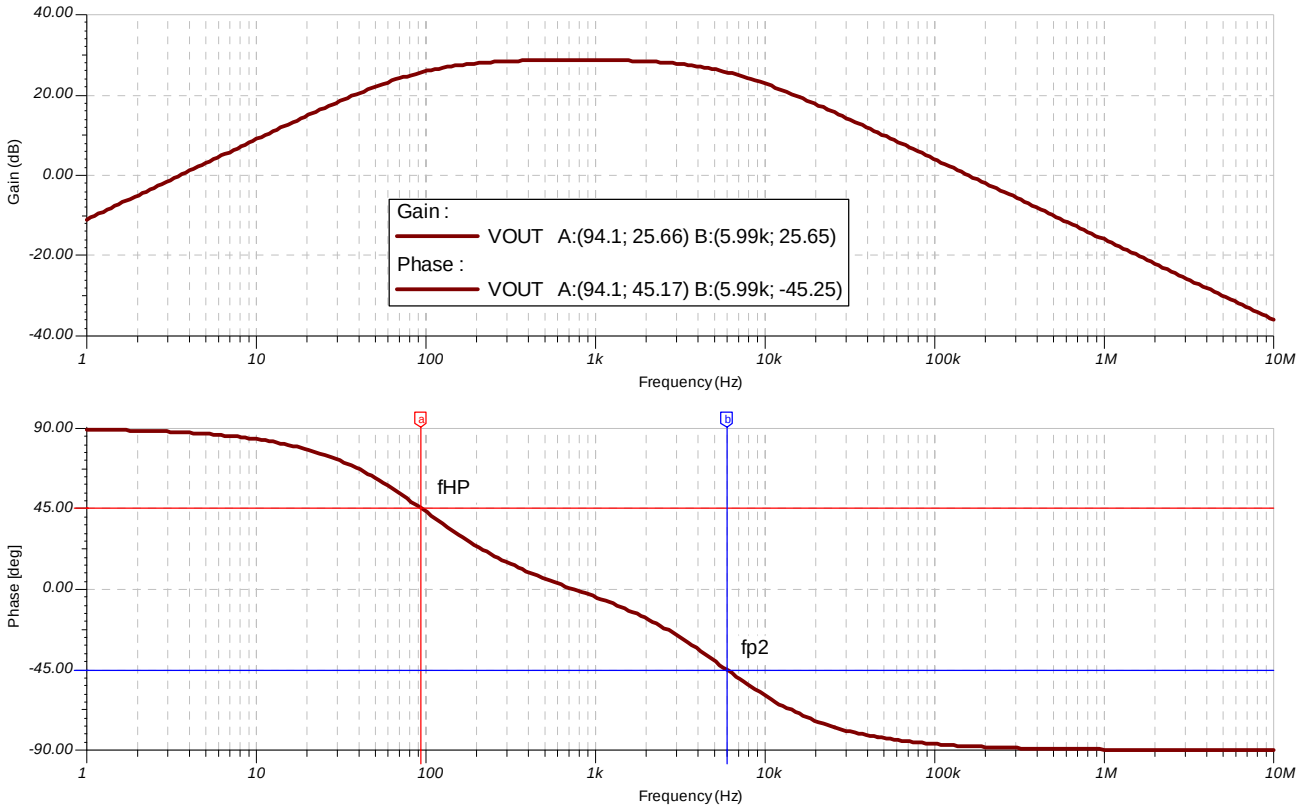


Fig. 8.12: f_{HP} & fp2 Actual Frequencies Test Results

Fig. 8.13 shows the test circuit for measuring the actual modified Aol curve. Notice how we have opened the closed loop op amp circuit between VOA and feedback point VT. CL is left connected directly to the output of the OPA348, U1. Now our modified Aol will be VOA ÷ VFB.

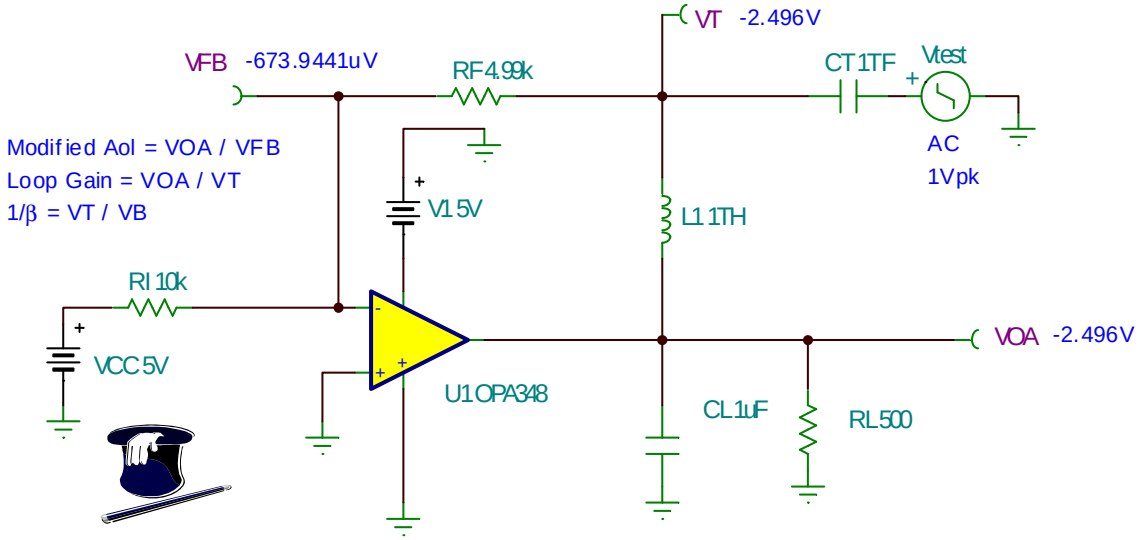


Fig. 8.13: Modified Aol Test Circuit

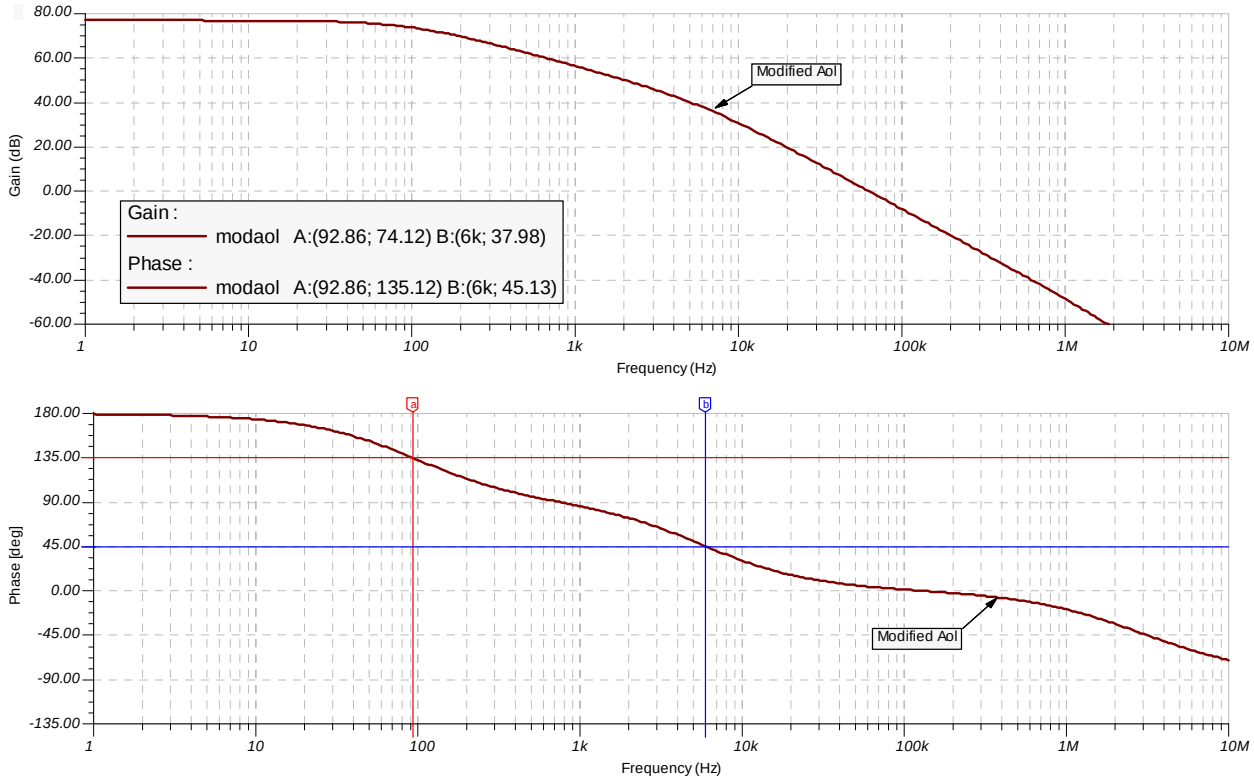
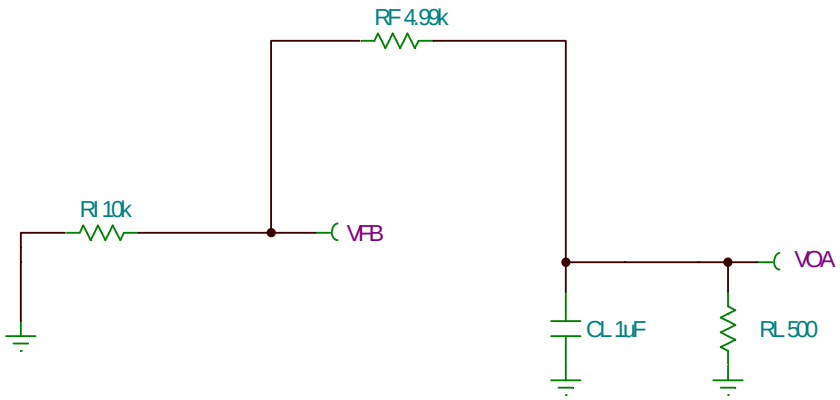


Fig. 8.14: Modified Aol Tina SPICE Results

Our Tina SPICE measured modified Aol curve is shown in Fig. 8.14. Note that the final values are f_{HP} = 92.86 Hz and fp2 = 6 kHz. The results form our filter analysis using Tina were f_{HP} = 94.1 Hz and fp2 = 5.99 kHz. Our rule-of-thumb, superposition approach had yielded f_{HP} = 149.44 Hz and fp2 = 5.53 kHz. Again we emphasize that our rule-of-thumb, superposition approach is close enough for a conceptual and sanity check that the actual Tina SPICE analysis is correct.



β = VFB/VOA
1/β = VOA/VFB

$$VFB = \frac{VOA * RI}{RF + RI}$$

Set VOA = 1

$$VFB = \frac{1 * 10k}{4.99k + 10k} = 0.667$$

1/β = 1/0.667 = 1.499 → 3.5dB

Fig. 8.15: 1/β with No Stability Compensation

In Fig. 8.15 we compute our 1/β value with no stability compensation. A simple resistive divider of the output voltage yields a 1/β of 3.5 dB.

On our modified Aol plot we plot 1/β for our uncompensated circuit in Fig. 8.16. Notice that we immediately see a 40dB/decade rate-of-closure and by our rule-of-thumb an unstable circuit.

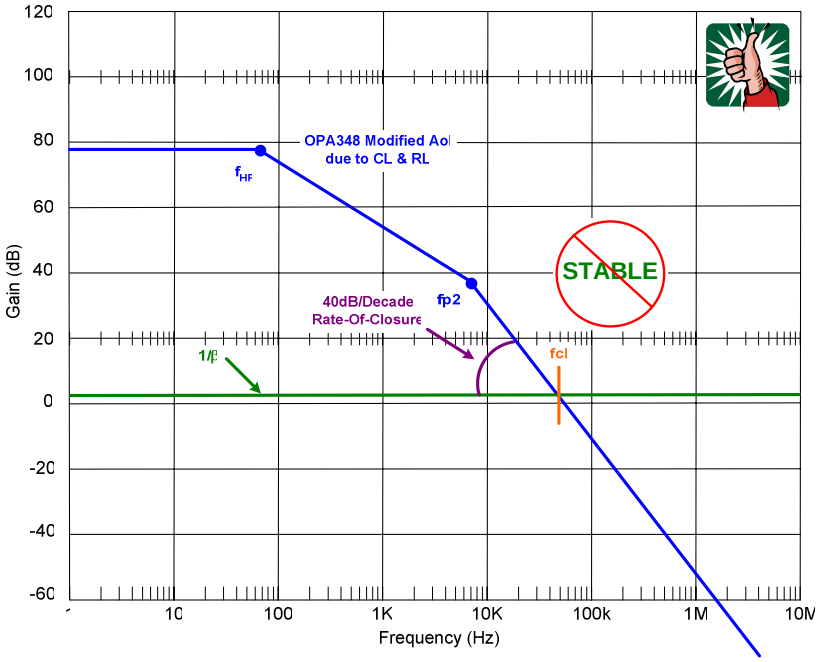


Fig. 8.16: Modified Aol Curve And 1/β

A Tina SPICE ac analysis of loop gain confirms our first-order suspicions (Fig. 8.17). Loop phase drops to 5° at fcl where loop gain goes to 0 dB. Although this circuit may not be an oscillator it is not one we wish to put into production at 1000 per month!

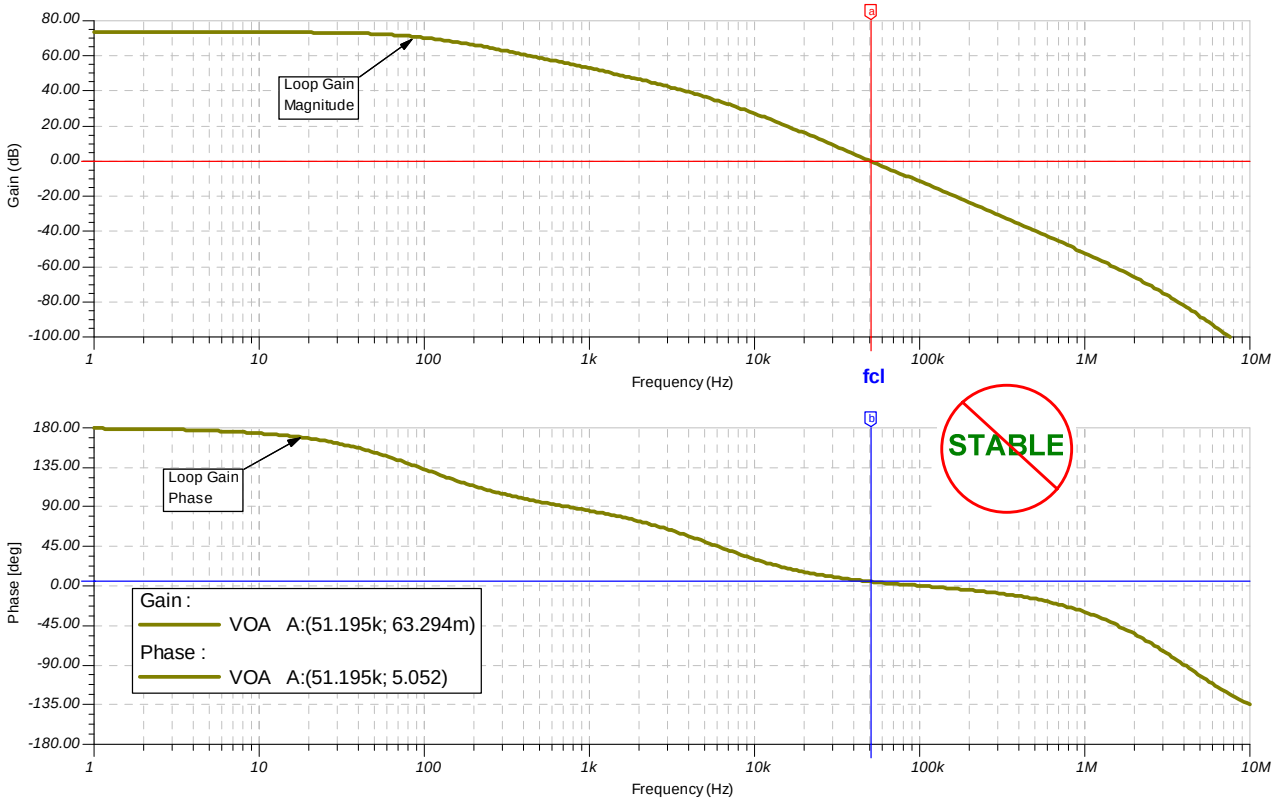


Fig. 8.17: Loop Gain Without Stability Compensation

As another real-world check we will do a transient test for stability using the circuit in Fig. 8.18.

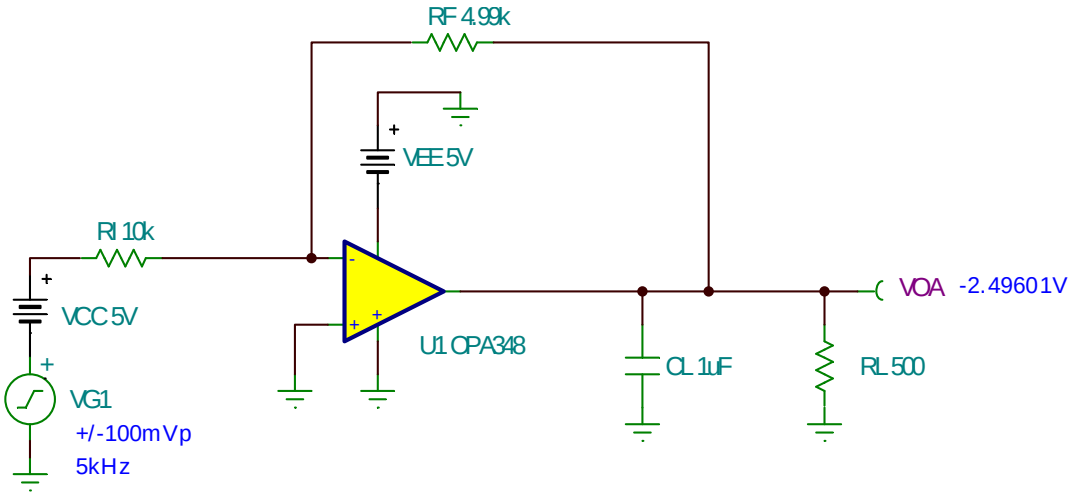


Fig. 8.18: Typical CMOS RRIO Op Amp

Our Tina SPICE transient results in Fig. 8.19 show a very high overshoot and much ringing in the output waveform. This should make us suspicious that we want to add compensation for a more stable circuit.

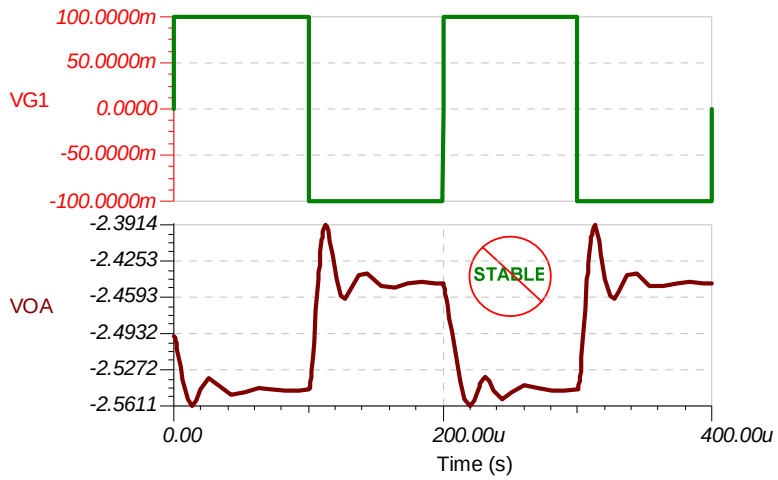


Fig. 8.19: Transient Test without Stability Compensation

Now let's compensate our circuit for a stable design (see Fig. 8.20).

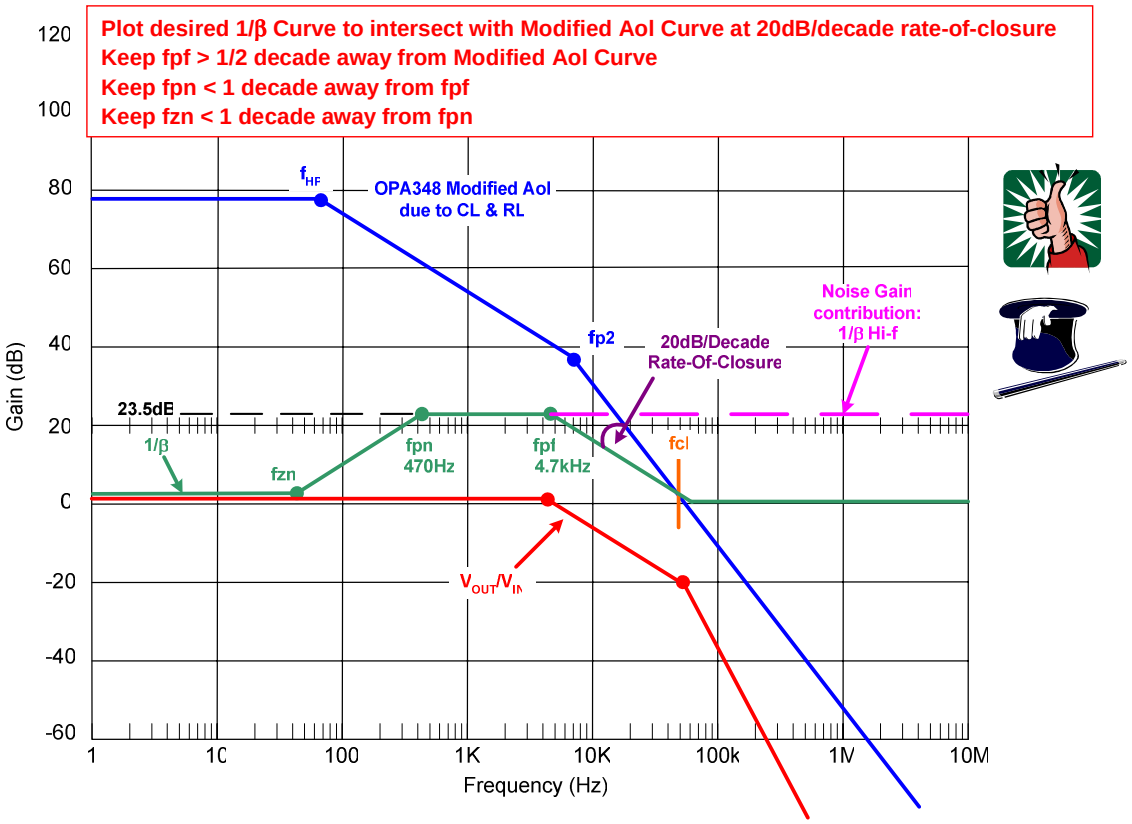


Fig. 8.20: First-Order Plots For Compensation

First we plot our modified Aol curve due to CL and RL. We know our dc 1/β is 3.5 dB. We see we need to somehow intersect a modified Aol curve at a rate-of-closure that is 20 dB/decade. If we just use noise gain we would need to raise the noise gain all the way up to 40 dB (x100). Instead we can use a noise gain of 20 dB (x10) and add CF to create a 20 dB/decade rate-of-closure at fcl. First we

start at fcl and work our way back with a -20 dB/decade slope. Note that fpf is at least ½ a decade away from the modified Aol curve. This allows for a modified Aol curve that can shift up to ½ a decade to the left before we run into a marginal stability situation again. This is a good rule-of-thumb for the real world. Now we place fpn one decade to the left of fpf. fzn will naturally occur one decade to the left of fpn due to our noise gain compensation topology.

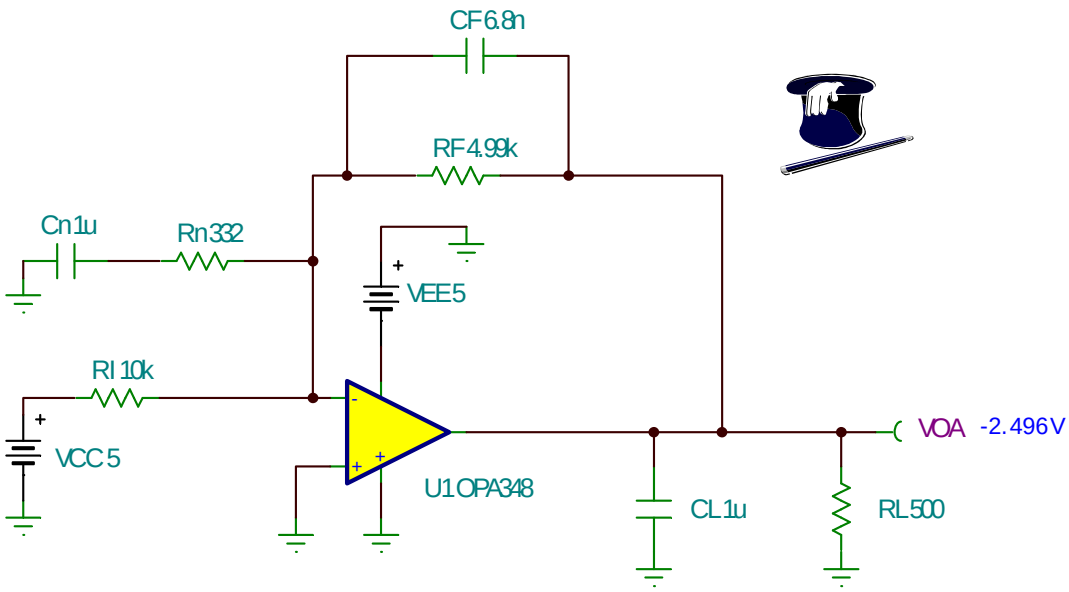


Fig. 8.21: Typical CMOS RRIO Op Amp

To create our desired 1/β curve we will use a combination of noise gain and CF (feedback capacitor in parallel with RF) as shown in Fig. 8.21. Notice that this can be viewed as a summing amplifier with zero volts (ground) summed in through Cn and VCC through RI. The net ac transfer function from VOA ÷ VCC we expect to be flat until we hit the pole created by RF in parallel with CF (Fig. 8.20).

Our noise gain & CF inverting detailed compensation calculations are shown in Fig. 8.22. This analysis is simplified by breaking it into three parts. First the dc 1/β is computed with Cn and CF = open. Next the high frequency portion of the noise gain compensation is computed by setting CF = open and Cn= short. fpn is created by the noise gain compensation and easily computed. Finally the CF compensation is computed by setting Cn to a short and computing a pole due to CF and RF. Closest standard component values are chosen in all cases. Smaller values of capacitors can be used if resistor values are all proportionally increased. However, larger value resistors will contribute to a higher overall noise value in the circuit. These design trade-offs are application dependent.

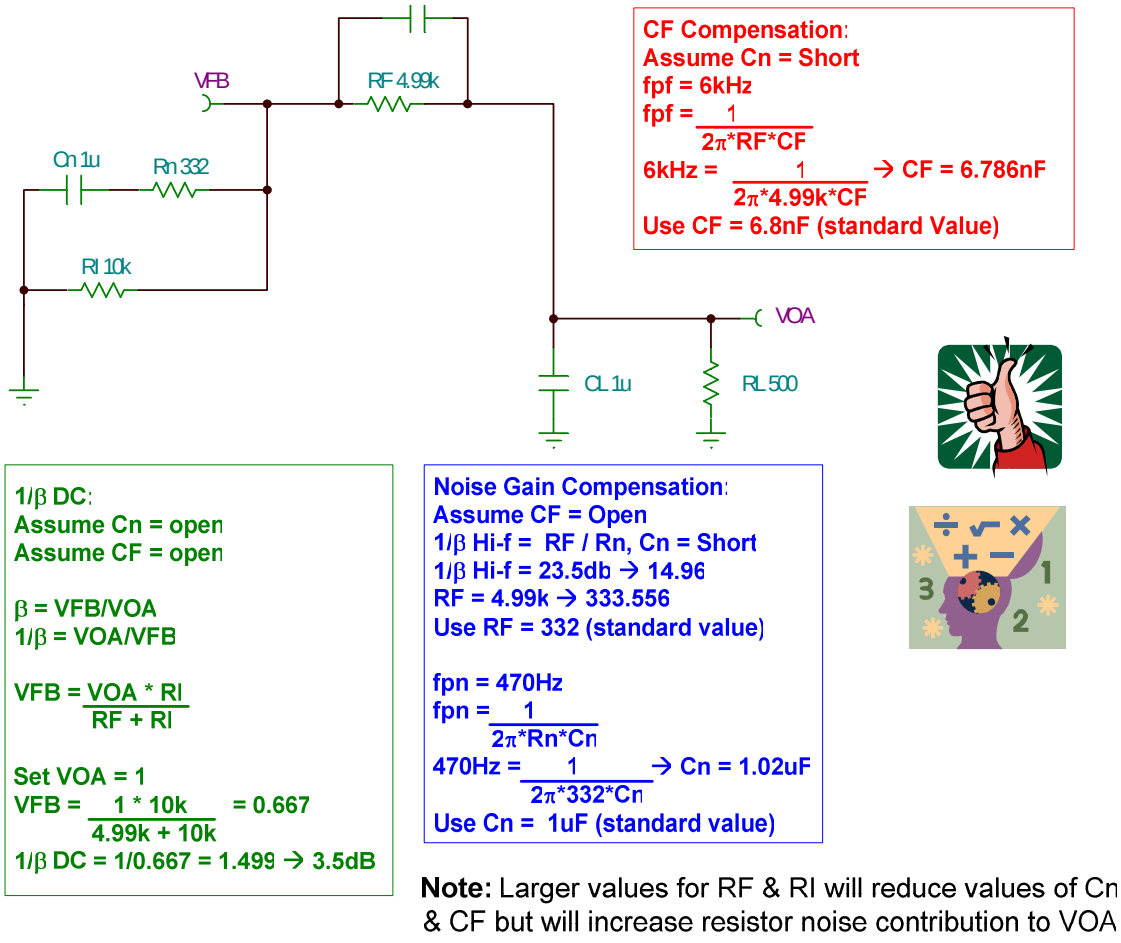


Fig. 8.22: Compensation Calculation Details

Our completed Noise Gain & CF Inverting circuit is shown in Fig. 8.23. This single circuit allows us to plot modified Aol, loop gain and 1/β. We find it most convenient to do one ac simulation run and plot modified Aol and 1/β followed by a second ac simulation for loop gain and phase.

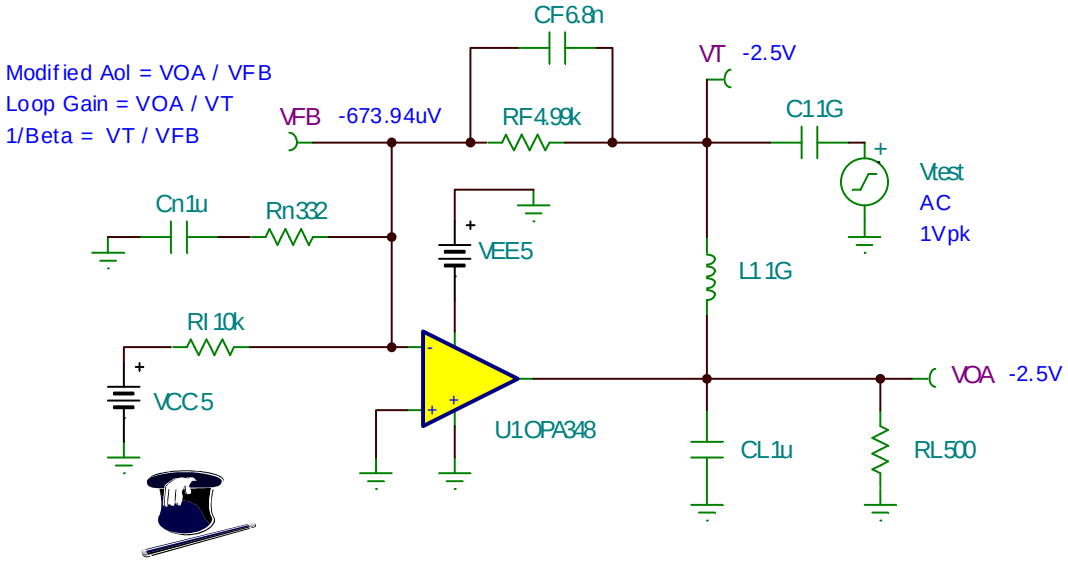


Fig. 8.23: Tina Ac Circuit With Stability Compensation

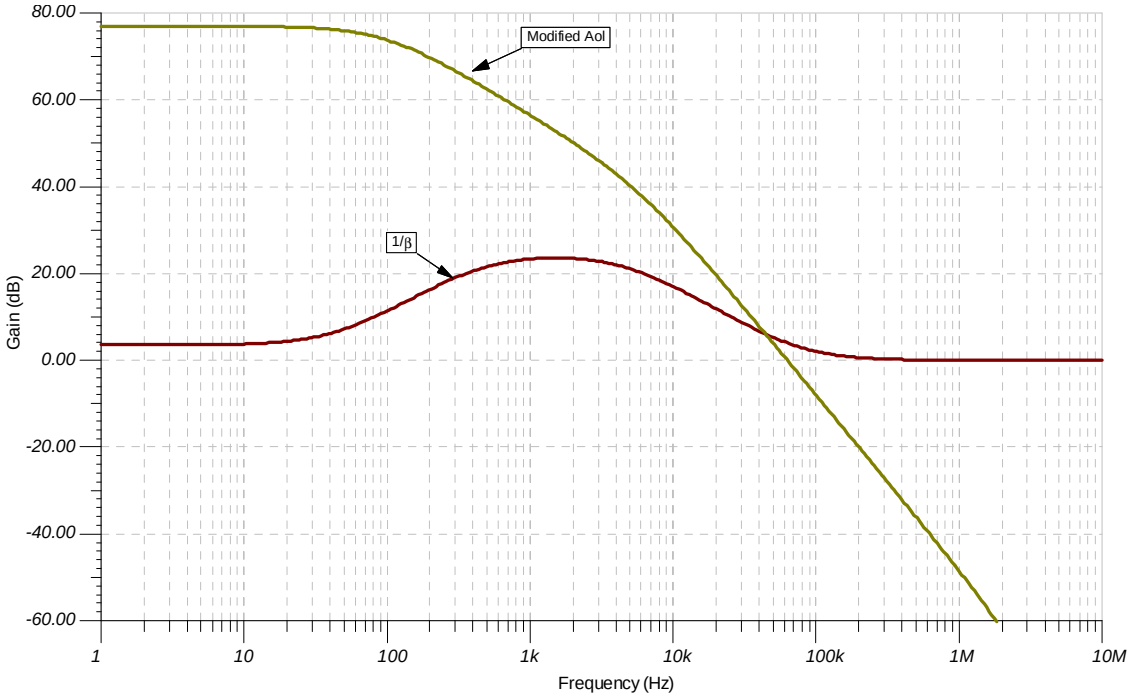


Fig. 8.24: Modified Aol & 1/β Tina Plots (With Stability Compensation)

For our completed circuit we see the 1/β and modified Aol curve (Fig. 8.24). This shows close comparison with our first-order analysis (Fig. 8.20) and produced the desired stability synthesis.

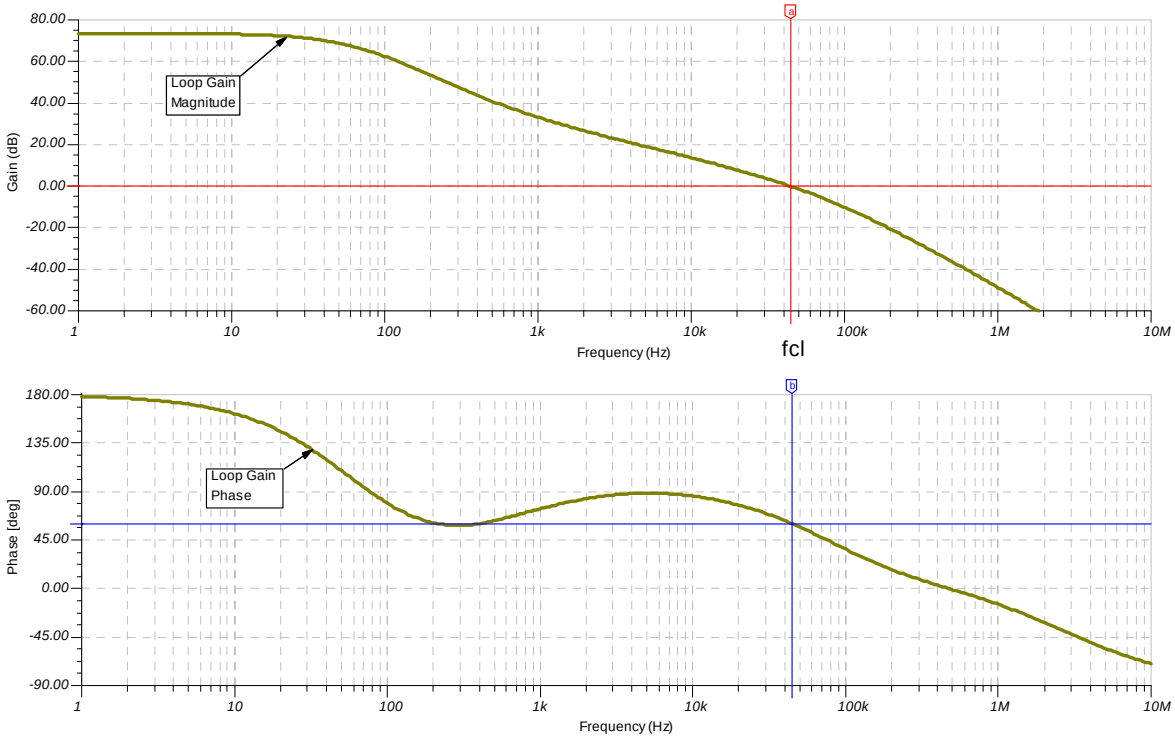


Fig. 8.25: Loop Gain Tina Plots (With Stability Compensation)

Loop gain magnitude and phase plots shown in Fig. 8.25 show our desired loop phase margin of >45° with loop phase never dipping below 45° for frequency <fcl which assures us of not only a stable circuit but excellent transient response.

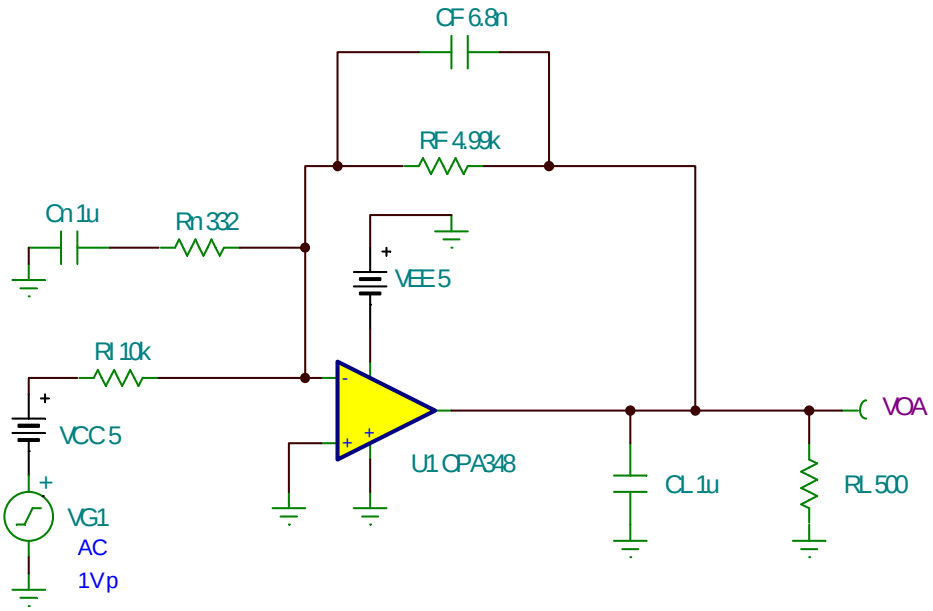


Fig. 8.26: VOUT ÷ VIN Ac Transfer Function Circuit (With Stability Compensation)

To confirm our overall closed-loop bandwidth, VOUT ÷ VIN or, specifically, VOA ÷ VG1 we will use the circuit in Fig. 8.26.

Tina simulation results in Fig. 8.27 show our closed-loop ac response to match our first-order predictions (Fig. 8.20) with -20 dB/decade at fp until we reach fcl where it changes to -60 dB/decade and follows the modified Aol curve from there on down.

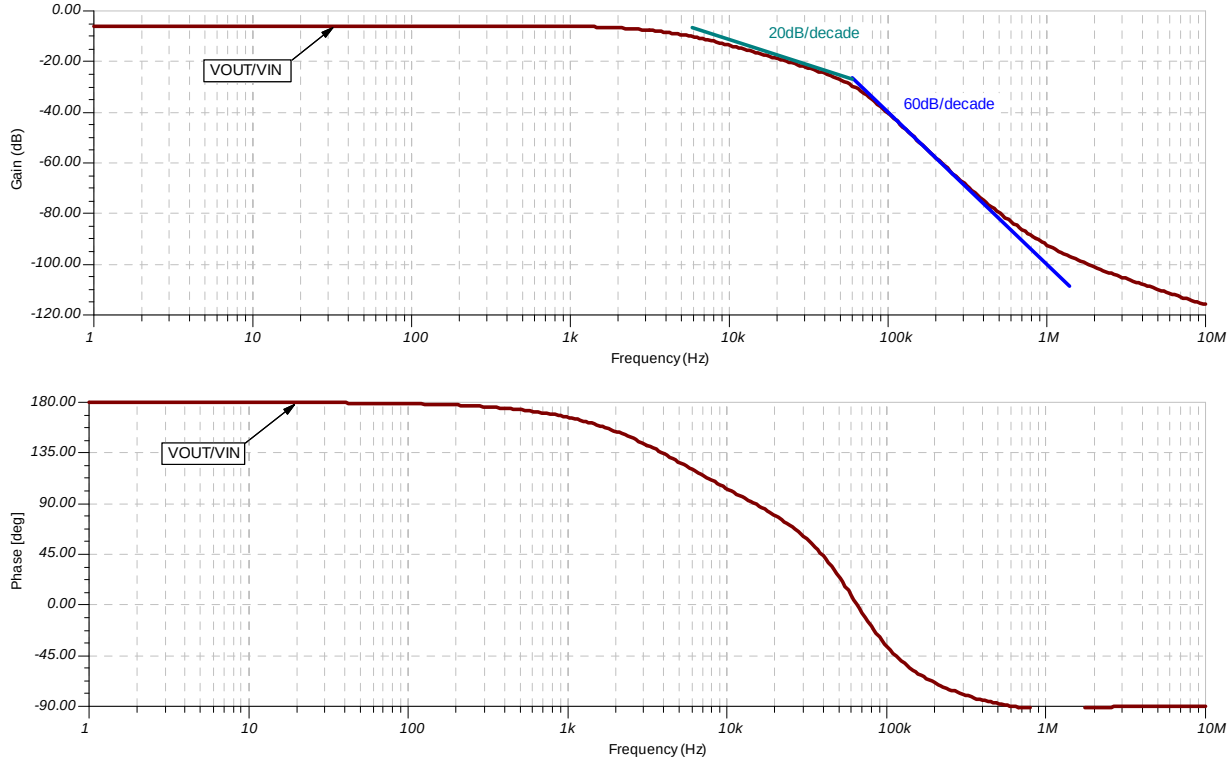


Fig. 8.27: VOUT ÷ VIN Ac Transfer Function (With Stability Compensation)

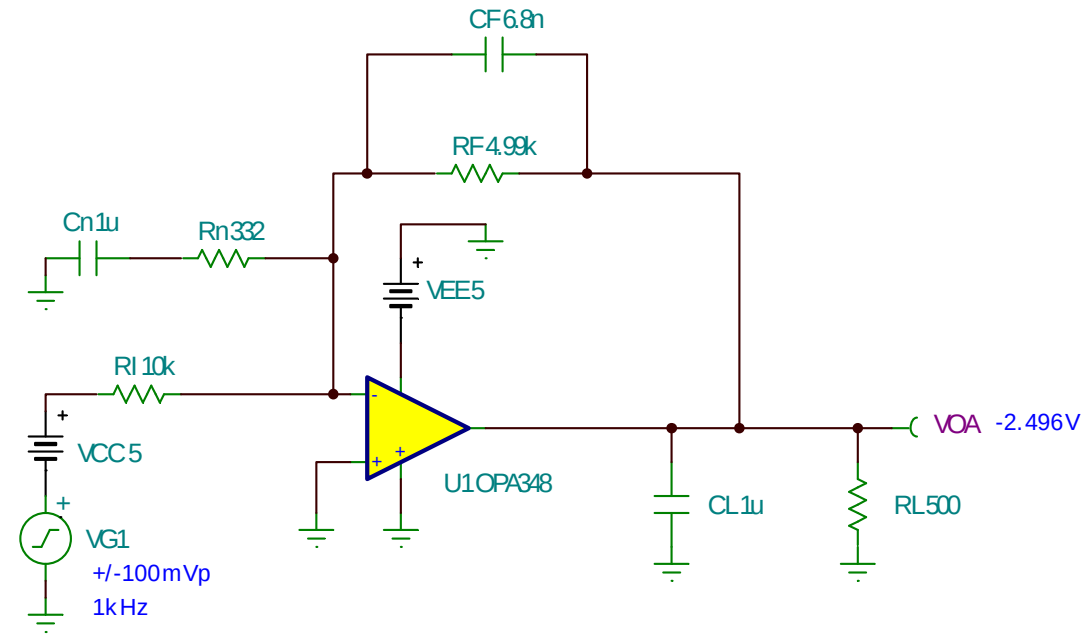


Fig. 8.28: Tina Transient Circuit (With Stability Compensation)

Let's also look at the transient response of our compensated circuit using the Tina SPICE circuit in Fig. 8.28. We expect a critically-damped response.

And indeed, as Fig. 8.29 shows, there is a direct correlation between our ac plots which checked for stability and phase margin and the transient response. We see a predictable, well-behaved transient response indicative of about a 60° phase margin.

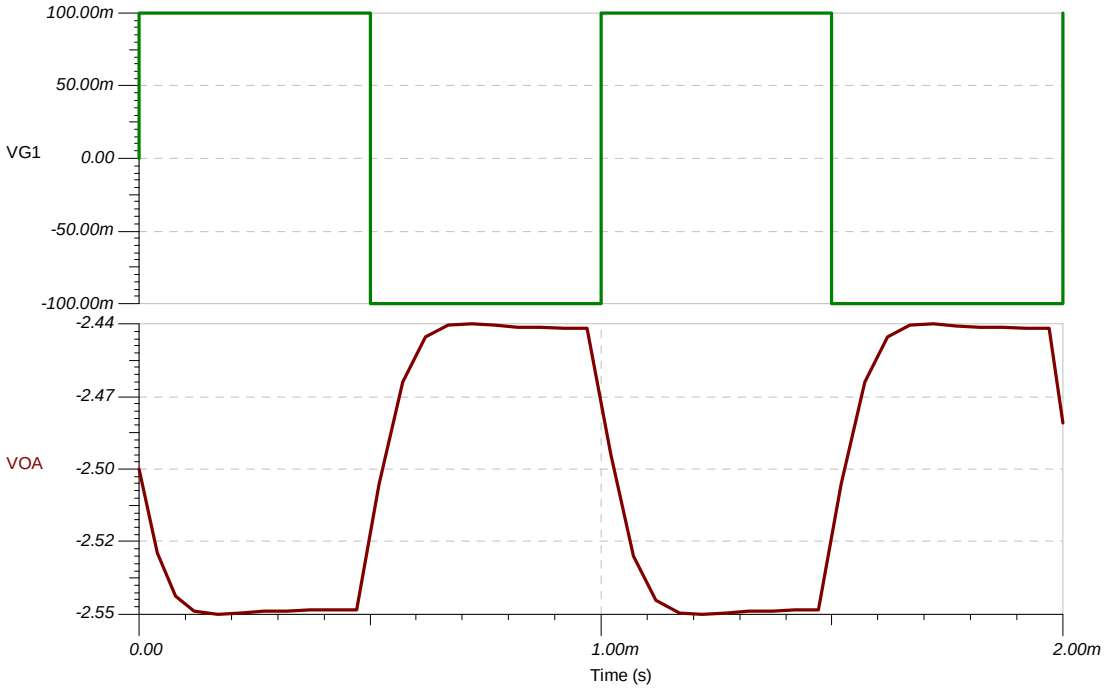


Fig. 8.29: Transient Analysis (With Stability Compensation)

Noise Gain & CF Non-Inverting

For our noise gain & CF non-inverting circuit we choose a common "Supply Splitter." This topology is often used on a single-supply system to create a mid-point reference (Fig. 8.30). We will use the same op amp (OPA348), RL (500 Ω), and CL (1 µF). Therefore we can use the same compensation as for our noise gain & CF inverting circuit. By inspection we see that the dc 1/β here will be 1 dB or 0 dB instead of the 3.5 dB on our noise gain & CF inverting circuit. However, in order for the noise gain to work as we desire here we need to ensure that VP is a low impedance at the frequency where XCn matches Rn or where fpn is located. Again we use a decade rule-of-thumb to set Vp Xac <10Rn. A standard value of CB1 = 15 µF is chosen. In addition it is a good design practice to use a 0.1 µF, CB2, in parallel with CB1 to ensure a good high frequency bypass. And we remember that here too higher values of resistors can result in lower values of capacitors with an increased noise contribution.

VP & CB1, CB2:
For Noise Gain Compensation to be Dominant VP must be an AC Low Impedance for f > fpn
fpn = 470Hz
At fpn (470Hz) set VP AC Impedance (Xac) < Rn/10
VP Xac @ fpn = 332/10 = 33.2
VP Xac @ fpn = $\frac{1}{2\pi * fpc * CB1}$
$33.2 = \frac{1}{2\pi * 332 * CB1}$ → CB1 = 14.4µF minimum
Choose CB1 = 15µF Tantalum for Low Frequency bypass of VP
Add CB2 = 0.1µF Ceramic for High frequency bypass of VP

Note: Larger values for RF & RI will reduce values of Cn, CF, and CB1 but will increase resistor noise contribution to VOA

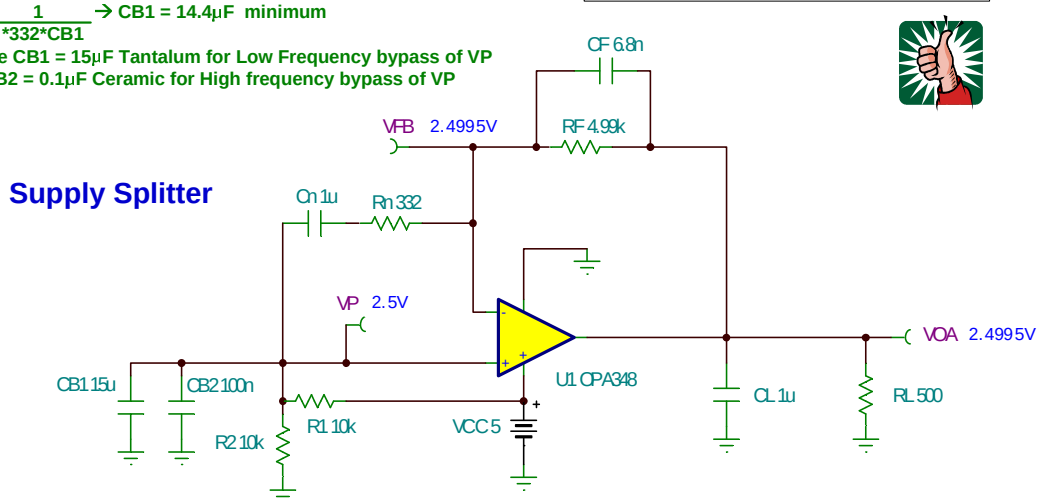


Fig. 8.30: Single-Supply Splitter

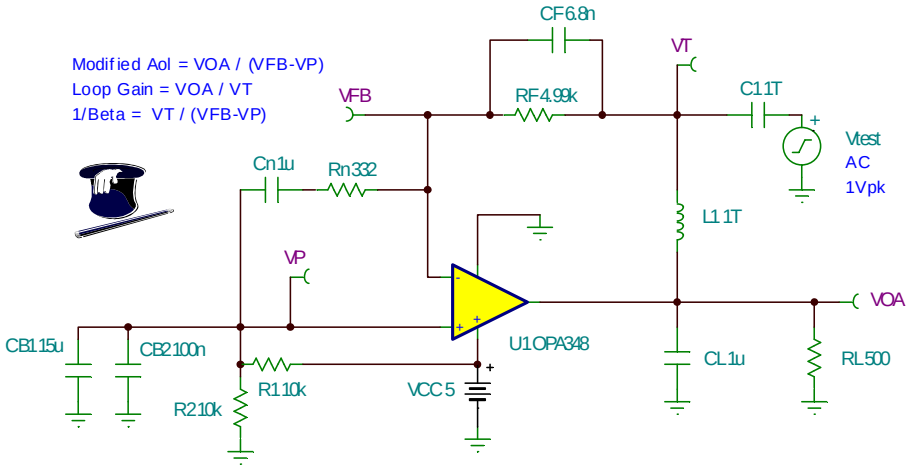


Fig. 8.31: Tina Ac Circuit With Stability Compensation

The complete circuit with stability compensation is shown in Fig. 8.31. From this topology we can use Tina SPICE ac analysis to check for stability.

The modified Aol curve and 1/β are shown in Fig. 8.32 and, to no surprise, similar to the noise gain & CF inverting plots (Fig. 8.24).

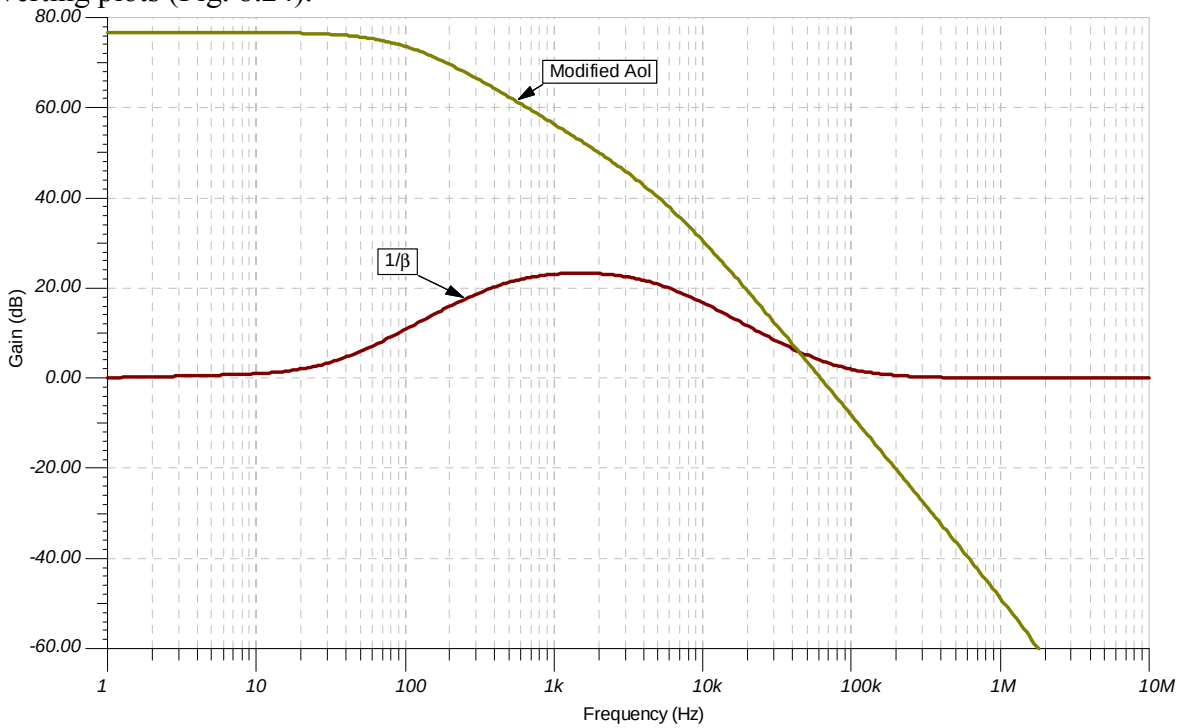


Fig. 8.32: Modified Aol & 1/β Tina Plots

Loop-gain magnitude and phase plots are shown in Fig. 8.33 and, once again, are similar to the noise gain & CF inverting case (see Fig. 8.25).

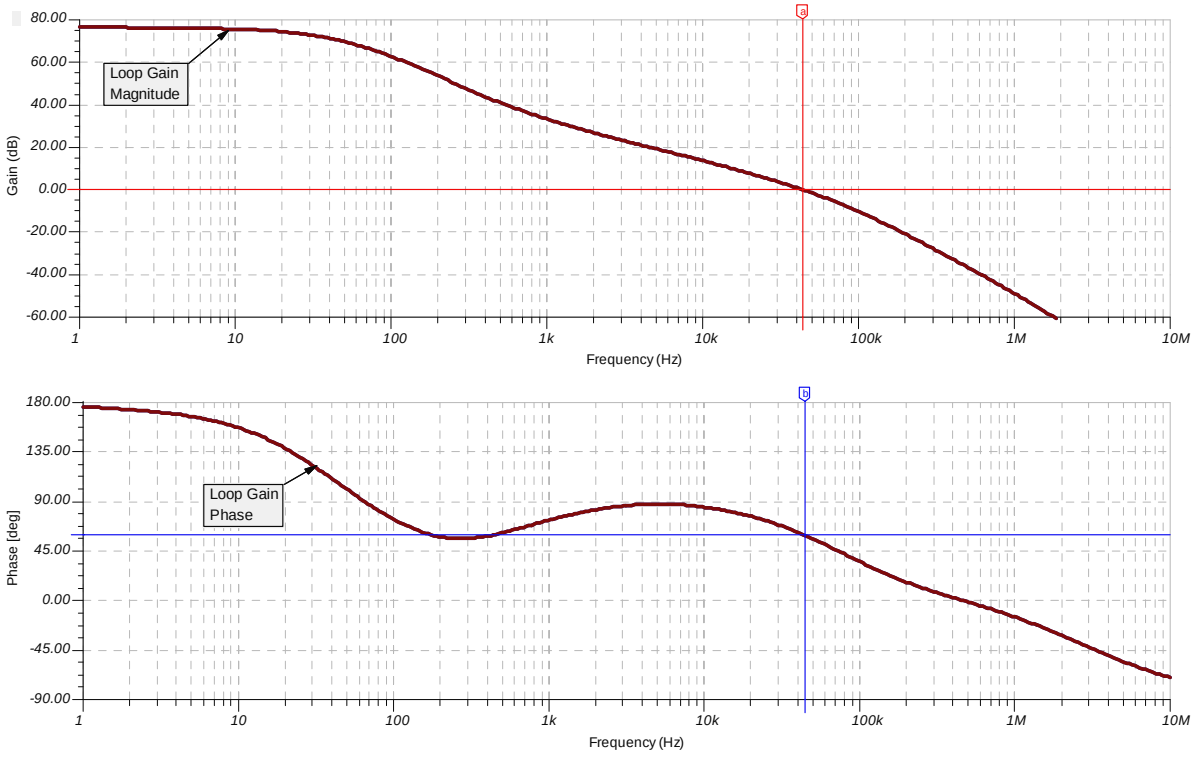


Fig. 8.33: Loop Gain Tina Plots

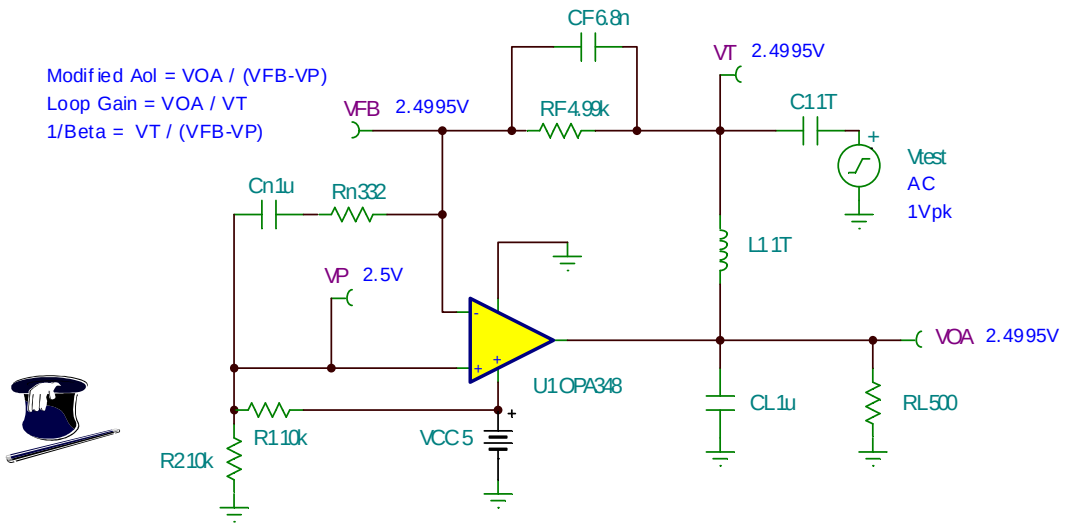


Fig. 8.34: Circuit Without CB1 & CB2

Let's use the circuit in Fig. 8.34 to investigate the effect of not making VP a low impedance as Cn becomes a short and noise gain begins to dominate.

As shown in Fig. 8.35 the 1/β computation without CB1 & CB2 is different than with them. Remember that β is the ratio of output voltage over feedback voltage to the inputs of the op amp. Many times in op amp circuits the feedback is only to the minus input and the ratio is clear to see. In this case we end up with a differential voltage across the op amps –input and +input. So now β = (VFB – VP) ÷ VOA and 1/β with VOA = 1 is 1 ÷ (VFB-VP), or the differential input voltage to the op amp. The dc 1/β = 1 by inspection since both Cn and Cf are open. When Cn becomes a short and Cf = open we have a resistive divider with RF, Rn, and R2//R1. When CF = short and Cn = short we still have a resistor divider but now with Rn and R2//R1.

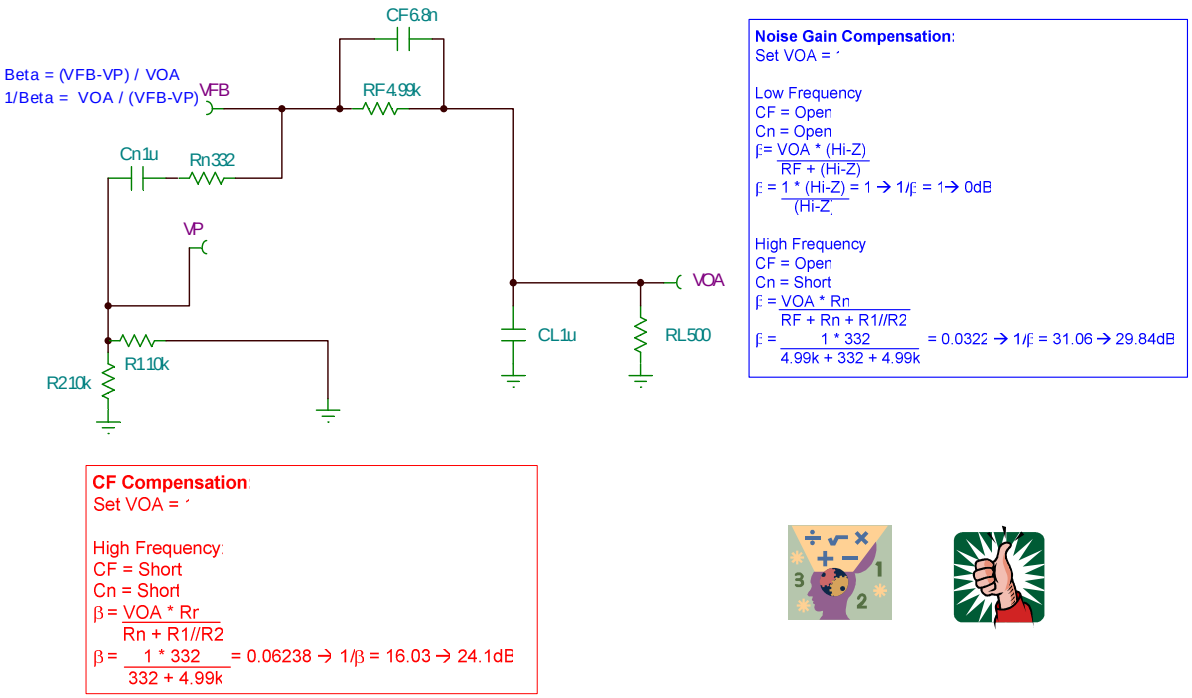


Fig. 8.35: Loop Gain Tina Plots

The results of not using CB1 & CB2 are displayed in Fig. 8.36. From our first-order criteria w/o CB1 & CB2 we have a 40 dB/decade rate-of-closure. With CB1 & CB2 we get the stability we designed for.

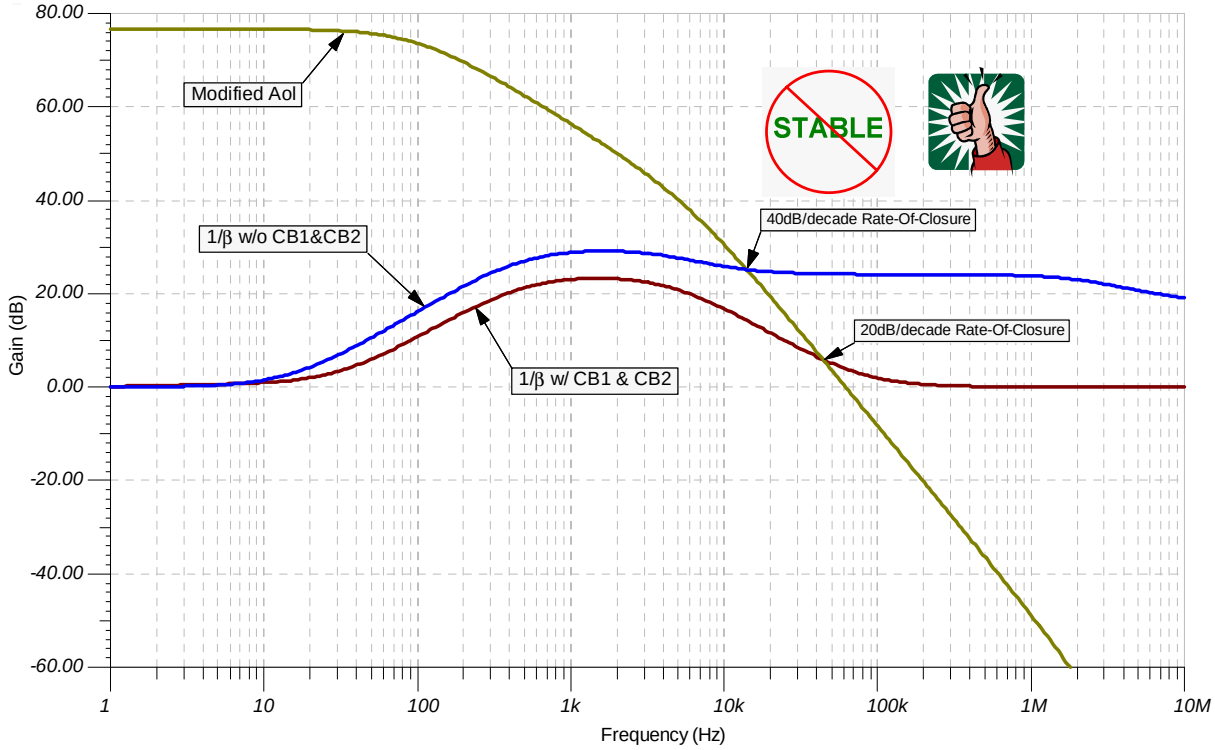


Fig. 8.36: Ac Analysis With And Without CB1 & CB2

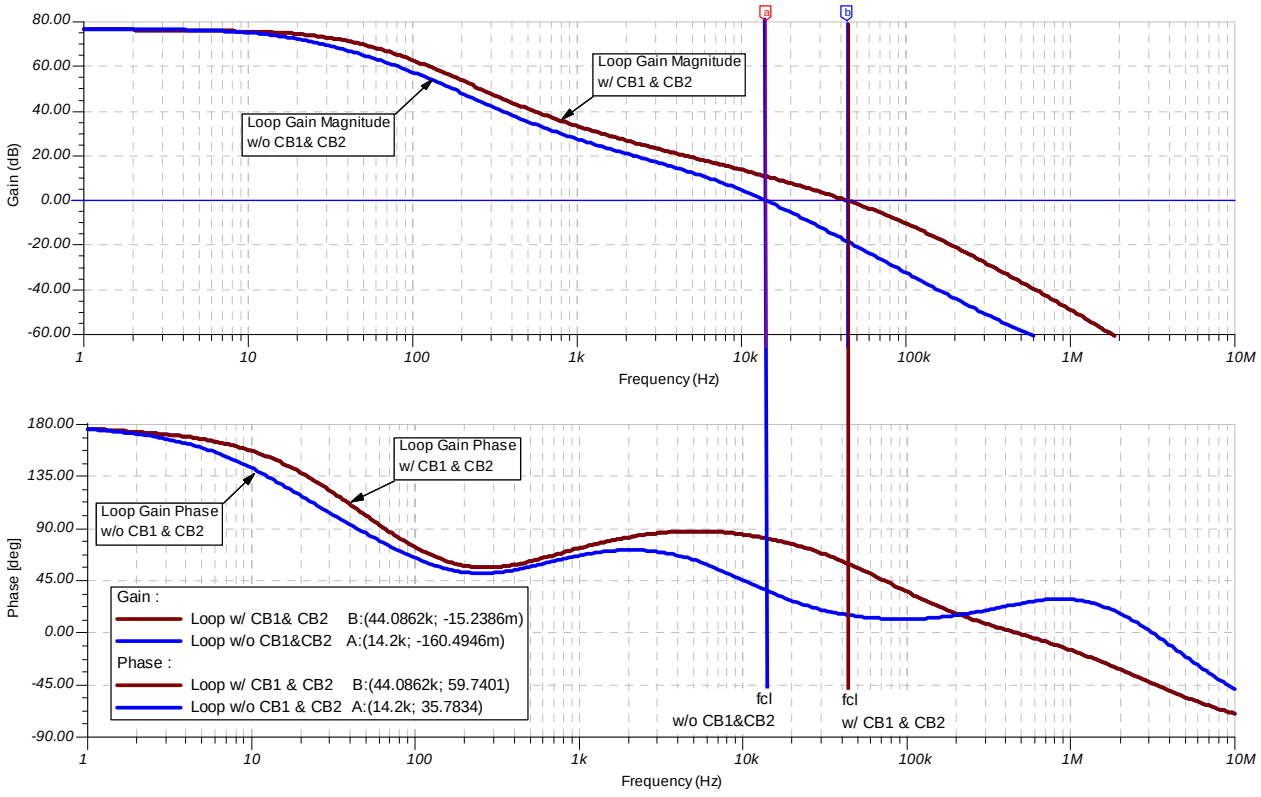


Fig. 8.37: Loop Gain With And Without CB1 & CB2

Loop-gain plots with and without CB1 & CB2 are shown in Fig. 8.37. Loop-gain phase margin with CB1 & CB2 was about 60°. Without CB1 & CB2 loop-gain phase margin is degraded to about 36°.

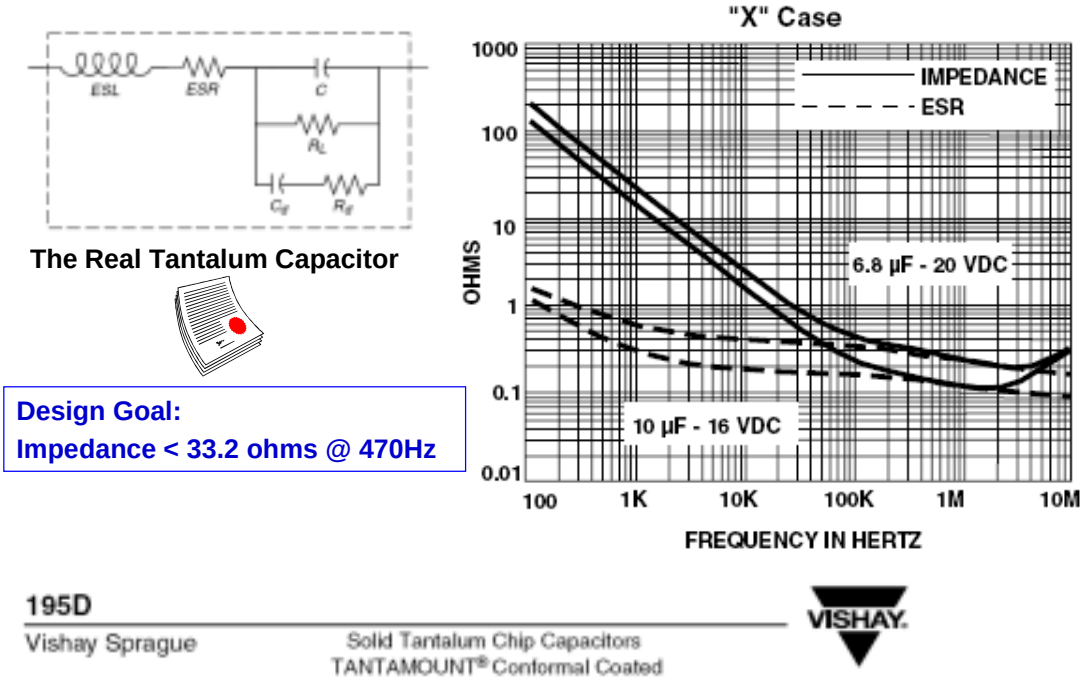


Fig. 8.38: A Word About Tantalum Capacitors

When capacitor values exceed about 1 µF, many times tantalum capacitors are used for their larger values of capacitance in a relatively small size. Tantalum capacitors are not just pure capacitance. They also have an ESR or resistive component along with smaller parasitic inductances and resistances. The most dominant component after their capacitance is their ESR. As see in Fig. 8.38 our goal for the noise gain & CF non-inverting circuit was <33.2 Ω at 470 Hz. If we look at the 10 µF curves at about 470 Hz we see an impedance of about 30 Ω. Therefore, this specific 10 µF capacitor could replace our 15 µF capacitor and work fine in our circuit. ESR varies depending upon the type of tantalum used. So we need to be careful what tantalum capacitor is used in our applications.

About The Author

After earning a BSEE from the University of Arizona, Tim Green has worked as an analog and mixed-signal board/system level design engineer for over 23 years, including brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, and CCD cameras. Tim's recent experience includes analog & mixed-signal semiconductor strategic marketing. He is currently the Linear Applications Engineering Manager at Burr-Brown, a division of Texas Instruments, in Tucson, AZ. He can be contacted at green_tim@ti.com

as published in...
analog ZONE