
Minimizing distortion in self-oscillating switching amplifiers

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Chapter 1

Introduction

Switched audio amplifiers is a field under continuous development, with several high performance commercial designs on the market today. Especially self-oscillating designs have gained a lot of attention in the recent years, because the feedback loop makes up the modulator. This results in high supply rejection and low distortion. Generally speaking there exist two types of these designs, respectively hysteretic modulated and phase modulated, each having their advantages and drawbacks. Both types in their basic form, suffer from the fact the the carrier frequency drops towards zero at a high modulation index. This increases distortion as an effect of decreased bandwidth in the modulator loop.

The objective of this project is the examine the possibility to improve the sound quality in self-oscillating switched amplifiers.

1.1 Initial design goals:

- To build a 100W (in 4Ω) power comparator suited for switched audio.
- To examine hysteresis and phase modulated self-oscillating topologies and measure their THD performance.
- To examine the possibilities of increasing the modulator openloop gain, down in the audio band, and achieve less distortion.
- To examine the possibilities to achieve a constant oscillation frequency for both hysteresis and phase modulated topologies.
- To derive some general design guidelines for supply decoupling.

Chapter 2

Switching amplifiers

A switching amplifier consists of a PWM modulated powerstage followed by a LC lowpass demodulation filter as shown in Figure 2.1. An undamped LC filter can result in a unstable amplifier and it's characteristics is of importance when included a self-oscillating loop. The

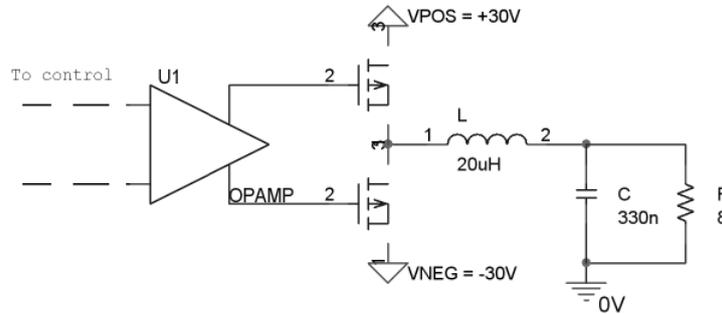


Figure 2.1: *Powerstage of with Lowpass LC demodulation filter*

transfer function for the LC filter is given in (2.1). Relating (2.1) to the general transferfunction for a 2. order system in (2.2) provides information about the quality factor Q (2.3) and the natural frequency ω_n (2.4).

$$LCR(s) = \frac{X_C \parallel R}{X_L + X_C \parallel R} = \frac{1}{s^2 CL + s \frac{L}{R} + 1} \quad (2.1)$$

$$H_{2.order}(s) = \frac{1}{s^2 \frac{1}{\omega_n^2} + s \frac{1}{Q\omega_n} + 1} \quad (2.2)$$

$$Q = R \sqrt{\frac{C}{L}} \quad (2.3)$$

$$\omega_n = \frac{1}{\sqrt{CL}} \quad (2.4)$$

For $Q > 0.5$ the system is underdamped with complex polepair and for $0.5 > Q$ the system is overdamped with two real poles. A typical LC-filter for switching amplifiers has a complex pole pair with a Q in the range of 1 – 5.

In Figure 2.2 the transient and frequency domain characteristics of a second order circuit with varying Q is given. An amplifier with no load has a very high Q value and does exhibit a very oscillatory behavioral which can lead to failure of the device. The problem can be solved by using a Zobel network to damp the filter or by means of including the filter in the feedback loop. This subject will be treated in the following chapters.

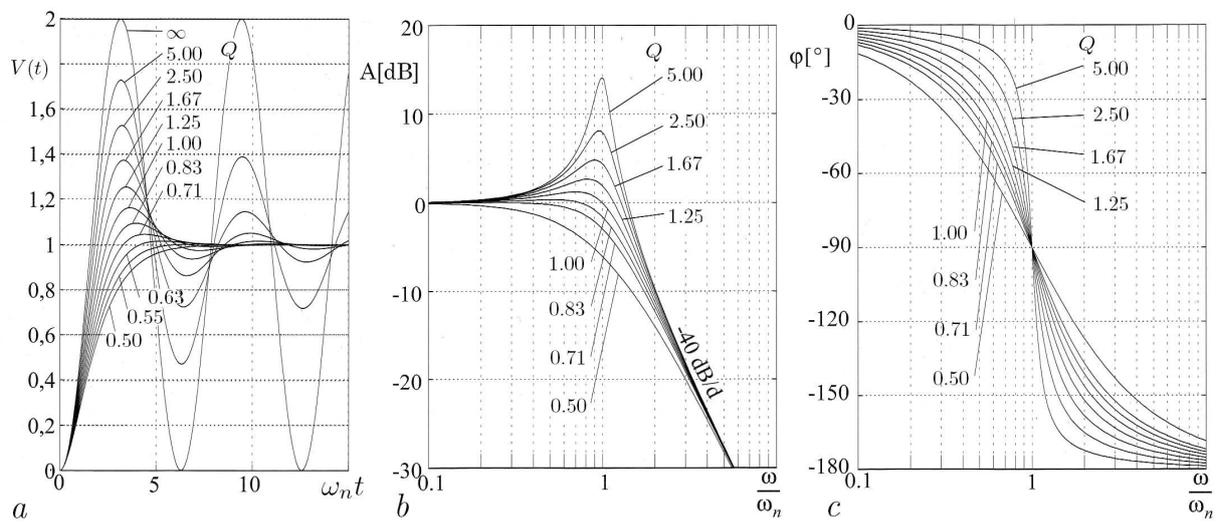


Figure 2.2: *Characteristic properties of a 2nd-order system: (a) Step responses, (b) and (c) bode plot.*

2.1 Types of distortion in switching amplifiers

It's very difficult to design a switching amplifier without feedback that achieves low distortion. The technical requirements for the power supply, the power stage and the PWM modulation are simply to large, as it will be shown in the following.

There are three dominating sources of distortion in switching amplifiers, respectively deadtime in the power stage, supply pumping and nonlinear PWM modulation.

According to [11] a full bridge openloop switching amplifier needs a supply resistance of $4m\Omega$ to achieve a distortion figure below $0.01\%THD$ due to supply pumping. The problem in a half-bridge configuration is even worse and would require a tightly regulated SMPS power-supply event to approach such a low impedance.

The nonlinear modulation in self-oscillating amplifiers is caused by a nonlinear carrier [2]. The amount of distortion is hard to predict and is best analyzed by simulation or actual implementation.

The effect of deadtime in the power stage is well understood [4] and can be predicted. In Figure 2.3 an output signal with deadtime can be seen. As long as the output inductor current ripple is larger than the load current at the moment of switching, its current is in the right direction to force the output stage node voltage to begin slewing to the other rail immediately when both MOSFETs turn off at the beginning of deadtime (this is natural commutation - also known as soft switching). For larger load currents, slewing doesn't commence until the end of deadtime when the other MOSFET forces the voltage to change. Thus, unlike a linear class-b amplifier (where deadtime is at zero output) there are two deadtime zones at non zero load current (symmetrically spaced about zero). A deadtime below $10ns$ is needed to achieve a distortion figure

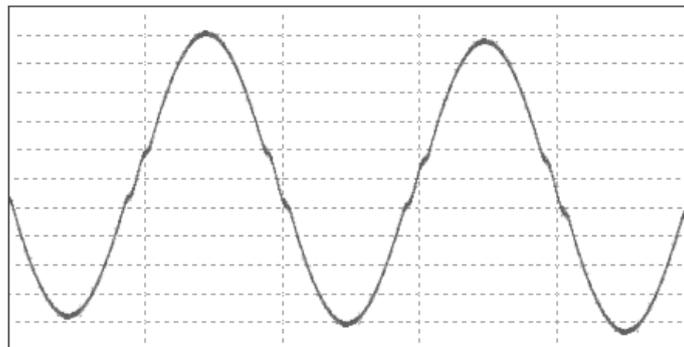


Figure 2.3: *Output waveform due to deadtime in the output stage. Two crossover zones are present.*

of $0.01\%THD$.

2.2 Self-oscillating amplifiers

Since it's expensive and difficult to achieve low distortion in an openloop amplifier, feedback should be applied. Self-oscillating topologies has one loop that provides feedback as well as carrying out the actual modulation. This provides high performance with a low complexity.

This small signal bandwidth of self-oscillating amplifiers includes the switching frequency, which comprises a loop gain that is several times larger than what can normally be accomplished in clocked amplifiers. The resulting output impedance becomes very small and the suppression of errors such as distortion and noise becomes large. A throughout analysis of achieving low

2.2. SELF-OSCILLATING AMPLIFIERS

distortion in self-oscillating amplifiers will be covered in the subsequent chapters.

Chapter 3

Passive implementations

An ideal hysteric loop has a 1st order characteristic with phase change of -90° in the modulation band¹, which translates to a single pole in origo in the s-plane. The only design parameter is the static loop gain, which determines the amplitude of the triangular carrier waveform.

A practical amplifier typically has a single LC-filter placed in series with the switching stage to attenuate the carrier waveform in a lossless manner. This introduces a complex pole pair to the loop. By adding a PID (proportional-integral-derivative) controller to the loop, a nearly 1st order characteristic can be achieved². A common implementation of this controller would be an active PI-lead³ opamp circuit. It is however possible to design a much cheaper passive PID controller.

In this chapter a head-to-head comparison of respectively a passive hysteric and a passive phase oscillating loop will be made.

3.1 The passive hysteric loop

Figure 3.1 illustrates a basic hysteric amplifier. It consists of a passive P-lag-lead controller, a power comparator with delay and a demodulation LC-filter. The combined transfer-function of the controller and the LC-filter should approach a 1st order characteristic in order to provide a linear carrier [2]. This design goal has been achieved by using the Advanced Optimization feature of PSpice to find the correct values for the complex passive PID controller.

A bode-plot of the combined transfer-characteristic can be seen in Figure 3.2.

The phase stays close to -90° from $10kHz$ and up to $3MHz$ which corresponding to a first order characteristic. A measure of how well a self-oscillating amplifier suppresses errors, such as distortion, is the loop-gain. A part of the loop-gain provided by the power comparator and is a function of delay [3], the other part is provided by the relative loop gain in the P-lag-lead+LC-filter loop.

In Figure 3.2 the hysteric window is designed for a switching frequency of $350kHz$.

Property 3.1 *The ratio between the amplitude at the switching frequency and a given point down in the audio band, provides a relative measure of the loop gain. This ratio should be kept as large as possible to achieve low THD and low output impedance.*

The relative loop-gain for the current hysteric is $30dB$.

¹From the frequency of oscillation and up to infinity.

²Ideally a complex zero pair, a real pole in origo and a real zero would be needed to achieve a 1. order characteristic.

³Since the order of the numerator in a transfer function can never exceed the denominator, a derivative term can not be implemented. The practical approach is a lead compensator, which consists of a slow zero followed by faster pole.

3.1. THE PASSIVE HYSTERETIC LOOP

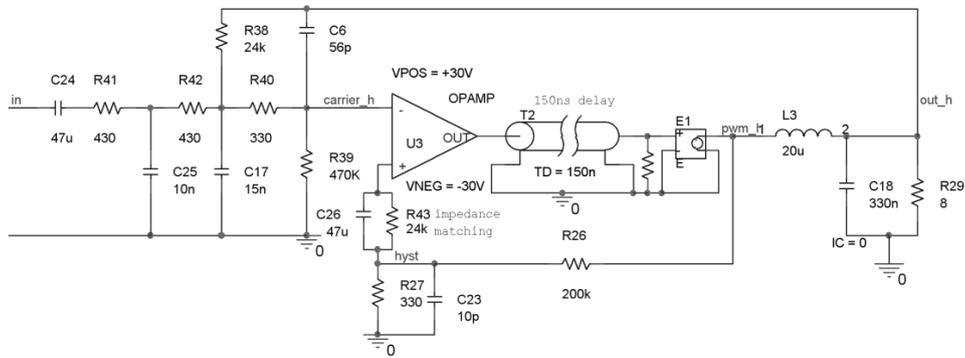


Figure 3.1: Conceptual passive-loop hysteretic amplifier. Passive P-lag-lead compensator (from feed to P-lag-lead), LC-filter and intended Power-comparator.

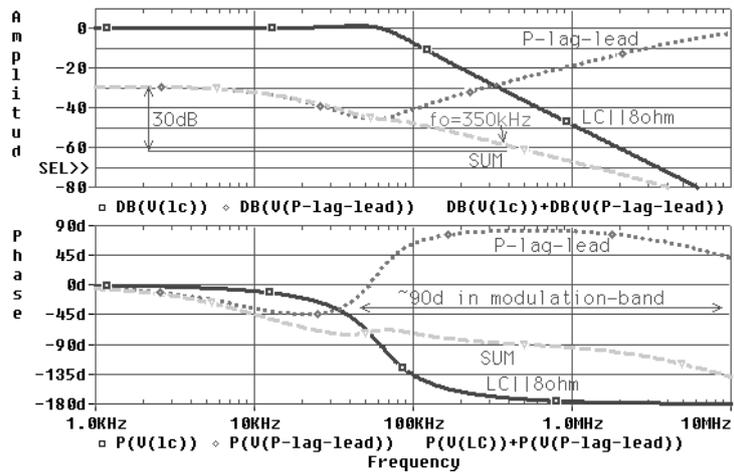


Figure 3.2: Bodeplot of passive hysteretic loop (SUM).

3.2 The diverted passive phase oscillating loop

The hysteric configuration can easily be turned into a phase oscillating amplifier Figure 3.3, by adding an extra pole to the P-lag-lead controller and removing the hysteretic window. The pole is made by placing a resistor in series with C_6 .

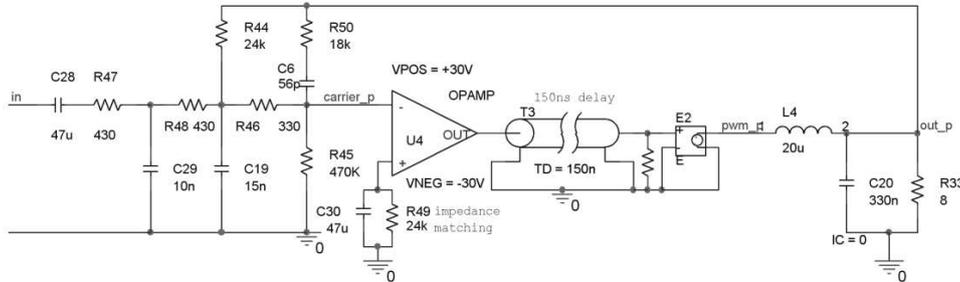


Figure 3.3: Implementation of passive phase oscillating amplifier.

The bode-plot of the phase-oscillating configuration can be seen in Figure 3.4.

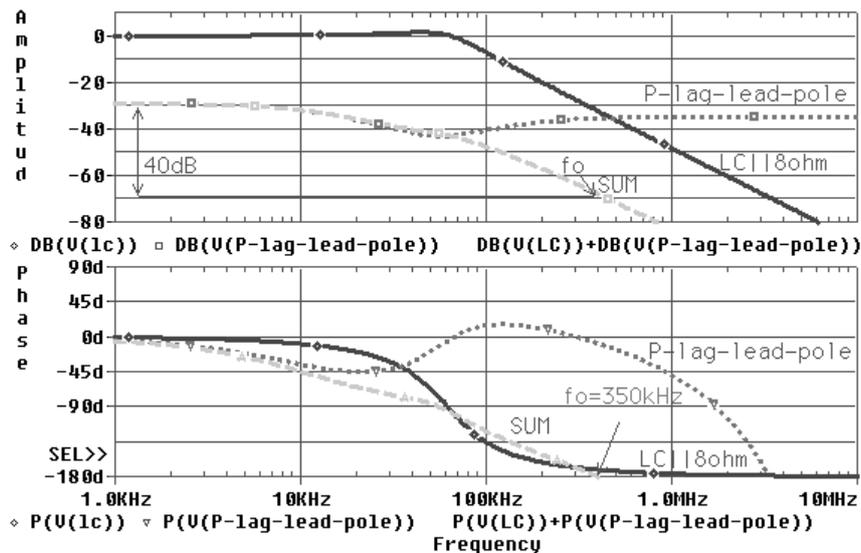


Figure 3.4: Bodeplot of passive phase oscillating loop (SUM).

The phase crosses -180° at $350kHz$ and therefore this will become the switching frequency. The relative loop-gain is $40dB$, which is $10dB$ more than for the hysteretic configuration. With no existing model of the small signal gain of the power comparator in phase-oscillating mode, the two relative loop gains cannot directly be compared.

3.3 Time domain performance of the hysteretic and the phase-oscillating amplifier

A simulation of the two amplifiers can be seen in Figure 3.5. The carrier of the two amplifiers can be seen in figure 3.5c and 3.5d. In the hysteretic oscillator the output stage switches when the triangular carrier crosses the hysteretic window. The phase-oscillating amplifier switches

3.3. TIME DOMAIN PERFORMANCE OF THE HYSTERETIC AND THE PHASE-OSCILLATING AMPLIFIER

when the carrier crosses zero.

The output voltage of the two amplifiers has an amplitude of $20V$ and a frequency of $1kHz$.

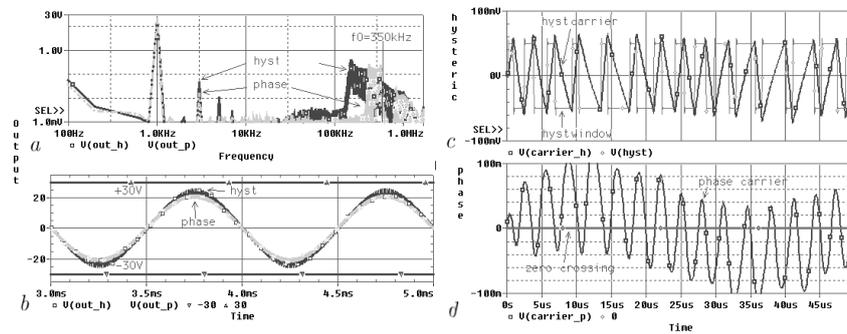


Figure 3.5: *a), b): Simulation of passive hysteric and passive phase oscillating amplifier at high modulation. c), d) Carrier of respectively hysteric and passive phase oscillating amplifier with a 10kHz referenc.*

With $\pm 30v$ rails the modulation is 66%. The FFT analysis of two amplifiers in 3.5a shows that they both suffer from THD due to nonlinear modulation. The phase-oscillating amplifier has a smaller distortion and a smaller drop in switching frequency than the hysteric amplifier. Figure 3.6 shows a PSpice simulation of THD versus amplitude for the two amplifiers.

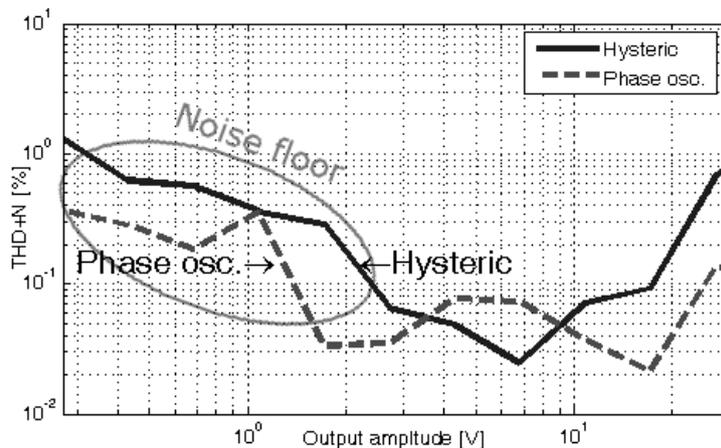


Figure 3.6: *PSpice simulated THD+N vs. amplitude for respectively hysteric and passive phase oscillating amplifier with a 1kHz tone. The plot is made in MATLAB, see appendix C.*

Both amplifiers has a THD of about 0.05% at a few volts output. The phase-oscillating amplifier does however perforce best at high modulation.

Using the power comparator, which will be described later in chapter 10, the hysteric and the phase-oscillating P-lag-lead loops has been build. The measured THD can be seen in Figure 3.7.

Although deadtime distortion and supply pumping was not included in the PSpice model, the THD performance does not differ much from reality. The phase-oscillating amplifier does again perform slightly better than the hysteric.

3.3. TIME DOMAIN PERFORMANCE OF THE HYSTERETIC AND THE PHASE-OSCILLATING AMPLIFIER

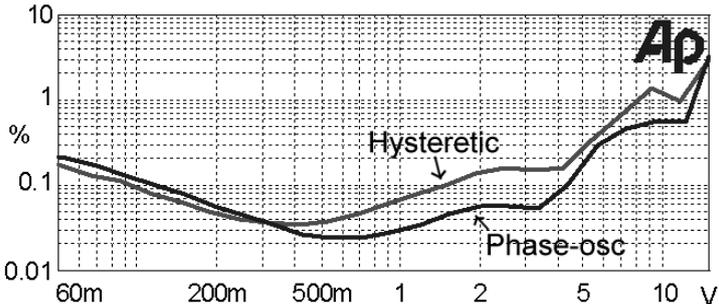


Figure 3.7: Measured THD+N vs. amplitude for respectively hysteric and passive phase oscillating amplifier with a 1kHz tone at +/- 20V rails.

Chapter 4

Second order active THD shaper

To reduce distortion in self-oscillating amplifiers, then relative loop gain has to be increased. In this chapter a general building block for THD shaping will be presented. In Figure 4.1 two active poles with a cutoff frequency at $8kHz$ has been added to the phase-oscillating amplifier from the previous chapter.

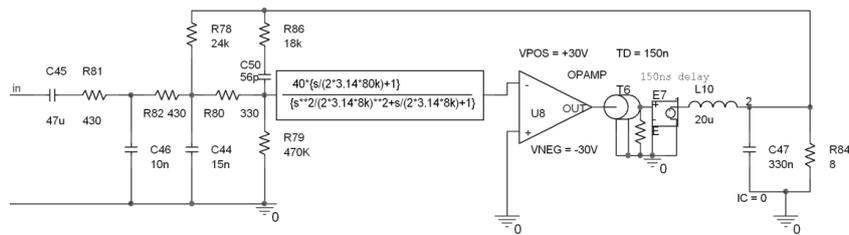


Figure 4.1: Improved phase-oscillating amplifier with two active poles.

To recover the phase two zeros at $80kHz$ has also been added to the circuit. The transfer function of the improved amplifier compared with the original one can be seen in Figure 4.2a.

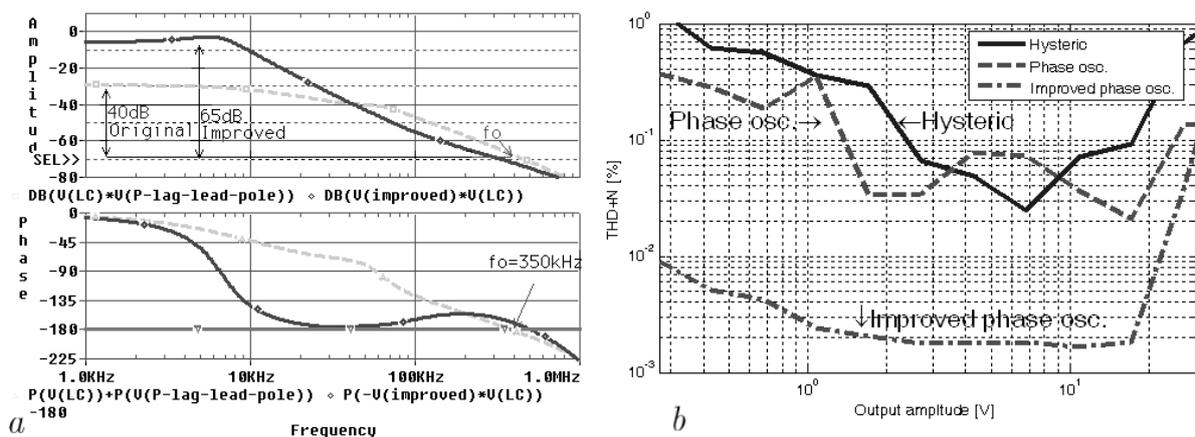


Figure 4.2: Improved phase-oscillating amplifier with two active poles.

The relative loop gain of the improved amplifier is $65dB$, which is $15dB$ more than the original one. The PSpice THD simulation in Figure 4.2b clearly shows that the improved relative loop-gain has a positive impact on distortion. The distortion has been decreased by $17dB$.

4.1 Active second order circuit

In Figure 4.2a a laplace table was used to add two active poles the loop. This laplace table can implemented with a modified version of active opamp circuit in Figure 4.3.

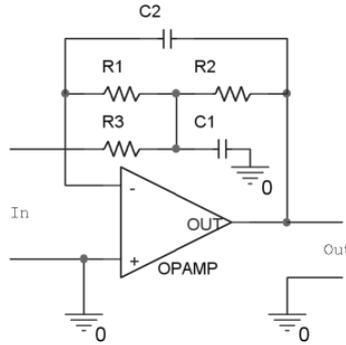


Figure 4.3: 2nd-order lowpas filter.

By nodal analyses the transfer function for 4.3 can be determined to (4.1):

$$H(s) = -\frac{R_2}{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 + R_1 R_3 + R_2 R_3) C_2 s + R_3} \quad (4.1)$$

By choosing the relations in (4.2), (4.1) reduce to (4.3):

$$\begin{aligned} \frac{C_1}{b^2} = C_2 = C \quad R_1 = R_2 = R_3 a = R \\ H(s) &= -a \frac{R}{\frac{R^3}{a} C^2 b^2 s^2 + \left(R^2 + \frac{R^2}{a} + \frac{R^2}{a}\right) C s + \frac{R}{a}} \\ &= -a \frac{1}{R^2 C^2 b^2 s^2 + RC(2+a)s + 1} \end{aligned} \quad (4.3)$$

It can be identified that (4.3) is a 2nd-order transfer function capable of realizing a static loop gain a which can be larger than unity. By relating (4.3) to general transfer function of a second order system in (2.2), then relation between the parameters (4.2) and the natural frequency together with the quality factor can be found (4.4):

$$\omega_p = \frac{1}{RCb} \quad Q_p = \frac{b}{2+a} \quad (4.4)$$

This relates into the final equations suited for design (4.5):

$$R_1 = R_2 = R \quad R_3 = \frac{R}{a} \quad C_1 = \frac{Q_p(2+a)}{R\omega_p} \quad C_2 = \frac{1}{R\omega_p Q_p(2+a)} \quad (4.5)$$

The resulting schematic can be found in Figure 4.4.

For the purpose of THD shaping, the lowpas filter is intended to be placed inside a closed loop. This requires a pair of zeros in the transfer function (4.3) in order to give the designer an opportunity to attain a certain phase margin. The filter (4.4) can be modified to realize complex as well as real zeros.

4.2 Real zeros

By placing a resistor i series with each capacitor in 4.4 two real zeros can be attained. This is shown in Figure 4.5(a). The angular velocity of the two zeros is chosen to be equal and is

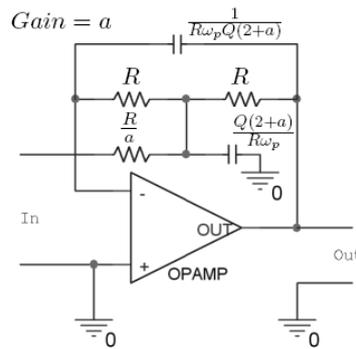


Figure 4.4: 2nd-order lowpas filter with design parameters.

equated with the general 1st-order RC cutoff relation in (4.6).

$$R_4 = \frac{1}{C_2 \omega_{z2}} = \frac{R \omega_p Q_p (2 + a)}{\omega_{z1}} \quad R_5 = \frac{1}{C_1 \omega_{z1}} = \frac{R \omega_p}{Q_p (2 + a) \omega_{z2}} \quad (4.6)$$

The resulting schematic can be found in Figure 4.5(b).

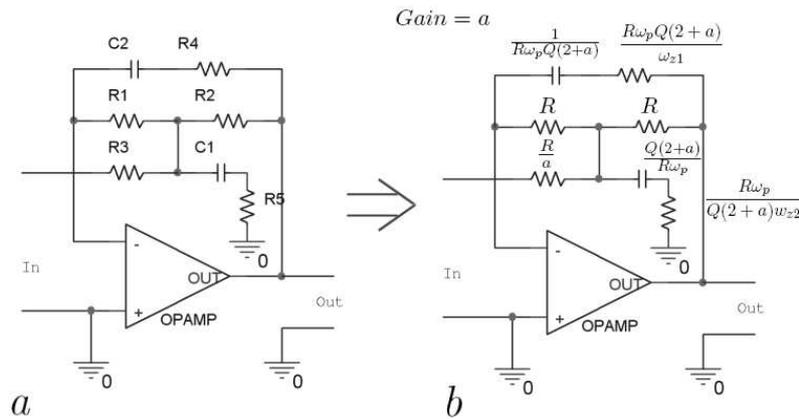


Figure 4.5: 2nd-order lowpas filter with real zeros.

4.3 Complex zeros

The relation between the quality factor and characteristics of zeros are the inverse of those shown for poles in Figure 2.2. In the frequency domain the phase change of complex zeros are much steeper than it is for real zeros. Because of this, complex zeros can be placed closer to the frequency where a given phase margin is wanted, than it is the case for real zeros.

Complex zeros are constructed by adding feed-forward to the filter, Figure 4.6.

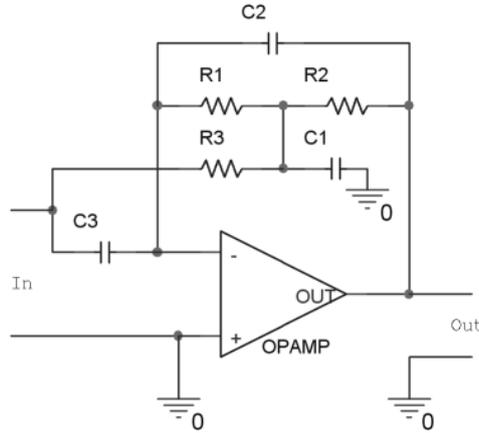


Figure 4.6: 2nd-order lowpas filter with complex zeros.

The transfer function becomes (4.7):

$$H(s) = -\frac{C_1 C_3 R_1 R_2 R_3 s^2 + (R_1 R_2 + R_1 R_3 + R_2 R_3) C_3 s + R_2}{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 + R_1 R_3 + R_2 R_3) C_2 s + R_3} \quad (4.7)$$

The term in the denominator is the same as previously in (4.1), which means that everything relating to the poles in the circuit stays unchanged. On account of this, the same simplifying relations from (4.2) are chosen again with one addition (4.8):

$$C_3 = C b^2 a e^{-2} \quad (4.8)$$

The transfer-function can now be written as (4.9):

$$H(s) = -a \frac{R^2 C^2 b^2 e^{-2} s^2 + R C b^2 e^{-2} (2 + a) s + 1}{R^2 C^2 b^2 s^2 + R C (2 + a) s + 1} \quad (4.9)$$

Relating (4.9) to general transfer function of a second order system in (2.2), the notation in (4.10) should be achieved:

$$H(s) = -a \frac{\frac{1}{\omega_z^2} s^2 + \frac{1}{\omega_z Q_z} s + 1}{\frac{1}{\omega_p^2} s^2 + \frac{1}{\omega_p Q_p} s + 1} \quad (4.10)$$

The relation between the parameters (4.8), the natural frequency and the quality factor becomes (4.11):

$$\omega_p = \frac{1}{R C b} \quad Q_p = \frac{b}{2 + a} \quad e = \frac{\omega_z}{\omega_p} \quad Q_z = \frac{e b}{2 + a} \quad (4.11)$$

This relates into the final design equations(4.12):

$$R_1 = R_2 = R \quad R_3 = \frac{R}{a} \quad C_1 = \frac{Q_p(2+a)}{R \omega_p} \quad C_2 = \frac{1}{R \omega_p Q_p(2+a)} \quad C_3 = \frac{\omega_p}{\omega_z^2 R Q_p(1+\frac{2}{a})} \quad (4.12)$$

4.4. HIGH-Q ZEROS

As a consequence of choosing ω_z the quality factor of the zeros becomes (4.13):

$$Q_z = Q_p \frac{\omega_z}{\omega_p} \quad (4.13)$$

the final filter schematic with design parameters is given in Figure (4.7)

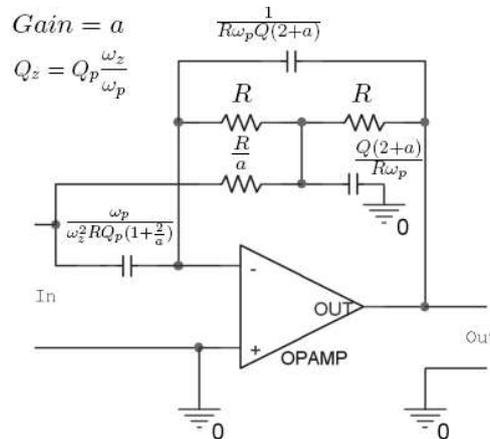


Figure 4.7: 2nd-order lowpas filter with complex zeros and design parameters.

4.4 High-Q zeros

The quality factor in (4.13) tends to become quite high. With just one decade between the two cutoff-frequencies and a reasonable quality factor of the poles, the zeros becomes nearly imaginary with a very large quality factor. For filter applications this is ofte a quite desirable and it's used in Chebyshev II, Hourglass and Elliptic (also know as Cauer) filters. The imaginary zeros will appear as a notch in the transfer function and can be used to increase the cutoff slope in lowpass filters without increasing the order.

In THD shaping applications however, a loop is closed around the filter and the very-high-Q poles has some undesirable effects:

Constrain 4.1 *The High-Q feed forward zeros can extend into the right half plane, provided the smallest amount of extra phase shift from of the opamp or parasitic components. This would result in a large negative phase shift instead of a positive phase shift which was intended.*

Constrain 4.2 *The switching frequency of self-oscillators tend to drop with increasing modulation. Because of this, the frequency response below the switching frequency affects behavior at high modulation. With a notch below the nominel switching frequency, the carrier signal becomes so attenuated when the modulation increases, that the modulator starts oscillating at a very low frequency and gets caught in that mode.*

With a quality factor below 2 the phase change is stille steep but the notch is avoided and there is no risk of having right-half-plane-zeros.

4.5 Reduced Q zeros

The filter in figure 4.7 can be modified to implement moderate zeros, by changing phase of the injected feed-forward signal within a smal frequency band. In Figure 4.8 C_3 is substituted with

a phase lag network. This introduces one extra pole and one extra zero to the transfer function (4.9) besides allowing Q-adjustment. However these can be made to cancel out by obeying (4.14) and (4.15).

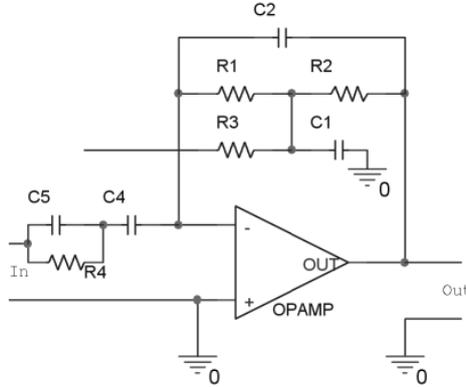


Figure 4.8: *2nd-order lowpass filter with complex zeros and adjustable quality-factor.*

The series capacitance of C_4 and C_5 should equal the originally C_3 and the cutoff-frequency of C_5 and R_4 should equal that of the zeros ω_z :

$$\frac{1}{C_3} = \frac{1}{C_5} + \frac{1}{C_4} \quad (4.14)$$

$$\omega_z = \frac{1}{C_5 R_4} \quad (4.15)$$

This leaves the ratio between C_4 and C_5 as the last degree of freedom:

$$\frac{C_4}{C_5} = k \Rightarrow C_5 = C_3 \left(1 + \frac{1}{k}\right) \quad C_4 = C_3(1 + k) \quad (4.16)$$

An analysis of the resulting large transfer function will not be carried out here, since it is possible to adjust the Q independently of any other parameters. Numerical analysis shows that by choosing k between 1 and 50 a nearly imaginary pair of zeros can be converted to attain a low Q in the order of respectively 4 and down to 1.

Chapter 5

Including the post LC-filter in the loop, a topology lineup

The output filter should be included in the feedback loop, in order to minimize the output impedance of an amplifier together with distortion caused by inductor saturation and nonlinear dielectric voltage characteristics. The main obstacle towards doing this, is the -180° phase shift asymptote introduced by the LC-filter after the cutoff frequency. A hysteretic loop needs only $\approx -90^\circ$ of phase-shift at HF and a phase-shift oscillating loop needs less than -180° before the idle switching frequency. The solution to this problem is introduce some way of recovering the phase at HF. Table 5.1 sums up some of the current self-oscillating topologies and the way in which the phase is recovered.

The COM/MECC was the first solution that included the LC-filter in the feedback loop by using feed-forward, but successful control of the filter is not presented. Mueta was the first to introduce the way of differentiating the capacitor voltage to approximate the ripple current. The circuit in work is an lead-compensator, which has been used well before 2002 in control engineering to provide a positive contribution to the phase shift that approaches 90° . The lead solution has later been reinvented under the name GLIM and also in the form of a phase-shift oscillator UCD.

The lead solution has proven itself worthy, but it does has some drawbacks. With a passive lead-compensator the voltage ripple component after the LC-filter has to be large, in order to have a sufficient small-signal gain after the lead-compensator. An active compensator does not require a large ripple voltage, but it has the penalty of cost. Especially the hysteretic solutions are prone to suffer from these drawbacks, since it needs -90° phase-shift well beyond the LC-filter cutoff frequency to produce a triangular carrier.

The BPCM together with the Leapfrog topology are two new solutions to the phase-recovery problem and they are, oppose to Mueta/GLIM, COM/MECC and UCD, not protected by patents. The Leapfrog approach uses a passive lossy ripple current circuit to recover the phase. Since current sense resistors on the rails are already needed in solutions with short-circuit protection, it does not necessarily introduce added cost or complexity to use this circuit. Together with BPCM, these two solutions approximate the inductor current instead of the capacitor current (lead solutions). This has the penalty of increased output impedance, since the inductor current includes the output current in addition the ripple current.

As it will be proposed in the following, the feed-forward approach can be extended to provide full control of the LC-filter. The key factor is to work with the combined frequency-response of the feedback and the feed-forward loops, instead of first closing the feed-forward loop and then the feedback loop around it. This will be covered in the following chapter 6.

Topology name Year published Oscillator type	Way of recovering phase	Note
Mueta [5] 2002 Hysteretic	Ripple current estimation by output capacitor differentiation.	A 1st order integrating feedback loop is recognized as being sufficient to achieve low THD. The output inductor effectively becomes integrator at HF and it's mentioned that the low frequency performance can be improved by adding a integrator to the loop at LF.
GLIM [6] 2004 Hysteretic	Ripple current estimation by output capacitor differentiation	A linear triangular carrier is recognize as the main way of achieving a linear modulation and thereby low distortion. Two loops are designed separately which combined give an approximately 1. order loop and linear carrier.
BPCM [1] 2006 Hysteretic	Ripple current estimation by lowpass filtering the inductor differetial voltage	Two loops are designed to combined give linear carrier.
COM/MECC [8] 1998 Phase-shift oscillation	Feedback is taken from before the output filter	The output filter is included in the loop but the majority of the feedback is taken from before the filter. A zobel network is needed to damp the filter.
UCD [7] 2005 Phase-shift oscillation	Rippel current estimation by output capacitor differentiation	The comparator delay is identified and used to provide a part of the delay that sets on the oscillation. Additional poles are added to the loop in order to suppress distortion. Somme steps are made towards a small-signal model.
Leapfrog (appendix A) 2005 Hysteretic	MOSFET current sense	The inductor current flows through the two power MOSFETs. A linear circuit using four BJTs and two small resistors (in the sub $100m\Omega$ region), one on each rail, forms an active current sense configuration with a current output.

Table 5.1: *Sum up of self-oscillating topologies that include the output filter in the feedback loop.*

Chapter 6

Feed-forward phase recovery

In subsection 4.3 it was analyzed how feed-forward can provide means of constructing complex zeros to recover the phase. This method can also be used with the post LC-filter in amplifiers by bypassing the filter at HF. The simplest approach is to sum the transfer-function of the filter with an attenuated signal proportional to the input signal as shown in 6.1a. Some practical values are given and the combined frequency-response in Figure 6.1c indicates that the phase does recover. The notch and the steep phase flank in the frequency-response indicates imaginary zeros, which is emphasized by the fact that, summing to signals that are approximately 180° out of phase will result in a pair of complex high-Q zeros.

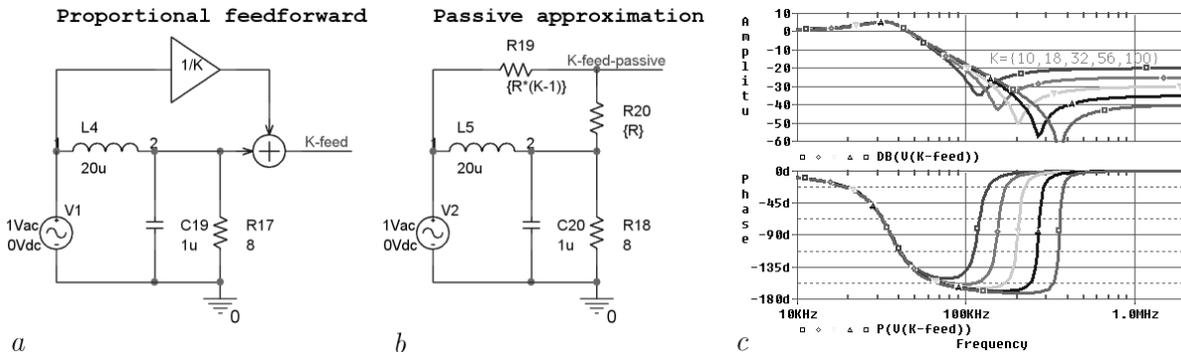


Figure 6.1: LC-filter with proportional feed-forward.

The combined transfer function of the circuit is given in (6.1):

$$H_{K-feed}(s) = \frac{1}{\frac{1}{\omega_p^2}s^2 + \frac{1}{\omega_p Q_p}s + 1} + \frac{1}{K} \quad \text{where} \quad \omega_p = \frac{1}{\sqrt{CL}} \quad \text{and} \quad Q_p = R\sqrt{\frac{L}{C}} \quad (6.1)$$

The transfer function can be rewritten to the form in (6.2):

$$\begin{aligned} H_{K-feed}(s) &= \frac{1+K\left(\frac{1}{\omega_p^2}s^2 + \frac{1}{\omega_p Q_p}s + 1\right)}{\frac{1}{\omega_p^2}s^2 + \frac{1}{\omega_p Q_p}s + 1} \\ &= \left(1 + \frac{1}{K}\right) \frac{\frac{1}{(1+K)\omega_p^2}s^2 + \frac{1}{(1+K)\omega_p Q_p}s + 1}}{\frac{1}{\omega_p^2}s^2 + \frac{1}{\omega_p Q_p}s + 1} \end{aligned} \quad (6.2)$$

It's now clear that the proportional feed-forward circuit does result in a pair of zeros since a second order term is present in the numerator. By breaking (6.2) into second order terms on the

6.1. FEED-FORWARD WITH ONE ZERO

form (6.3), information about the cutoff frequency of the complex poles and the quality factor (6.4) is revealed:

$$H_{K-feed}(s) = \left(1 + \frac{1}{K}\right) \frac{\frac{1}{\omega_z^2} s^2 + \frac{1}{\omega_z Q_z} s + 1}{\frac{1}{\omega_p^2} s^2 + \frac{1}{\omega_p Q_p} s + 1} \quad (6.3)$$

$$\omega_z = \omega_p \sqrt{1 + K} \quad Q_z = Q_p \sqrt{1 + K} \quad (6.4)$$

In relation to Constrain 4.1 and Constrain 4.2 high-Q zeros are not practical in self-oscillating amplifiers. The circuit in 6.1 is therefore more a proof on concept than a practical approach.

6.1 Feed-forward with one zero

To avoid high-Q zeros, the phase of the feed-forward signal should be negative at the amplitude where the two summed signals cross each other. In Figure 6.2a the feed-forward signal comes from lag-compensator with attenuation K and cutoff-frequency ω_{p2} . By this the transfer-function becomes first order at HF. In Figure 6.2c the lag cutoff-frequency is chosen to be the same as the cutoff-frequency in (6.4). In this way the phase of the feed-forward signal becomes $\approx -45^\circ$ where the amplitude of the two signals cross each other.

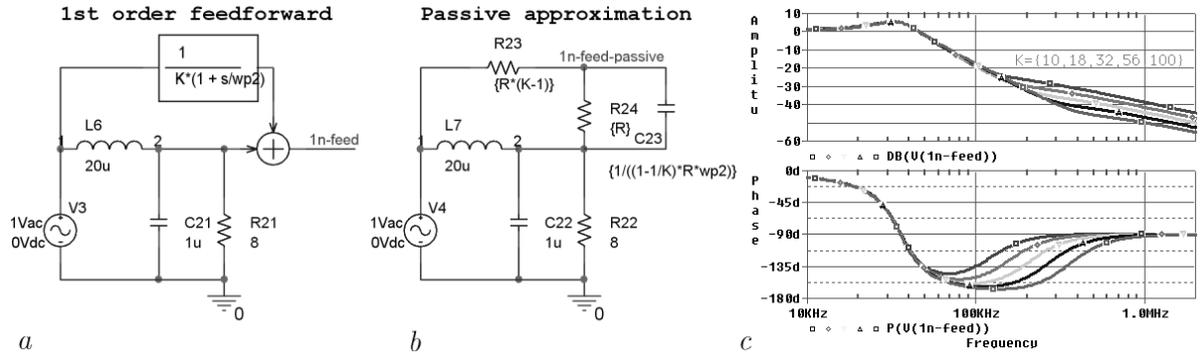


Figure 6.2: LC-filter feed-forward that reduces the transfer function to first order at HF.

The transfer-function of the circuit is given in (6.5):

$$\begin{aligned} H_{1n-feed}(s) &= \frac{1}{\frac{1}{\omega_p^2} s^2 + \frac{1}{\omega_p Q_p} s + 1} + \frac{1}{K \left(\frac{a}{\omega_{pa}} s + 1 \right)} \quad \text{where } a = \frac{\omega_p}{\omega_{p2}} \\ &= \left(1 + \frac{1}{K}\right) \frac{\frac{1}{(1+K)\omega_p^2} s^2 + \frac{1+aQ_pK}{(1+K)Q_p\omega_p} s + 1}{\left(\frac{1}{\omega_p^2} s^2 + \frac{1}{\omega_p Q_p} s + 1\right) \left(\frac{a}{\omega_{pa}} s + 1\right)} \end{aligned} \quad (6.5)$$

The circuit in Figure 6.2 appears to introduce one zero to the transfer-function, but it can be verified from (6.5) that it actually introduces an extra pair of zeros and an extra real pole to the transfer-function. In Figure 6.2c one of these zeros approximately cancels out with the extra pole.

By breaking (6.5) into first and second order terms, the cutoff frequency and the quality factor becomes:

$$\omega_z = \omega_p \sqrt{1 + K} \quad Q_z = Q_p \sqrt{1 + K} \frac{1}{1 + Q_p a K} \quad (6.6)$$

The cutoff frequency and the quality-factor can now be adjusted independently. It is possible to make one of the zeros cancel out perfectly with the extra pole in the transfer-function, by choosing $Q_z = 0.5$ and $\omega_{p2} = \omega_z$.

6.2 Practical feed-forward examples

Figure 6.3 illustrates three differed examples of feed-forward together with their transfer characteristics.

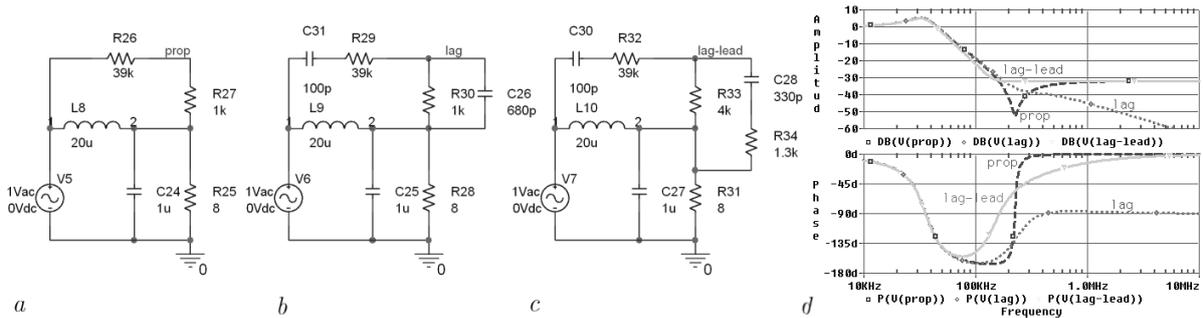


Figure 6.3: *Self-oscillating amplifier with feed-forward.*

(a) uses proportional feed-forward as described in section 6 and is included as a reference. (b) uses lag feed-forward as described in subsection 6.1. Complex zeros with one pole on top are realized to get at steep phase change. C_{31} is added so that as much of the signal comes from the LC-filter down in the low-frequency-band. In this way the signal from the LC-filter is more than $40dB$ larger than the feed-forward signal below $20kHz$ and full filter control is achieved. (c) uses lag-lead feed-forward and is not described in the previous sections. Because the numerator in the transfer-function becomes of order three the zeros can only be found numerically. By proper design the configuration implements two zeros with variable Q . C_{30} has the same function as C_{31} .

6.3 Self-oscillating amplifier with feed-forward phase recovery

To demonstrate the practical use of feed-forward around the post LC-filter look at the self-oscillating amplifier configuration in Figure 6.4a.

The circuit consists of an input summing lowpass amplifier $U8$, a second order THD shaper with $40dB$ gain $U7$, a power comparator on $+/- 30V$ rails $U6$, $150ns$ delay $T3/E2$ and a LC filter with feed-forward. Two sinus sources are present respectively the reference $V10$ and the error source $V12$. The open-loop transfer-characteristic is given in 6.4(b). Two -180° crossings are present, but only the fastest one will start the amplifier oscillating. The relative loop gain is $94dB$ in the audio band and the ideale oscillating frequency sets in at $790kHz$.

Figure 6.4c and 6.4d shows a time domain simulation with FFT analysis of the amplifier respectively with the reference source the or error source active.

No distortion components due to nonlinear modulation can be spottet in the FFT analysis when the source is active. PSpice computes a THD of 0.00078% with 10 harmonics, but it's really just a measure of the noise floor. In the band between $10kHz$ and $500kHz$ it can be seen that the loop gain is suppression the noise floor. The amplitude of ripple component on top of the sinus is roughly $10mV$ although the carrier is $142mV$.

With the $10V$ error source active only $91\mu V$ is present on the output, which corresponds to an

6.3. SELF-OSCILLATING AMPLIFIER WITH FEED-FORWARD PHASE RECOVERY

error suppression of 101db. Since the error source is placed after the LC-filter, feed-forward does prove full control of the filter.

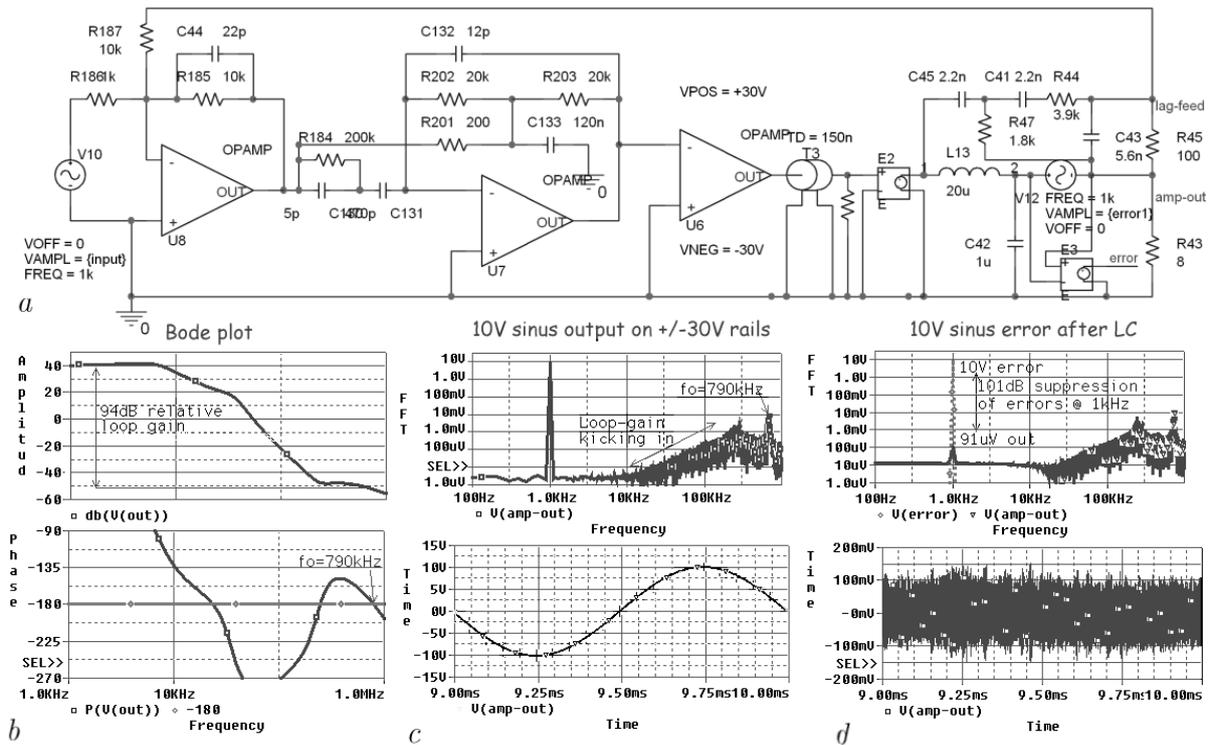


Figure 6.4: Three different feed-forward configurations and their transfer characteristic.

Chapter 7

Self-oscillating amplifiers with a constant switching frequency

A common problem in self-oscillating amplifiers is that the SF (switching frequency) drops when the modulation approaches 100%. This causes the ripple voltage on the output LC-filter to increase together with increased distortion, because the loop-gain drops. There exist examples, within the literature of self-oscillating amplifiers of how to achieve a reduced drop in SF for hysteretic amplifiers: [10] is a patent from 1992 that utilize a variable hysteretic window using a multiplier. [9] utilize a variable modulator forward gain, which results in a reduced drop in SF. In the following a hysteretic amplifier without a drop in SF will be presented. With a simple discrete circuit, the hysteretic windows is changed inverse proportional to the output voltage. A way of achieving a reduced drop in SF for phase-oscillating amplifiers will also be presented.

7.1 Switching frequency with a variable hysteretic window

According to [9] the SF of an ideal hysteretic modulator¹ drops as function of modulation with the following relation:

$$f_s(M) = f_{s,idle} (1 - M^2) \quad (7.1)$$

By altering the hysteretic window with the same relation, the SF can be held constant (7.2):

$$V_{window}(M) = V_0(1 - M^2) \quad (7.2)$$

It is however not easy to implement square function with analog components. With proportional regulation of the hysteretic window (7.3), the SF can be limited to never drop below the idle SF (7.4).

$$V_{window}(M) = V_0(1 - M) \quad (7.3)$$

$$f_s(M) = f_{s,idle} (1 + M - M^2) \quad (7.4)$$

The SF as function of modulation is plotted in Figure 7.1. The penalty of using proportional regulation instead of square regulation is that the SF rises 25% above the idle SF at 50% modulation, instead of being constant.

Because the SF never drops below idle with proportional regulation, the solution is a satisfying approximation.

¹An ideal hysteretic modulator has an 1st order open-loop transfer characteristic, i.e. a pure integrator.

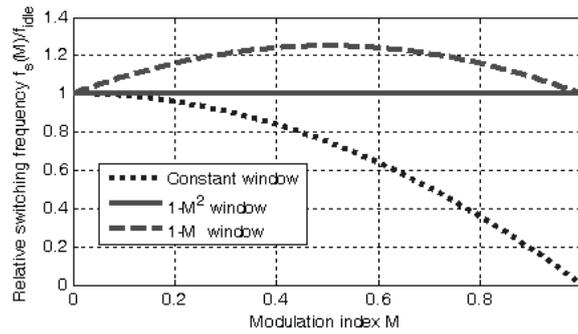


Figure 7.1: Relative switching frequency as function of modulation index with respectively a constant, a (7.2) varied and a (7.3) varied hysteretic window.

7.2 Discrete implementation of variable hysteretic window

As it will be presented, the hysteric window can easily be varied proportional to the modulation by the use of discrete components. In Figure 7.2 a simple hysteretic modulator can be seen. It is included as a reference and can be modified to implement constant SF.

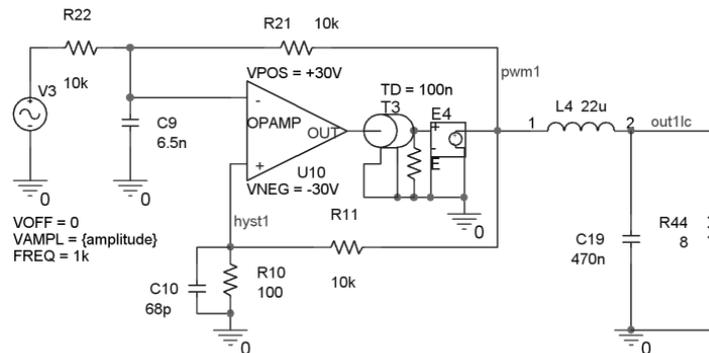


Figure 7.2: Simple self-oscillating amplifier with a constant amplitude hysteretic window.

The circuit consists of a power-comparator U_{10} with $100ns$ delay, a constant hysteretic window R_{10} , R_{11} , C_{10} and an integrator approximation R_{21} , R_{22} , C_9 . For demodulation a lowpass LC-filter is included which is not included in the loop.

With the ABM (Analog Behavioral Modelling) library in PSpice, the hysteretic window can be changed to vary as in (7.3) proportional to the reference voltage, see Figure 7.3.

This circuit serves as a reference of what can ideally be achieved with proportional regulation in terms of SF versus modulation and THD.

The discrete implementation of the circuit can be seen in Figure 7.4. The hysteretic window is changed in proportion to the lowpass filtered PWM signal, instead of the input voltage. This is done because a practical amplifier won't have an input voltage with an amplitude that extends to the rails of the power supply.

The circuit consists of two current followers Q_1 and Q_2 which look into R_{32} and create the hysteretic voltage across this resistor. The current through the two transistors is decreased when the modulation increases and follows the relation in (7.3). By alternating turning Q_1 or Q_2 on, by using the PWM signal from the power comparator (through R_{29} and R_{30}), the voltage across R_{32} switches between the upper and the lower hysteretic voltage limit. R_{33} is included to avoid the windows from decreasing down to zero. Therefore the implementation does not drop below idle

7.2. DISCRETE IMPLEMENTATION OF VARIABLE HYSTERETIC WINDOW

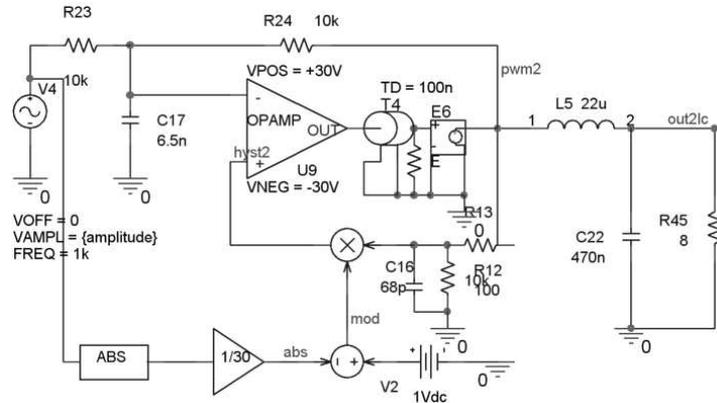


Figure 7.3: Simple self-oscillating amplifier with an ideal model of a hysteretic window witch is varied proportional to the input voltage.

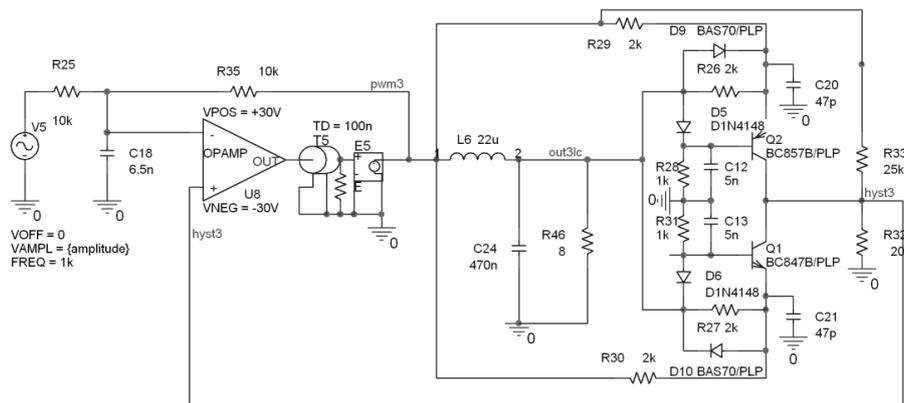


Figure 7.4: Simple self-oscillating amplifier with a discrete implementation of a hysteretic window witch is varied proportional to the lowpass-filtered output voltage.

7.2. DISCRETE IMPLEMENTATION OG VARIABLE HYSTERETIC WINDOW

frequency when the modulation rises above 95% modulation.

7.3 Time domain analysis of discrete implementation

A time domain simulation with FFT analysis of the three amplifiers Figure 7.2, Figure 7.3 and Figure 7.4 can be seen in Figure 7.5.

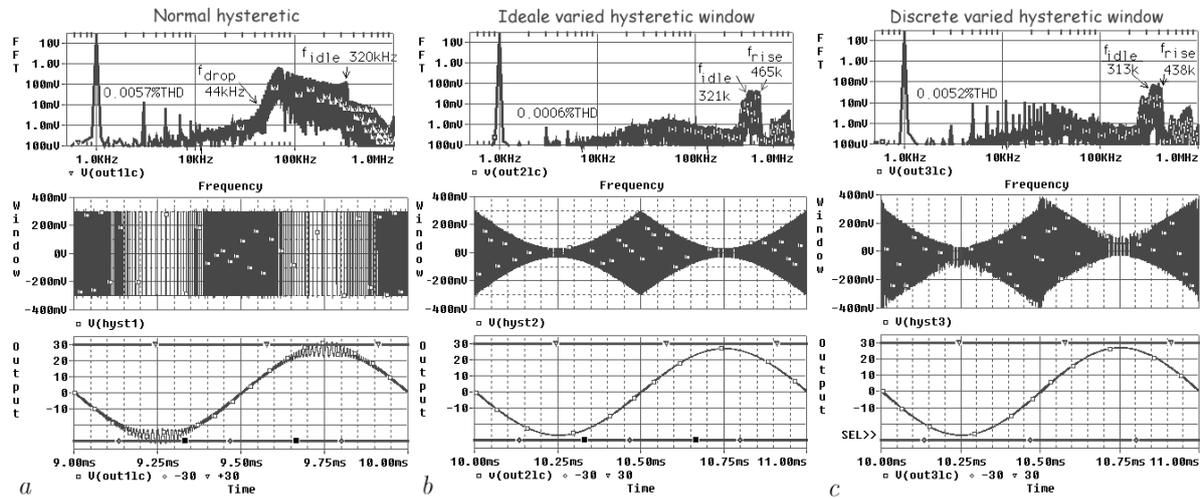


Figure 7.5: Time domain analysis of the three schematics in Figure 7.2, Figure 7.3 and Figure 7.4 with a modulation index of $M = 90\%$.

The modulation is $M = 90\%$ in all three cases. The constant window amplifier (Figure 7.5a) clearly shows a drop in SF and the ripple voltage on the output is large when the signal approaches the rails. The distortion harmonics due to the drop in loop gain are visible and THD² is 0.0057%. This low distortion is achieved because the loop gain is spend on THD suppression rather than amplification of the reference to the output. An amplifier with 20dB gain would show an THD which is 10 times larger.

The simulation results of the ideale varied hysteric window can be seen in Figure 7.5b. The SF does not drop below idle which results in a large improvement in ripple voltage and THD (0.0006%). By comparing this to Figure 7.5c, it shows that the discrete circuit performance as well as the ideal version in terms of SF and ripple. The circuit does however show an increased THD (0.0052%) compared to the ideal version (0.0006%) and about the same THD as the normal version. The increased THD is mainly caused by parasitic capacities in the discrete components that distorts the hysteric window at HF. By choosing BJT's with lower parasitic capacities and reducing the size of the resistors does improve the performance.

As it is proven in the previous chapters, the loop gain can be increased with more than 40dB with one opamp. The THD of the discrete solution is therefore not a problem in a complete design.

²10 harmonics are included in the THD analysis.

7.4 Constant switching frequency in phase-oscillating amplifiers

There are no previous recordings in literature of achieving a constant SF with phase oscillating amplifiers. Throughout work of this project, several attempts have been towards achieving a constant SF with phase-oscillators and some preliminary observations have been made. Consider the amplifier configuration in Figure 7.7a. It differs from normal phase-oscillating amplifiers with the fact that it has complex poles in the loop approximately at the SF. Complex poles exhibit an oscillatory step response (see Figure 2.2) and therefore works as a clock generator within the loop. The complex poles can be identified in the transfer-characteristic in Figure 7.7b at around $300kHz$, with a steep phase change at the -180° cross point. The relative loop gain is only $10dB$ so it cannot be expected that the amplifier will work well in terms of THD.

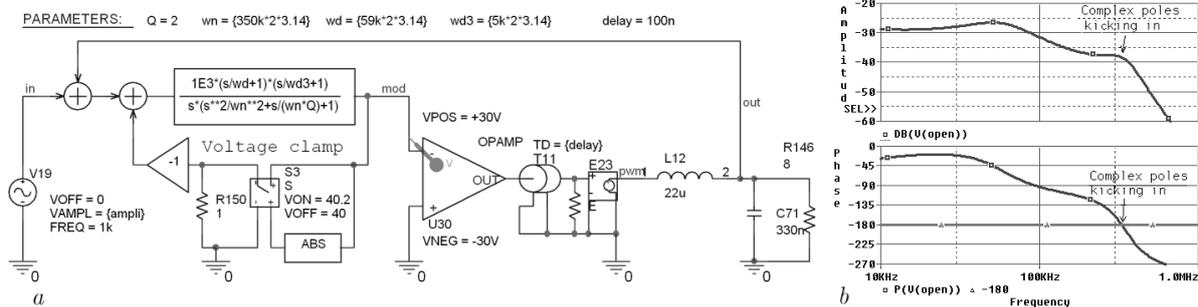


Figure 7.6: Simple phase-oscillating amplifier with constant SF.

The time domain simulation of the amplifier can be seen in Figure 7.7 with respectively a modulation of 27%, 53% and 80%. From looking at the three FFT spectra, it can be identified that the SF stays very constant at $\approx 215kHz$. At $M = 80\%$ however the amplifier starts to oscillate in a second mode, which can be seen as two separated spectral tops close to each other in the FFT window. In a normal self-oscillating amplifier the drop in frequency appears as a continuous band in the FFT window. This complex-pole topology appears to oscillate in modes rather than in a continuous frequency band.

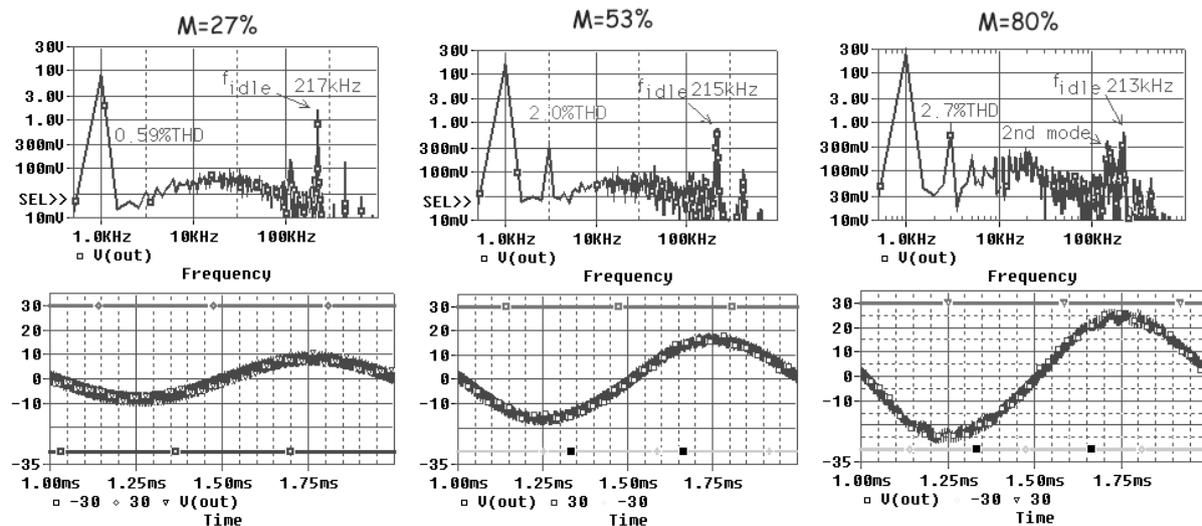


Figure 7.7: Simple phase-oscillating amplifier with constant SF.

The distortion of the amplifier is very large, but this can be explained by its low loop-gain.

7.4. CONSTANT SWITCHING FREQUENCY IN PHASE-OSCILLATING AMPLIFIERS

Adding more loop gain would be necessary for audio applications, but precautions should be made. Complex-pole oscillation is not a very attractive mode of oscillation and is an evident candidate for further research.

Chapter 8

Supply decoupling

The non ideal behavior of physical components is the main concern when it comes to the practical implementation of a circuit. From a small signal point of view, capacitors are linear and without any parasitic components. In reality a series inductance ESL and a frequency dependent series resistance ESR is present. For some dielectrics, the capacitance is also a strong function of the terminal voltage and ambient temperature. When low distortion is desired in audio processing a C0G/NP0 ceramic or a film capacitor is chosen. For supply decoupling however, the main concern is parasitic components rather than linearity. Electrolytic capacitors has a very high capacitance to volume ratio, but lacks in ESR and ripple current rating. Often a large amount of electrolytics are needed to handle a given ripple current. A relatively new type of solid electrolytic capacitors are becoming available at various suppliers and does have improved specifications. The voltage rating is however below $25V$ and the price is high. Ceramic capacitors in the μF range is not always preferred choice in switch-mode applications, but it is the optimal choice in terms of price, signal integrity and space utilization as it will be shown in the following. With local supply decoupling, some precautions has to be made to avoid ringing on the power lines. The problem will be analyzed in the following.

8.1 Ringing on power lines

The impedance of the non ideal capacitor with ESR and ESL is given in equation (8.1). It has one pole in origo and two high-frequency zeros:

$$\begin{aligned} Z &= X_L + X_C + R \\ &= sL + \frac{1}{sC} + R \\ &= \frac{1}{sC} (s^2LC + sCr + 1) \end{aligned} \tag{8.1}$$

An ideal capacitor would only have one pole in origo. The ESL is responsible for the complex zero pair and the ESR affects the quality factor.

Because of the high series inductance and resistance of electrolytic capacitors, it's often desired to place one or several ceramic capacitors in parallel. Such a configuration can be seen in Figure (8.1). Typical values for ESR and ESL is included in the figure. The ceramic capacitor provides local decoupling and the electrolytic capacitor is placed some distance away in the power-supply. Lw is the parasitic inductance in the PCB wires between the two components and is approximately $0.5nH/mm$ on a $2.4mm$ FR4 board (see chapter 9).

The voltage response for a given sinusoidal load current of the two components respectively separately and parallel is given in Figure 8.2a and 8.2b. The parallel configuration exploits the best of the two capacitors and has a constantly low impedance up to a few Mhz . There

8.1. RINGING ON POWER LINES

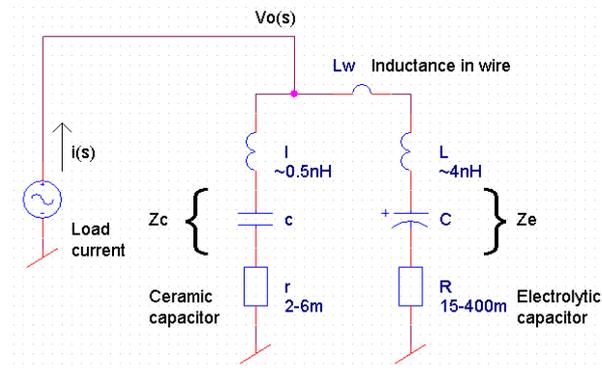


Figure 8.1: A ceramic and electrolytic capacitor in parallel.

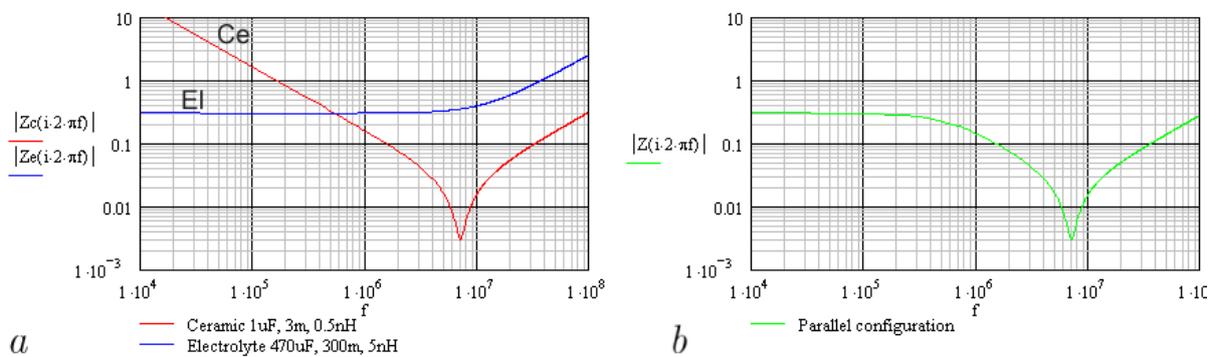


Figure 8.2: Typical single and parallel impedance of a ceramic and a electrolytic capacitor.

can however arise problems if the distance between the to components is large (large parasitic inductance) or the ESR of the electrolytic is lower. In Figure 8.3 the ESR of the electrolytic is reduced from $300m\Omega$ to $30m\Omega$. The $30m\Omega$ of ESR is not unforseen in an amplifier with a large ripple current and a parallel configuration of electrolytics. The parallel current response

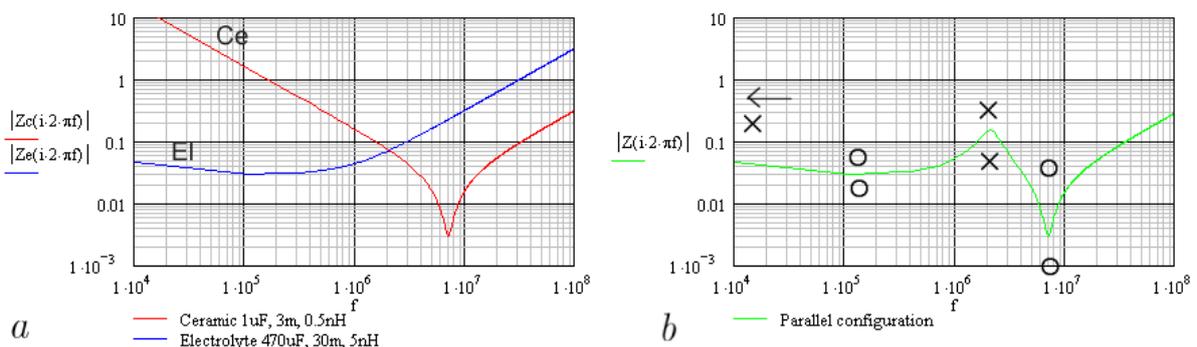


Figure 8.3: Low ESR parallel configuration and it's poles and zeros.

in Figure 8.3b has a visible pair of complex poles in the area where the impedance of the two components cross each other. It's this pair of poles that cause ringing in a supply with local decoupling. A common approach is to add a zobel network¹ on the supply to damp the ringing, but this is not the optimal solution. By designing a ladder of capacitors in parallel with the

¹A capacitor in series with a resistor.

right ratios and distances, ringing can be avoided.

8.2 Proper design of local supply decoupling

The combined impedance of the two capacitors in Figure 8.1 is the following:

$$\frac{V(s)}{i(s)} = Zc \parallel Ze = \frac{1}{s(c+C)} \cdot \frac{(s^2cl+scr+1)(s^2C(L+L_w)+sCR+1)}{s^2c \parallel C(l+L+L_w)+sc \parallel C(r+R)+1} \quad \text{where} \quad c \parallel C = \frac{cC}{c+C} \quad (8.2)$$

The complex pole pair is identified in the denominator and it's dependent on all the values in the circuit. The important thing is that the quality factor of the poles does not rise above 0.7 – 0.8 since this would result in a oscillatory characteristic (see Figure 2.2). The quality factor of the poles is:

$$Q_p = \sqrt{\frac{l+L+L_w}{c \parallel C} \frac{1}{r+R}} \quad (8.3)$$

It can be seen that to avoid ringing, high ESR, low ESL, large capacitors and short distances are needed. This is just opposite properties than we want from a space and economically point of view. Although the physics of nature is against it, it is possible to finde good solutions to the problem.

To reduce the design problem the assumptions (8.4) can be made.

$$c \ll C \quad l \ll L + L_w \quad r \ll R \Rightarrow l + L + L_w \approx L + L_w \quad c \parallel C \approx c \quad (8.4)$$

$$Q_p = \sqrt{\frac{L+L_w}{c} \frac{1}{R}} \quad (8.5)$$

The quality factor (8.5) is now only dependent on the ESR of the electrolytic, the capacitance of the ceramic and the parasitic inductance of the trace/electrolytic. With $Q = 0.8$, $10nH$ of inductance and $30m\Omega$ resistance a ceramic capacitor of $17\mu F$ is needed for local supply decoupling. This is a much larger value than would normally be chosen but recently quite a few manufacturer makes ceramics this large and at a low price. The advantage of this choice is that only one ceramic is needed in a switching power-stage where the ripple current is around $10A_{rms}$. The common solution would be to choose a large number of electrolytics as local supply decoupling. With a power supply that has a ESR larger than $30m\Omega$, common ceramics in the range from $1\mu F$ to $10\mu F$ can be chosen. A switching frequencies above $200kHz$ ceramics in this range proves sufficient to reduce the voltage ripple on the rails.

The conclusion is that large ceramics is the optimal choice for supply-decoupling of a switching power stage both in terms of signal integrity, prince and space.

8.3 Manufactures of large ceramics

A short list of manufactures that produces large ceramics with a voltage rating suited for split-supply switching amplifiers i given in the following:

TDK produces the the MegaCAP at $22\mu F$ with a $50V$ rating and X7R dielectric on a $6.5x5.5mm$ footprint. Murata produces several $10\mu f$ ceramics with a $50V$ rating and a X7R dielectric on a $5.7x5.0mm$ footprint. Other manufactures are: Kement with $2.7\mu F$ at $50V$ (F3102Z5U) , Nippon Chemi-Con with $47\mu F$ at $50V$ (ce-thptmp-e-060127 and ce-ntp-e-060127) and Skywell with $10\mu F$ at $50V$.

A ceramic with at $10\mu F$ with a $50V$ rating can be acquired from around 0.38\$ in large quantities².

²www.mouser.com part number 81-GRM32DF51H106ZA01

Chapter 9

Parasitic components in PCB traces

In the previous chapter 8 it was proven that the inductance in PCB traces is a contributor to bad signal integrity on the power-rail in switching amplifiers. If the inductance in the PCB traces can be minimized, it will allow the use of smaller ceramic capacitors for local supply decoupling. A way of calculating parasitic components on a PCB will be presented in the following.

9.1 PCB traces

Every PCB trace has a parasitic inductance, a parasitic capacitance and frequency dependent resistance, which can have a strong influence on signal integrity. These parasitic effects has an influence at high frequencies and therefore the PCB should be treated as being a RF circuit. For long traces, the incremental parasitic components will cause the signal to oscillate along the wire. In this case transmission line theory applies rather than small signal theory. The maximum permissible bandwidth where small signal theory still applies is given in (9.1).

$$BW = \frac{c}{10L\sqrt{\epsilon_{eff}}} \quad (9.1)$$

L is the length of the trace, ϵ_{eff} is the effective permittivity and c is the speed of light. This bandwidth is around $160MHz$ for $L = 10cm$ of on a standart FR4 PCB ($\epsilon_{eff} \approx 3.3$). This implies that the parasitic components can be treated as small signal discrete components in switching amplifiers.

9.2 Microstrip traces

The traces on a standart two side PCB forms a microstrip transmission line. A cross section of a microstrip is shown figure 9.1.

Since the electrical field E and the magnetic fluc B partly exists in air and in the intervening dielectricum it's not a straight forward process to analyse a microstrip line. However there exist several curve fit approximations based on actual obtained results. The work done by *I. J. Bahl* and *D. K. Trivedi*¹ introduces an effective permittivity (9.2) and a corrected characteristic

¹I. J. Bahl and D. K. Trivedi, "A Designer's Guide to Microstrip Line", Microwaves, May 1977, pp. 174-182.

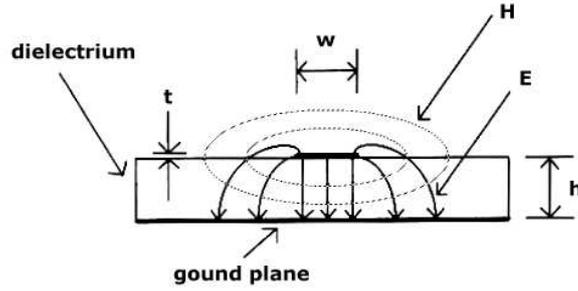


Figure 9.1: *Conductive strip placed over an infinite ground plane, separated by a dielectric.*

impedance (9.3) with very high accuracy.

$$\epsilon_{eff} = \begin{cases} \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2} \left[\frac{1}{\sqrt{1+12\frac{h}{w}}} + 0.04(1 - \frac{w}{h})^2 \right] & \text{for } \frac{w}{h} < 1 \\ \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2} \frac{1}{\sqrt{1+12\frac{h}{w}}} & \text{for } \frac{w}{h} \geq 1 \end{cases} \quad (9.2)$$

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_{eff}}} \ln \left(8 \frac{h}{w} + 0.25 \frac{w}{h} \right) & \text{for } \frac{w}{h} < 1 \\ \frac{120\pi}{\sqrt{\epsilon_{eff} \left[\frac{w}{h} + 1.393 + \frac{2}{3} \ln \left(\frac{w}{h} + 1.444 \right) \right]}} & \text{for } \frac{w}{h} \geq 1 \end{cases} \quad (9.3)$$

The characteristic impedance and the effective permittivity is related to the incremental inductance and incremental capacitance as in equation (9.4):

$$Z_0 = \sqrt{\frac{L}{C}} \quad (9.4)$$

With knowledge of the speed of propagation, two equations exists (9.4), (9.5) with two unknowns, leading to a solution for L and C :

$$v = \frac{1}{\sqrt{LC}} \quad (9.5)$$

In free space the speed of propagation is $c = 3E8m/s$. In a dielectricum with a given permittivity things slow down:

$$v = \frac{c}{\sqrt{\epsilon_{eff}}} \quad (9.6)$$

The solution to the incremental size of L and C becomes:

$$L = \frac{Z_{0eff} \sqrt{\epsilon_{eff}}}{c} \quad (9.7)$$

$$C = \frac{\sqrt{\epsilon_{eff}}}{Z_0 c} \quad (9.8)$$

Where Z_{0eff} is given in (9.3) and ϵ_{eff} is given in (9.2).

9.3 Traces on a standart FR4 PCB

The most common material for a PCB is FR4 glasfibre coated with one layer of copper on each side. The permittivity is usually $4.7F/m$ and a standart board hight is $1.6mm$. These two specs is enough to determine the incremental components of a PCB trace as function of width. This is shown in figure (9.2). The MATLAB script for generating this figure can be found in appendix B. The most interesting thing to notice from figure (9.2) is the incremental inductance as func-

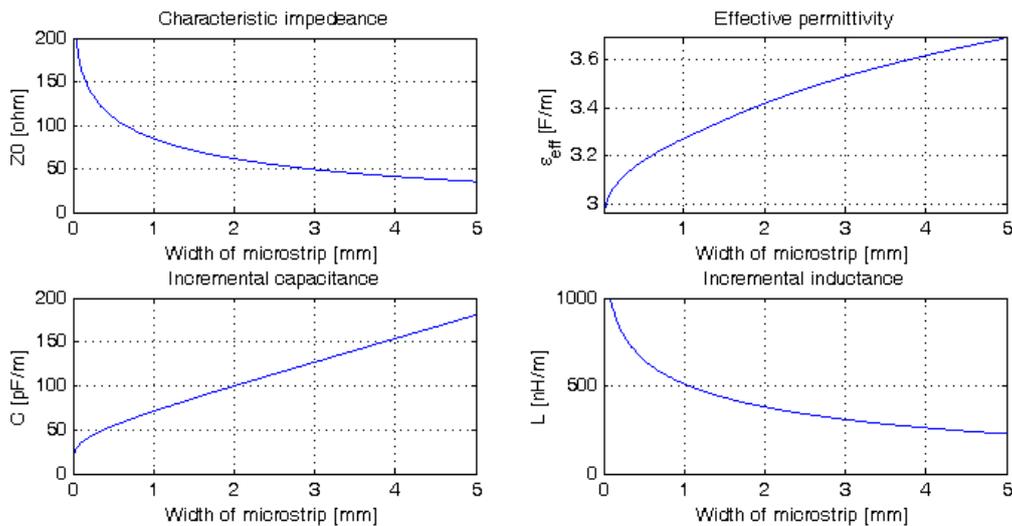


Figure 9.2: *Characteristic impedance, effective permittivity, incremental inductance and incremental capacitance of a microstrip transmission line as function of width. Data is based on FR4 board with $\epsilon = 4.7F/m$ and hight 1.6mm.*

tion of width, which is a very important parameter for traces carrying high currents with fast transients. The effect of a high trace inductance is seen as ringing consecutive with a transient flank, due to capacities in both end of the line resonating with the inductance. This ringing effect is covered in the previous chapter 8.

9.4 Incremental inductance in traces

The incremental inductance for some common trace widths is listed in tabel 9.1. It's seen that the incremental inductance is reduced considerable in wide traces. A 5.0mm trace therefore has less that a third of the incremental inductance of a small signal 0.3mm wire. Both trace resistance and signal integrity speaks in favor of wide traces. The hight of a PCB is also a

Width	[mm]	0.30	0.50	1.0	1.5	3.0	5.0
L	[nH/m]	750	649	512	434	308	227

Table 9.1: *Incremental inductance of a copper trace on a 1.6mm FR4 PCB as function of width.*

very important parameter when trying to reduce the incremental inductance. Table 9.2 lists the values for a 0.30mm and a 5.0mm trace as function of five industrial PCB heights. Halving the hight from 1.6mm to 0.78mm nearly halves the incremental inductance. It's seen that everything speaks in favor of a thin PCB as long as the reduced mechanical strength dosen't become a problem. Thermal properties are also imported in thin PCB because of the better coupling between copper on the two sides.

Hight	[mm]	0.78	1.2	1.6	2.4	3.2
L for $w = 0.30mm$	[nH/m]	608	694	750	832	889
L for $w = 5.0mm$	[nH/m]	137	187	227	291	340

Table 9.2: *Incremental inductance of a copper trace on a FR4 PCB as function of board hight.*

9.5 Microstrip summary

PCB traces carrying large currents with fast transients can suffer from bad signal integrity, due to parasitic inductance in the trace resonating with capacities in the ends. A LC-circuit forms a second order filter with ripples considerably if the Q value becomes above 0.7. Based on microstrip theory it's shown that thin PCBs with wide traces suffer the least parasitic components. Traces in gate drive circuits, supply rails, high current nodes and power outputs should therefore be designed with this knowledge to avoid high Q values.

Chapter 10

The power comparator

A general building block in self-oscillating amplifiers is the power-comparator. It consists of a small-signal comparator, level shifting, gate drivers and a MOSFET power stage. Optional features such a short-circuit protection is preferred.

Integrated comparators and gate drivers are expensive and only run on low voltages. This requires a low voltage split supply for the comparator and a single supply for the gate drivers. By building a discrete power comparator expenses can be cut and no low voltage supplies are needed. Level shifting can also be made as an integrated part of the comparator.

In the following a discrete power-comparator is presented. It has a low propagating delay and implements all the features described above.

10.1 The discrete power-comparator

In figure 10.1 a discrete power-comparator realization can be seen.

The input signal is feed to a bipolar differential stage and buffered by common emitter folded cascade current mirror. Since the signal is transferred as a current, the miller capacities in the input stage does not affect the speed.

In the bottom of the split-supply the differential current is converted to a single-ended voltage. RF transistors are used to improve speed.

The subsequent circuit blocks is the gate driver and the power stage. The high-side driver uses differential signaling and is therefore very fast in turning both on and off. Deadtime is provided by using different turn-on and turn-off resistors on the MOSFET gates.

As a safety feature, the current through the two MOEFETs is monitored by a short-circuit protection circuit. If the current rises above $40A$ the power-comparator shuts down for $5ms$.

The split power-supply is decoupled by two $22\mu F$ 50V ceramic capacitors, which according to chapter 8 is enough.

The MOSFET voltage rating is 100V so the whole circuit can be operated safely at a $+/- 40v$ supply. This is enough to deliver $200W$ in a 4Ω load.

10.2 Measurements

The whole circuit has been build and the print layout can be seen in Appendix D. By applying a square wave signal of $50mV$ to the input terminals, the propagation delay of the whole power-comparator has been measured. The delay for a rising output flank is $94ns$ and for a falling flank it's $46ns$. This is much better specifications than many IC circuits has. The discrete power-comparator is therefor both cheap and high performing solution.

10.2. M

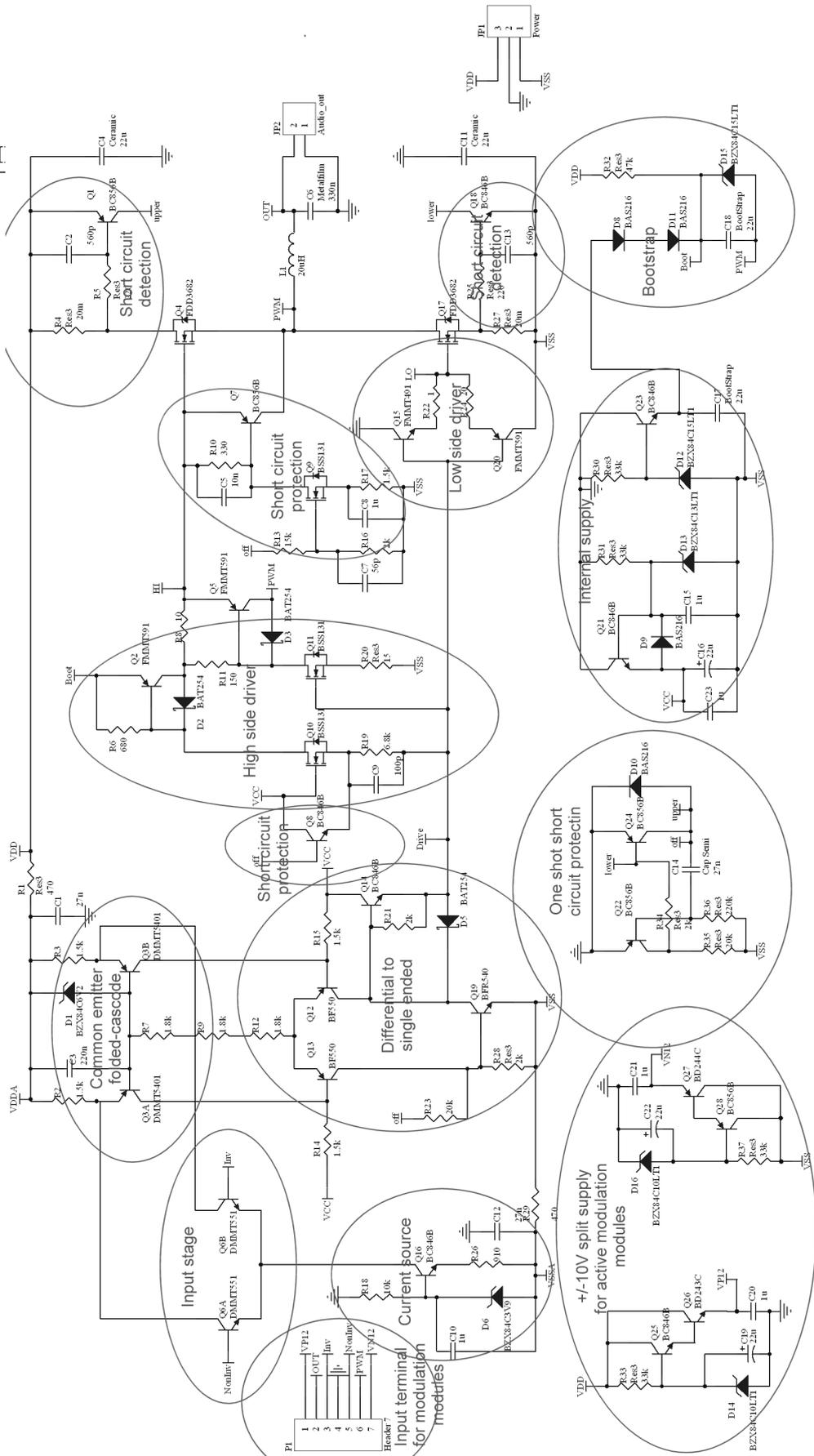


Figure 10.1: Discrete power-comparator with short-circuit protection.

Chapter 11

Conclusion

A passive-loop hysteretic and phase-oscillating amplifier with 0.05% of THD has been presented. By adding active poles to the modulator loop the distortion of any self-oscillating amplifier can be improved. An active opamp circuit that has two poles and zeros is used for this purpose and the design equations are derived.

To reduce the output impedance of an amplifier and suppressing distortion caused by magnetic saturation, the post LC filter should be included in the modulator loop. A new feed-forward approach that does this is presented and demonstrated to perform an error suppression of 101dB. The resulting THD is too low to be measured.

A common problem with self-oscillating amplifiers is that the switching frequency drops when the modulation is increases. To solve this problem, both a hysteretic and a phase oscillating amplifier with a constant switching frequency is presented.

When it comes to implementing power electronics on a PCB, some precautions should be made to avoid ringing on the supply rails. A model of the power supply has been introduced and ceramic capacitors in the range of $1\mu F$ to $10\mu F$ has been shown to be the best choice for local supply decoupling.

The power-comparator is the main component in a switching amplifier. It requires several internal supply voltages and uses expensive integrated circuits. A cheap discrete power comparator has been designed and the propagation below 100ns outperforms most integrated solutions.

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Appendix A

Leapfrog

Appendix B

transmission_line.m

MATLAB script for calculating the characteristic impedance, effective permittivity, incremental inductance and incremental capacitance of a microstrip transmission line as function of width. The output graph can be found on page 38 in figure 9.2.

```
1 % Calculations based on:
2 % I. J. Bahl and D. K. Trivedi, "A Designer's Guide to Microstrip Line",
3 % Microwaves, May 1977, pp. 174-182.
4 %
5 % The equations can be found on the following site:
6 % http://www.microwaves101.com/encyclopedia/microstrip.cfm
7 %
8 % The following page has a calculator that takes
9 % loss into account: http://mcalc.sourceforge.net/
10
11 clear Z0_v W;
12
13 H=1.6;
14 e_r=4.7; %FR4 is typically 4.7 but varies between 4.0 and 5.0
15
16 W=0.01:0.01:5;
17 for i=1:length(W)
18     if (W(i)/H)<1
19         e_eff=(e_r+1)/2+(e_r-1)/2*((1+12*H/W(i))^-0.5)+0.04*(1-W(i)/H)^2);
20         Z0=60*e_eff^(-0.5)*log(8*H/W(i)+0.25*W(i)/H);
21     else
22         e_eff=(e_r+1)/2+(e_r-1)/2*(1+12*H/W(i))^-0.5);
23         Z0=120*pi/(e_eff^0.5*(W(i)/H+1.393+2/3*log(W(i)/H+1.444)));
24     end
25     Z0_v(i)=Z0;
26     e_eff_v(i)=e_eff;
27 end
28
29 %Impedance
30 subplot(2,2,1);
31 plot(W,Z0_v); grid on;
32 xlabel('Width of microstrip [mm]'); ylabel('Z0 [ohm]');
33 title('Characteristic impedance');
34 axis([0 5 0 200])
35
36 %Relative permittivity
37 subplot(2,2,2);
38 plot(W,e_eff_v); grid on;
39 xlabel('Width of microstrip [mm]'); ylabel('\epsilon_{eff} [F/m]');
40 title('Effective permittivity');
41 axis tight;
```

```
42
43 %Capacitance per length
44 C=sqrt(e_eff_v)./(3*10^8*Z0_v);
45 subplot(2,2,3);
46 plot(W,C*1E12); grid on;
47 xlabel('Width of microstrip [mm]'); ylabel('C [pF/m]');
48 title('Incremental capacitance');
49
50 %Inductance per length
51 L=sqrt(e_eff_v).*Z0_v./(3*10^8);
52 subplot(2,2,4);
53 plot(W,L*1E9); grid on;
54 xlabel('Width of microstrip [mm]'); ylabel('L [nH/m]');
55 title('Incremental inductance'); axis([0 5 0 1000])
```

Appendix C

passives_thd.m

MATLAB script for plotting PSpice simulated THD+N for passive realisations of respectively a hysteric and phase oscillating amplifier.

```
1
2 A      = 27.1* [0.01  0.0158  0.0251  0.0398  0.0631  0.1    0.1585
3 thd_h  =      [0.251  0.398  0.631  1      1.58  2.51];
4 thd_p  =      [1.3    0.620  0.567  0.362  0.2909  0.0657  0.0487
5 thd_p2b =      [0.0248  0.0712  0.0915  0.6732  1.49  2.73];
6
7 thd_p  =      [0.3677  0.2829  0.18629  0.3528  0.03345  0.03471  0.07730
8 thd_p2b =      [0.07286  0.0372  0.02118  0.13313  0.14272  2.686];
9 thd_p2b =      1E-3*[9.043  5.120  4.193  2.398  2.068  1.794  1.799
10 thd_p2b =      [1.829  1.641  1.838  37.88  1495  2744];
11
12 loglog(A,thd_h,'-',A,thd_p,'--',A,thd_p2b,'-.','LineWidth',3); grid on
13 axis([min(A) 30 0.001 1]);
14 ylabel('THD+N [%]'); xlabel('Output ampltude [V]');
15 legend('Hysteric','Phase osc.','Improved phase osc.');
```

Appendix D

Discrete power comparator print layout

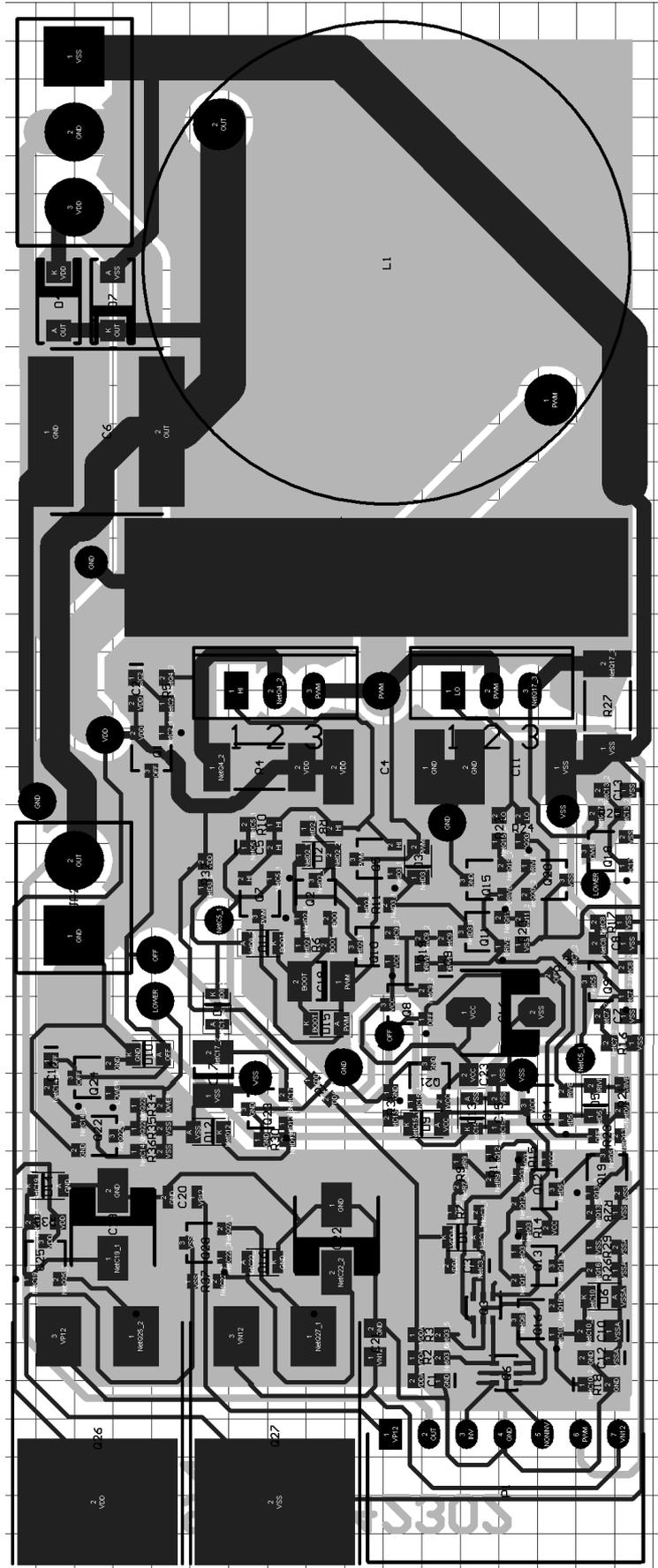


Figure D.1: Discrete power-comparator print layout.