SM1150 LDMOS TRANSISTOR

Document Number: SM1150
Rev. Preliminary Datasheet

1000MHz-1100MHz, 500W, 50V High Power RF LDMOS FETs

SM1150

SM1150E

- Typical Performance (In Demo Fixture): P_{-1dB}= 520 Watts @ 1100 MHz, V_{DD} = 50 Volts, I_{DQ} = 100 mA, pulse width =10 us, Duty cycle =1%.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)	P_{-3dB} (W)	η_D@P_{-3} (%)
1100 MHz	16.8	520	57	560	60

- Capable of Handling 10:1 VSWR, @ 50Vdc, 1100 MHz, 520 Watts pulsed output Power Designed for Enhanced Ruggedness.
- Typical P_{out} = 560 Watts @ 3 dB Compression Point, pulsed @ 1100 MHz

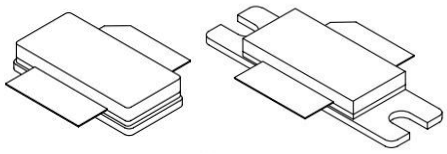


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+52	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 520 W pulsed, V_{DD}=50 Vdc, I_{DQ} = 100 mA	$R_{\theta JC}$		°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 85V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 300 μA)	$V_{GS(th)}$	——	1.8	——	V
Gate Quiescent Voltage	$V_{GS(Q)}$	——	2.75	——	V

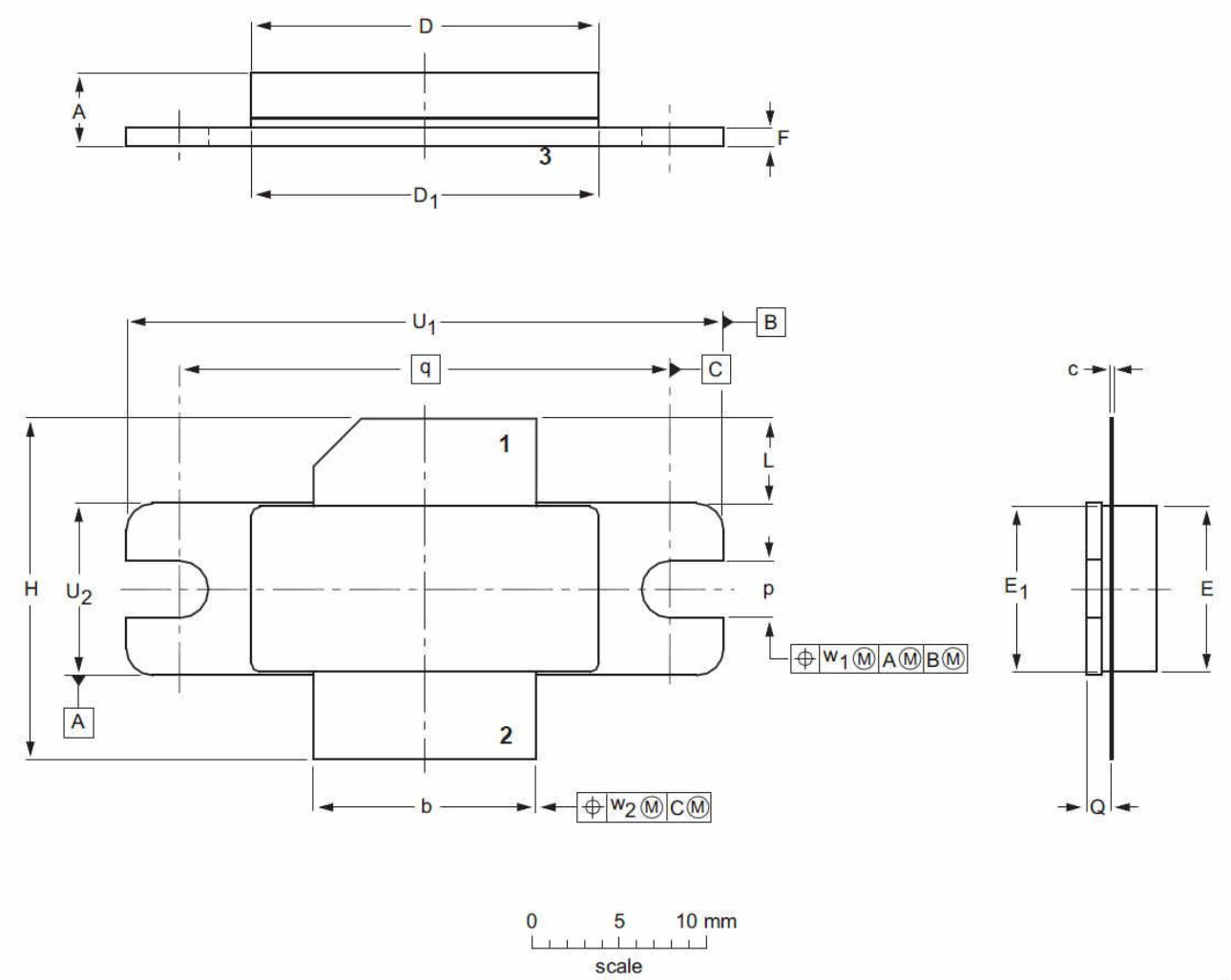
(V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)					

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 1100 MHz, pulsed signal Measurements.

Power Gain	G_p	———	16.8	———	dB
Drain Efficiency@P3dB	η_D	———	60	———	%
1 dB Compression Point	P_{-1dB}	———	520	———	W
3dB Compression Point	P_{-3dB}	———	560	———	W
Input Return Loss	IRL	———	-10	———	dB

Package Outline

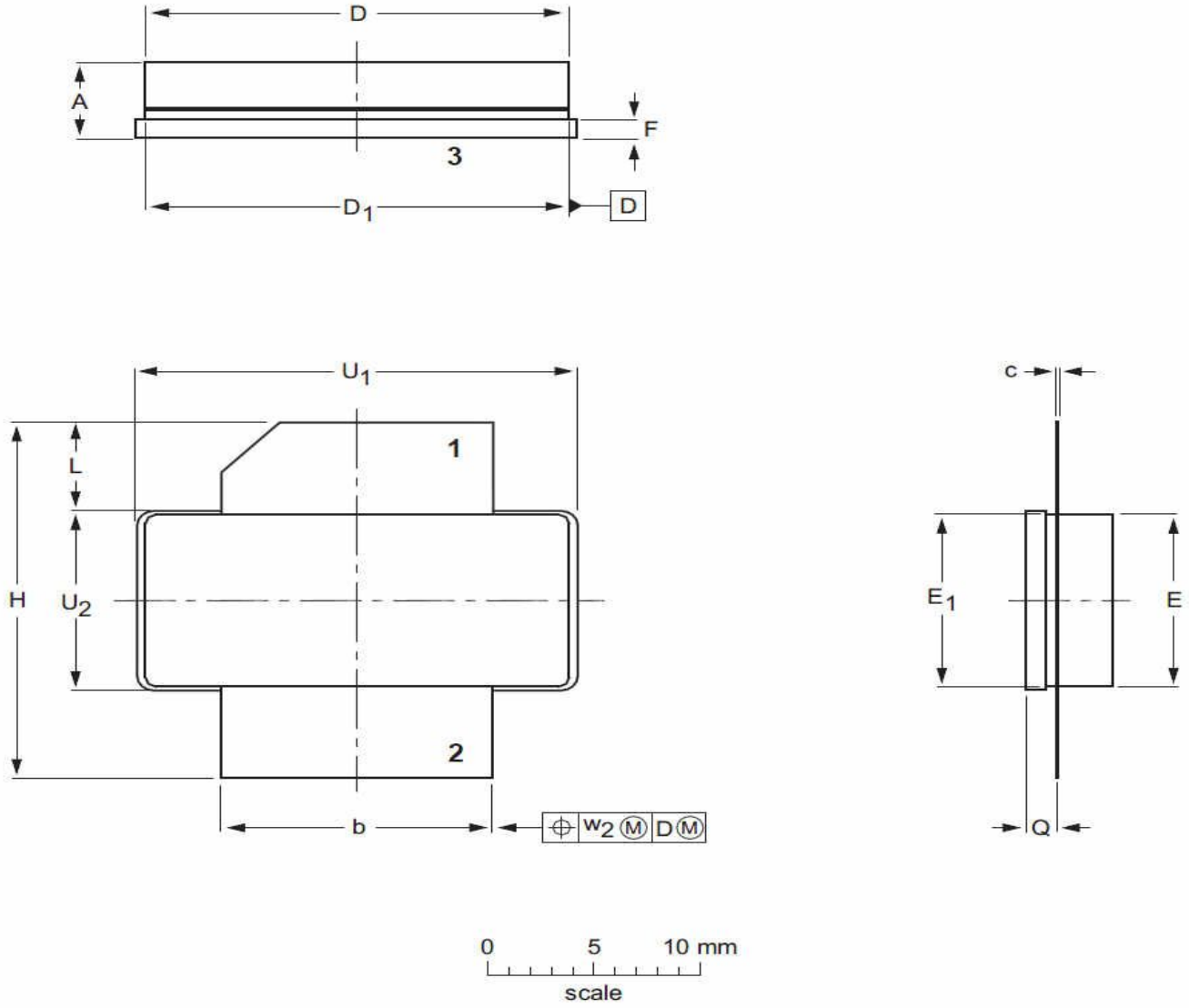
Flanged ceramic package; 2 mounting holes; 2 leads



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Earless flanged ceramic package; 2 leads



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OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013