A 126DB D-RANGE CURRENT-MODE ADVANCED SEGMENTED DAC

NORIO TERADA & SHIGE NAKAO

Texas Instruments Japan*, Kanagawa, Japan

A new current-mode multi-bit DAC has been designed to meet the needs of high-end audio with dynamic-range of 126dB and THD+N of 0.00025%. This performance is accomplished in monaural mode, which is constructed with 2-channel DAC of plus and minus signal input and an external instrumentation amplifier configuration at the output. Each channel has dynamic-range of 123dB and THD+N for full-scale signal of 0.00025%. In this paper, the design concept of the chip, especially for analog design, is discussed.

INTRODUCTION

D/A converter IC's with a continuous-time output stage using current mode have been attractive for the high-end audio market. High SNR can be achieved at the output of external I-V conversion OPA, because of the nature of system configuration. In high-end audio systems, low-noise OPAs with relatively higher power supply, $V_{CC}OPA$, are used. In this way, the DAC can supply low-noise current signal into the OPA regardless of the DAC power supply, $V_{CC}DAC$ as shown in Figure 1.

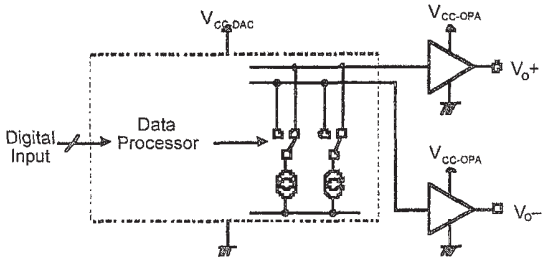


Figure 1. Schematic of Current-mode DAC Architecture

output voltage defined by the power supply voltage of the switched capacitor analog filters. Furthermore, switched-capacitor filters have R-C bandwidths in the hundreds of MHz range, and can suffer from clock noise in the system board, which generates unexpected tones and other interference.

An example architecture of such a current output DAC is the multi-bit sign-magnitude DAC with trim resistor [1]. The advantage of this type of DAC is less clock feed-through noise and flat noise floor over wide frequency bandwidth. The DAC consists of a trimmed R-2R ladder and weighed current segments. Chief disadvantage of this DAC is cost penalty due to area of trim resistor and trim time.

The analog performance presented in this paper has been achieved by combining the advantages of both current segment and sigma-delta DACs. This new architecture is called "Advanced Segment DAC Interpolated by Sigma-Delta". The architecture of the DAC is discussed in "OVERVIEW OF THE CONVERSION ARCHITECTURE" Section. Design issues for accomplishing high analog performance are discussed in "CURRENT SEGMENT DAC DESIGN" Section. The application circuit and the achieved analog performance are presented in "MEASURED RESULT" Section.

*Formerly Burr Brown Japan

OVERVIEW OF THE CONVERSION ARCHITECTURE

Fundamental concept of the presented DAC is a multi-level architecture generating the current output by driving the current source DAC with a corresponding digital signal code as shown in Figure 2. The advantage of the multi-level architecture is robustness to clock jitter.

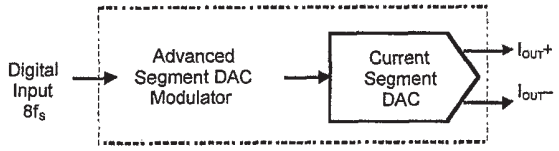


Figure 2. Fundamental Concept of Advanced Segmented DAC

Jitter Sensitivity

In case of multi-level architecture, analog output level error owing to jitter t_{jn} at n_{th} sampled signal is proportional to the difference between n_{th} signal level A_n and $(n-1)_{th}$ signal level A_{n-1}, as $[A_n - A_{n-1}]t_{jn}$. It should be noted that transition value of $|A_n - A_{n-1}| = A/(N-1)$ is dominant, here A is the full-scale output and N is the number of level. Accordingly, the output level error originated by jitter can be reduced with increase in level number. Fourier transform of the error gives the jitter noise spectrum as following equation [2];

$$E_{multi}(f) = f_S \sum_{n=1}^{N-1} [A_n - A_{n-1}]\, t_{jn}\, exp(-i2\pi n f / f_S) \quad .. (1)$$

Here, f_S is the sampling frequency.

From this equation, improvement of robustness for the multilevel DAC is roughly proportional to the number of level. Figure 3 shows the simulated dynamic range for 67-level DAC and 8-level DAC as a function of clock jitter. In most consumer audio systems, the random jitter component is less than 200ps. For high-end application, 100ps is generally realized. Therefore, 120dB plus dynamic range can be accomplished by a 67-level DAC.

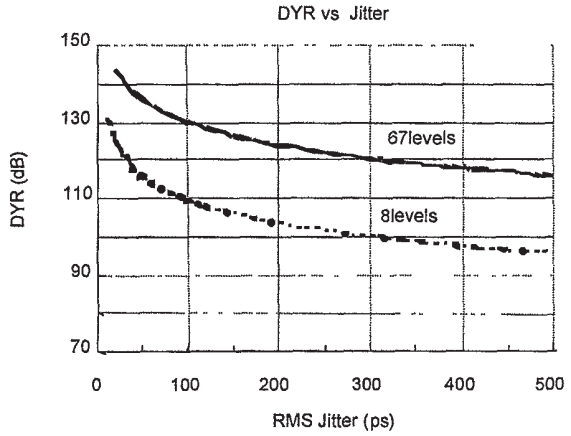


Figure 3. Simulated Dynamic Range as a function of RMS clock jitter

Advanced Segmented DAC architecture

Figure 4 shows the block diagram of advanced-segmented DAC [3]. The digital signal output from the conventional digital filter is divided into two bit-groups. The upper and lower bit-groups are processed in a segment code converter and a 5-Level ΣΔ modulator, respectively. These data streams are summed into a multi-bit data stream. Here, 1 Level of ΣΔ modulator is equivalent to 1LSB of the code converter. As the result, the summing function becomes simple. The data stream is applied to an advanced data-weighted averaging block in the digital domain. And then it goes to a current segment DAC output stage.

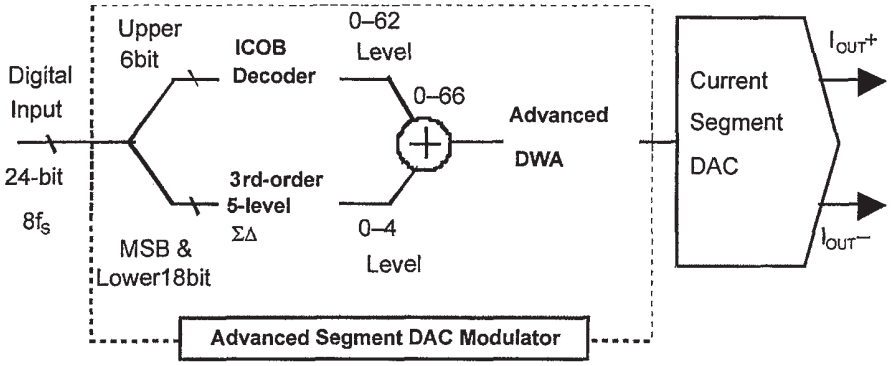


Figure 4. Audio DAC block diagram (Advanced Segment DAC interpolated by Sigma-delta)

Figure 5 shows the summing function of processed upper bit data and lower bit data in a simplified form. 1 Level of ΣΔ modulator is equivalent to 1LSB of Decoder. As the result, the summing function becomes very simple. Total output signal becomes similar to a 9 level multi-bit sigma-delta output in this example. In the actual chip presented here, it is 67 levels. However, this architecture is basically different from such conventional multi-bit sigma-delta modulators.

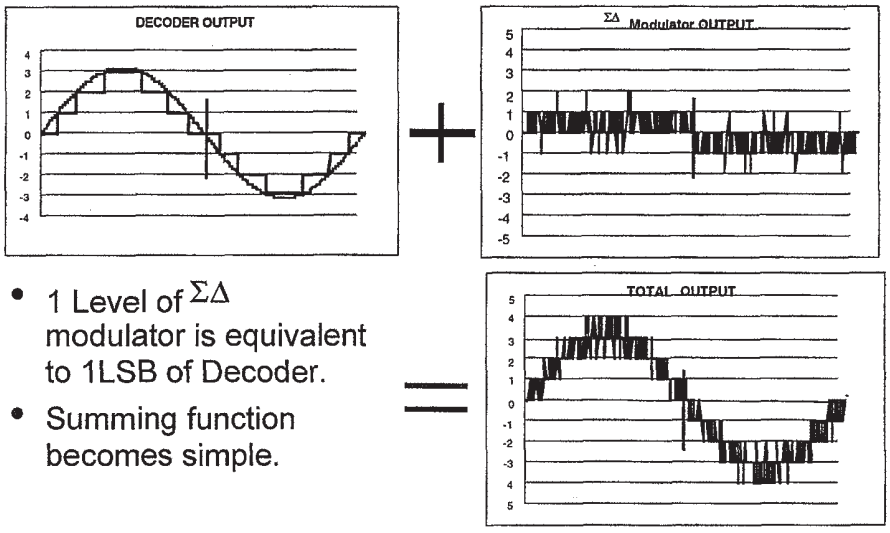


Figure 5. Summing function of upper and lower bit data in digital domain

CURRENT SEGMENT DAC DESIGN

A differential configuration of current switches provide plus and minus current for the differential outputs. This topology keeps the constant current flow in the chip and reduces the switching noise significantly.

Biasing of current source is designed to be stable by using a servo amplifier as shown in Figure 6. The full-scale current output should be determined by external I-V conversion stage design.

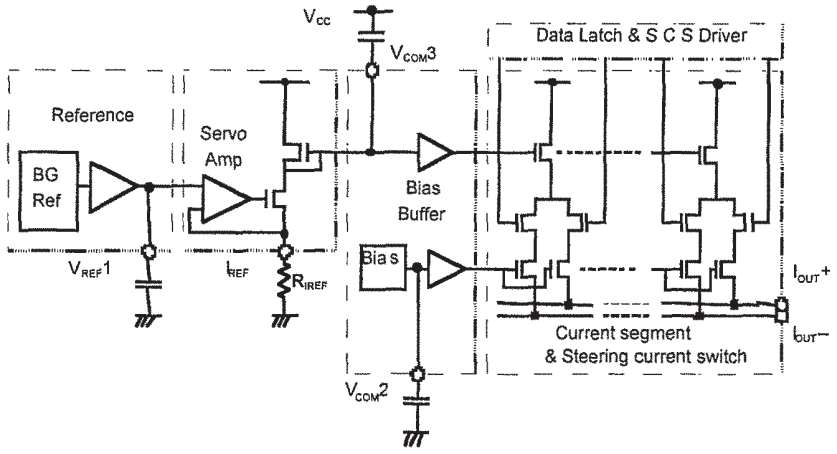


Figure 6. Schematic of the current segment and the biasing circuit

Figure 7 schematically shows equivalent circuit of current source and the external I-V transformer stage, which consists of the MOS transistor as a current source and output I-V conversion OPA with feedback resistor. The noise voltage in 20kHz band width is 1.0μVrms to 1.5μVrms for general OPA of audio application. Therefore, the OPA output voltage should be 1.5Vrms in order to accomplish 120dB dynamic range without A-weight. On the other hand, the noise voltage of current source (en) referred at MOS gate input noise is amplified by following equation;

$$V_{O\text{-}noise} = en\ R_F / (1/gm_0 + R_S) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

Here, gm_0 is transconductance of MOS transistor and R_S is source resistance.

Considering this noise factor associated with output voltage requirement, output current of full-scale of this DAC is defined 8mA for $I_{OUT}+$ and $I_{OUT}-$, respectively.

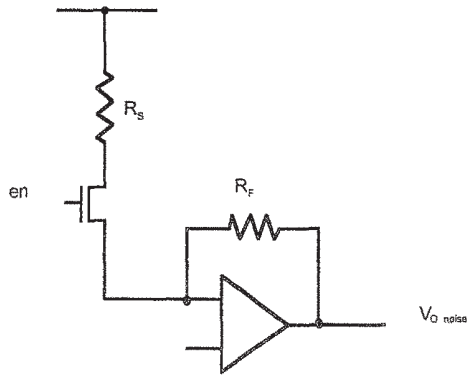


Figure 7. Schematic of equivalent circuit of current source and the external I-V converter stage

MEASURED RESULT

Figure 8 shows the application circuit of I-V conversion realizing a 3rd order active low pass filter. Corner frequency of the filter is 45kHz, suitable for f_S = 96kHz DVD signal. Monaural mode can be accomplished by differencing Analog Plus Output and Analog Minus Output.

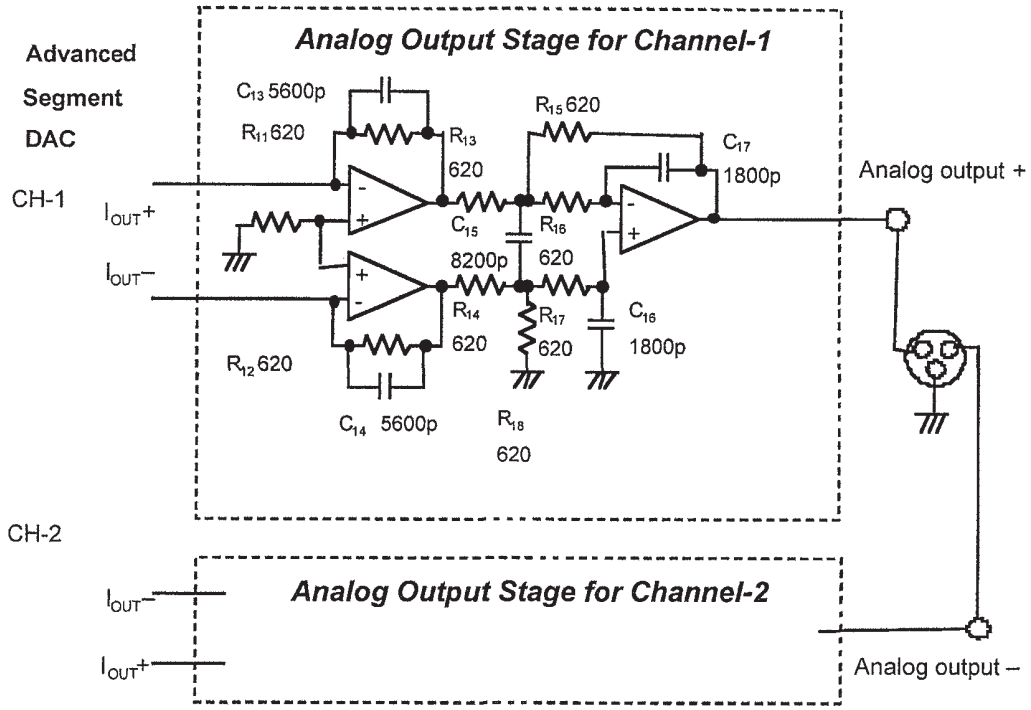
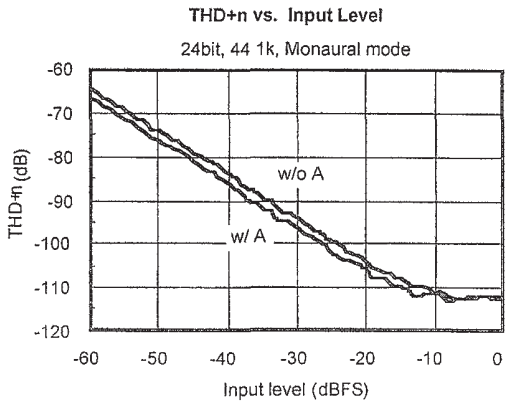


Figure 8. Application circuit of I-V conversion realizing a 3rd order active low pass filter

Total harmonic distortion curve as a function of input level shows monotonic decreasing and achieves –112dB (0.00025%) at the full scale for input signal f_S = 44.1kHz as shown in Figure 9. Achievement of THD+N for full scale is limited by external OPA performance.

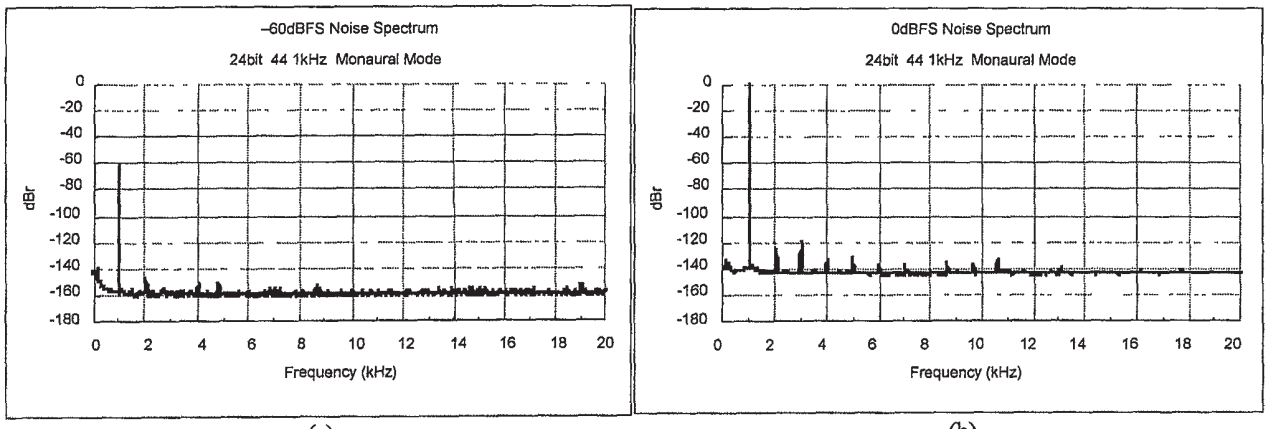
Figure 10 (a) and (b) show the FFT plot of an input 1kHz sine wave with –60dB and 0dBFS amplitude, respectively.

Figure 11 (a) and (b) show the output waveform of 24bit, –120dBFS signal for the 123dB single channel mode and 126dB monaural mode, respectively



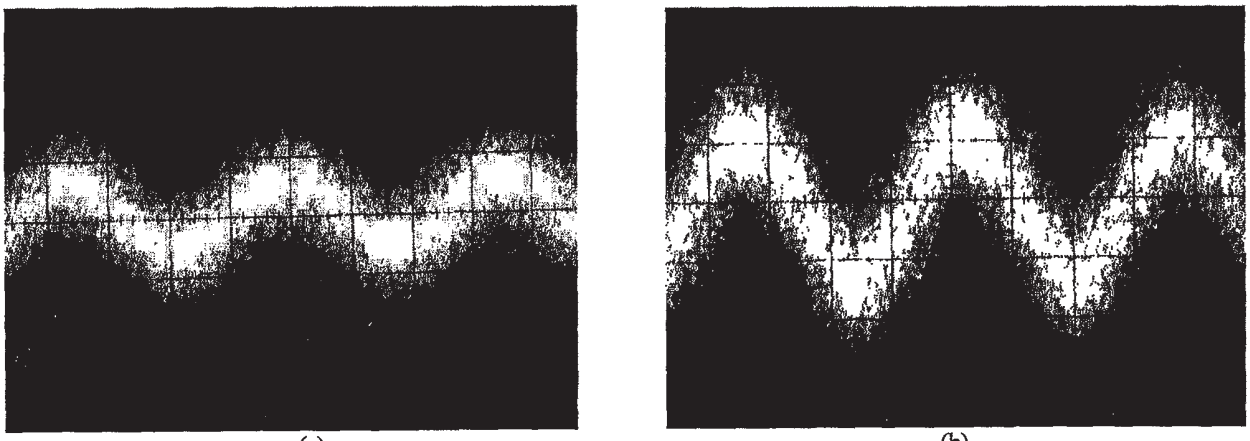
(Monaural Mode THD+n/FS = 0 00025%, DR = 126 3dB)

Figure 9. THD+N as a function of input signal



(a) (b)

Figure 10. FFT spectrum of 1kHz -60dBFS signal(a) and 0dBFS signal (b)



(a) (b)

Figure 11. Output waveform of 1kHz, 24bit, –120dBFS signal for the 123dB single channel mode (a) and 126dB monaural mode (b), respectively. Vertical axis is 5mV/div.

CONCLUSION

A novel current-mode multi-bit DAC is demonstrated for both high-end audio fans and engineers, which combines the advantages of a segment sign-magnitude DAC and the multi-bit sigma delta DAC. The architecture has overcome the various drawbacks of conventional multi-bit and achieved 126dB dynamic range with THD+N 0.00025% for Full Scale signal.

REFERENCES

[1] Burr-Brown, Product Data Sheet PCM1704

[2] C. Dunn and M.O.Hawksford, "Is the AESEBU/SPDIF digital audio interface flawed?", presented at the 93rd Convention of the Audio Engineering Society, October, San Francisco, 1992.

[3] S. Nakao, H. Terasawa, H.Aoyagi, N. Terada and T. Hamasaki " A 117dB D-Range Current-mode Multi-bit Audio DAC for PCM and DSD Audio Playback", at the 109th Convention of the Audio Engineering Society, September, Los Angeles, 2000.