# CLOCKING THE AD7760

The AD7760 requires an external low jitter clock source. This signal is applied to the MCLK pin, and the MCLKGND pin is used to sense the ground from the clock source. An internal clock signal (ICLK) is derived from the MCLK input signal. The ICLK controls all internal operations of the AD7760. The maximum ICLK frequency is 20 MHz, but due to an internal clock divider, a range of MCLK frequencies can be used. There are two ways to generate the ICLK:

$ICLK = MCLK$ ($\overline{CDIV} = 1$)

$ICLK = MCLK/2$ ($\overline{CDIV} = 0$)

These options are selected from the control register (see the AD7760 Registers section for more details). On power-up, the default is ICLK = MCLK/2 to ensure that the part can handle the maximum MCLK frequency of 40 MHz. For output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 6, output data rates of 192 kHz, 96 kHz, and 48 kHz are achievable with this ICLK frequency. As mentioned previously, this ICLK frequency can be derived from different MCLK frequencies.

It is recommended that the MCLK signal applied to the AD7760 has a 50-50 mark-space ratio. When operating in clock divide-by-1 mode (that is, $\overline{CDIV} = 1$), using higher mark-space ratios reduces the maximum MCLK frequency that can be applied to the AD7760 yielding maximum performance. For example, using a mark-space ratio of 60-40 (with $\overline{CDIV} = 1$) reduces the maximum MCLK frequency that will yield the maximum INL and THD performance to 16 MHz.

## BUFFERING THE MCLK SIGNAL

The MCLK signal for the AD7760 must be buffered before being input to the MCLK pin on the AD7760 device. This can be done simply by routing the MCLK signal to both inputs of an AND gate (see Figure 47).

The recommended buffer is the NC7SZ08M5, which is a two-input AND gate from Fairchild Semiconductor. Using the buffer with a supply voltage of 5 V is advised to achieve optimum performance from the AD7760.

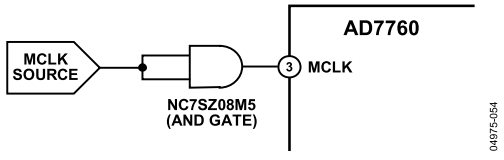


*Figure 47. Buffering the MCLK Signal Using the NC7SZ08M5 AND Gate*

## MCLK JITTER REQUIREMENTS

The MCLK jitter requirements depend on a number of factors and are given by

$$t_{j(rms)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR\,(dB)}{20}}}$$

where:
*OSR* = oversampling ratio = $f_{ICLK}/ODR$.
$f_{IN}$ = maximum input frequency.
*SNR(dB)* = target SNR.

### *Example 1*

This example can be taken from Table 6, where:
*ODR* = 2.5 MHz.
$f_{ICLK}$ = 20 MHz.
$f_{IN}$ (max) = 1 MHz.
*SNR* = 108 dB.

$$t_{j(rms)} = \frac{\sqrt{8}}{2 \times \pi \times 10^{6} \times 10^{5.4}} = 1.79 \text{ ps}$$

This is the maximum allowable clock jitter for a full-scale, 1 MHz input tone with the given ICLK and output data rate.

### *Example 2*

Take a second example from Table 6, where:
*ODR* = 48 kHz.
$f_{ICLK}$ = 12.288 MHz.
$f_{IN}$ (max) = 19.2 kHz.
*SNR* = 120 dB.

$$t_{j(rms)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^{3} \times 10^{6}} = 133 \text{ ps}$$

The input amplitude also has an effect on these jitter figures. For example, if the input level was 3 dB below full-scale, the allowable jitter would be increased by a factor of √2, increasing the first example to 2.53 ps rms. This happens when the maximum slew rate is decreased by a reduction in amplitude. Figure 48 and Figure 49 illustrate this point, showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.