SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOS DRIVE

INTRODUCTION

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced.

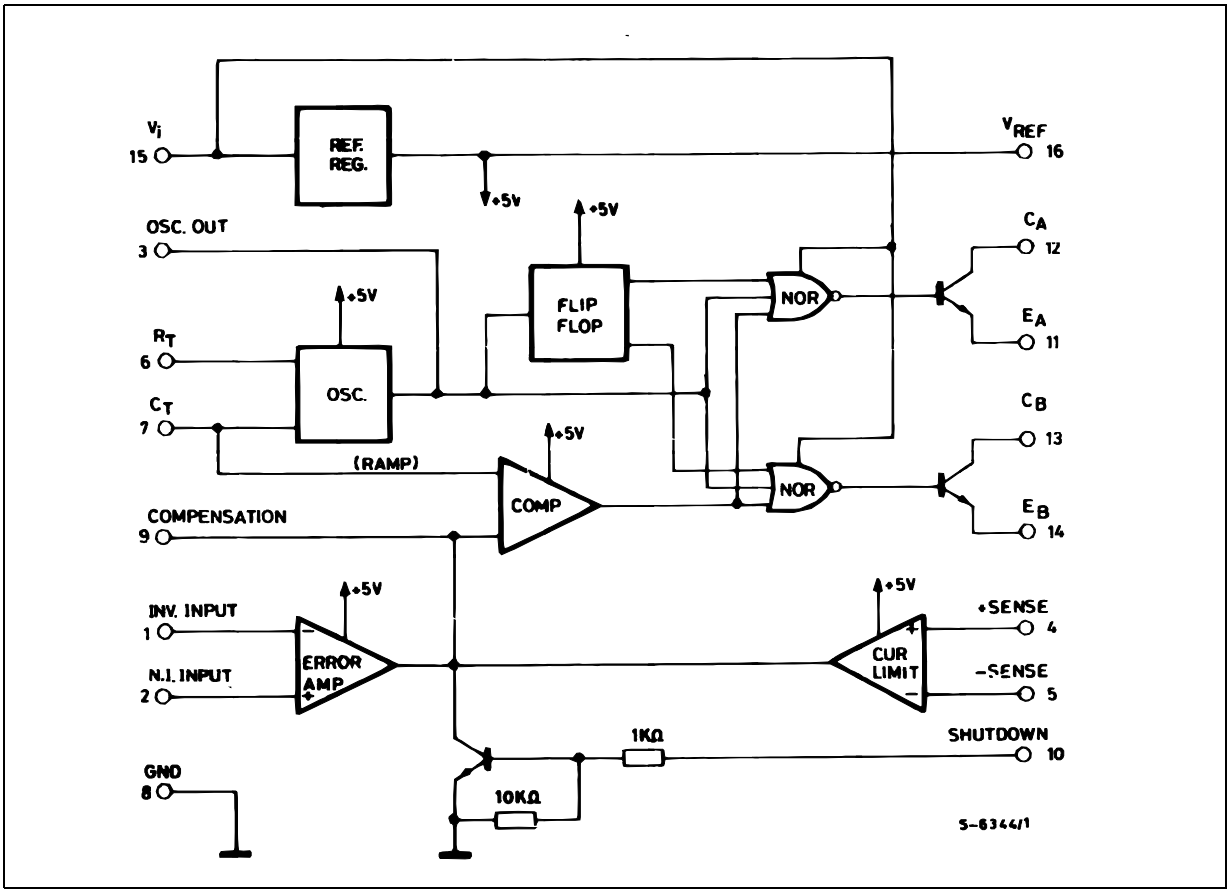
Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical Power Mos which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs.

In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000 pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complimentary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Figure 1 : The SG1524 relating PWM block diagram.
This design was the first complete I.C. control chip for switch mode power supplies.

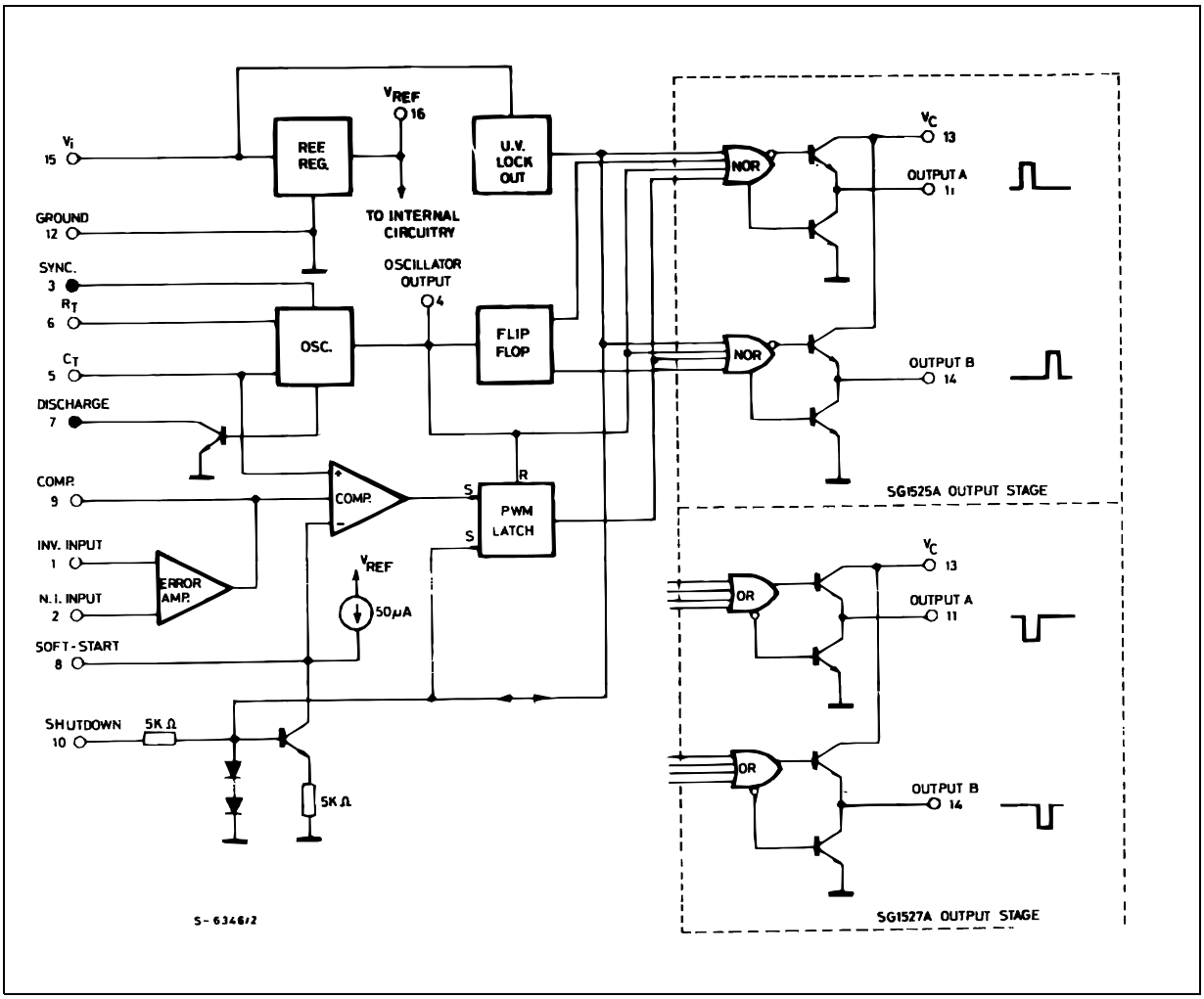


INTEGRATING MORE POWER SUPPLY FUNCTIONS

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in figure 1, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated : 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the SG1525A is shown in figure 2. Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the SG1525A device defined by an output configuration which is high during the ON pulse, and the SG1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see figure 3) for the SG1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

Figure 2 : The SG1525A family represents a "second generation" of IC controllers.

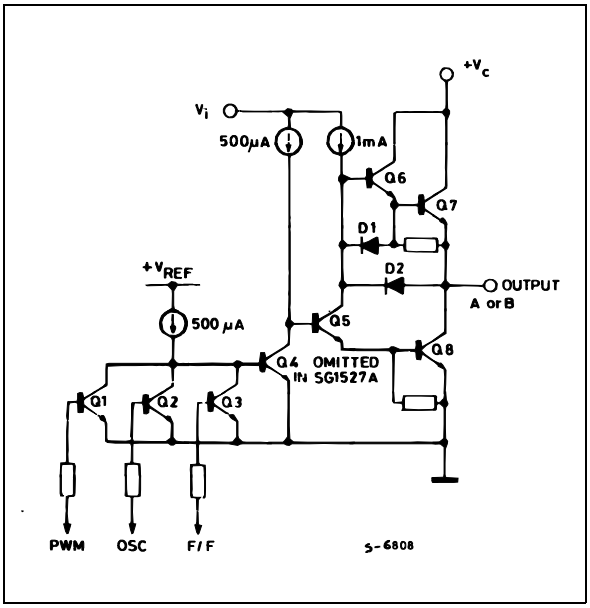


"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_i supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_i, the output cannot rise higher than approximately 1 1/2 volts below V_i.

Figure 3 : One of Two Power Output Stages Contained within the SG1525A which Conduct Alternately due to the Internal Flip-

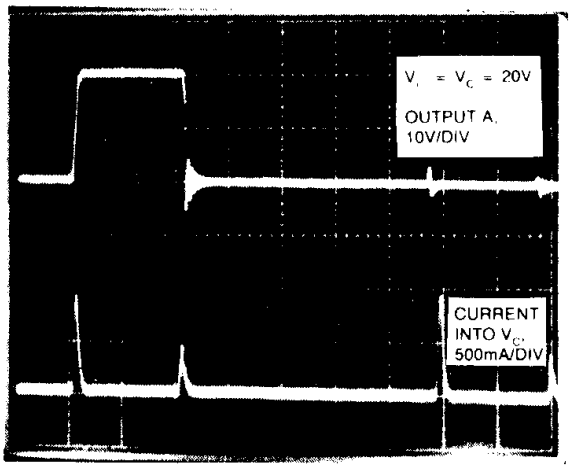


During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100ns. A typical current waveform at V_C is shown in figure 4. This transient will normally be decoupled from the rest of the control power by a 0.1 µF capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

The output saturation characteristics of this stage are shown in figure 5. The source transistor, Q_7 is a straight forward Darlington and its saturation voltage remains between 1 and 2 V out to 400 mA under the assumption that $V_i \geq V_{CC}$. The sink transistor, Q_8, however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1 mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2 V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8. With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

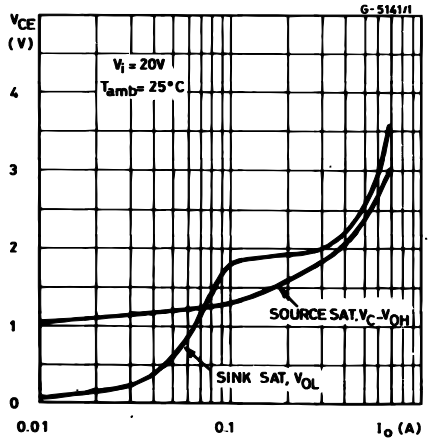
A typical output configuration for a push-pull bipolar transistor power stage is shown in fig. 6. With a stea-

Figure 4 : Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.



dy state base drive current from the SG1525A of 100 mA, this stage should be able to switch 1 to 5 A of transformer primary current, depending upon the choice of transistors. The sum of R_1 and R_2 determine the maximum steady state output current of the SG1525A while their ratio defines the voltage

Figure 5 : The output saturation characteristics of the SG1525A provide both high drive current an low hold-off voltage.



across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1. With the values given, the output current and voltage waveforms are shown in figure 7 for a one microsecond pulse. If power MOS are used for the output switches as shown in figure 8, the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the power device.

Push-pull direct transformer drive is also particularly advantageous with SG1525A as shown in figure 9.

Figure 6 : A Typical Push-pull Converter Power Stage Using External Bipolar Power Transistor Switches

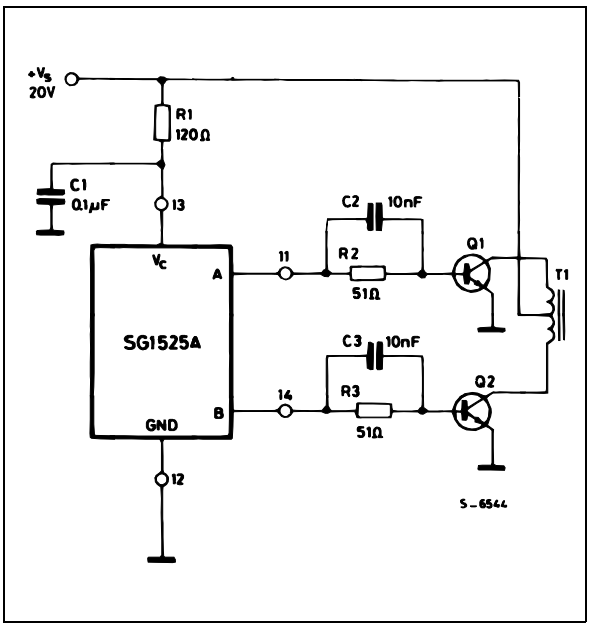
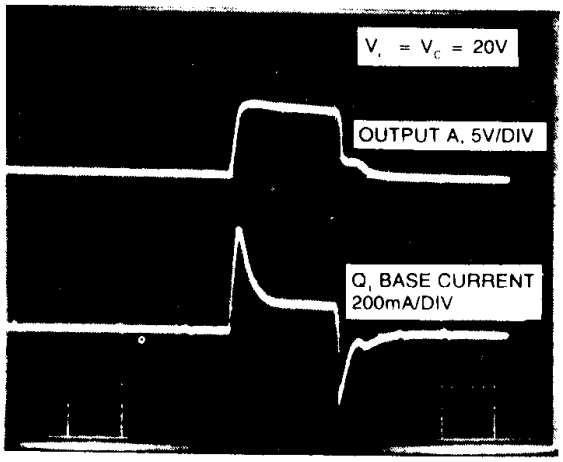


Figure 7 : Base current waveforms (figure 6 circuit) show the enhanced turn-on and turn-off current possible with the SG1525A.



A version of this configuration is required for isolation when the control circuit is referenced to the secondary side of an off-line power system, and to provide level shifting of drive signals for bridge and full bridge switching. The configuration of figure 9 has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the SG1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

A useful single-ended configuration, typical of buck regulators, is shown in figure 10. Here the SG1525A outputs are grounded and the PWM signal is taken from the V_C terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

Figure 8 : Replacing bipolar transistors with power MOS provides even greater simplicity due to the low driving impedances of the SG1525A in each transition.

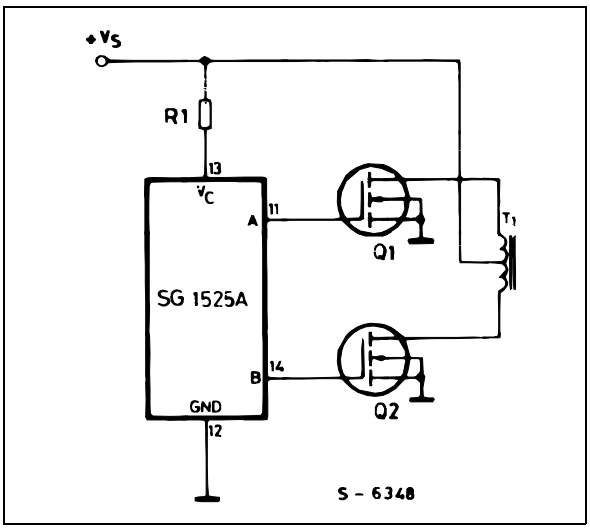


Figure 9 : The SG1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary center-tap.

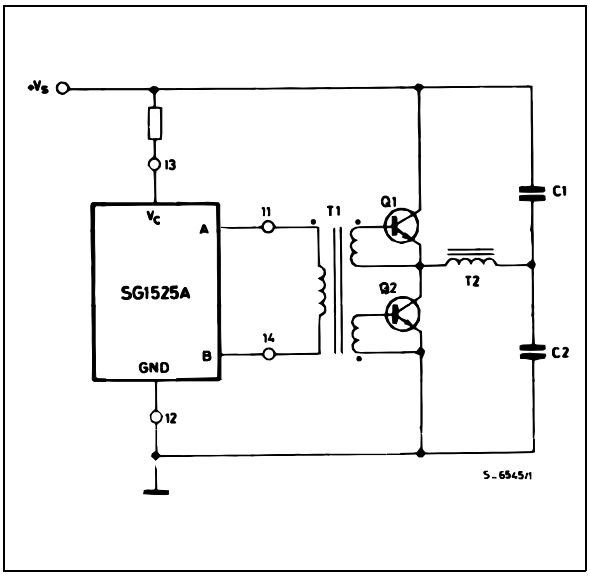
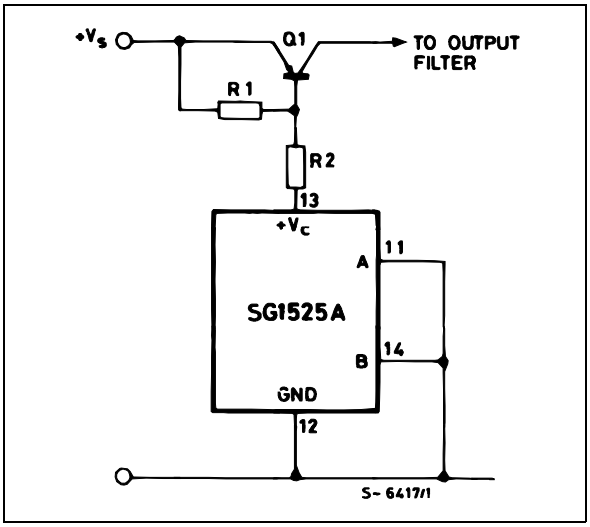


Figure 10 : A single-ended Ground-referenced Power Stage for a Flyback or Boost Regulator.



CONTROLLING POWER SUPPLY START-UP

Although the advantages of the SG1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the SG1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2 1/2 V of supply voltage which is less than the vol-tage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8 V insuring that all the remaining SG1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5 V. There is about 500 mV of hysteresis built in to eliminate clamp oscillation at threshold.

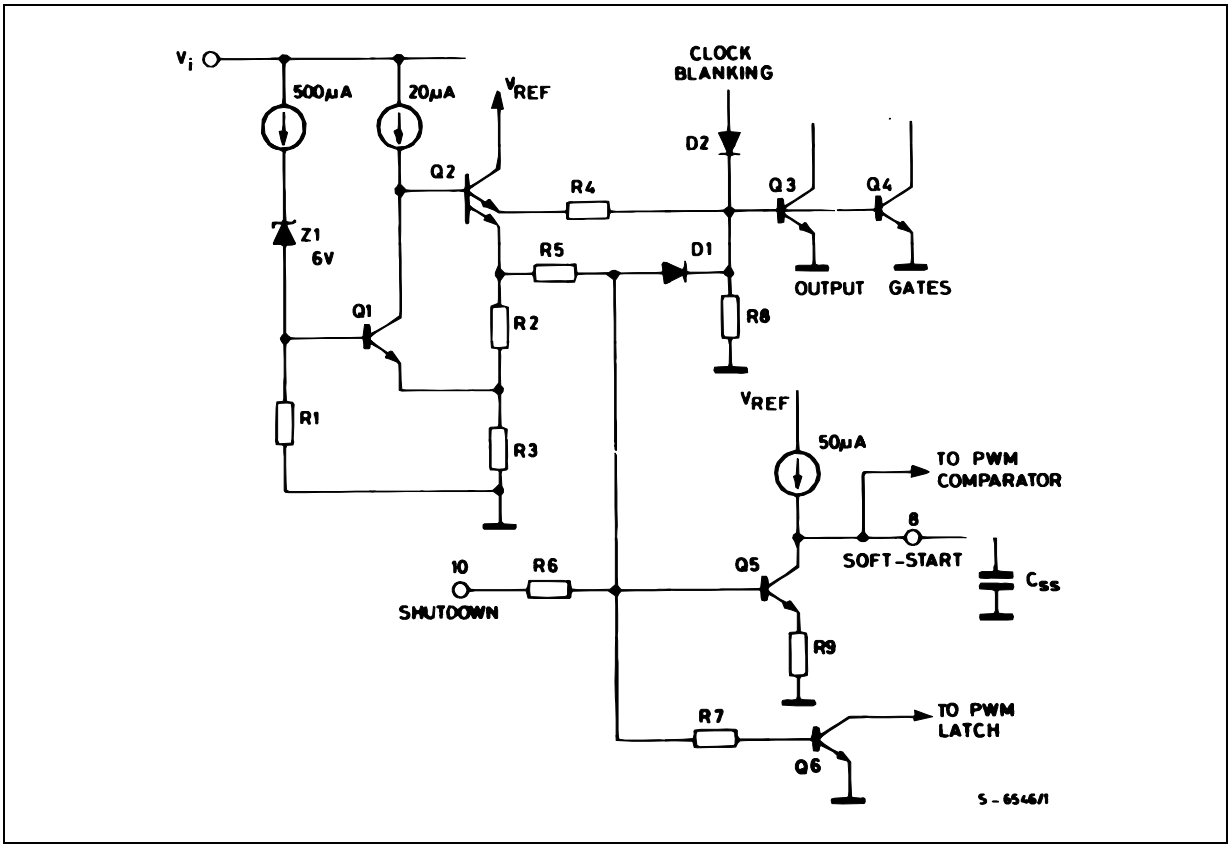
Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100 % duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50 µA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in figure 11.

Q_3 and Q_4 are the output gates normally driven by the oscillator through D_2 to provide output blanking between pulses. (One of these transistors is shown as Q_2 in figure 3). At low supply voltages, Q_2 conducts with base drive from the 20 µA current source. Q_2 provides three functions. First, current through R_4 activates the output gates with minimum voltage drop. Second, current through R_5 activates the shutdown transistor Q_5 holding the soft-start capacitor, C_{SS}, discharged. Third, R_2 provides a small bucking voltage across R_3 for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1, that transistor turns on. This turns off Q_2, activating the outputs and allowing C_{SS} to begin to charge from the internal 50 µA current source. The time to reach approximately 50 % duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50\ \mu A}\right) C_{SS}$$

Figure 11 : The Internal Power Turn-on, Soft-start, and Shutdown Circuitry of the SG1525A.



POWER SUPPLY SHUTDOWN

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the SG1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to figure 11, the base of Q_5 is turned on by a signal which is clamped to approximately 1.4 V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4. This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R_9, becomes a 100 µA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200 ns through D_1. Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100 µA

discharge of C_{SS}. However, if the activation pulse on pin 10 has a duration shorter than 1/3 of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS}, recycling soft-start.

Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

REGULATING PWM PERFORMANCE IMPROVEMENTS

The SG1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below :

REFERENCE REGULATOR

The output voltage of this regulator is internally trimmed to 5.1 V $\pm$ 1 % during manufacture, eliminating the need for adjusting potentiometers in most applications.

ERROR AMPLIFIER

SG1525A uses the same basic transconductance amplifier as the SG1524 with an important difference : it is powered by V_i rather than V_{REF}. Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM COMPARATOR

The significant benefit of the SG1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The SG1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momenetarily activating the shutdown circuitry within the SG1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

OSCILLATOR

The functions of the oscillator within the SG1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple SG1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of figure 12 for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8, which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2. The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D. As long as C_T is discharging, the clock output is high, blanking the outputs.

Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately :

$$f \approx \frac{1}{C_T\,(.07\,R_T + 3\,R_D)}$$

External synchronization can easily be accomplished with a 2.8 V positive pulse at pin 3. This will turn on Q_9, lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered : First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200 ns ; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple SG1525A devices together, one need only to define a master with the correct R_TC_T time constant, connect its output pin to the slave sync pins, and set each slave R_TC_T for a time constant 10-20 % longer than the master.

Figure 12 : A Simplified Schematic of the SG1525A's Oscillator Circuitry.

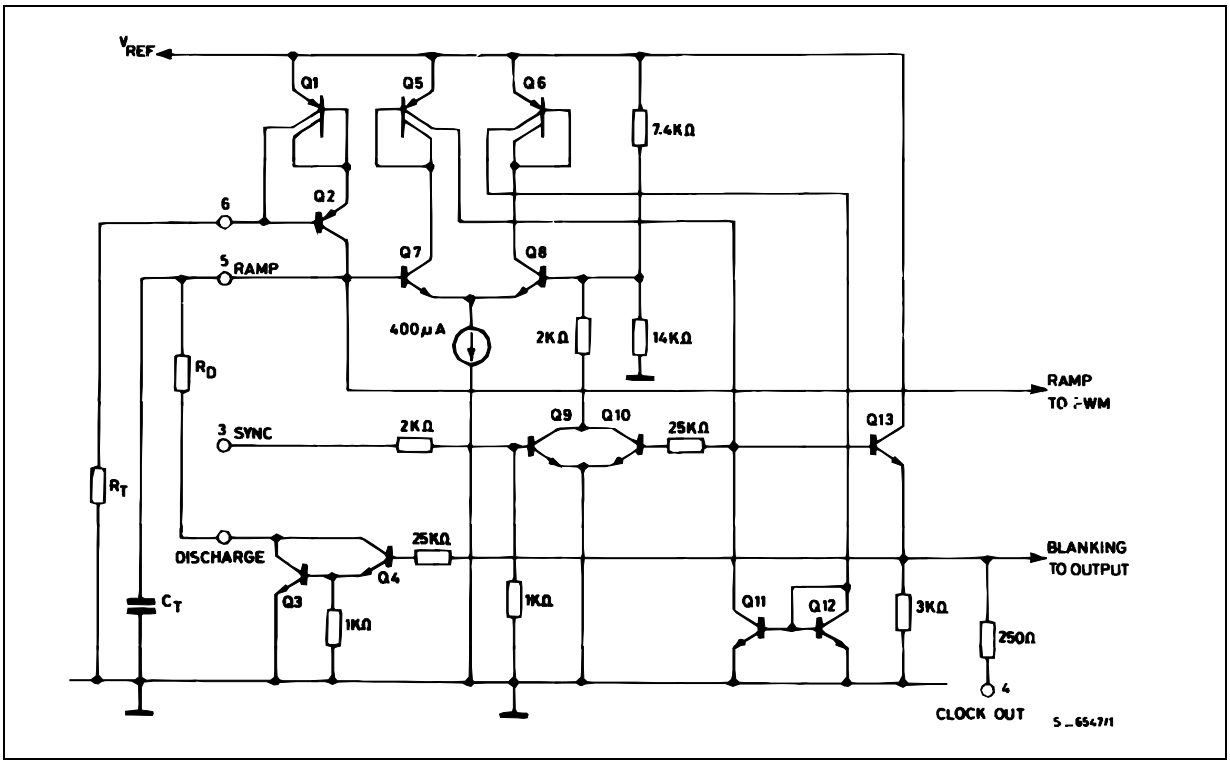
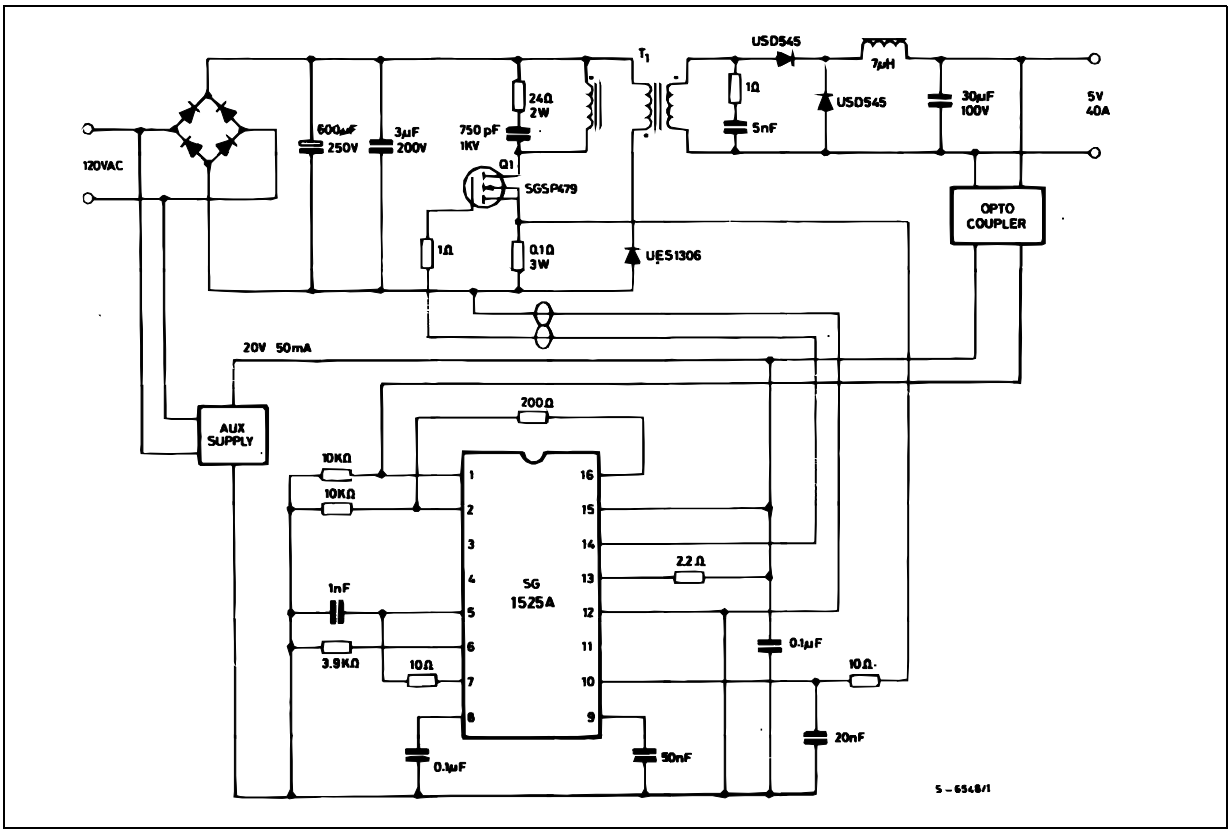


Figure 13 : 200 W, Off-line Forward Converter.



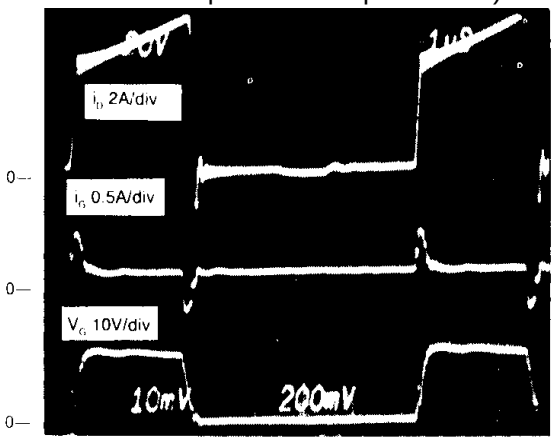
A 200 WATT, OFF-LINE, FORWARD CONVERTER

The ease of interfacing the SG1525A into a practical power supply system can be illustrated by the off-line, power converter shown in figure 13. This 200 W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a L123 or LM723. One other undefined block in figure 13 is the auxiliary power supply which supplies the low voltage, low current bias supply for the SG1525A and the drive for Q_1 the power switch. The choice of the SGSP479 power MOS for this switch keeps the total power requirements from the auxiliary supply at less than 1 W ; readily implemented with a small, line-driven transformer.

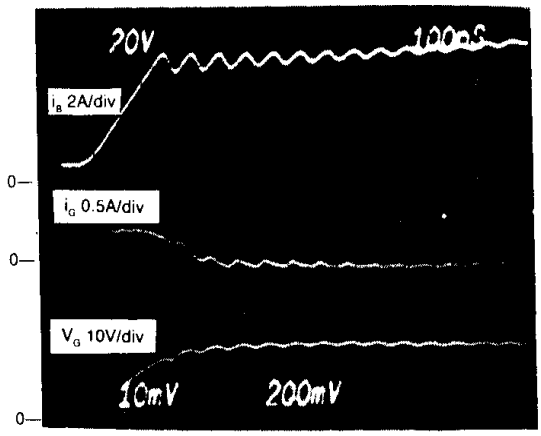
This converter is designed to operate at 150 kHz which is accomplished by running the SG1525A at 300 kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50 %, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12 kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the 0.05 µF capacitor on pin 9.

The totem-pole output of the SG1525A is used to advantage to drive Q_1 by providing a 400 mA peak current to charge and discharge the power MOS gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in figure 14.

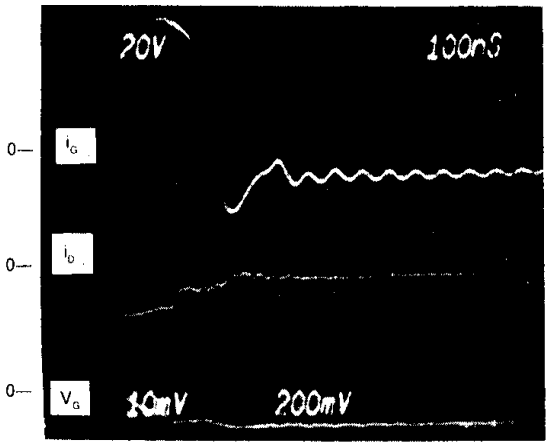
Figure 14 : Current and Voltage Waveforms for the 200 W Off-line Forward Converter with a SG1525A Direct Driven Power MOS Switch (operating frequency is 150 KHz with output current equal to 40 A).



1 µs/div
a) Waveforms of I_D, I_G, V_G



b) Risetime
= 90 ns



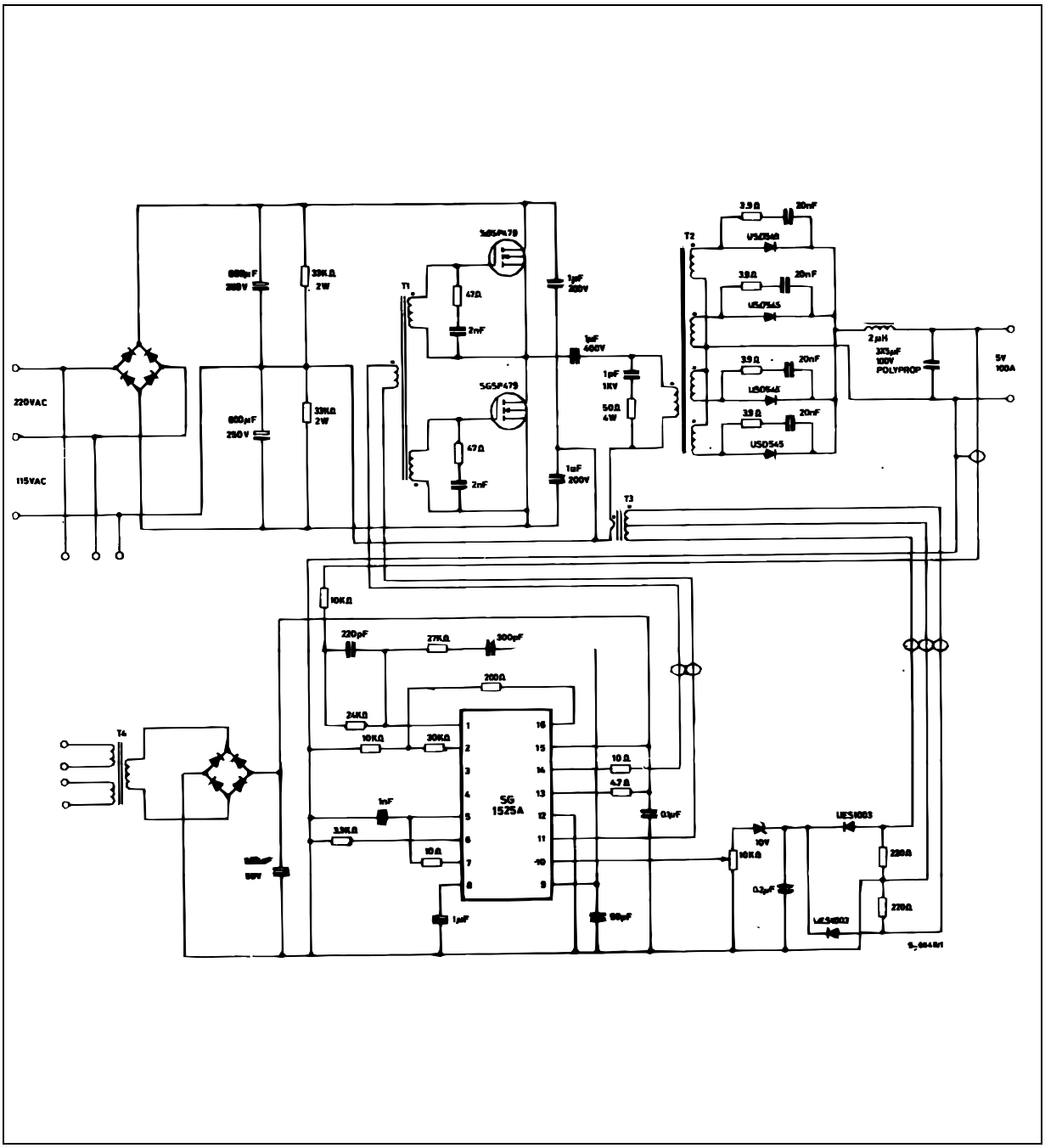
c) Falltime
= 30 ns

When operating at full load, the efficiency of this converter is 73 % with by far the greatest power losses occurring in the output rectifiers-even though Schottky devices have been selected.

Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in SGSP479 with the 0.1 Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the SG1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

Figure 15 : 500 W, 100 kHz Half-bridge Schematic.



Transformer winding data

500 W, 100 kHz, Off-Line, Half-Bridge Converter :

T1 Core : Ferrox 486T250-3C8
Pri : 14 T #22AWG
Sec (2) : 7 T #22AWG

T2 Core : Ferrox EC52-3C8 (EE)
Pri : 14 T, 2 layers, 2 #16AWG in parallel
Sec (2) : each 2 T, C.T., copper strap
0.01" x 0.8"

T3 Core : Ferrox 486T250-3C8
Pri : 1 T
Sec : 20 T, C.T. #22AWG

T4 117 V/220 V, 25 V, 0.15 A, 50-60 Hz

L1 Core : Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

500 WATT, OFF-LINE, HALF-BRIDGE CONVERTER

The circuit shown in figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer.

The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the SG1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

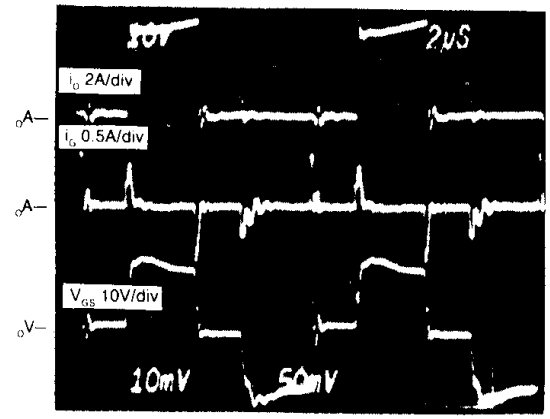
Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.

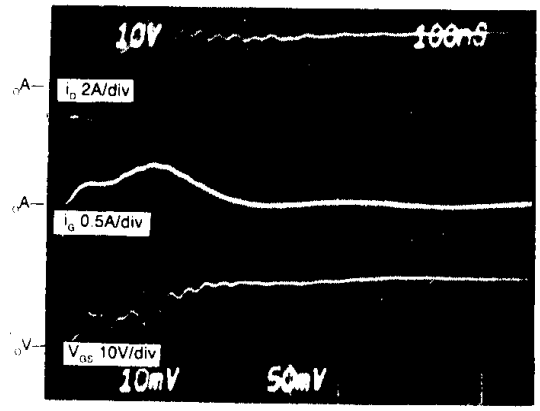
Current limiting is provided by current transformer T3 in series with the primary of the power transformer T2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the SG1525A.

Waveforms of the converter are shown in the scope photos of figure 16. Current rise and fall times are 20 ns and 10 ns.

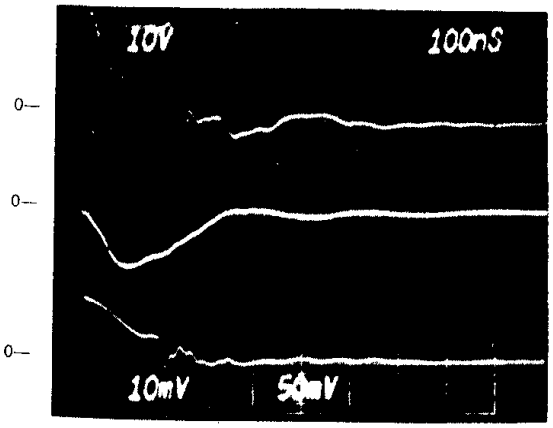
Figure 16 : Performance Waveforms for the Half-bridge, 500 W, 100 kHz Converter with Output Current of 80 A.



2 µs/div
a) Waveforms of I_D, I_G, V_G



100 ns/div
b) Risetime



100 ns/div
c) Falltime

IMPROVED PERFORMANCE ; LESS COMPLEXITY

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the SG1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.