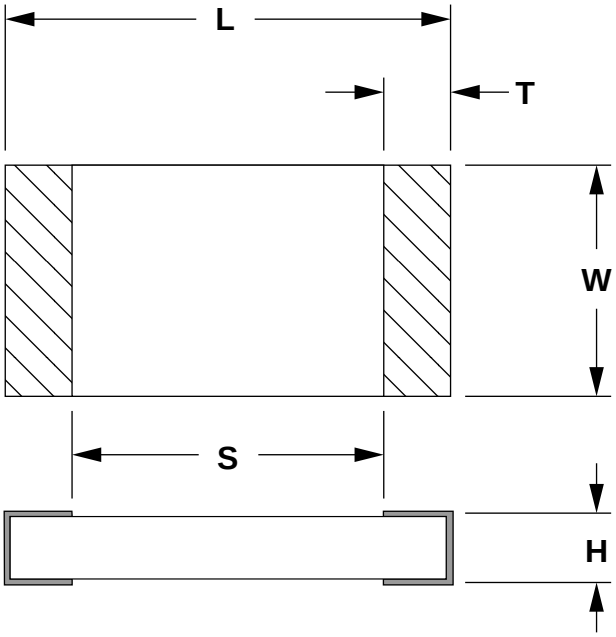
4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for chip resistors.



IPC-782-8-1-2

mm [in] Component Identifier	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	1.00	1.10	0.40	0.70	0.48	0.60	0.10	0.30	0.40
1608 [0603]	1.50	1.70	0.70	1.11	0.70	0.95	0.15	0.40	0.60
2012 [0805]	1.85	2.15	0.55	1.32	1.10	1.40	0.15	0.65	0.65
3216 [1206]	3.05	3.35	1.55	2.32	1.45	1.75	0.25	0.75	0.71
3225 [1210]	3.05	3.35	1.55	2.32	2.34	2.64	0.25	0.75	0.71
5025 [2010]	4.85	5.15	3.15	3.92	2.35	2.65	0.35	0.85	0.71
6332 [2512]	6.15	6.45	4.45	5.22	3.05	3.35	0.35	0.85	0.71

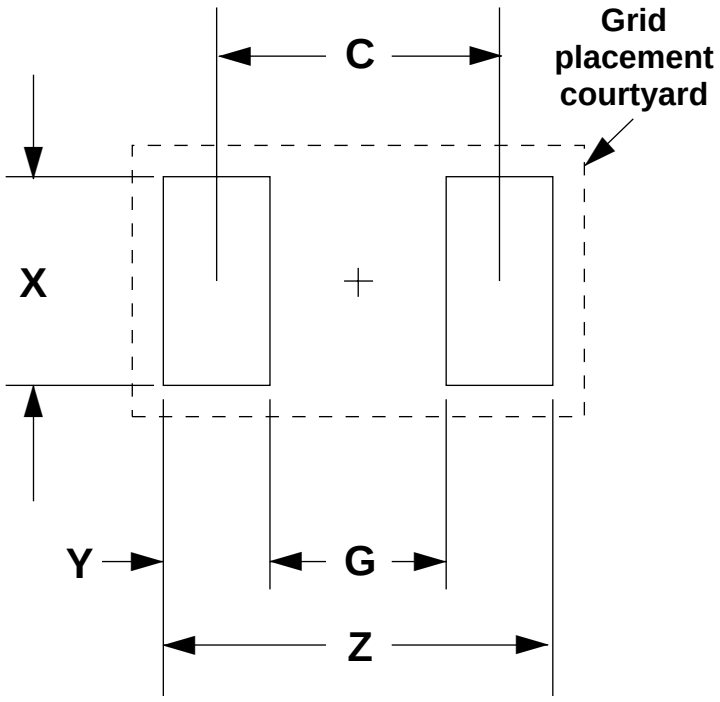
Figure 2 Chip resistor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for chip resistors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



IPC-782-8-1-3

RLP No.	Component Identifier (mm) [in.]	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	Placement Grid (No. of Grid Elements)
100A	1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
101A	1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
102A	2012 [0805]*	3.20	0.60	1.50	1.30	1.90	4x8
103A	3216 [1206]*	4.40	1.20	1.80	1.60	2.80	4x10
104A	3225 [1210]*	4.40	1.20	2.70	1.60	2.80	6x10
105A	5025 [2010]*	6.20	2.60	2.70	1.80	4.40	6x14
106A	6332 [2512]*	7.40	3.80	3.20	1.80	5.60	8x16

**Note:* If a more robust pattern is desired for wave soldering devices larger than 1608 [0603], add 0.2 mm to the Y-dimension, and consider reducing the X-dimension by 30%. Add a ''W'' suffix to the number; e.g., 103W.

Figure 3 Chip resistor land pattern dimensions

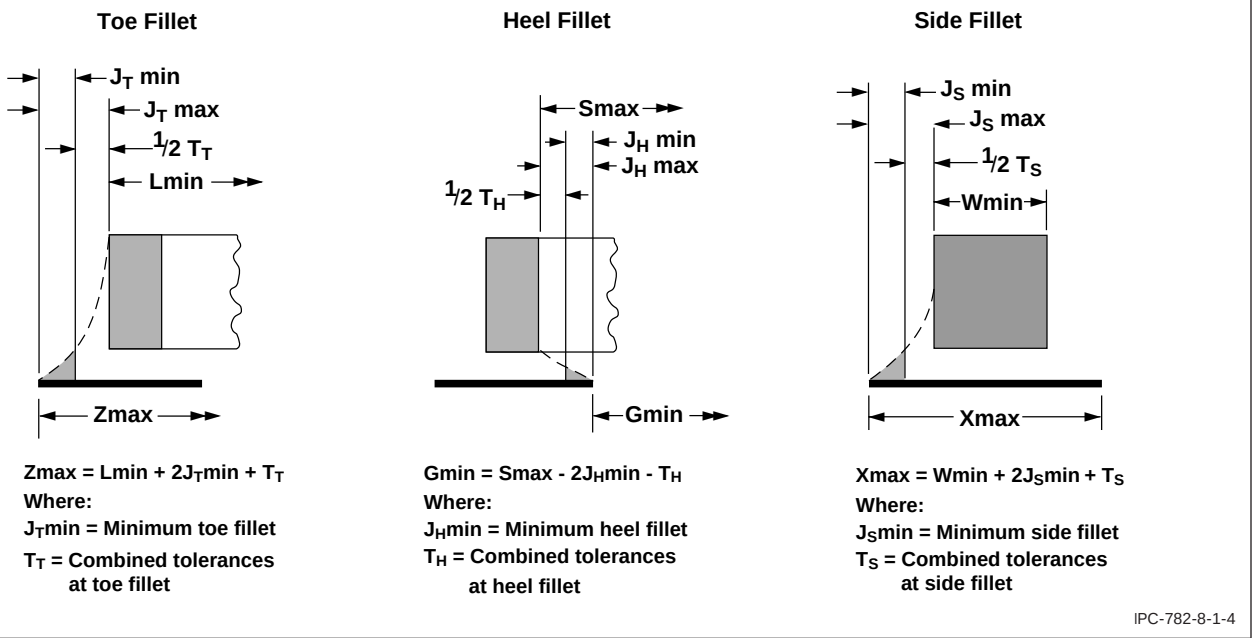
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed, and are given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions.)

The dimensions for the statistical minimum and maximum solder joint fillets at the toe, heel, or side (J_T, J_H, or J_S) have been determined based on the equations detailed in Section 3.3. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



IPC-782-8-1-4

RLP No.	Tolerance (mm) Assumptions		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	J_{Tmin}	J_{Tmax}	C_S	J_{Hmin}	J_{Hmax}	C_W	J_{Smin}	J_{Smax}
100A	0.10	0.10	0.10	0.51	0.60	0.30	–0.02	0.15	0.12	0.02	0.11
101A	0.10	0.10	0.20	0.53	0.65	0.41	0.04	0.25	0.25	0.01	0.15
102A	0.10	0.10	0.30	0.51	0.68	0.77	–0.03	0.36	0.30	0.03	0.20
103A	0.10	0.10	0.30	0.51	0.68	0.77	0.17	0.56	0.30	0.01	0.18
104A	0.10	0.10	0.30	0.51	0.68	0.77	0.17	0.56	0.30	0.01	0.18
105A	0.10	0.10	0.30	0.51	0.68	0.77	0.27	0.66	0.30	0.01	0.18
106A	0.10	0.10	0.30	0.46	0.63	0.77	0.32	0.71	0.30	–0.09	0.08

Figure 4 Tolerance and solder joint analysis