ESS Technology, Inc.

ES9008
Sabre Reference Audio DAC
Datasheet

OVERVIEW

The Sabre Reference (ES9008) Highest Performance Audio DAC is the world's first 8-channel audio DAC to bring true professional digital audio to the mass consumer home entertainment market.

Using ESS's patented Hyperstream™ architecture and patent-pending Time Domain Jitter Eliminator, the Sabre Reference Audio DAC outperforms the best audiophile equipment with unprecedented 134dB DNR and -118dB THD+N, delivering true studio quality audio to digital audio applications such as HD-DVD, Blu-ray, SACD, DVD-Audio, DVD, CD, home theatre, set top boxes and digital TV.

The Sabre Reference's flexible input architecture accepts SPDIF or PCM data from 16-24 bits up to a 192 kHz sampling rate, and also accepts 1-bit DSD data supporting native SACD audio.

The Sabre Reference sets a new standard for high quality audio performance in a cost effective, compact, easy to use form factor for today's most demanding digital audio applications.

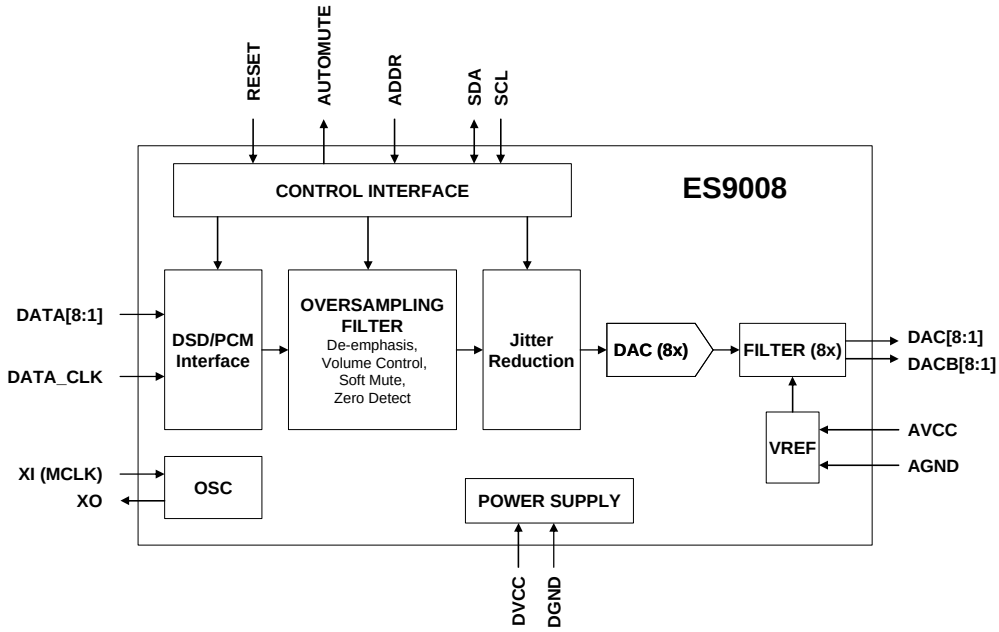
KEY FEATURES

Innovation	Benefit
Patented HyperStream™ Architecture o DNR: 134dB (mono mode) o DNR: 128dB (8-channel mode) o THD+N: -118dB	Unprecedented dynamic range and low distortion allowing true reproduction of audio as it is mastered at recording studio
Patent-pending Time Domain Jitter Reduction	Unmatched audio clarity free from input clock jitter allowing simple system design and layout
48-bit accumulator and 28-bit processing	Distortion free signal processing
Auto-detect PCM/ DSD converter	Universal (e.g. DVD/SACD) audio playback
8-channel DAC in 64-LQFP	Reduces PCB footprint and simplifies board layout
Low power (150mW for 8 channels)	Simplifies power supply design
Customizable output configuration	Mono, stereo, 4 or 8-channel output in current or voltage mode based on performance criterion
Universal digital input	All-digital SPDIF, PCM (I2S, MSB/LSB justified 16, 20 or 24-bit) or DSD input
Integrated DSP functions	Click-free soft mute and volume control Programmable filter characteristics for PCM/DSD Programmable Zero detect De-emphasis for 32, 44.1 and 48kHz sampling

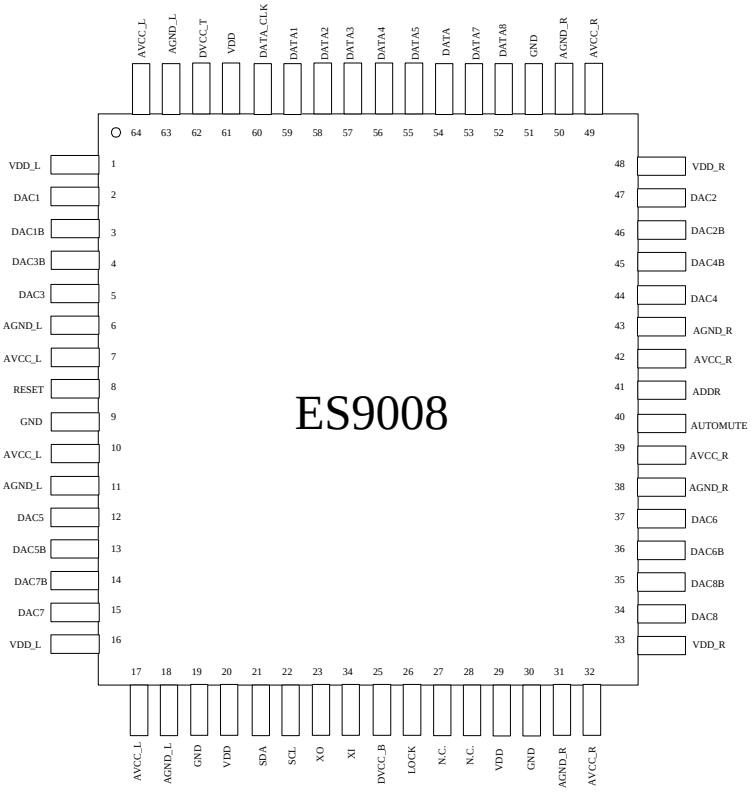
APPLICATIONS

- Blu-ray / HD-DVD players
- SACD / DVD-Audio players
- Audio receivers
- Home theater receivers
- Professional audio equipment

FUNCTIONAL BLOCK DIAGRAM



PIN LAYOUT



PIN DESCRIPTION

Pin	Name	I/O	Description
1	VDD_L	-	Analog Power (+1.2V) for Left channels
2	DAC1	O	Differential Positive Analog Output 1
3	DAC1B	O	Differential Negative Analog Output 1
4	DAC3B	O	Differential Negative Analog Output 3
5	DAC3	O	Differential Positive Analog Output 3
6	AGND_L	-	Analog Ground for Left channels
7	AVCC_L	-	Analog Power (+3.3V) for Left channels
8	RESET	I	Global Reset
9	GND	-	Digital Ground
10	AVCC_L	-	Analog Power (+3.3V) for Left channels
11	AGND_L	-	Analog Ground for Left channels
12	DAC5	O	Differential Positive Analog Output 5
13	DAC5B	O	Differential Negative Analog Output 5
14	DAC7B	O	Differential Negative Analog Output 7
15	DAC7	O	Differential Positive Analog Output 7
16	VDD_L	-	Analog Power (+1.2V) for Left channels
17	AVCC_L	-	Analog Power (+3.3V) for Left channels
18	AGND_L	-	Analog Ground for Left channels
19	GND	-	Digital Ground
20	VDD	-	Digital Power (+1.2V) for core of chip
21	SDA	I/O	I2C SDA
22	SCL	I	I2C SCL
23	XO	O	Xtal oscillator output
24	XI (MCLK)	I	Xtal oscillator input (Note: can also just be a clock input)
25	DVCC_B	-	Digital Power (+3.3V) for bottom pad ring of chip
26	LOCK	O	Lock output
27	N.C.		Not connected (leave open)
28	N.C.		Not connected (leave open)
29	VDD	-	Digital Power (+1.2V) for core of chip
30	GND	-	Digital Ground
31	AGND_R	-	Analog Ground for Right channels
32	AVCC_R	-	Analog Power (+3.3V) for Right channels
33	VDD_R	-	Analog Power (+1.2V) for Right channels
34	DAC8	O	Differential Positive Analog Output 8
35	DAC8B	O	Differential Negative Analog Output 8
36	DAC6B	O	Differential Negative Analog Output 6
37	DAC6	O	Differential Positive Analog Output 6
38	AGND_R	-	Analog Ground for Right channels
39	AVCC_R	-	Analog Power (+3.3V) for Right channels

Pin	Name	I/O	Description
40	AUTMOMUTE	O	Automute
41	ADDR	I	Chip Address Select
42	AVCC_R	-	Analog Power (+3.3V) for Right channels
43	AGND_R	-	Analog Ground for Right channels
44	DAC4	O	Differential Positive Analog Output 4
45	DAC4B	O	Differential Negative Analog Output 4
46	DAC2B	O	Differential Negative Analog Output 2
47	DAC2	O	Differential Positive Analog Output 2
48	VDD_R	-	Analog Power (+1.2V) for Right channels
49	AVCC_R	-	Analog Power (+3.3V) for Right channels
50	AGND_R	-	Analog Ground for Right channels
51	GND	-	Digital Ground
52	DATA8	I	DSD Data8
53	DATA7	I	DSD Data7
54	DATA6	I	DSD Data6
55	DATA5	I	DSD Data5 OR PCM Data CH7/CH8
56	DATA4	I	DSD Data4 OR PCM Data CH5/CH6
57	DATA3	I	DSD Data3 OR PCM Data CH3/CH4
58	DATA2	I	DSD Data2 OR PCM Data CH1/CH2
59	DATA1	I	DSD Data1 OR PCM Frame Clock OR SPDIF Input
60	DATA_CLK	I	PCM Bit Clock OR DSD Bit Clock
61	VDD	-	Digital Power (+1.2V) for core of chip
62	DVCC_T	-	Digital Power (+3.3V) for top pad ring of chip
63	AGND_L	-	Analog Ground for Left channels
64	AVCC_L	-	Analog Power (+3.3V) for Left channels

Table 1

FUNCTIONAL DESCRIPTION

PCM, SPDIF and DSD Pin Connections

The following tables show how the pins are used for PCM and DSD audio formats.

PCM Audio Format

Pin Name	Description
DATA1	Frame clock
DATA[2:5]	8-channel PCM serial data
DATA_CLK	Bit clock for PCM audio format

Table 2

SPDIF Audio Formant
Note: XI clock (MCLK) must be > 386*FS when using SPDIF input.

Pin Name	Description
DATA1	Spdif input ()

Table 3

DSD Audio Format

Pin Name	Description
DATA[1:8]	8-channel DSD data input
DATA_CLK	Bit clock for DSD data input

Table 4

Feature Description

Soft Mute
When Mute is asserted the output signal will ramp to the -∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is 0.0078125*FS dB/s, where FS = DATA_CLK/64 in PCM serial or DSD modes, or SPDIF sampling rate in SPDIF mode.

Zero Detect
The use of the zero detect function to drive an external mute circuit is not required, but is recommended for designs that need the absolute maximum signal-to-noise ratios on an idle channel.

- In PCM serial mode, the Zero Detect output pin “AUTOMUTE” will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896/(<Register#9>*DATA_CLK) Seconds.
- In SPDIF mode, the Zero Detect output pin “AUTOMUTE” will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896/(<Register#9>*(64*FS) Seconds, where FS is the SPDIF sampling rate.
- In the DSD Mode, the Zero Detect output pin “AUTOMUTE” will become active when any 8 consecutive values in the DSD stream have as many 1’s and 0’s for a length of time defined by 2096896/(<Register Automute_time>*DATA_CLK) Seconds. The following table summarizes the conditions.

Mode	Detection Condition	Time
PCM	Data is continuously lower than <Register Automute_lev >	2096896/(<Register Automute_time >*DATA_CLK)
SPDIF	Data is continuously lower than <Register Automute_lev >	2096896/(<Register Automute_time >*(64*FS)) where FS is the SPDIF sampling rate
DSD	Equal number of 1s and 0s in every 8 bits of data	2096896/(<Register Automute_time >*DATA_CLK)

Table5

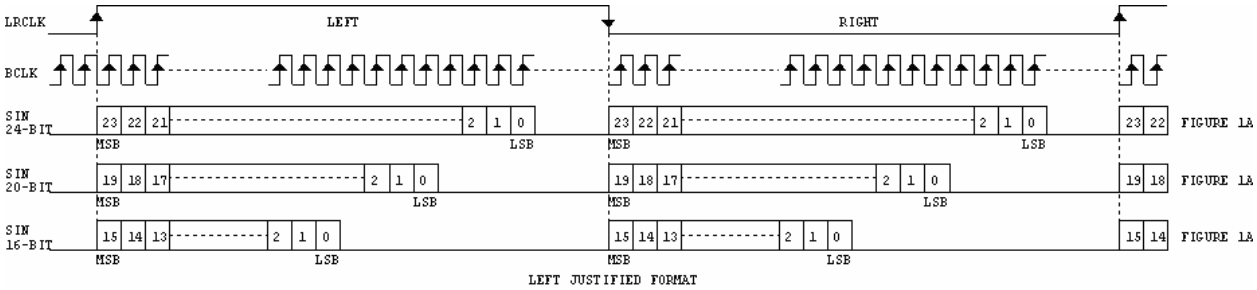
De-emphasis
The de-emphasis feature is included for audio data that has utilized the 50/15uS pre-emphasis for noise reduction. There are 3 de-emphasis filters, one for 32 kHz, 44.1 kHz and 48 kHz.

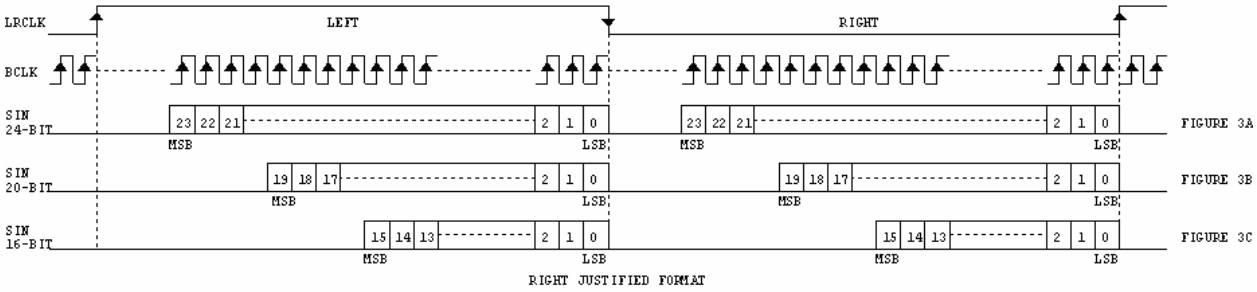
Volume Control
Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps.
Each 0.5dB step transition takes 64 intermediate levels. The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

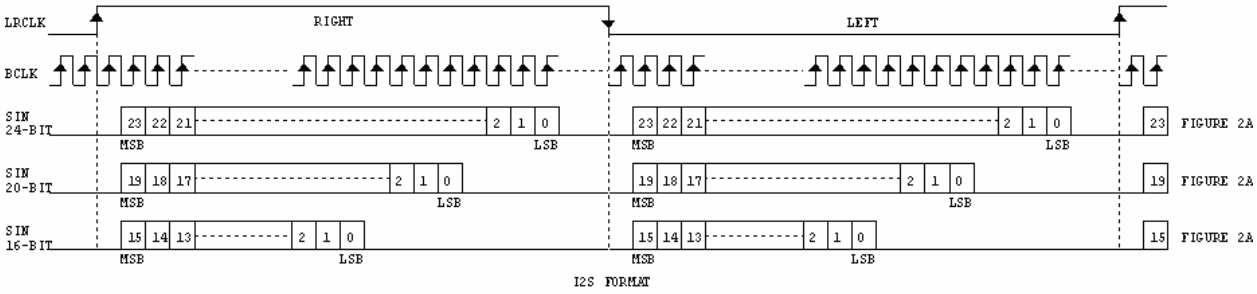
PCM Audio Interface Formats
Several interface formats are provided so that direct connection to common audio processors is possible. The available formats and their accompanying diagrams are listed in the following table. The audio interface format can be set by programming the registers.

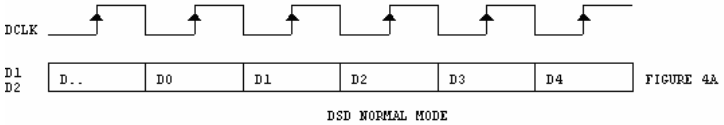
Format	Description	Figure
0	MSB First, Left Justified, up to 24-bit data	1A
1	I2S, up to 24-bit data	2A
2	MSB First, Right Justified, 24-bit data	3A
3	MSB First, Right Justified, 20-bit data	3B
4	MSB First, Right Justified, 16-bit data	3C
5	DSD Normal Mode	4A
6	DSD Phase Mode	4B

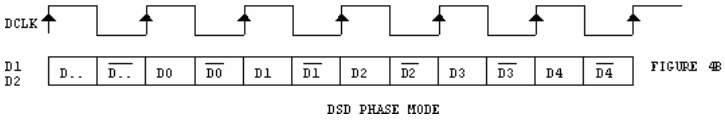
Table 6











System Clock (XI / MCLK)
A system clock is required for proper operation of the digital filters and modulation circuitry.
The system clock must be greater than 192*Fs for SERIAL/DSD inputs, or greater than 386*FS for SPDIF input.

Data Clock
This must be 64*FS for SERIAL / DSD modes, and is not required for SPDIF mode.

Digital Filters
There are numerous applications for a stereo DAC so for added flexibility; two digital filter settings are possible, sharp roll-off and a slow roll-off for PCM mode. For DSD mode, there are 4 available filters with cutoffs at 47kHz, 50kHz, 60kHz, and 70kHz.

Serial Control Interface

The registers inside the chip are programmed via an I2C interface. The diagram below shows the timing for this interface. The chip address can be set to 2 different settings via the “ADDR” pin. The table below summarizes this.

ADDR	CHIP ADDRESS
0	0x90
1	0x92

Table 7

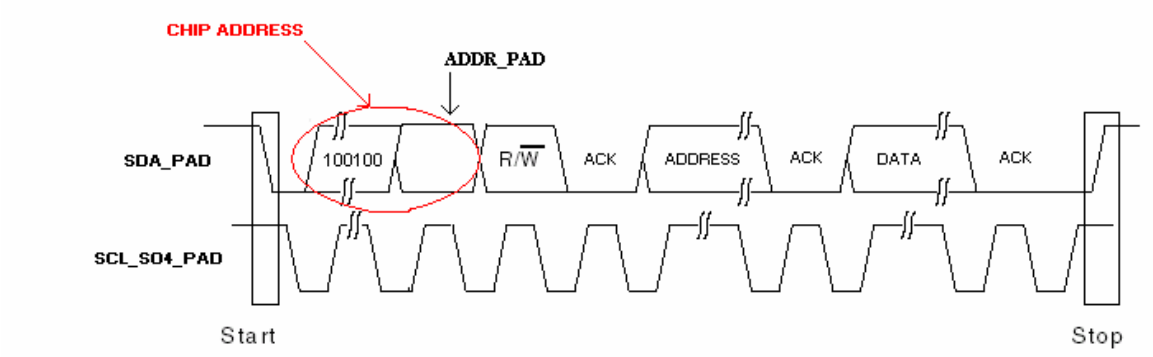


Diagram 1

Notes:

1. The “ADDR” pin is used to create the CHIP ADDRESS. (0x90, 0x92)
2. The first byte after the chip address is the “ADDRESS” this is the register address.
3. The second byte after the CHIP ADDRESS is the “DATA” this is the data to be programmed into the register at the previous “ADDRESS”.

Register Settings:

Register #0: Volume of DAC0 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #1: Volume of DAC1 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #2: Volume of DAC2 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #3: Volume of DAC3 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #4: Volume of DAC4 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #5: Volume of DAC5 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #6: Volume of DAC6 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #7: Volume of DAC7 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #8: Automute_lev **(default = 1'b0,7'd104)**
[7] : SPDIF_ENABLE.
- 1'b0 = Use either I2S or DSD input
- 1'b1 = Use SPDIF input

[6:0] : Automute trigger point in dB's = -REG_VALUE

Register #9: Automute_time **(default = 8'd4)**
Larger REG_VALUE = less time.
Smaller REG_VAULE = longer time.
Time in Seconds = 2096896/(REG_VALUE*DATA_CLK).

Register #10: Mode Control 1 **(default = 8'b00001110)**
Default is 24bit,I2S ,NO-DEEMP,UNMUTE.
[7:6] : 24/20/16 Bit for Serial Data Modes.
- 2'b00 = 24Bit
- 2'b01 = 20Bit
- 2'b10 = 16Bit
- 2'b11 = 24Bit

[5:4] : LJ/I2S/RJ Serial Data Modes.
- 2'b00 = I2S
- 2'b01 = LJ
- 2'b10 = RJ
- 2'b11 = I2S

[3] : RESERVED
- o Must be set to 1'b1 for normal operation.

[2] : JITTER_REDUCTION_ENABLE.

1'b0 = Bypass and stop JITTER_REDUCTION.
1'b1 = Use JITTER_REDUCTION.

[1] : BYPASS_DEEMPHASIS FILTER
1'b0 = Use De-emphasize Filter
1'b1 = Bypass De-emphasize Filter

[0] : MUTE DAC'S
1'b0 = Unmute All DAC's
1'b1 = Mute All DAC's

Register #11: Mode Control 2 (default = 8'b10000101)

[7] : RESERVED (must be set to 1'b1 for normal operation).
- Must be set to 1'b1 for normal operation.

[6:5] : RESERVED.
[4:2] : DPLL BANDWIDTH
3'b000 => No Bandwidth
3'b001 => Lowest Bandwidth
3'b010 => Low Bandwidth
3'b011 => Med-Low Bandwidth
3'b100 => Medium Bandwidth
3'b101 => Med-High Bandwidth
3'b110 => High Bandwidth
3'b111 => Highest Bandwidth
[1:0] : DE-EMPHASIS DELECT
2'b00 = 32kHz
2'b01 = 44.1kHz
2'b10 = 48kHz
2'b11 = RESERVED

Register #12: Mode Control 3 (default = 8'b00100000)

[7:0] : RESERVED
- Must be set to 8'b00100000 for normal operation.

Register #13: Polarity (default = 8'b00000000)

[7] : POLARITY OF DAC8
1'b0 = In-Phase
1'b1 = Anti-Phase
[6] : POLARITY OF DAC7
1'b0 = In-Phase
1'b1 = Anti-Phase
[5] : POLARITY OF DAC6
1'b0 = In-Phase
1'b1 = Anti-Phase
[4] : POLARITY OF DAC5
1'b0 = In-Phase
1'b1 = Anti-Phase
[3] : POLARITY OF DAC4
1'b0 = In-Phase
1'b1 = Anti-Phase
[2] : POLARITY OF DAC3
1'b0 = In-Phase
1'b1 = Anti-Phase
[1] : POLARITY OF DAC2
1'b0 = In-Phase

1'b1 = Anti-Phase
[0] : POLARITY OF DAC1
1'b0 = In-Phase
1'b1 = Anti-Phase

Register #14: DAC3/4/7/8 Source IIR Bandwidth, FIR Rolloff (default = 8'b00000011)

[7] : SOURCE OF DAC8
1'b0 = DAC8
1'b1 = DAC6
[6] : SOURCE OF DAC7
1'b0 = DAC7
1'b1 = DAC5
[5] : SOURCE OF DAC4
1'b0 = DAC4
1'b1 = DAC2
[4] : SOURCE OF DAC3
1'b0 = DAC3
1'b1 = DAC1
[3] : RESERVED
- Must be set to 1'b1 for normal operation.

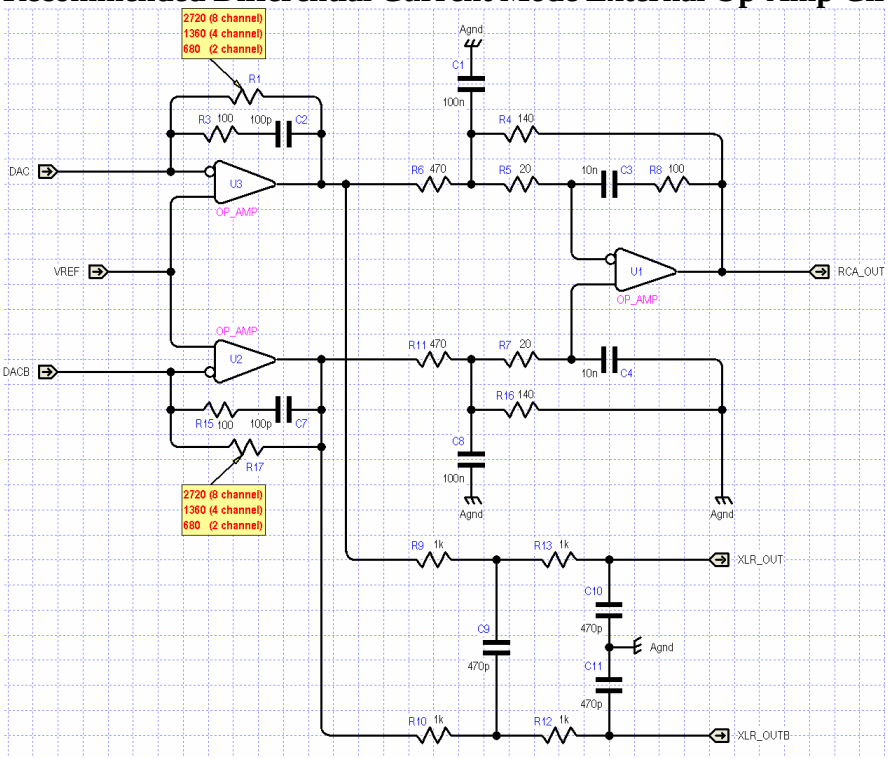
[2:1] : IIR BANDWIDTH
1'd0 = Normal
1'd1 = 50k
1'd2 = 60k
1'd3 = 70k
[0] : FIR ROLLOFF SPEED
1'b0 = Slow Rolloff
1'b1 = Fast Rolloff

Register #15: Mode Control 4 (default = 8'b01010101)

[7:0] : RESERVED
- Must be set to 8'b00000000 for normal operation.

APPLICATION DIAGRAMS

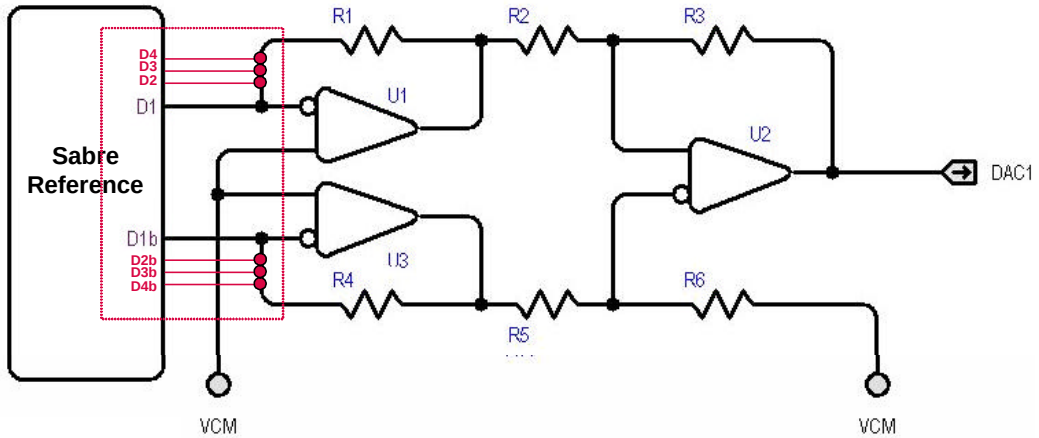
Recommended Differential Current Mode External Op-Amp Circuit



Stereo Quad-differential Current Mode

Sabre Reference in stereo "quad-differential" current mode

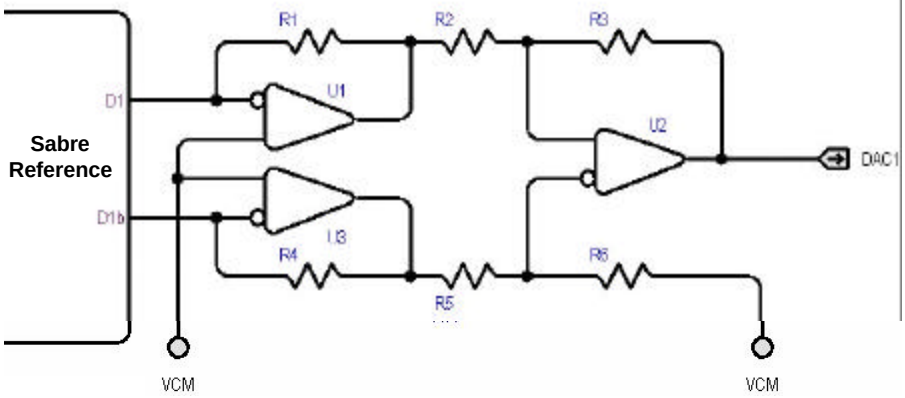
(DNR: 132dB, THD: -118dB)



8-channel Differential Current Mode

Sabre Reference in 8-channel differential current mode

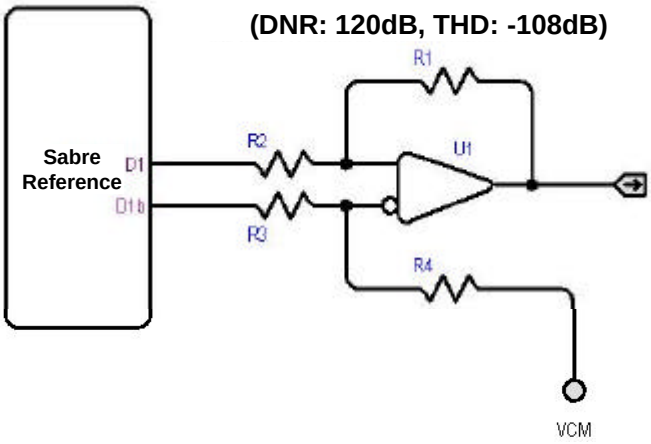
(DNR: 128dB, THD: -118dB)



8-channel Differential Voltage Mode

Sabre Reference in voltage mode

(DNR: 120dB, THD: -108dB)



ABSOLUTE MAXIMUM RATINGS

PAREMETER	RATING
Storage temperature	-65°C to 105°C
Voltage range for 5V tolerant pins	-0.5V to +5.5V
Voltage range for all other pins	-0.5V to (DVCC_T+0.5V) or -0.5V to (DVCC_B+0.5V)

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

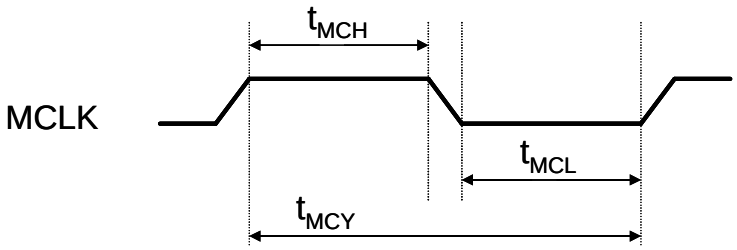
RECOMMENDED OPERATING CONDITIONS

PAREMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	0°C to 70°C
Digital core supply voltage	VDD	1.2V ± 5%, [*TBD*] mA nominal
Digital power supply voltage	DVCC_T, DVCC_B	3.3V ± 5%, [*TBD*] mA nominal
Analog 1.2V supply voltage	VDD_L, VDD_R	1.2V ± 5%, [*TBD*] mA nominal
Analog power supply voltage	AVCC_L, AVCC_R	3.3V ± 5%, [*TBD*] mA nominal

DC ELECTRICAL CHARACTERISTICS *[TBD]*

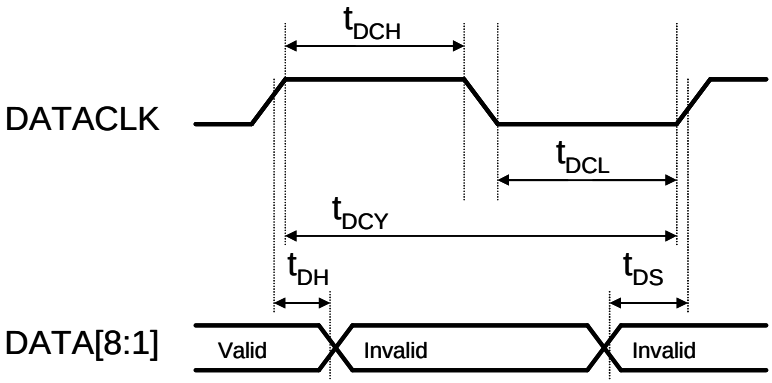
SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
V_{IH}	High-level input voltage	2.0	DVCC_T or DVCC_B	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2.0	5.5	V	All 5V tolerant inputs
V_{IL}	Low-level input voltage	-0.3	0.8	V	All input TTL levels except CLK
V_{CLKH}	CLK high-level input	2.0	DVCC_B+0.25	V	TTL level input
V_{CLKL}	CLK low-level input	-0.3	0.8	V	
V_{OH}	High-level output voltage	3.0		V	I_{OH} = 1mA
V_{OL}	Low-level-output voltage		0.45	V	I_{OL} = 4mA
I_{LI}	Input leakage current		±15	µA	
I_{LO}	Output leakage current		±15		
C_{IN}	Input capacitance		10	pF	fc = 1MHz
C_O	Input/output capacitance		12		
C_{CLK}	CLK capacitance		20	pF	fc = 1MHz

MCLK Timing



Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	6		ns
MCLK pulse width low	T_{MCL}	6		ns
MCLK cycle time	T_{MCY}	13		ns
MCLK duty cycle		45:55	55:45	

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	20		ns
DATA_CLK pulse width low	t_{DCL}	20		ns
DATA_CLK cycle time	t_{DCY}	44		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	2		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

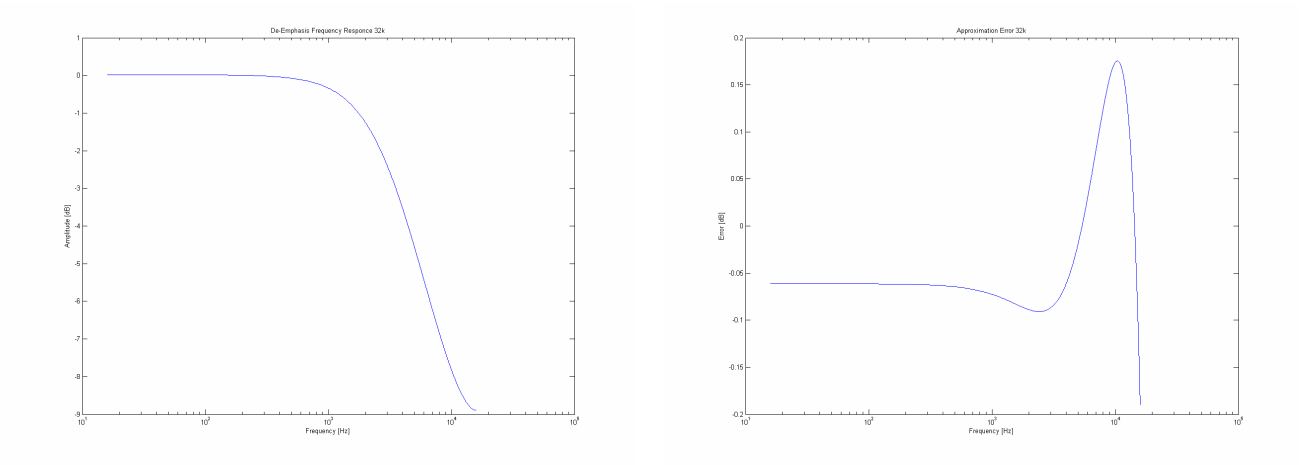
ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

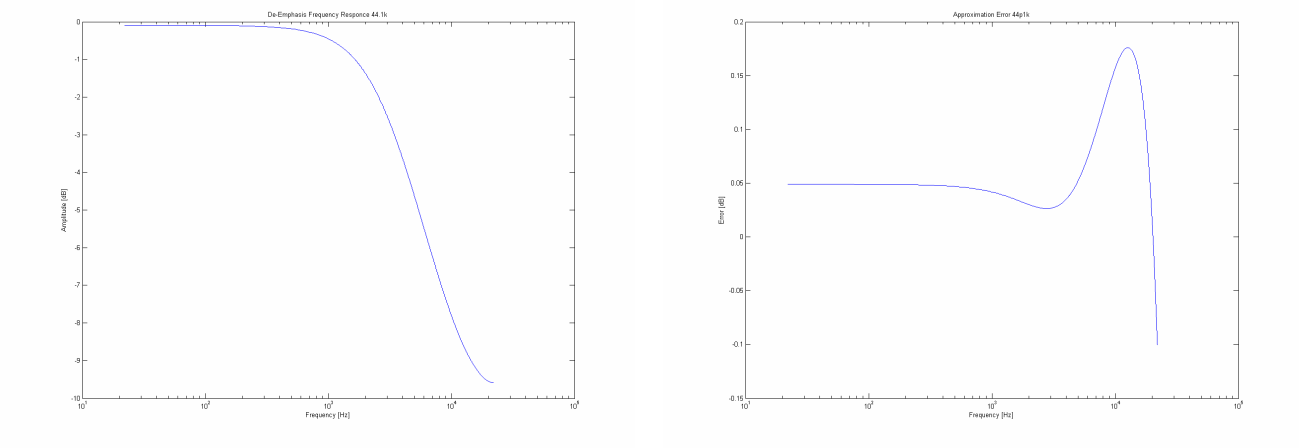
1. T_A=25°C, AVCC=3.3V, DVCC=1.2V, fs =44.1kHz, MCLK=27Mhz and 24-bit data
2. SNR/DNR: A-weighted over 20-20kHz in averaging mode
3. THD+N: un-weighted over 20-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				24		Bits
MLCK				>192		Fs
DYNAMIC PERFORMANCE						
DNR (mono differential current mode)		-60dBFS		134		dB-A
DNR (stereo differential current mode)		-60dBFS		132		dB-A
DNR (8-ch differential current mode)		-60dBFS		128		dB-A
DNR (8-ch differential voltage mode)		-60dBFS		120		dB-A
THD+N (differential current mode)		0dBFS		-118		dB
THD+N (differential voltage mode)		0dBFS		-108		dB
PCM sampling frequency					200	kHz
Level Linearity Error		-115dBFS		±0.3		dB
ANALOG OUTPUT						
Differential current output range		Full-scale out		4.224		mA pp
Differential current output offset		Bipolar zero out to virtual ground at voltage Vg (V)		2.112 – 1.28*Vg		mA
Differential voltage output range		Full-scale out		3.3		V pp
Differential voltage output offset		Bipolar zero out		1.65		V
Digital Filter Performance						
De-emphasis error					±0.2	dB
Mute Attenuation				127		dB
PCM Filter Characteristics (Sharp Roll Off)						
Pass band		±0.05dB			0.454	fs
		-3dB			0.49	fs
Stop band		< -115dB	0.546			dB
Group Delay				256/fs		s
PCM Filter Characteristics (Slow Roll Off)						
Pass band		±0.05dB			0.308	fs
		-3dB			0.454	fs
Stop band		< -100dB	0.814			dB
Group Delay				39/fs		s
DSD Filter Characteristics						
Pass band		-3dB		50/60/70		kHz
Stop band attenuation				18		dB/oct

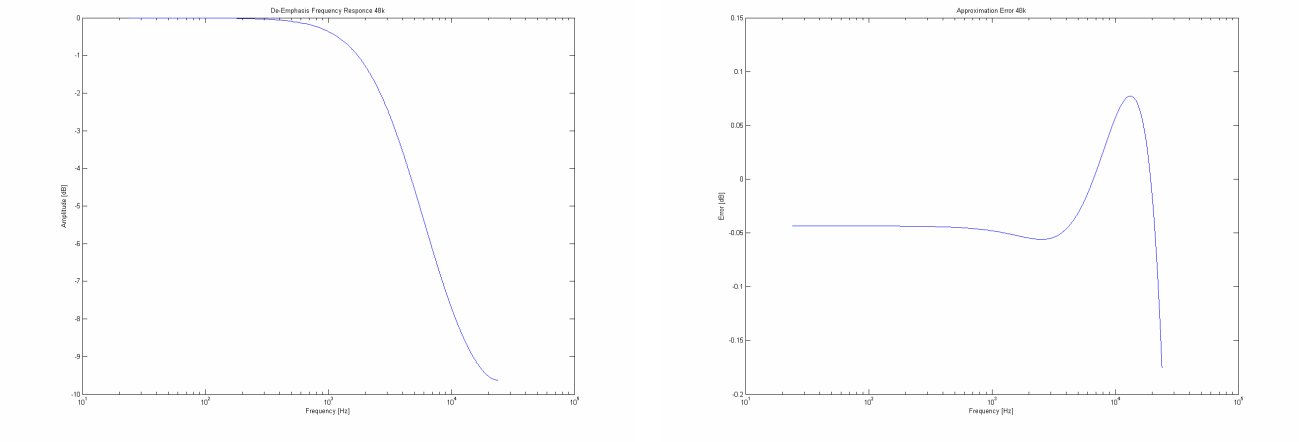
PCM DE-EMPHASIS FILTER RESPONSE (32kHz)



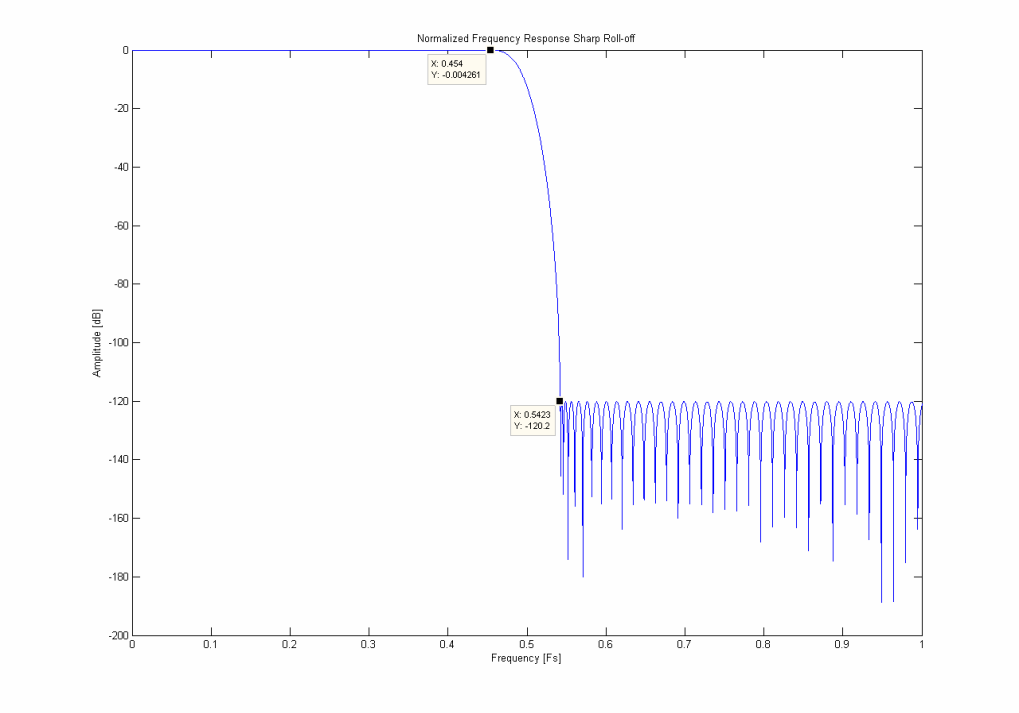
PCM DE-EMPHASIS FILTER RESPONSE (44.1kHz)



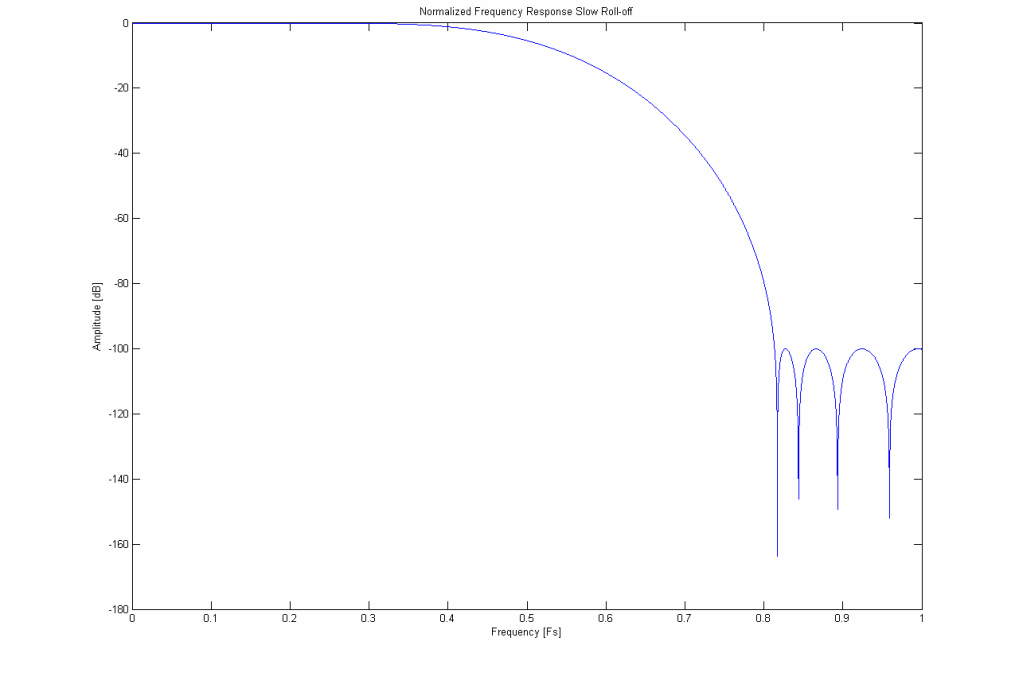
PCM DE-EMPHASIS FILTER RESPONSE (48kHz)



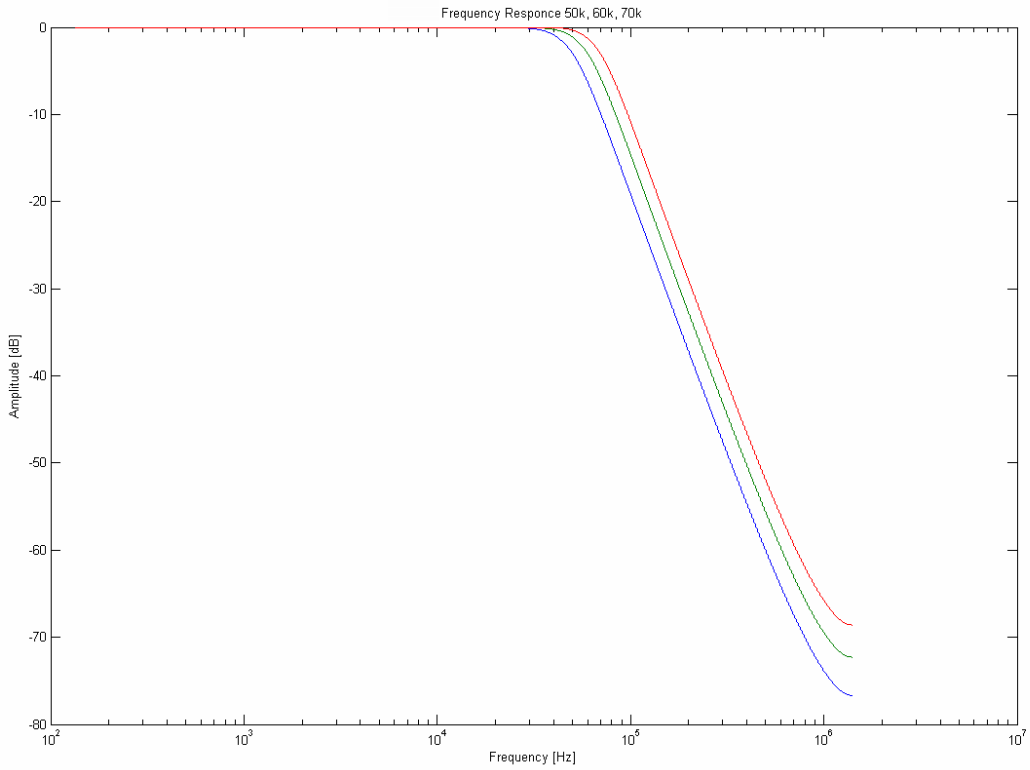
PCM SHARP ROLL-OFF FILTER RESPONSE



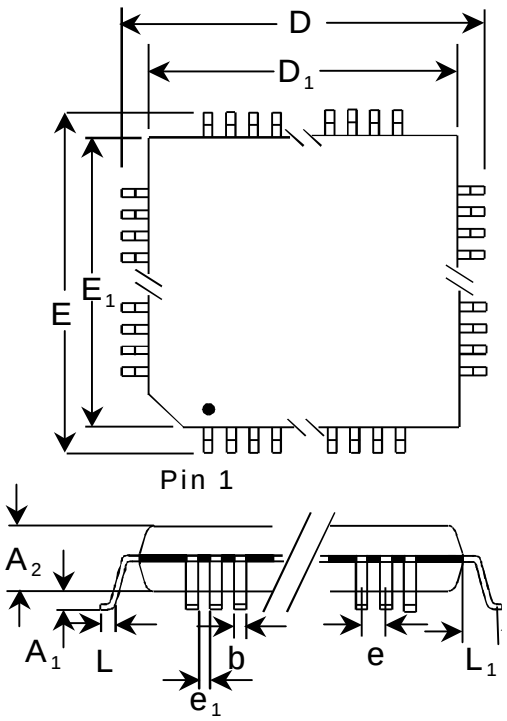
PCM SLOW ROLL-OFF FILTER RESPONSE



DSD FILTER RESPONSE



64 Pin LQFP Mechanical Dimensions



		MILLIMETERS		
Symbol	**Description**	**Min.**	**Nom.**	**Max.**
D	Lead-to Lead, X-axis	11.75	12.00	12.25
D1	Package's Outside, X-axis	9.90	10.00	10.10
E	Lead-to Lead, Y-axis	11.75	12.00	12.25
E1	Package's Outside, Y-axis	9.90	10.00	10.10
A1	Board Standoff	0.05	0.10	0.15
A2	Package Thickness	1.35	1.40	1.45
b	Lead Width	0.17	0.22	0.27
e	Lead Pitch		0.50 BSC	
e_1	Lead Gap	0.23	0.28	0.33
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
	Coplanarity			0.102
	Foot Angle	0º		7º
	No. of Leads in X-axis		16	
	No. of Leads in Y-axis		16	
	No. of Leads Total		64	
	Package Type		LQFP	

ORDERING INFORMATION

Part Number	Description	Package
ES9008S	Sabre Reference 8-channel Audio DAC	64-pin LQFP

The letter S at the end of the part number identifies the package type LQFP.

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