

2-Channel Audio Processor IC**PT2315**

DESCRIPTION

PT2315 is a two-channel digital audio processor utilizing CMOS Technology. Volume, Bass, Treble and Balance Controls are incorporated into a single chip. Loudness Function is also provided to build a highly effective electronic audio processor having the highest performance and reliability with the least external components. All functions are programmable using the I²C Bus. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage for audio application. Housed in a 20-pin DIP/SO Package, PT2315 is pin-to-pin compatible with TDA7315 and is very similar in performance with the later.

FEATURES

- CMOS Technology
- Least External Components
- Treble and Bass Control
- Loudness Function
- Input/Output for External Noise Reduction System/Equalizer
- 2 Independent Speaker Controls for Balance Function
- Independent Mute Function
- Volume Control in 1.25 dB/step
- Low Distortion
- Low Noise and DC Stepping
- Controlled by I²C Bus Micro-Processor Interface
- Pin-to-pin Compatible with TDA7315

APPLICATIONS

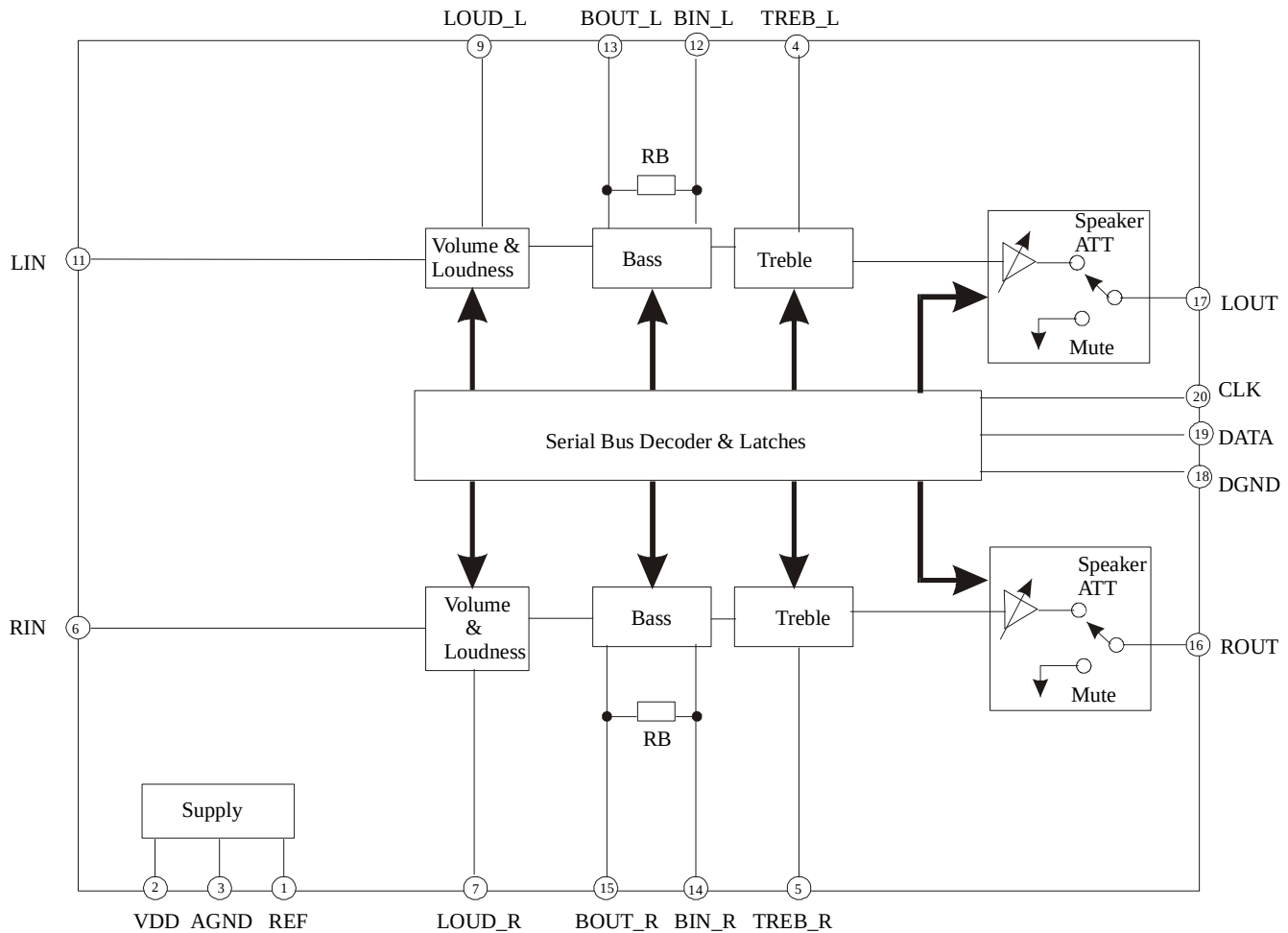
- Car Stereo (Audio)
- Hi-Fi Audio System
- Can be used in all I²C System Applications

Note: Purchase of I2C Component of Princeton Technology Corporation (PTC) conveys a license under Philips I2C Patent Right to use these components in any I2C System, provided that the system conforms to the I2C Standard Specification defined by Philips

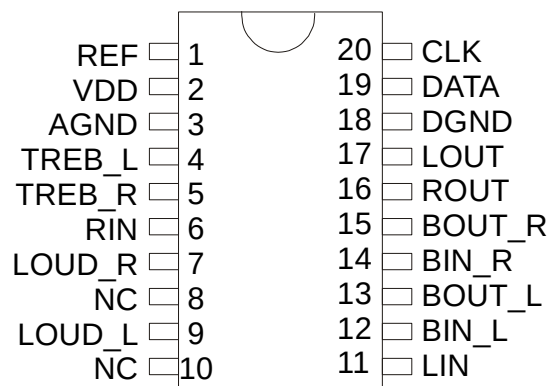
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BLOCK DIAGRAM



PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
REF	-	Analog Reference Voltage (1/2 VDD)	1
VDD	-	Supply Input Voltage	2
AGND	-	Analog Ground	3
TREB_L	I	Left Channel Input for Treble Controller	4
TREB_R	I	Right Channel Input for Treble Controller	5
RIN	I	Audio Processor Right Channel Input	6
LOUD_R	I	Right Channel Loudness Input	7
LOUD_L	I	Left Channel Loudness Input	9
LIN	I	Audio Processor Left Channel Input	11
BIN_L	I	Left Bass Controller Input Channel	12
BOUT_L	O	Left Bass Controller Output Channel	13
BIN_R	I	Right Bass Controller Input Channel	14
BOUT_R	O	Right Bass Controller Output Channel	15
ROUT	O	Right Speaker Output	16
LOUT	O	Left Speaker Output	17
DGND	-	Digital Ground	18
DATA	I	Control Data Input	19
CLK	I	Clock Input for Serial Data Transmission	20
NC	-	No Connection	8, 10

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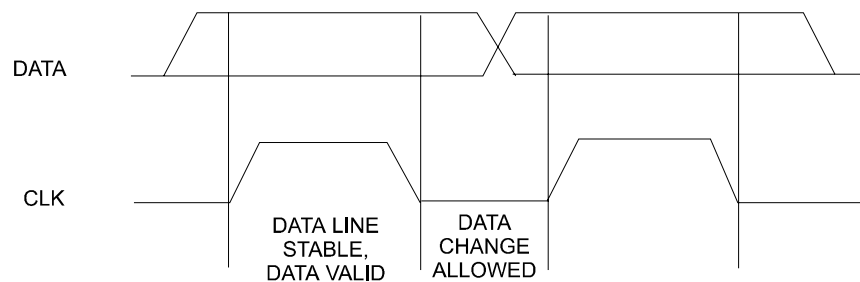
FUNCTIONAL DESCRIPTION

I²C BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2315 via the DATA and CLK. The DATA and CLK make up the BUS Interface

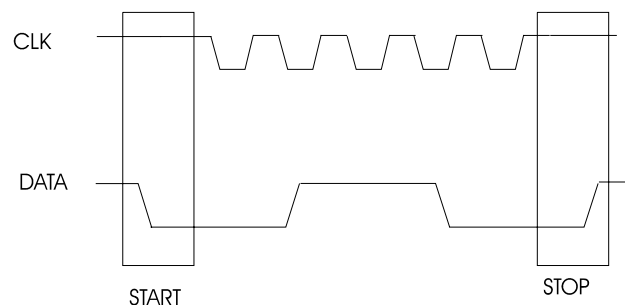
DATA VALIDITY

A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW State of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

A Start Condition is activated when 1) the CLK is set to HIGH and 2) DATA shifts from HIGH to LOW State. The Stop Condition is activated when 1) CLK is set to HIGH and 2) DATA shifts from LOW to HIGH State. Please refer to the timing diagram below.



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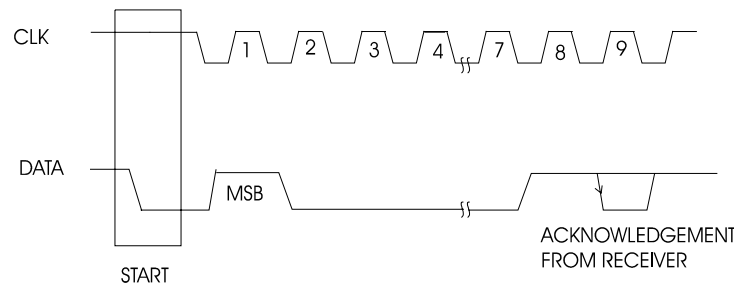
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BYTE FORMAT

Every byte transmitted to the DATA Line consist of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μ P) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μ P transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

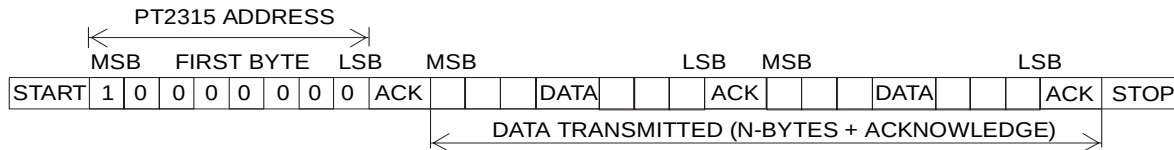
The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the PT2315 address. The 8th Bit of the Byte must be "0". PT2315 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

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Please refer to the diagram below:



Note: ACK= ACKNOWLEDGE
MAX. CLOCK SPEED = 100KBITS/S

SOFTWARE SPECIFICATION

PT2315 ADDRESS

PT2315 Address is shown below.

1 MSB	0	0	0	0	0	0	0 LSB
----------	---	---	---	---	---	---	----------

DATA BYTES

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	*	*	L	*	*	Loudness Control
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

where Ax = 1.25 dB steps; Bx = 10 dB steps; Cx = 2 dB steps; * = no effect

VOLUME

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5 dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25 dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75

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					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker L (Left) is given by: 1 0 0 1 1 0 0 0.

MSB							LSB	FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker L
1	0	1	B1	B0	A2	A1	A0	Speaker R
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

LOUDNESS FUNCTION

The following table shows the detailed description of the Loudness Function. For example, when the Loudness Function is turned ON, the code format is -- 0 1 0 0 0 0 0 0

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MSB							LSB	FUNCTION
0	1	0	*	*	L	*	*	Loudness Control
					0			Loudness ON
					1			Loudness OFF

Note: *=No Effect

BASS AND TREBLE DATA BYTES

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by : 0 1 1 1 0 0 0 1.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit: dB

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
Vs	Operating Supply Voltage	10.5	V
Tamb	Operating Ambient Temperature	-20 to 75	oC
Tstg	Storage Temperature Range	-40 to +125	oC

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs	Supply Voltage	6	9	10	V
VCL	Max. Input Signal Handling	2	2.5		Vrms
THD	Total harmonic Distortion (V = 1Vrms, f = 1KHz)		0.07	0.15	%
S/N	Signal to Noise ratio		95		dB
Sc	Channel Separation (f = 1KHz)		85		dB
	Volume Control 1.25dB step	-75		0	dB
	Bass & Treble Control 2dB step	-14		+14	dB
	Balance Control 1.25dB step	-37.5		0	dB
	Mute Attenuation		75		dB

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ELECTRICAL CHARACTERISTICS

(Unless specified: Tamb = 25°C, Vc=9V, RL=100KΩ, Rg = 600Ω, all controls flat (G=0), f=1KHz)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply						
Vcc	Supply Voltage		6	9	10	V
Is	Supply Current			30	40	mA
Volume Control						
RIV	Input Resistance		20	30	40	KOhm s
CRANGE	Control Range		65	70	75	dB
AVMIN	Min. Attenuation		-1	0	1	dB
AVMAX	Max. Attenuation		65	70	75	dB
ASTEP	Step Resolution		0.5	1.25	1.75	dB
EA	Attenuation Set Error	AV=0 to -20dB AV=-20 to -60dB	-1.25 -3.0	0	1.25 2	dB dB
Speaker Attenuators						
CRANGE	Control Range		35	37.5	40	dB
SSTEP	Step Resolution		0.5	1.25	1.75	dB
EA	Attenuation Set Error				1.5	dB
AMUTE	Output Mute Attenuation		70	75		dB
Bass Control (1)						
Gb	Control Range	Max. Boost/Cut	+ 12	+ 14	+ 16	dB
BSTEP	Step Resolution		1	2	3	dB
RB	Internal Feedback Resistance		34	44	58	KOhm s
Treble Control (1)						
Gt	Control Range	Max. Boost/Cut	+ 13	+ 14	+ 15	dB
TSTEP	Step Resolution		1	2	3	dB
Audio Outputs						

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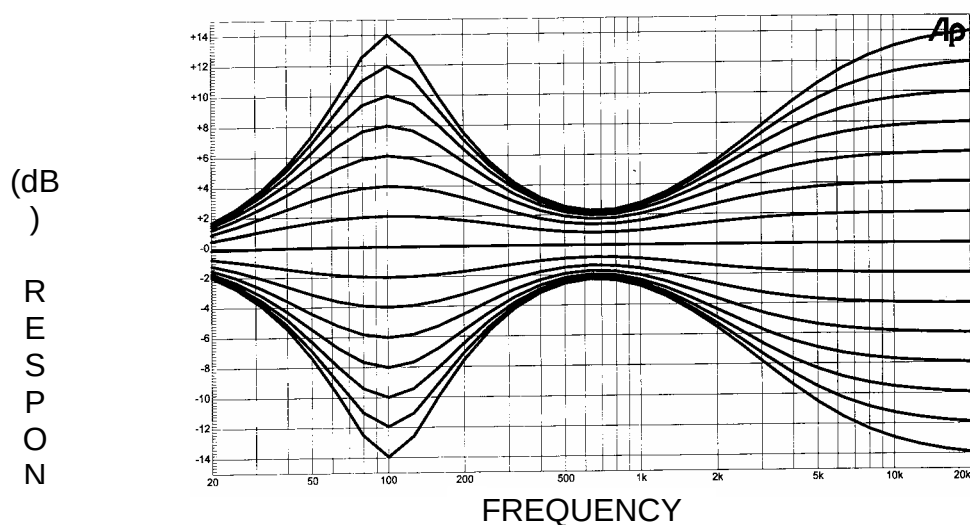
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Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOCL	Clipping Level	d=0.3%	2	2.5		Vrms
ROUT	Output Resistance		-	40	45	Ohms
VOUT	DC Voltage Level		4.2	4.5	4.8	V
General						
eNO	Output Noise	BW==20-20KHz, flat Output Muted All gains=0dB		-97 -92		dB dB
		A Curve All Gains=0dB		-100		dB
S/N	Signal to Noise Ratio	All Gains=0dB Vo=1Vrms		95		dB
d	Distortion	AV=0, VIN=1Vrms AV=-8.75dB, VIN=1Vrms AV=-8.75dB, VIN=0.3Vrms		0.1 0.07 0.03	0.3 0.15 0.1	% % %
Sc	Channel Separation Left/Right		80	90		dB
Bus Inputs						
VIL	Input Low Voltage				1	V
VIH	Input High Voltage		3			V
IIN	Input Current		-5		+5	uA
Vo	Output Voltage SDA Acknowledge	Io=1.6mA			0.4	V

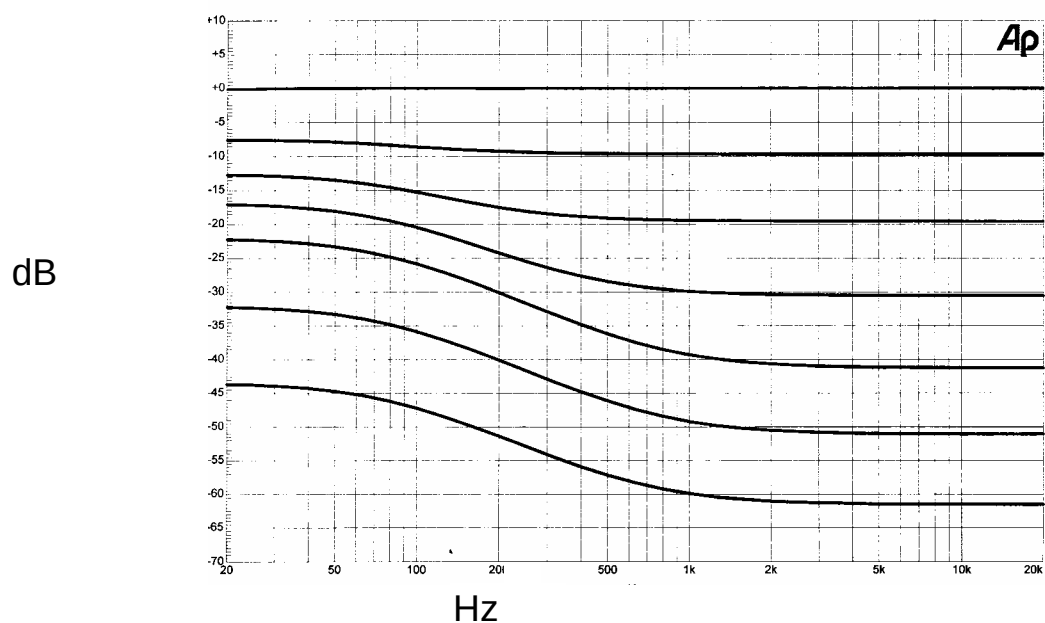
Note: (1) For the Bass and Treble Response, please refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.

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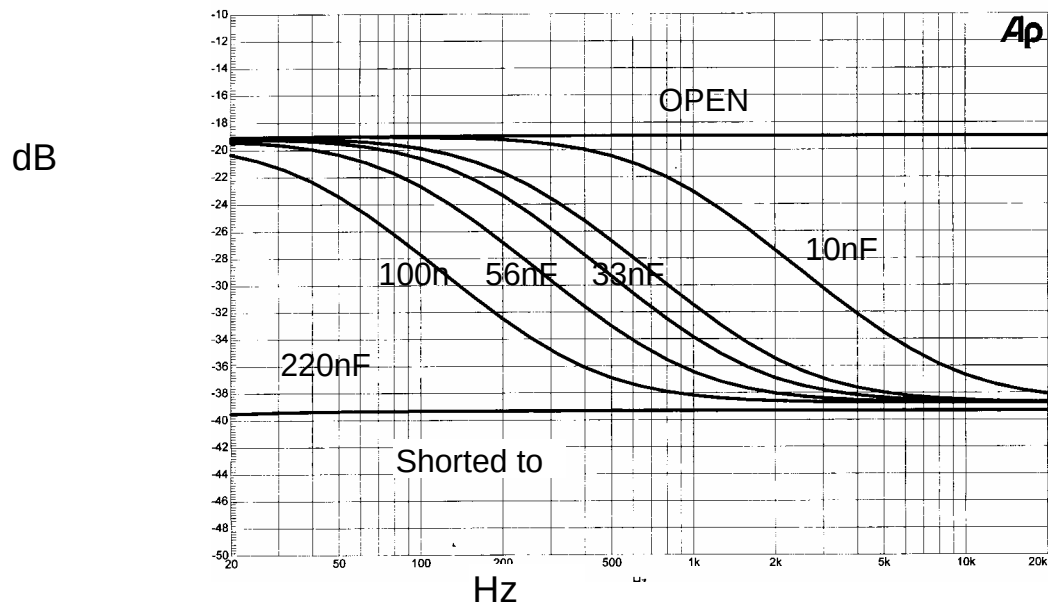
Typical Tone Response (with the ext. Components indicated in the test circuit)



PT2315: Loudness vs Volume Attenuation Frequency Response ($C_{10}=C_{11}=100\text{nF}$)

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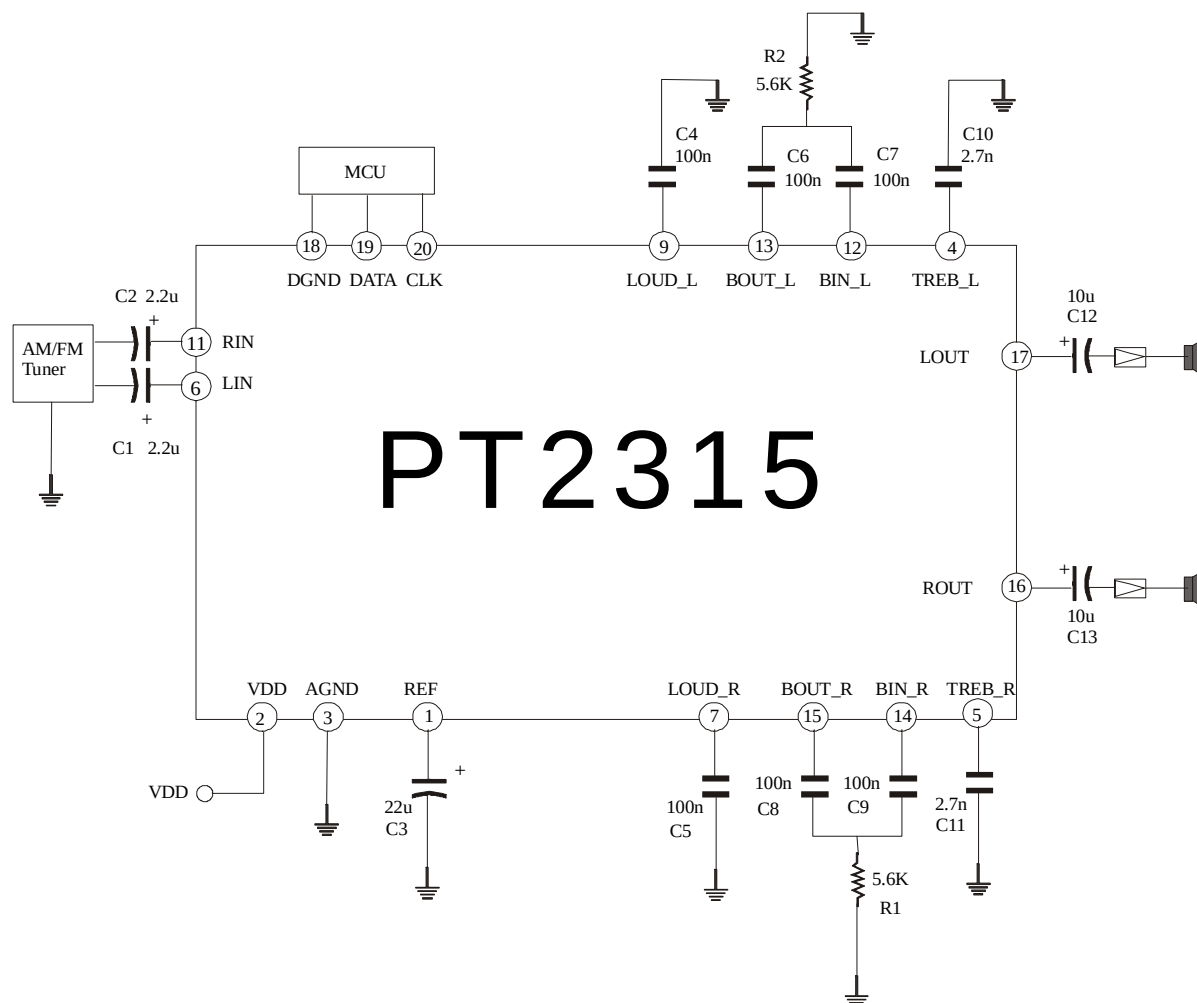


PT2315 : C₁₀, C₁₁ vs Loudness Frequency Response (Volume=-40dB, All other controls are flat)

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APPLICATION CIRCUIT



ORDER INFORMATION

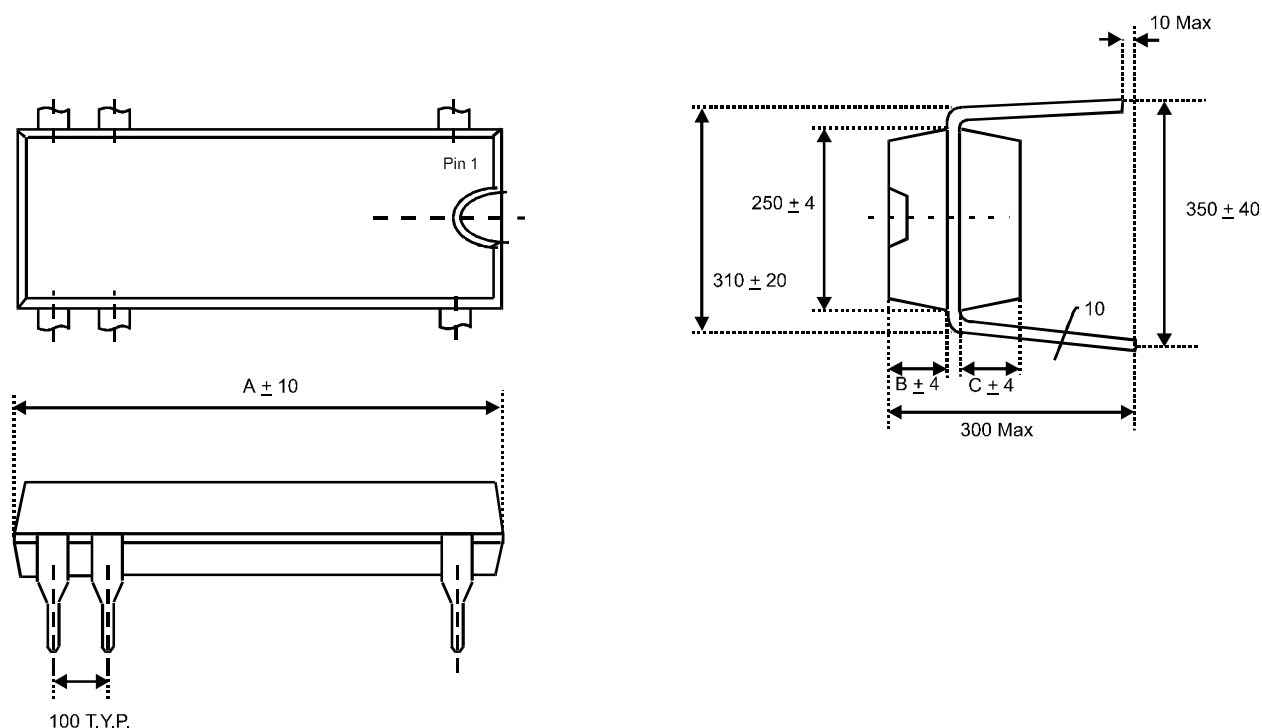
Valid Part Number	Package Type
PT2315-D	20 Pins, DIP (300 mil)
PT2315	20 Pins, SO (300 mil)

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PACKAGE INFORMATION

20 PINS, DIP PACKAGE

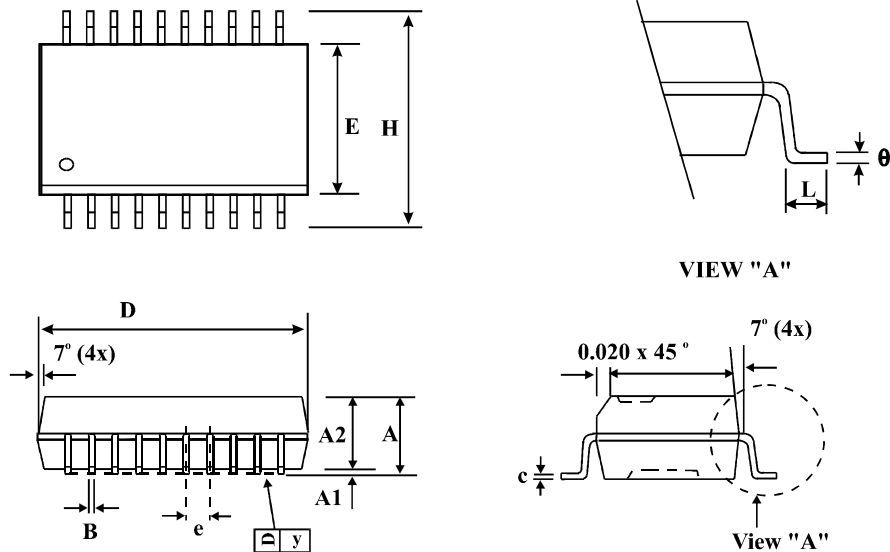


Symbol	Dimensions In Millimeters
A	1020
B	60
C	60

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20 PINS, SO PACKAGE (300 MIL)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	-	2.31	-	-	0.091	-
B	.033	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	12.60	12.80	12.90	0.496	0.504	0.508
E	7.39	7.49	7.59	0.291	0.295	0.299
e	-	1.27	-	-	0.050	-
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	0	8°

Note:

1. Controlling Dimension : Inch
2. Lead Frame Material : Copper 194
3. After solder plating lead thickness will be 0.015" max.
4. Dimension "D" does not include mold flash, protrusions or gate burrs.
5. Dimension "E" does not include interlead flash or protrusions.
6. Tolerance : ± 0.010 " unless otherwise specified.
7. Otherwise dimensions follow acceptable spec.