Laurel Electronics Co., Ltd.

OLED Module Specification

Model No.: LEC2041-W56

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RECORD OF REVISION

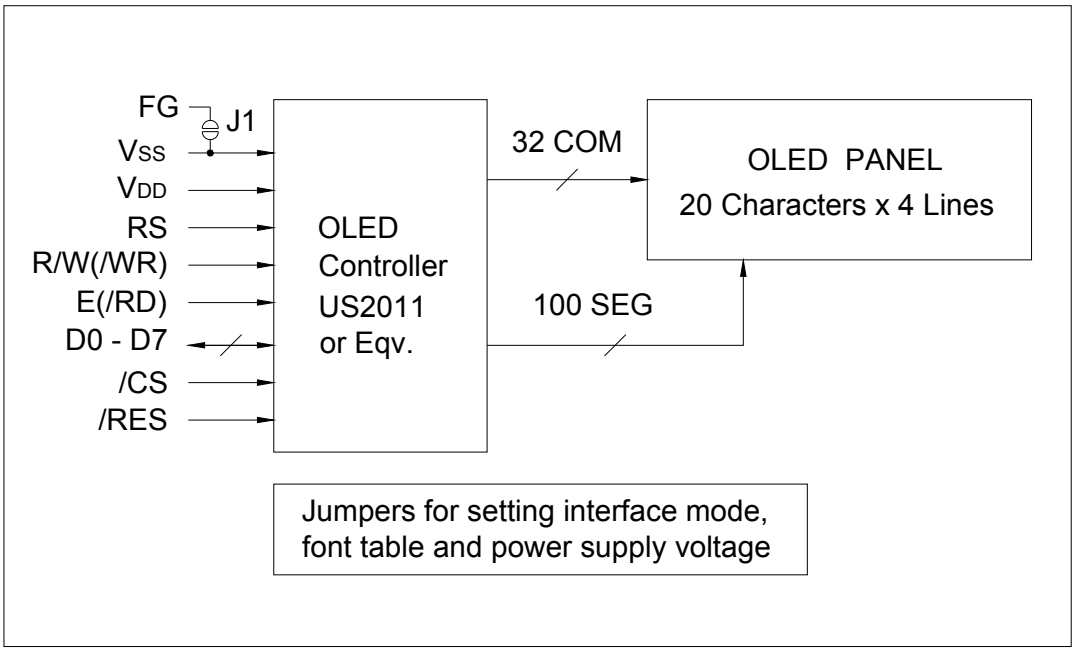
Rev.	Date	Page	Item	Description
0.1	2019/09/03	-	-	New release

1. BASIC SPECIFICATIONS

1.1 Features

Item	Specifications	Unit
Screen Size	2.89 (Diagonal)	inch
Display Format	20 Characters x 4 Lines	-
OLED Type	Passive matrix	-
Display Color	White characters on black background	-
Driving Method	1/32 duty	-
Viewing Direction	Free	-
Outline Dimension (WxHxT)	98.0 x 60.0 x 9.5	mm
Viewing Area (WxH)	73.0 x 24.0	mm
Active Area (WxH)	70.42 x 20.82	mm
Character Size (WxH)	2.97 x 4.77	mm
Dot Size (WxH)	0.57 x 0.57	mm
Weight	38	g
Controller	US2011	-
Font Table	English, Western European, Russian and Japanese	-
Interface	4/8-bit parallel (8080 or 6800), 3/4-wire SPI or I^2C	-
Power Supply (V_{DD})	3.3 to 5.5	V

1.2 Block Diagram



1.3 CN1/CN2 Terminal Functions (4/8-bit 6800 MPU interface)

Pin No.	Symbol	Level	Function
1	VSS	0V	Ground (connects to frame ground via jumper J1)
2	VDD	3.3V to 5.5V	Power supply. Refer to section 1.7 and section 3.2
3	NC	-	No connection
4	RS	H/L	Data or command selection RS="H": Display data; RS="L": Command code
5	R/W	H/L	Read or write selection R/W="H": Read operation; R/W="L": Write operation
6	E	H, H→L	Enable signal. In read mode (R/W="H"), data appears at D0 to D7 when E is "H". In write mode (R/W="L"), data of D0 to D7 is latched at the falling edge of E.
7	D0	H/L	In 8-bit mode, used as low order bi-directional data bus. In 4-bit mode, open these terminals or pull them to VDD.
8	D1	H/L	
9	D2	H/L	
10	D3	H/L	
11	D4	H/L	In 8-bit mode, used as high order bi-directional data bus. In 4-bit mode, used as both high and low order data bus.
12	D5	H/L	
13	D6	H/L	
14	D7	H/L	
15 to 16	NC	-	No connection

1.4 CN1/CN2 Terminal Functions (4/8-bit 8080 MPU interface)

Pin No.	Symbol	Level	Function
1	VSS	0V	Ground (connects to frame ground via jumper J1)
2	VDD	3.3V to 5.5V	Power supply. Refer to section 1.7 and section 3.2
3	NC	-	No connection
4	RS	H/L	Data or command selection RS="H": Display data; RS="L": Command code
5	/WR	L	Write signal. Data is latched at the rising edge of /WR.
6	/RD	L	Read signal. Data appears at D0 to D7 when /RD is "L".
7	D0	H/L	In 8-bit mode, used as low order bi-directional data bus. In 4-bit mode, open these terminals or pull them to VDD.
8	D1	H/L	
9	D2	H/L	
10	D3	H/L	
11	D4	H/L	In 8-bit mode, used as high order bi-directional data bus. In 4-bit mode, used as both high and low order data bus.
12	D5	H/L	
13	D6	H/L	
14	D7	H/L	
15	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
16	/CS	L	Chip selection signal. Chip is enabled when /CS is "L".

1.5 CN1/CN2 Terminal Functions (3/4-wire SPI interface)

Pin No.	Symbol	Level	Function
1	VSS	0V	Ground (connects to frame ground via jumper J1)
2	VDD	3.3V to 5.5V	Power supply. Refer to section 1.7 and section 3.2
3	NC	-	No connection
4	RS	H/L	In 4-wire SPI mode, RS is data or command selection. RS="H": Display data; RS="L": Command code In 3-wire SPI mode, RS is not used. Connect it to VSS.
5	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
6	/CS	L	Chip selection signal. Chip is enabled when /CS is "L".
7	SCL	L→H	Serial clock input. Data is shifted at the rising edge of SCL.
8	SI	H/L	Serial data input
9 to 14	NC	-	Keep these terminals open or connect them to VDD or VSS
15 to 16	NC	-	No connection

Note: 3/4-wire SPI interface mode supports write operation only; read operation is not supported.

1.6 CN1/CN2 Terminal Functions (I^2C interface)

Pin No.	Symbol	Level	Function
1	VSS	0V	Ground (connects to frame ground via jumper J1)
2	VDD	3.3V to 5.5V	Power supply. Refer to section 1.7 and section 3.2
3	NC	-	No connection
4	SA0	H/L	Slave address
5	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
6	NC	-	No connection
7	SCL	H/L	I^2C bus serial clock input
8	SDA	H/L	I^2C bus serial data input/output
9 to 14	NC	-	Keep these terminals open or connect them to VDD or VSS
15 to 16	NC	-	No connection

1.7 Set Power Supply Voltage VDD by on Board Jumper

This OLED module supports 3.3V to 5.5V power supply. The relationship of JV1 jumper status, V1_OPT level and power supply voltage VDD is below.

JV1 Jumper Status	V1_OPT Level	VDD Voltage
Open	1	**3.5V to 5.5V <Default>**
Close	0	3.3V to 3.5V

1.8 Set Interface Bus Mode by on Board Jumpers

The interface bus mode is determined by terminals IM[2:0]. The relationship of the jumper status, IM[2:0] level and interface bus mode is below.

Jumper Status (C=Close; O=Open)										IM[2:0] Level	Interface Bus Mode
JIM2	JIM1	JIM0	JRW	JE	JCSG	JRES	JCS	J15	J16		
O	O	O	C	C	C	O	O	O	O	0 0 0	**8-bit 6800 <Default>**
O	O	C	C	C	O	O	O	C	C	0 0 1	8-bit 8080
O	C	O	O	O	O	C	C	O	O	0 1 0	4-wire SPI
O	C	C	O	O	C	C	O	O	O	0 1 1	I^2C
C	O	O	C	C	C	O	O	O	O	1 0 0	4-bit 6800
C	O	C	C	C	O	O	O	C	C	1 0 1	4-bit 8080
C	C	O	O	O	O	C	C	O	O	1 1 0	3-wire SPI
C	C	C	O	O	C	C	O	O	O	1 1 1	I^2C

1.9 Set Font Table by on Board Jumpers

There are total four sets of font tables built in the OLED controller. The font table is selected by terminals FT[1:0]. The relationship of the jumper status, FT[1:0] level and font table is below.

Jumper Status (C=Close; O=Open)		FT[1:0] Level	Font Table
JFT1	JFT0		
O	O	0 0	**English Japanese <Default>**
O	C	0 1	Western European - I
C	O	1 0	English Russian
C	C	1 1	Western European - II

Note: If the software font table set function is enabled, the font table is selected by register option FTS[1:0]. At the same time, the font table selected by terminals FT[1:0] is invalid.

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	-0.3	5.6	V
Input Voltage	V_I	-0.3	V_{DD} + 0.3	V
Operating Temperature	Topr	-40	80	°C
Storage Temperature	Tstg	-40	80	°C

Cautions: Stresses above those listed as ‘absolute maximum ratings’ may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. OPTICAL & ELECTRICAL CHARACTERISTICS

3.1 Optical Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Brightness Note 1	Lbr		30	40	-	cd/m^2
Color Chromaticity (White)	CIEx	CIE 1931	0.25	0.29	0.33	
	CIEy	CIE 1931	0.27	0.31	0.35	
Contrast Ratio	Cr	Dark Room	10,000:1	-	-	
Life Time Note 2		40 cd/m^2	80,000	-	-	hour
		30 cd/m^2	10,000	-	-	hour

Note:

1. VDD = 5.0V, 100% display area turned on, the contrast data register value = 80H.
   Brightness is related to VDD. The brightness will be lower if used with lower VDD voltages.
2. The life time is defined as the brightness decreases to 50% initial brightness at Ta=25°C, 50% checkerboard. The life time at Ta=25°C is estimated at accelerated operation at high temperature conditions. Luminance of the active pixels will degrade faster than the inactive pixels. Using a screen saver or the Display OFF command can extend the life time of the OLED.

3.2 DC Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	Jumper JV1 Open (Default)	3.5	5.0	5.5	V
		Jumper JV1 Close	3.3	-	3.5	V
OLED Driving Voltage	VPP	Note 7	-	12.0	12.5	V
Input High Voltage	VIH		0.7VDD	-	VDD	V
Input Low Voltage	VIL		0	-	0.3VDD	V
Output High Voltage	VOH	IOH = -0.5mA	0.7VDD	-	VDD	V
Output Low Voltage	VOL	IOH = 0.5mA	0	-	0.3VDD	V
Supply Current	IDD	VDD = 5.0V Note 1	-	27.0	34.0	mA
		VDD = 5.0V Note 2	-	42.0	52.0	mA
		VDD = 5.0V Note 3	-	65.0	82.0	mA
		VDD = 3.3V Note 4	-	25.0	32.0	mA
		VDD = 3.3V Note 5	-	35.0	44.0	mA
		VDD = 3.3V Note 6	-	47.0	60.0	mA

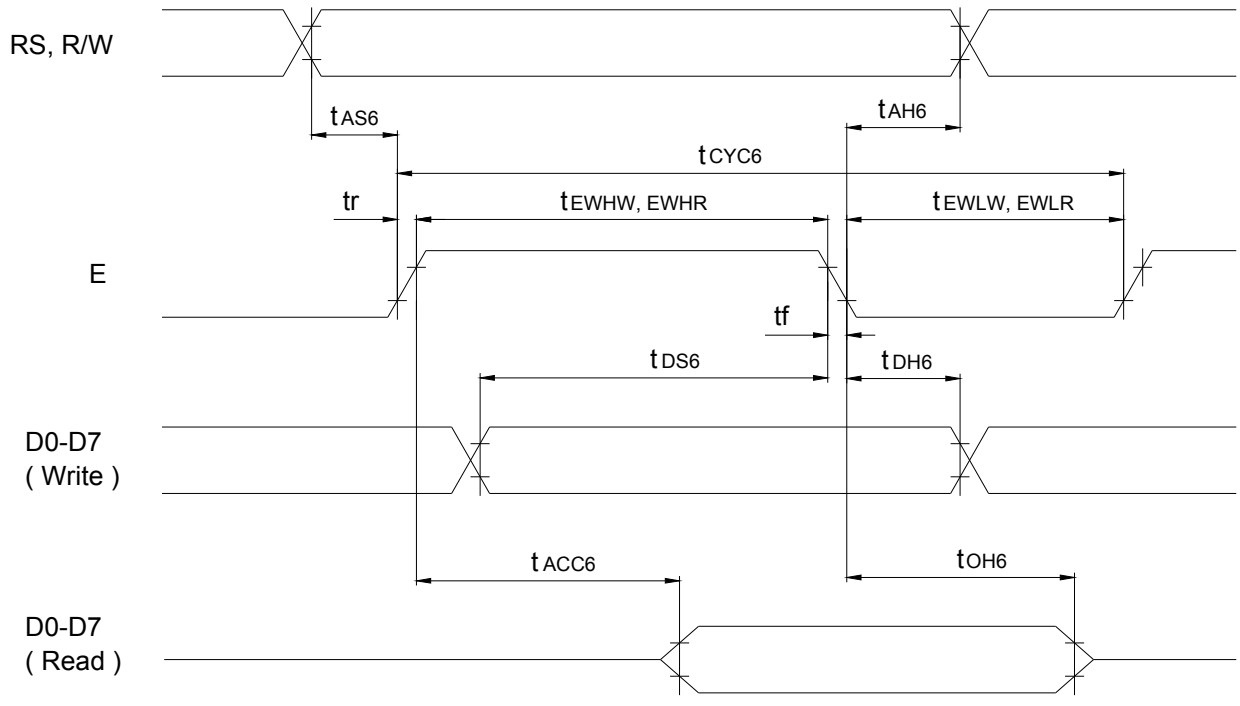
Note:

1. 30% display area turned on, the contrast register value = 80H
2. 50% display area turned on, the contrast register value = 80H
3. 100% display area turned on, the contrast register value = 80H
4. 30% display area turned on, the contrast register value = CFH
5. 50% display area turned on, the contrast register value = CFH
6. 100% display area turned on, the contrast register value = CFH
7. VPP voltage changes with the supply voltage VDD and OLED brightness

3.3 4/8-bit 6800 MPU Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

Item	Symbol	Min.	Max.	Unit
System Cycle Time	t_{CYC6}	500	-	ns
Address Setup Time	t_{AS6}	0	-	ns
Address Hold Time	t_{AH6}	0	-	ns
Data Setup Time	t_{DS6}	66	-	ns
Data Hold Time	t_{DH6}	25	-	ns
Data Output Disable Time (C_L=100pF)	t_{OH6}	16	140	ns
Data Output Access Time (C_L=100pF)	t_{ACC6}	-	280	ns
Enable High Pulse Width (Write)	t_{EWHW}	166	-	ns
Enable High Pulse Width (Read)	t_{EWHR}	200	-	ns
Enable Low Pulse Width (Write)	t_{EWLW}	166	-	ns
Enable Low Pulse Width (Read)	t_{EWLR}	166	-	ns
Rise Time	t_r	-	25	ns
Fall Time	t_f	-	25	ns

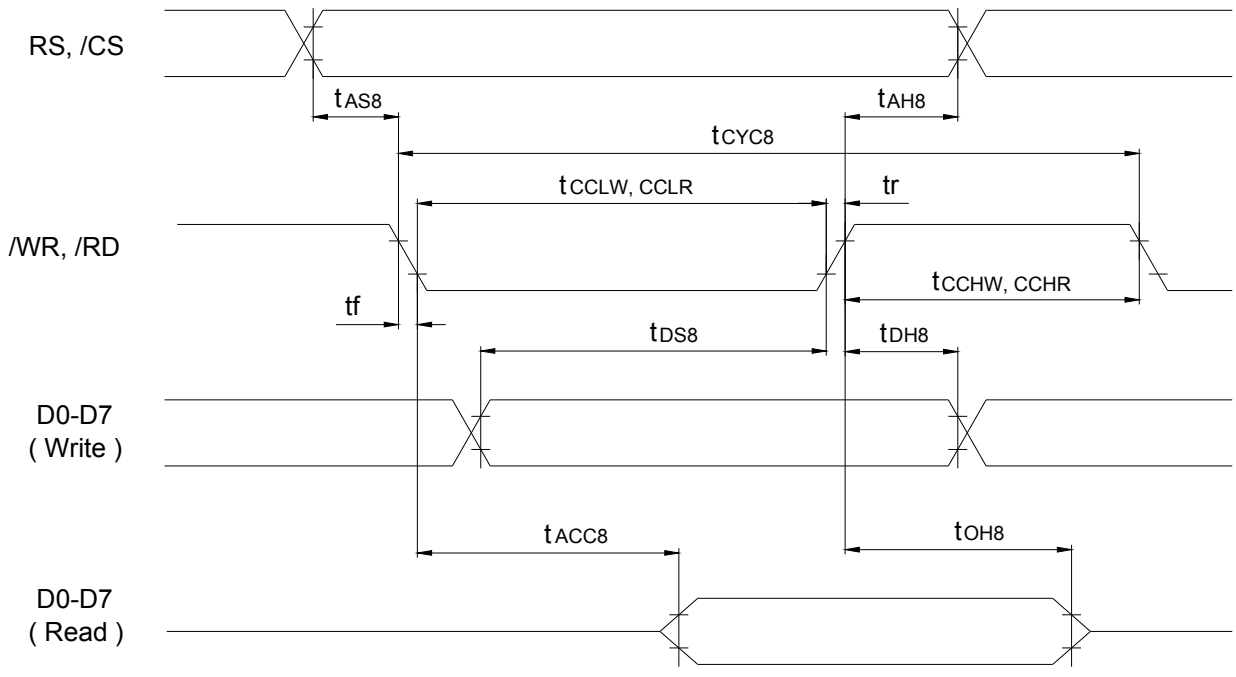
Note: /CS is fixed to Vss by jumper in 6800 MPU Interface mode.



Bus Read/Write Timing (6800 Series MPU)

3.4 4/8-bit 8080 MPU Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

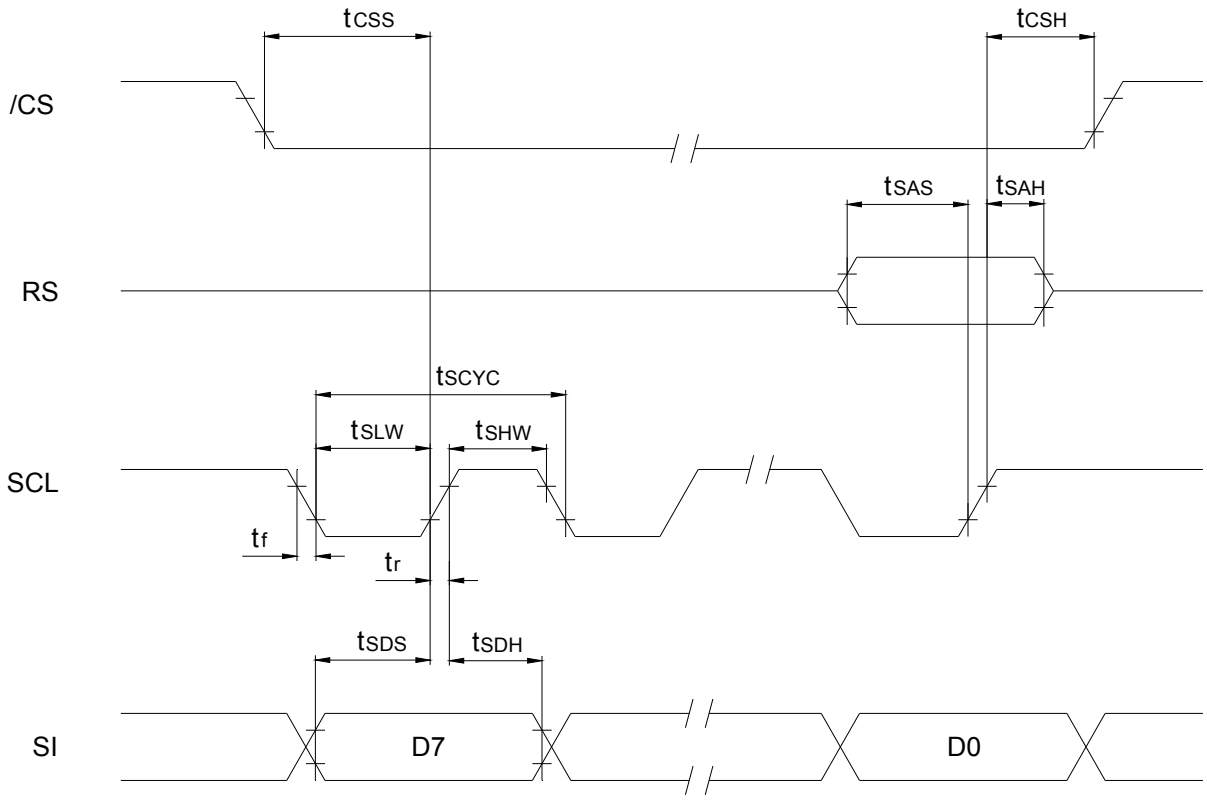
Item	Symbol	Min.	Max.	Unit
System Cycle Time	t_{CYC8}	500	-	ns
Address Setup Time	t_{AS8}	0	-	ns
Address Hold Time	t_{AH8}	0	-	ns
Data Setup Time	t_{DS8}	66	-	ns
Data Hold Time	t_{DH8}	25	-	ns
Data Output Disable Time (C_L=100pF)	t_{OH8}	16	110	ns
Read Access Time (C_L=100pF)	t_{ACC8}	-	230	ns
Write Low Pulse Width	t_{CCLW}	166	-	ns
Read Low Pulse Width	t_{CCLR}	200	-	ns
Write High Pulse Width	t_{CCHW}	166	-	ns
Read High Pulse Width	t_{CCHR}	166	-	ns
Rise Time	t_r	-	25	ns
Fall Time	t_f	-	25	ns



Bus Read/Write Timing (8080 Series MPU)

3.5 4-wire SPI Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

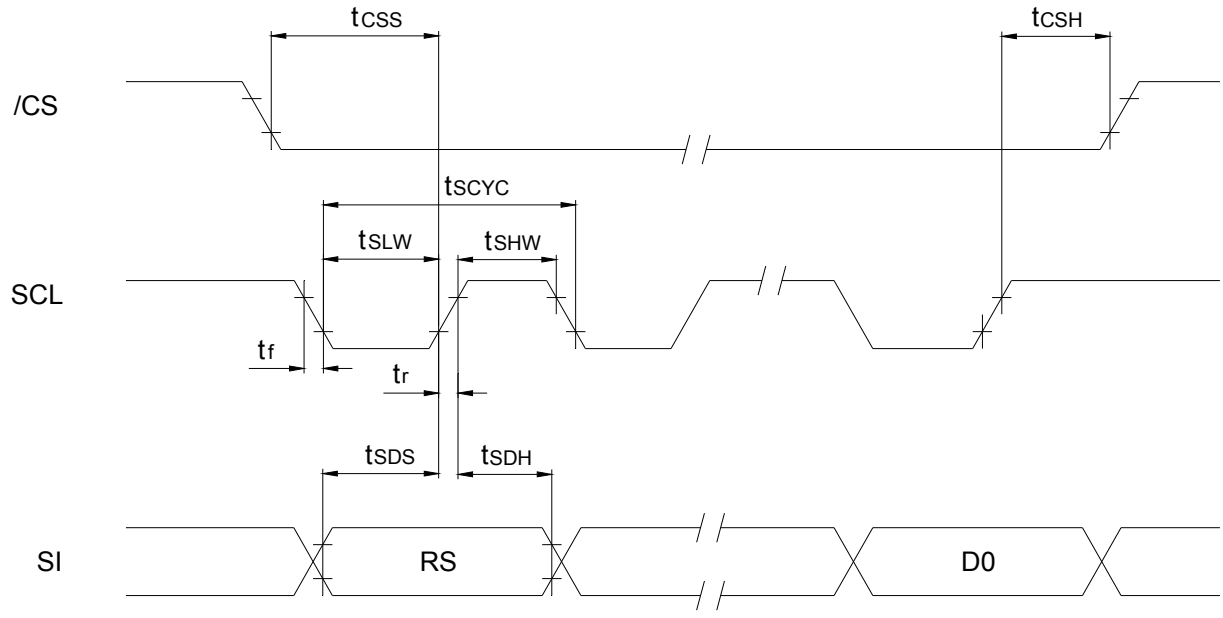
Item	Symbol	Min.	Max.	Unit
Serial Clock Cycle	t_{SCYC}	500	-	ns
Address Setup Time	t_{SAS}	300	-	ns
Address Hold Time	t_{SAH}	300	-	ns
Data Setup Time	t_{SDS}	200	-	ns
Data Hold Time	t_{SDH}	200	-	ns
/CS Setup Time	t_{CSS}	240	-	ns
/CS Hold Time	t_{CSH}	120	-	ns
Serial Clock High Pulse Width	t_{SHW}	200	-	ns
Serial Clock Low Pulse Width	t_{SLW}	200	-	ns
Rise Time	t_r	-	30	ns
Fall Time	t_f	-	30	ns



4-wire SPI Interface Timing

3.6 3-wire SPI Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

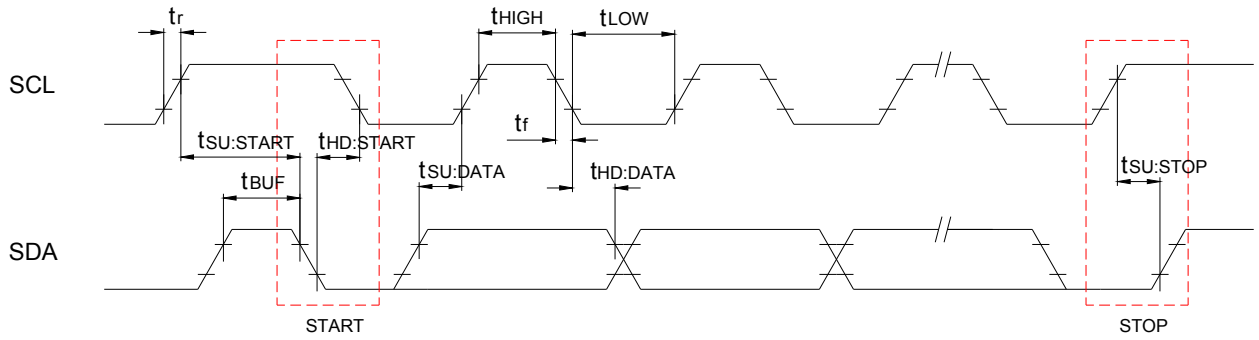
Item	Symbol	Min.	Max.	Unit
Serial Clock Cycle	t_{SCYC}	500	-	ns
Data Setup Time	t_{SDS}	200	-	ns
Data Hold Time	t_{SDH}	200	-	ns
/CS Setup Time	t_{CSS}	240	-	ns
/CS Hold Time	t_{CSH}	120	-	ns
Serial Clock High Pulse Width	t_{SHW}	200	-	ns
Serial Clock Low Pulse Width	t_{SLW}	200	-	ns
Rise Time	t_r	-	30	ns
Fall Time	t_f	-	30	ns



3-wire SPI Interface Timing

3.7 I²C Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

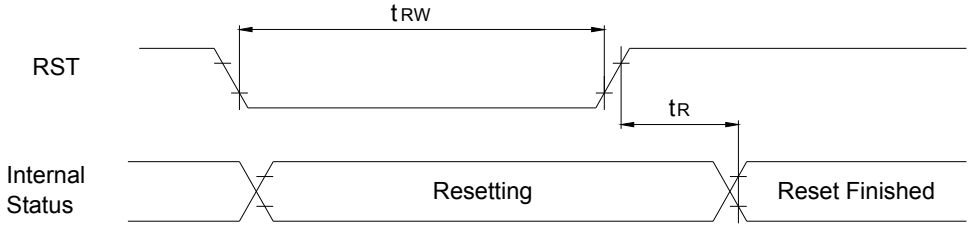
Item	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	DC	400	KHz
SCL Clock Low Pulse Width	t_{LOW}	1.3	-	μs
SCL Clock High Pulse Width	t_{HIGH}	0.6	-	μs
Data Setup Time	$t_{SU:DATA}$	100	0	ns
Data Hold Time	$t_{HD:DATA}$	0	0.9	μs
SCL, SDA Rise Time	t_r	20 + 0.1Cb	300	ns
SCL, SDA Fall Time	t_f	20 + 0.1Cb	300	ns
Capacity Load on Each Bus Line	Cb	-	400	pF
START Setup Time	$t_{SU:START}$	0.6	-	μs
START Hold Time	$t_{HD:START}$	0.6	-	μs
STOP Setup Time	$t_{SU:STOP}$	0.6	-	μs
Bus Free Time Between STOP and START Condition	t_{BUF}	1.3		μs



Serial Bus Timing Characteristics (for I²C)

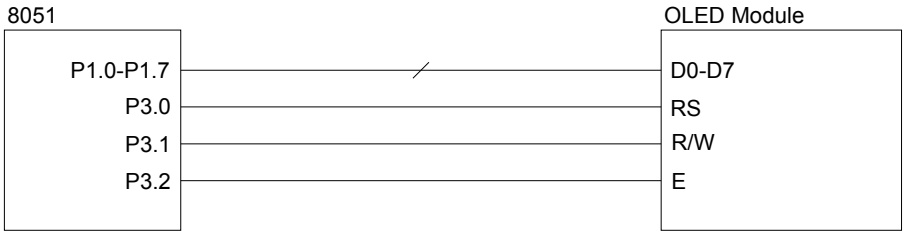
3.8 Reset Timing Characteristics (3.3V to 5.5V, Ta=25°C)

Item	Symbol	Min.	Max.	Unit
Rest Time	t_R	-	2.0	μs
Reset Low Pulse Width	t_{RW}	10.0	-	μs

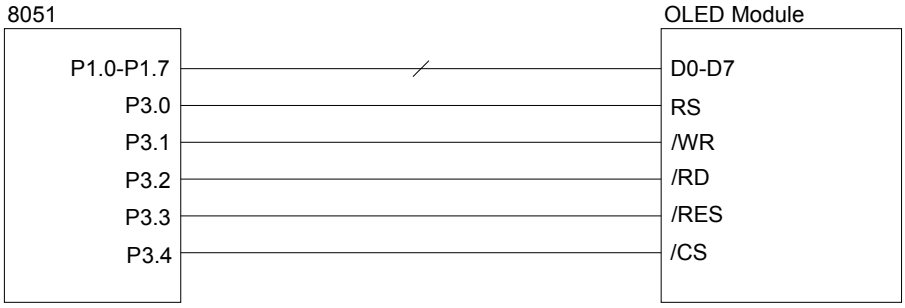


Reset Characteristics

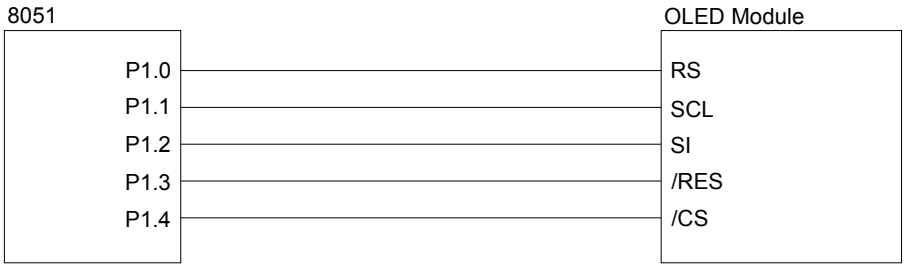
3.9 Connection with MPU



a. 6800 8-bit parallel interface

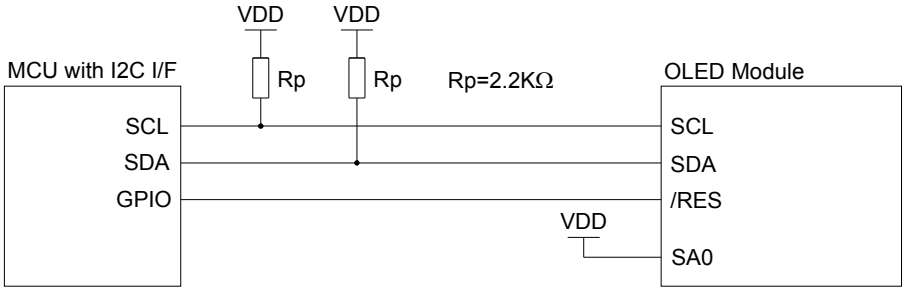


b. 8080 8-bit parallel interface



c. 4-wire SPI interface

d. 3-wire SPI interface



e. I2C interface

4. OPERATING PRINCIPLES & METHODS

4.1 Registers

The OLED controller has two types of registers, Instruction Register (IR) and Data Register (DR).
The Instruction Register is a write only register to store command codes (i.e. Display Clear, Cursor Home and others), Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address.
The Data Register is a read/write register used as a temporary storage for data that are going to be written into the DDRAM or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.
When RS = “H”, the inputs at D7 to D0 are interpreted as data and will be written to the Data Register.
When RS = “L”, the inputs at D7 to D0 are interpreted as command, they will be decoded and written to the corresponding Instruction Registers. Refer to the table below.

RS	R/W(/WR)	Function
0	0	Command write operation (MPU writes command to Instruction Register)
	1	Read Busy Flag (D7) and Address Counter (D6 to D0)
1	0	Data write operation (MPU writes data to DDRAM or CGRAM)
	1	Data read operation (MPU reads data from DDRAM or CGRAM)

4.2 Busy Flag (BF)

When the busy flag is “1” the module is performing an internal operation and the next instruction will not be accepted. The busy flag outputs to D7 when RS = 0 and a read operation is performed. The next instruction must not be written to the module until the busy flag is “0”.

4.3 Address Counter (AC)

The Address Counter (AC) assigns addresses to the DDRAM or the CGRAM.
When the address information is written into the IR, this address information is sent from the IR to the AC. The selection of either DDRAM or CGRAM is also determined concurrently by the same instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter (AC) is automatically increased or decreased by 1. The contents of AC are output to D0 to D6 when RS is “0” and a read operation is performed.

4.4 Display Data RAM (DDRAM)

The Display Data RAM (DDRAM) stores the display data represented in 8-bit character codes. Its capacity is 80 x 8 bits or 80 characters. The Display Data RAM that is not used for the display can be used as a general data RAM.
The DDRAM address (ADD) is set in the Address Counter (AC) as a hexadecimal. The Address Counter can be written by using the “Set DDRAM Address” instruction and be read by using the “Read Busy Flag and Address” instruction. In each case, data bits D0 to D6 represent the DDRAM address. In the read operation, bit D7 represents the “Busy Flag”.

MSB LSB

BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Relations between DDRAM addresses and display positions on the display are shown below.

Display position →		1	2	3	---	18	19	20
DD RAM Address	Line 1	00H	01H	02H	---	11H	12H	13H
	Line 2	40H	41H	42H	---	51H	52H	53H
	Line 3	14H	15H	16H	---	25H	26H	27H
	Line 4	54H	55H	56H	---	65H	66H	67H

When display shift operation is performed, the DDRAM address moves as follows:
For left shift:

Display position →		1	2	3	---	18	19	20
DD RAM Address	Line 1	01H	02H	03H	---	12H	13H	14H
	Line 2	41H	42H	43H	---	52H	53H	54H
	Line 3	15H	16H	17H	---	26H	27H	00H
	Line 4	55H	56H	57H	---	66H	67H	40H

For right shift:

Display position →		1	2	3	---	18	19	20
DD RAM Address	Line 1	27H	00H	01H	---	10H	11H	12H
	Line 2	67H	40H	41H	---	50H	51H	52H
	Line 3	13H	14H	15H	---	24H	25H	26H
	Line 4	53H	54H	55H	---	64H	65H	66H

4.5 Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 5 x 7 dots or 5 x 10 dots character patterns from 8-bit character codes. The OLED controller builds in four sets of font tables as English Japanese, Western European-I, English Russian and Western European-II. Users can use software or the on-board jumpers to select suitable font table. Refer to table 4.6.2 to table 4.6.5.

4.6 Character Generator RAM (CGRAM)

The Character Generator RAM (CGRAM) is used to generate user-defined character patterns in either 5 x 8 dots or 5 x 10 dots character patterns. The CGRAM is a 64 x 8 bits RAM which can generate eight 5 x 8 dots character patterns or four 5 x 10 dots character patterns. The character patterns generated by the CGRAM can be rewritten. The relationship between CGRAM address, DDRAM data and the character patterns is shown in Table 4.6.1.

To program a 5 x 8 dots character pattern into the CGRAM location (for example, character code 01H), the following steps should be taken.

A. Use the “Set CGRAM address” command to position the CGRAM pointer to the 1st row of character code 01H (CGRAM address=48H).
B. Use the “Write Data to CGRAM or DDRAM” command to write the top row of the custom character (only lower 5-bit of character pattern data is valid).

C. The CGRAM address is automatically increased if the I/D bit is set in the “Entry Mode Set” command. When this is the case, return to step B until all rows of the character are written.
D. After writing all 8 rows of data, use the “Set DDRAM address” command to return the address counter to a DDRAM location.
E. To display the custom character written above, use the “Write Data to CGRAM or DDRAM” command with the data code 01H to display the character in the DDRAM address.

Table 4.6.1 Relationship between CGRAM address, Character Codes (DDRAM Data) and Character Patterns (CGRAM Data)

(5x8 dots character patterns)

Character Code (DDRAM Data)	CGRAM Address		CGRAM Data	Pattern No.
D7 D6 D5 D4 D3 D2 D1 D0	A5 A4 A3	A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 x 0 0 0	0 0 0	0 0 0	x x x 0 1 1 1 0	Pattern 1
		0 0 1	x x x 1 0 0 0 1	
		0 1 0	x x x 1 0 0 0 1	
		0 1 1	x x x 1 1 1 1 1	
		1 0 0	x x x 1 0 0 0 1	
		1 0 1	x x x 1 0 0 0 1	
		1 1 0	x x x 1 0 0 0 1	
		1 1 1	x x x 0 0 0 0 0	Cursor
. . . . .	. . .	. . .	. . .	. . . . .
0 0 0 0 x 1 1 1	0 0 0	0 0 0	x x x 1 0 0 0 1	Pattern 8
		0 0 1	x x x 1 0 0 0 1	
		0 1 0	x x x 1 0 0 0 1	
		0 1 1	x x x 1 1 1 1 1	
		1 0 0	x x x 1 0 0 0 1	
		1 0 1	x x x 1 0 0 0 1	
		1 1 0	x x x 1 0 0 0 1	
		1 1 1	x x x 0 0 0 0 0	Cursor

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 patterns).
2. CGRAM address bits 0 to 2 designate the line position within a character pattern. The 8th line is the cursor position and display is determined by the logical OR of the 8th line and the cursor. The 8th line CGRAM data bits 0 to 4 must be set to “0”. If any of the 8th line CGRAM data bits 0 to 4 is set to “1”, the corresponding display location will light up regardless of the cursor position.
3. When the character code bits 4 to 7 are set to “0”, then the CGRAM Character Pattern is selected. However as the character code bit 3 is an ineffective bit, the “A” in the character pattern example is selected by both character code “00H” or “08H”.
4. “1” for CGRAM data corresponds to selected pixels and “0” for non-selected pixels.

Table 4.6.2 CGROM Character Code Table (FT[1:0]=00, English Japanese)

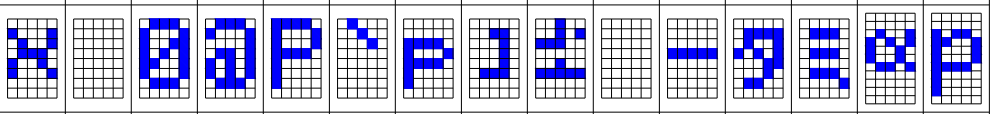
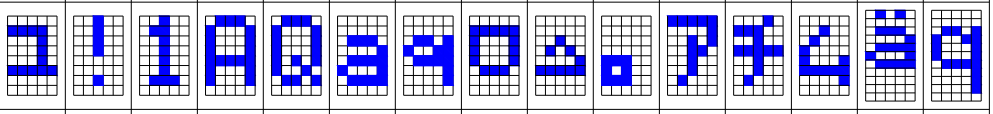
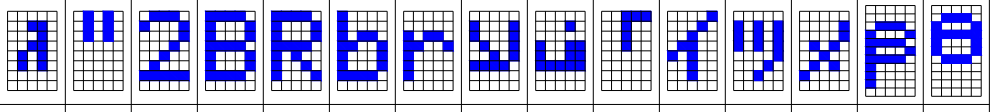
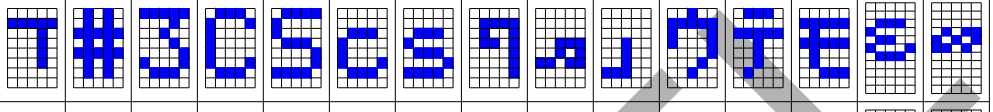
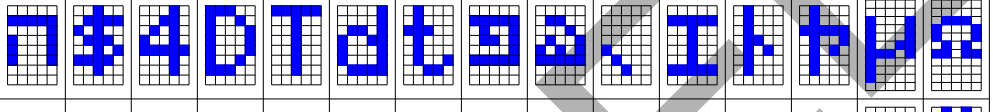
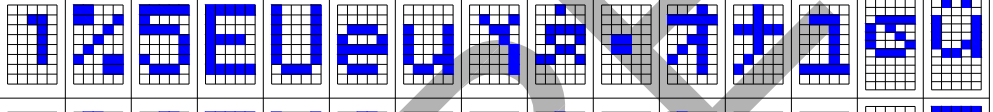
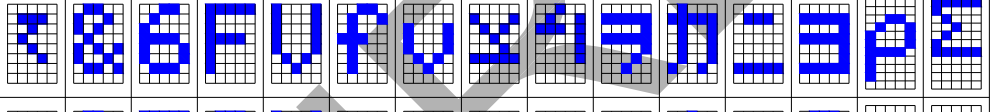
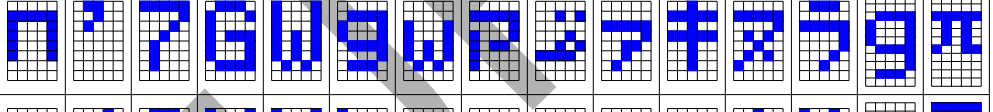
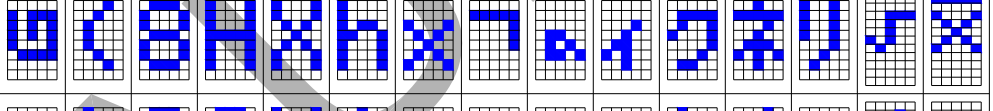
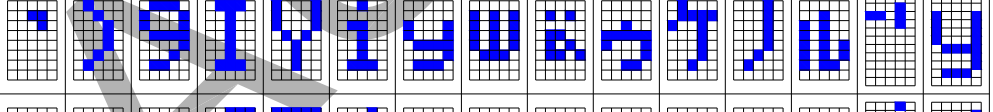
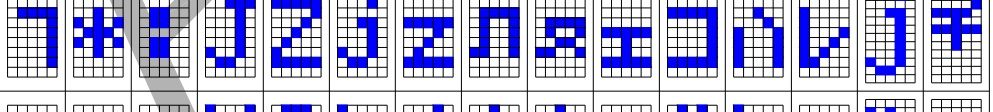
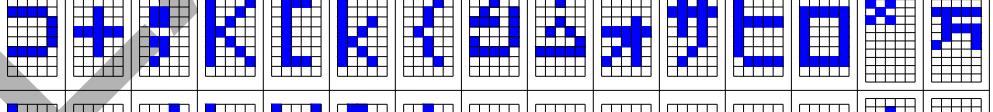
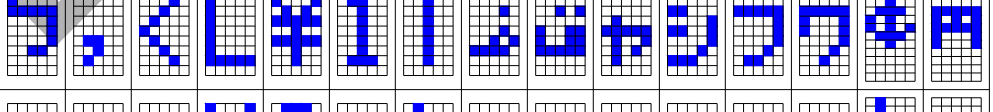
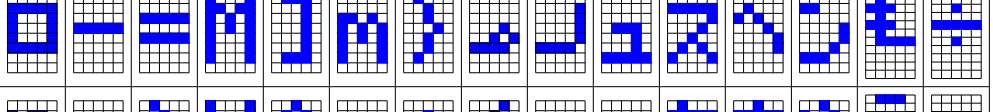
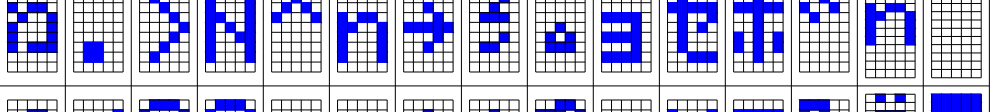
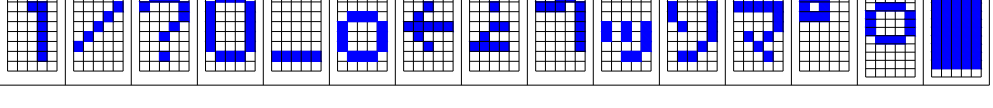
Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Table 4.6.3 CGROM Character Code Table (FT[1:0]=01, Western European - I)

Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Table 4.6.4 CGROM Character Code Table (FT[1:0]=10, English Russian)

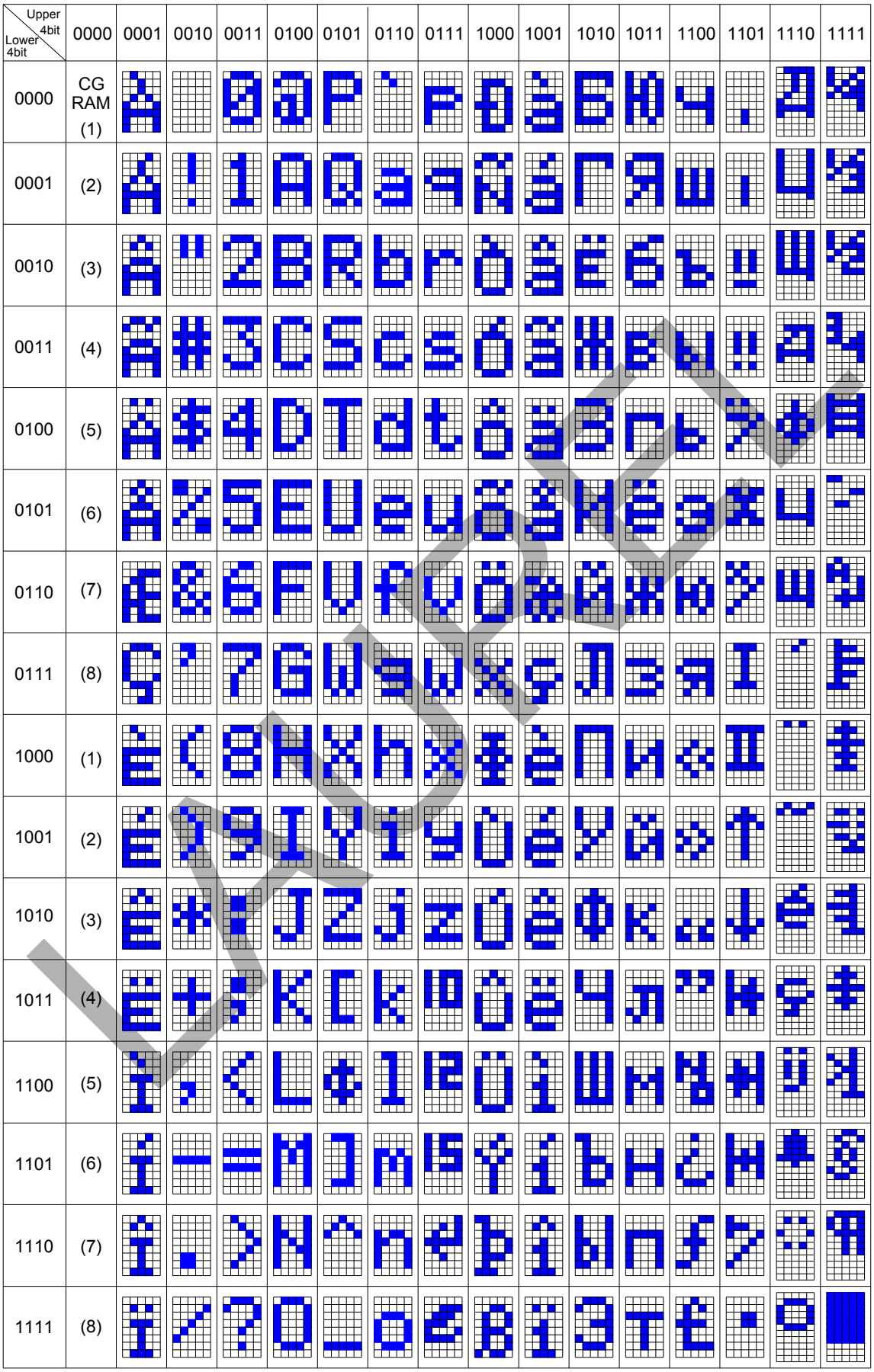
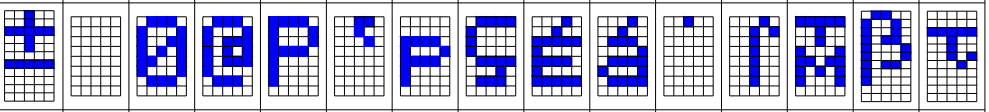
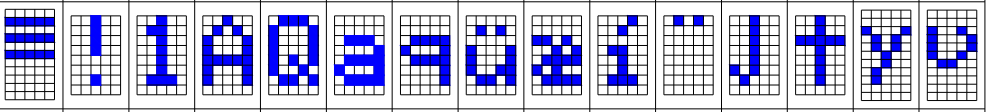
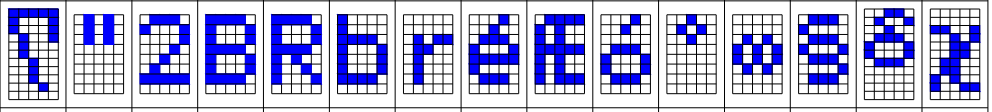
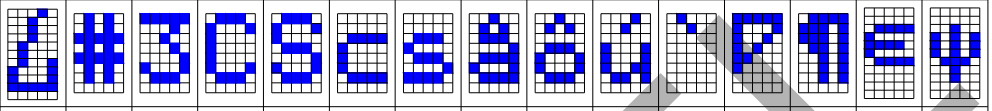
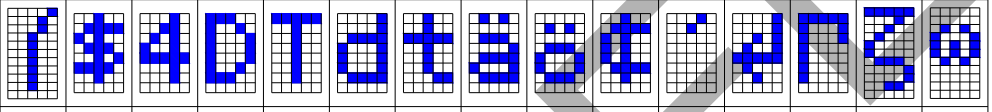
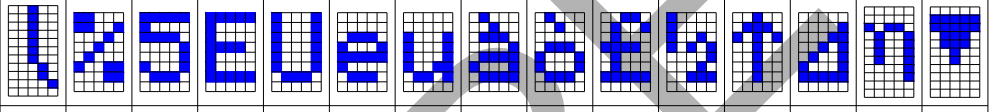
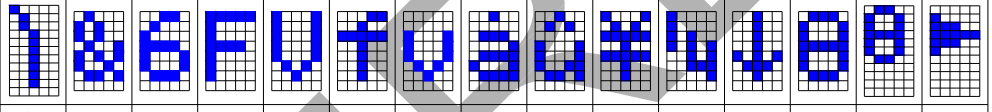
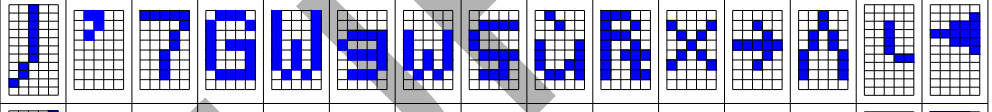
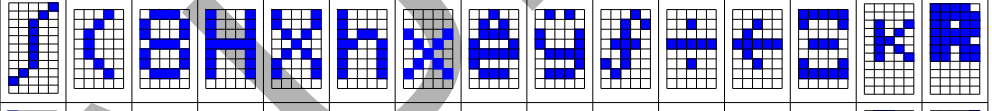
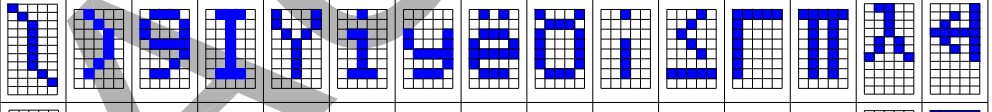
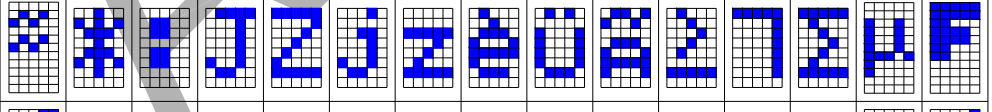
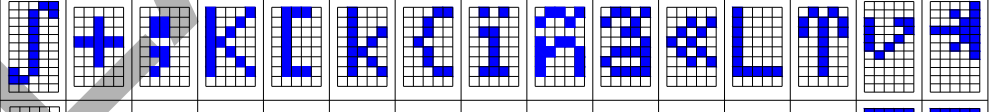
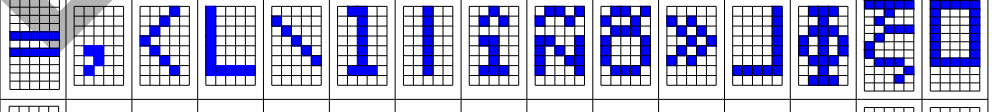
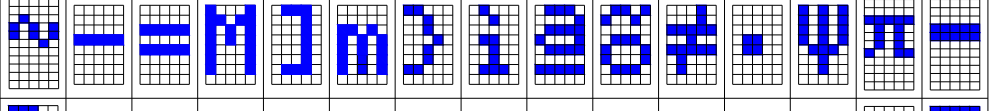
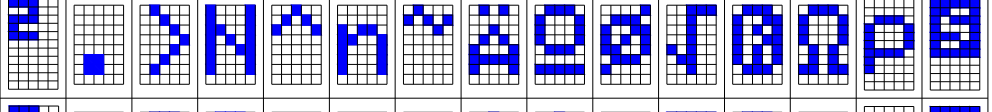
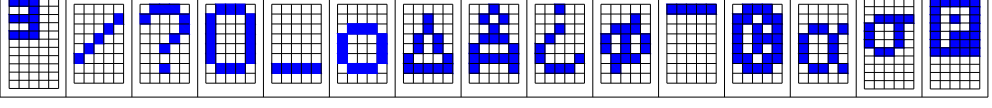


Table 4.6.5 CGROM Character Code Table (FT[1:0]=11, Western European - II)

Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

5. DISPLAY CONTROL COMMANDS

Command Table 1

Command	Command code										Description
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display and set DDRAM address to 00H. (POR=01H)
Return Home	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to 00H in AC and return shifted display to its original position. The contents of DDRAM remain unchanged.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Set cursor move direction and enable the shift of entire display. These operations are performed during data write or read. (POR=06H)
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Set ON/OFF of entire display (D), cursor ON/OFF (C), and blinking of cursor position character (B). (POR=08H)
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Move cursor or shift entire display without changing DDRAM contents.
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length(DL: 8-bit/4-bit), number of display lines (N: 2-line/1-line) and display font (F: 5x8 dots/5x11 dots). (POR=30H)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. Subsequent data access is for CGRAM.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. Subsequent data access is for DDRAM.
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) and address counter (AC).
Write data to CGRAM or DDRAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DDRAM or CGRAM.
Read data from CGRAM or DDRAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM or CGRAM.

"*": Don't care

Command Table 2

Command	Command code										Description
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Command Table 2	0	0	1	1	1	0	1	1	1	1	Double-byte command. Enter extended command table 2. (EFH, FAH)
	0	0	1	1	1	1	1	0	1	0	
Exit Command Table 2	0	0	1	1	1	1	1	1	1	0	Double-byte command. Exit from extended command table 2. (FEH, EBH)
	0	0	1	1	1	0	1	0	1	1	
Divide Ratio/ Oscillator Frequency Data Set	0	0	0	0	0	1	0	0	0	0	Double-byte command. Set the frequency of the internal display clocks. (POR=51H)
	0	0	Oscillator Frequency				Divide Ratio				
Contrast Level Set	0	0	0	1	0	0	0	0	0	0	Double-byte command. Set contrast level. (POR=80H)
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
VPP & Com/ Seg Direction Set	0	0	0	1	0	1	0	0	0	0	Double-byte command. Set VPP Voltage, Com/ Seg data direction and DC-DC pump mode. (POR=03H)
	0	0	0	0	CMS	SHL	0	DCS	VPP[1:0]		
Font Table & Cursor Blinking Set	0	0	1	0	0	0	0	0	0	0	Double-byte command. Set the font table and cursor blinking duty. (POR=20H)
	0	0	0	BD[2:0]			0	FTE	FTS[1:0]		
Read IC ID	0	1	0	On/Off	ID						Read controller IC ID and display on/off flag.

Notes: Check the busy flag before sending commands to the display. If the busy flag is not checked, the time between each command must be longer than the command execution time.

Please refer to US2011 data sheet for details of the command descriptions.

6. INITIALIZATION AND POWER OFF

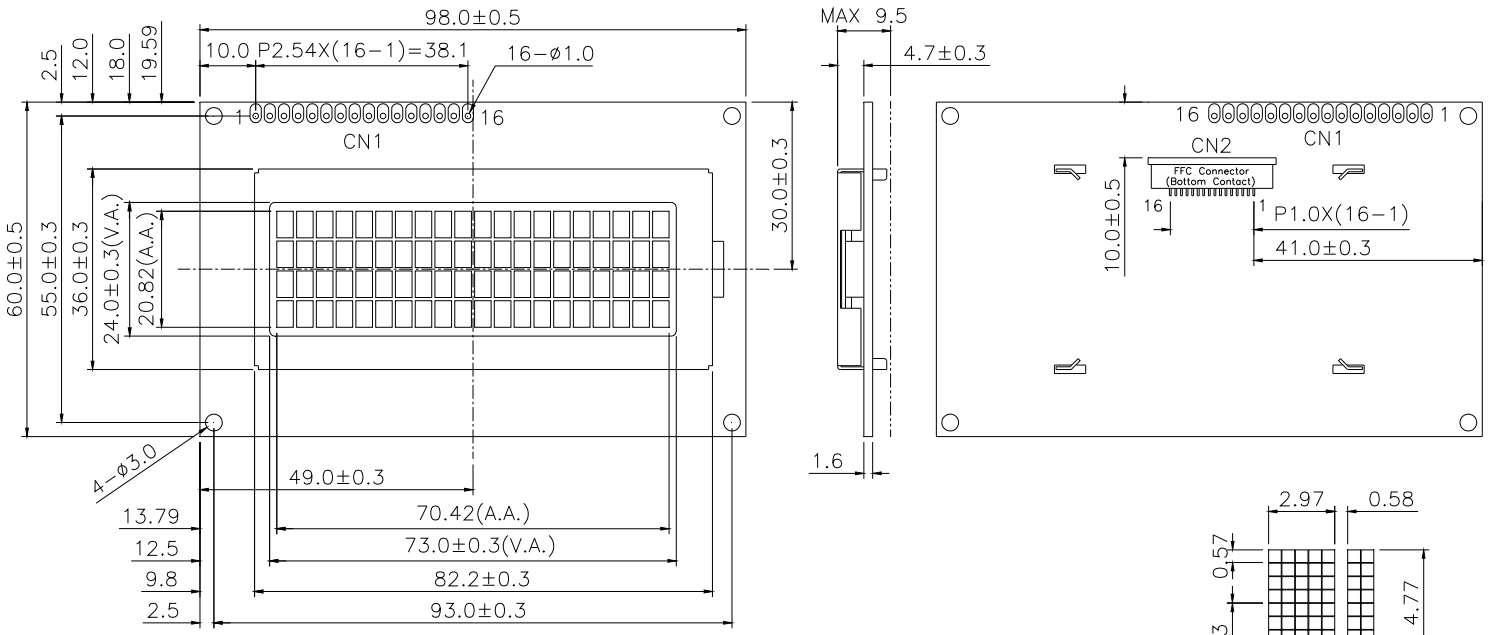
6.1 Power on Initialization Sequence

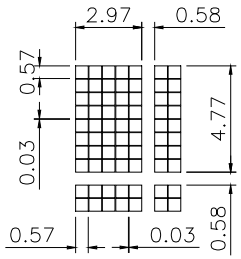
No.	Command	Description
1	Power on	Power on and wait more than 15ms after VDD stabilized
2	Reset (skip this step for 6800 interface mode)	a. Set /RES = "L" b. Wait more than 100us c. Set /RES = "H" d. Wait more than 1ms
3	Function Set: 38H	8-bit data length, 2-line display, 5x8 font
4	Display Off: 08H	Display off, cursor off, blink off
5	Enter Extended Command Table 2: EFH, FAH	Enter extended command table 2
6	Set Display Clock Divide Ratio/Oscillator Frequency: 10H, 51H	Divide ratio = 2, oscillator frequency = fosc
7	Set Contrast Control Register: 40H, 80H or 40H, CFH	Contrast control register = 80H (when VDD=4.5V to 5.5V) or = CFH (when VDD=3.3V to 4.5V)
8	Set VPP Voltage & Com/Seg Direction: 50H, 03H	VPP=12V, COM1--> COM32, SEG1 --> SEG100, 3 times dc-dc pump mode
9	Set Font Table & Cursor Blinking Duty: 80H, 20H	Blinking Duty = 300ms Disable software font table set function
10	Exit Extended Command Table 2: FEH, EBH	Exit extended command table 2
11	Set Entry Mode: 06H	DDRAM address increments by 1, the display is not shifted.
12	Clear Display: 01H	Clear the display
13	Set Display On: 0CH	Display on, cursor off, cursor blinking off
14	End of initialization	Delay 200ms and start to send other commands

6.2 Power off Sequence

No.	Command	Description
1	Optional status	Normal operation
2	Display Off: 08H	Set display off and wait 1ms
3	Power off	

7. DIMENSIONAL OUTLINE





CN1/CN2(6800 4/8−BIT PARALLEL I/F MODE)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SYMBOL	Vss	VDD	NC	RS	R/W	E	D0	D1	D2	D3	D4	D5	D6	D7	NC	NC

CN1/CN2(8080 4/8−BIT PARALLEL I/F MODE)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SYMBOL	Vss	VDD	NC	RS	/WR	/RD	D0	D1	D2	D3	D4	D5	D6	D7	/RES	/CS

CN1/CN2(3/4−SPI I/F MODE)

PIN NO.	1	2	3	4	5	6	7	8	9−16
SYMBOL	Vss	VDD	NC	RS	/RES	/CS	SCL	SI	NC

CN1/CN2(I2C I/F MODE)

PIN NO.	1	2	3	4	5	6	7	8	9−16
SYMBOL	Vss	VDD	NC	SA0	/RES	NC	SCL	SDA	NC

			DWN.	LY	TITLE	LCM OUTLINE DIMENSION	
			CHK.	LYJ	PART NO.	LEC2041	
			APPD.		DWG. NO.	LEC2041−WXA	
A	New issue	2019.02.15	REV.	A	UNIT	mm	PROJECTION
REV.	DESCRIPTION	DATE	DATE	2019.02.15	SCALE	NTS	SHEET 1 OF 1

8. PRECAUTIONS FOR USE OF OLED MODULES

8.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the internal organic substance leaks out, be sure not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of the display or the adjoining areas of the module since this may damage the cell structure.
4) The polarizer covering the surface of OLED module is soft and easily scratched. Please be careful when handling the OLED module.
5) If the surface of the OLED module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
   · Isopropyl alcohol
   · Ethyl alcohol
   Solvents other than those mentioned above may damage the polarizer. Especially, do not use the followings:
   · Water
   · Ketone
   · Aromatic Solvents
6) When mounting the OLED module make sure it is free of twisting, warping and distortion. Distortion has great influence upon the display quality. Be sure the outer case holding the OLED module has sufficient rigidity.
7) Do not forcibly pull or bend the FPC terminals, apply stress to driver IC and the surrounding molded sections.
8) Do not disassemble nor modify (enlarging or making extra holes, etc.) the OLED module.
9) NC terminals should be open.
10) If the logic circuit power is off, do not apply the input signals.
11) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   · Be sure to ground the human body when handling the OLED module.
   · Tools required for assembly, such as soldering irons, must be properly grounded.
   · To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   · The surface of the OLED module is covered with a protective film. Exercise care when peeling off this protective film since static electricity may be generated.

8.2 Storage Precautions

1) When storing the OLED modules, put them in static electricity preventive bags and avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. Store the OLED modules in the packaged state when they were shipped from the manufacturer.
2) Exercise care to minimize corrosion of the electrodes. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

8.3 Design Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for the OLED module. Damage may happen if these values are exceeded,
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to

satisfy VIL, VIH specifications, including making the signal line cable as short as possible.

3) Pay sufficient attention to avoid occurrence of the mutual noise interference occurred by peripheral devices.
4) To cope with EMI, take necessary measures on the outputting side of equipment.
5) When fastening the OLED module, fasten the external plastic housing section or the PCB.

8.4 Others

1) When an OLED module operates for a long of time with fixed patterns, the display patterns may remain on the screen as ghost images and slight contrast deviation may occur. If the operation is interrupted and the display is left unused for a while, normal state can be restored. This phenomenon does not adversely affect the reliability of the OLED module.
2) To minimize the performance degradation resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   · Pins and electrodes
   ·Pattern layouts such as the FPC
3) Although the OLED module store the operation state data by the commands and the indication data, excessive external noise can enter into the module and the internal status may be changed. It is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
4) We recommend users to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.
5) Request the qualified companies to handle industrial wastes when disposing of the OLED modules.