



# AKD4495-SA

## AK4495 Sound Quality Evaluation Board Rev.0

### 1. GENERAL DESCRIPTION

The AKD4495-SA is a sound quality evaluation board for AK4495. The AKD4495-SA has digital audio interfaces, enabling to interface to digital audio systems via optical or coaxial connector.

#### ■ Ordering Guide

AKD4495-SA --- AK4495 Sound Quality Evaluation Board  
(Control software and USB cable are included in this package.)

### 2. FUNCTION

- Three digital audio interfaces
  - Coaxial Input
  - Optical Input
  - 10pin Header for serial control mode
- USB control port
- On-board Analog output buffer and LPF circuit

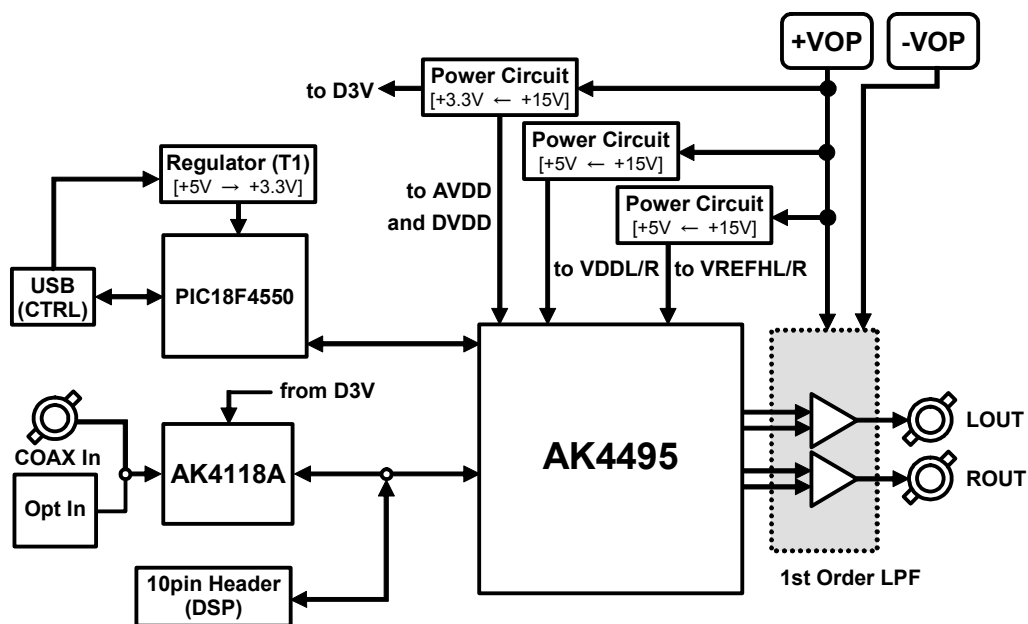


Figure 1. AKD4495-SA Block Diagram (Note 1)

Note 1. Circuit diagram and PCB layout are attached at the end of this manual.

Coaxial connection is recommended when evaluating the sound quality.

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## 4. Evaluation Board Diagram

### ■ Board Diagram

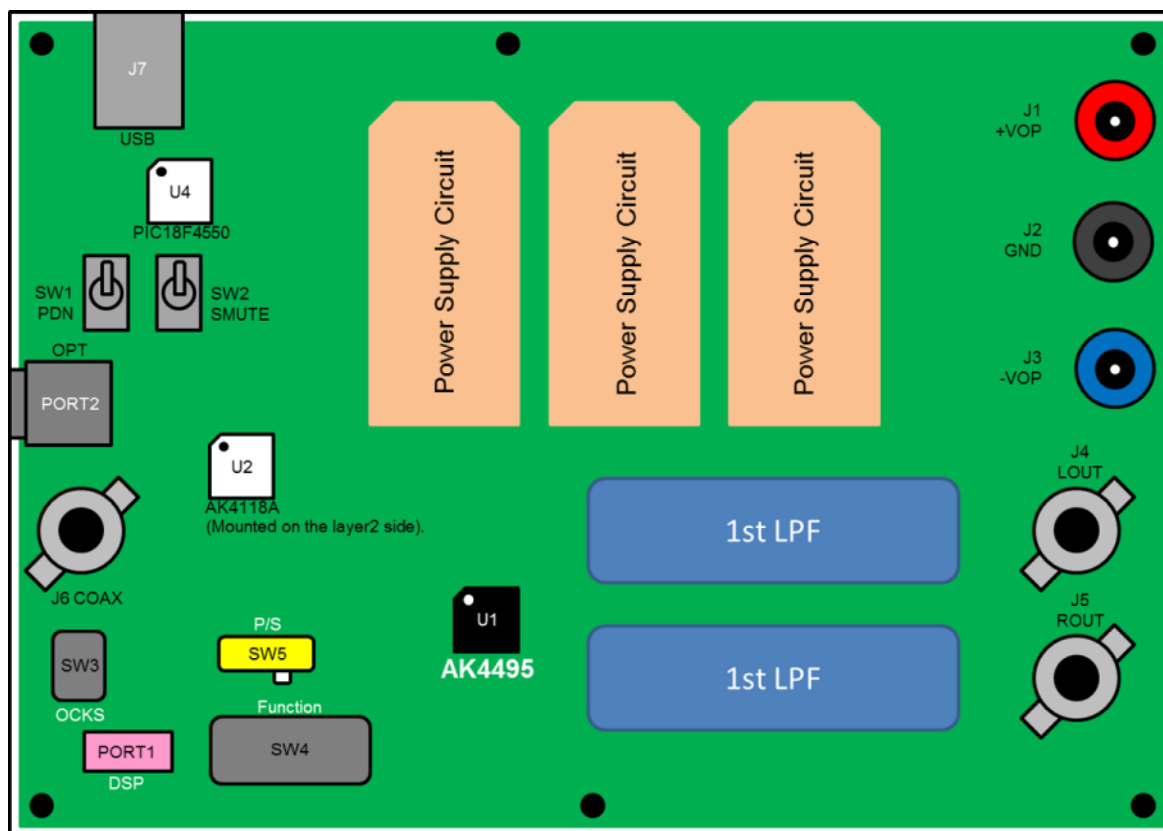


Figure 2. Board Diagram

### ■ Description

- (1) Power Supply and GND connector (+VOP, GND, -VOP)  
Refer to the “■ Set up the power supply lines”.
- (2) SPDIF input connector (J6 / BNC connector, PORT2 / Optical connector)  
SPDIF signal Input to the AK4118A.  
When using J6 (BNC connector), Set to R32 = “0 ohm” and R31 = “open”.  
When using PORT2 (Optical connector), Set to R32 = “open” and R31 = “0 ohm”.
- (3) Analog output connector (J4 / J5, BNC connector)  
Single-ended output connector.

## (4) DSP PORT (PORT1)

10 pin header for interfacing with external data sources, enabling to connect other audio systems.

When using PORT1 (DSP), Set to R14, R18, R22, R28 = “open” and R13, R16, R21, R24, R23 = “0 ohm”.

| Pin | I/O | Function   | pin | I/O | Function |
|-----|-----|------------|-----|-----|----------|
| 1   | I   | MCLK       | 2   | P   | GND      |
| 3   | I   | BICK/DCLK  | 4   | P   | GND      |
| 5   | I   | LRCK/DSDR  | 6   | P   | GND      |
| 7   | I   | SDATA/DSDL | 8   | P   | GND      |
| 9   | I   | WCK        | 10  | P   | GND      |

Table 1. Pin Assignment of DSP PORT

## (5) AK4118A (U2)

AK4118A has Digital Audio I/F Transceiver.

When evaluating the sound quality, Using AK4118A with SPDIF signal.

## (6) PIC18F4550 (U4)

USB control chip.

Control registers of the AK4495 can be set by a PC via USB port.

## (7) Slide switch (SW3 / SW4)

Mode setting switch for AK4118A and AK4495.

Upper-side is “ON (H)” and lower-side is “OFF (L)”.

Refer to “■ Switch Setting”.

## 5. Operation Sequence

### ■ Set up the Power Supply Lines

| Name | Color | Voltage  | Breakdown                                         | Note               |
|------|-------|----------|---------------------------------------------------|--------------------|
| +VOP | Red   | +12~+15V | Power circuit,<br>Input / Output Buffer (OP Amp.) | Must be connected. |
| -VOP | Blue  | -12~-15V | Input / Output Buffer (OP Amp.)                   | Must be connected. |
| GND  | Black | 0V       | Ground                                            | Must be connected. |

Table 2. Power Supply Lines ([Note 2](#))

Note 2. Each supply line should be distributed separately from the power supply unit

### ■ Evaluation Mode

#### (1) D/A Evaluation using the AK4118A (DIR) (Coaxial connector) < default >

The AK4118A generates MCLK, BICK, LRCK, SDATA from the data from the BNC connector (J6). Evaluations using a test CD and etc. are available([Note 3](#)).

Setting: R31 = “open”, R32 = “0 ohm”

Note 3. Coaxial connection is recommended when evaluating the sound quality.

#### (2) D/A Evaluation using the AK4118 (DIR) (Optical connector)

The AK4118A generates MCLK, BICK, LRCK, SDATA from the data from the optical connector (PORT2). Evaluations using a test CD and etc. are available.

Setting: R31 = “0 ohm”, R32 = “open”

#### (3) All interface signals including the master clock are supplied externally (PORT1)

Setting: R18, R22, R25, R28 = “open”, R16, R21, R24, R23 = “0 ohm”

## ■ Switch Setting

### (1) Parallel / Serial Control Mode select switch.

[SW5] (P/S): Mode selects to “Parallel Control Mode” or “Serial Control Mode”.

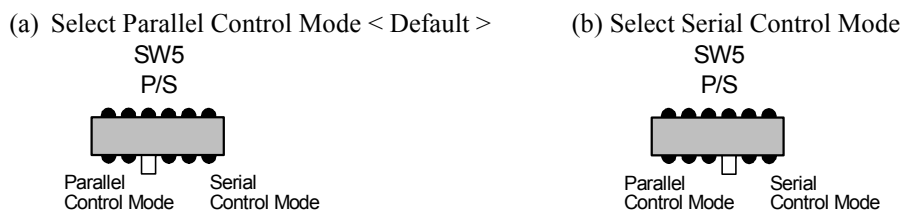


Figure 3. P/S Setting (Note 4)

Note 4. When using “**Serial Control Mode**”, SW4 [No.5] is assignment by CAD0 pin and SW4 [No.9] is assignment by CAD1 pin.  
In addition, Except for SW4 [No.5 and No.9] is disabled.

### (2) Other switch setting

Upper-side is “ON (H)” and lower-side is “OFF (L)”.

[SW2] (SMUTE): Soft-mute setting of AK4495. Keep “L” during normal operation.

[SW3] (SW DIP-2): AK4118A Setting

| No. | Name  | ON (“H”)                                                             | OFF (“L”) | Default |
|-----|-------|----------------------------------------------------------------------|-----------|---------|
| 1   | OCKS1 | Master Clock setting for AK4118A<br>Refer to <a href="#">Table 5</a> |           | ON      |
| 2   | OCKS0 |                                                                      |           | OFF     |

Table 3. AK4118A Mode Setting

[SW4] (SW DIP-10): AK4495 Setting

| No. | Name        | ON (“H”)                                                                | OFF (“L”)                          | Default |
|-----|-------------|-------------------------------------------------------------------------|------------------------------------|---------|
| 1   | SD          | Digital Filter Setting<br>Refer to <a href="#">Table 8</a>              |                                    | ON      |
| 2   | SLOW        |                                                                         |                                    | OFF     |
| 3   | DIF0        | Audio I/F Format Setting for AK4495<br>Refer to <a href="#">Table 6</a> |                                    | OFF     |
| 4   | DIF1        |                                                                         |                                    | ON      |
| 5   | DIF2 / CAD0 | CAD0pin=“H”                                                             | CAD0pin=“L”                        | OFF     |
| 6   | I2C         | I2C-bus Control Mode                                                    | 3-wire Serial Control Mode         | OFF     |
| 7   | DEM0        | De-emphasis Control<br>Refer to <a href="#">Table 7</a>                 |                                    | ON      |
| 8   | DEM1        |                                                                         |                                    | OFF     |
| 9   | ACKS / CAD1 | Auto Setting Mode<br>CAD1pin=“H”                                        | Manual Setting Mode<br>CAD1pin=“L” | OFF     |
| 10  | DFP         | Super Slow roll-off Filter<br>ON                                        | Super Slow roll-off Filter<br>OFF  | OFF     |

Table 4. AK4495 Mode Setting

| OCKS1 | OCKS0 | MCKO1 |
|-------|-------|-------|
| L     | L     | 256fs |
| H     | L     | 512fs |
| H     | H     | 128fs |

&lt;Default&gt;

Table 5. AK4118A Master Clock Setting

| Mode | DIF2 | DIF1 | DIF0 | Input Format                       | LRCK | BICK  |
|------|------|------|------|------------------------------------|------|-------|
| 0    | 0    | 0    | 0    | 16-bit LSB justified               | H/L  | ≥32fs |
| 1    | 0    | 0    | 1    | 20-bit LSB justified               | H/L  | ≥48fs |
| 2    | 0    | 1    | 0    | 24-bit MSB justified               | H/L  | ≥48fs |
| 3    | 0    | 1    | 1    | 24-bit I <sup>2</sup> S compatible | L/H  | ≥48fs |
| 4    | 1    | 0    | 0    | 24-bit LSB justified               | H/L  | ≥48fs |
| 5    | 1    | 0    | 1    | 32-bit LSB justified               | H/L  | ≥64fs |
| 6    | 1    | 1    | 0    | 32-bit MSB justified               | H/L  | ≥64fs |
| 7    | 1    | 1    | 1    | 32-bit I <sup>2</sup> S compatible | L/H  | ≥64fs |

&lt; Default &gt;

Table 6. AK4495 Audio I/F Format

| DEM1 | DEM0 | Mode    |
|------|------|---------|
| 0    | 0    | 44.1kHz |
| 0    | 1    | OFF     |
| 1    | 0    | 48kHz   |
| 1    | 1    | 32kHz   |

&lt; Default &gt;

Table 7. De-emphasis Control

| SD | SLOW | Mode                              |
|----|------|-----------------------------------|
| 0  | 0    | Sharp roll-off filter             |
| 0  | 1    | Slow roll-off filter              |
| 1  | 0    | Short delay sharp roll-off filter |
| 1  | 1    | Short delay slow roll-off filter  |

&lt; Default &gt;

Table 8. Digital Filter Setting

**■ Power ON**

Upper-side is “ON (H)” and lower-side is “OFF (L)”.

Power-down reset by SW1(PDN) must be made once after power up the evaluation board. Put the SW1 to “L” for power-down reset of the AK4495 and AK4118A, and the return them to “H” to release the power-down states.

[SW1] (PDN): Resets the AK4495 and AK4118A (Keep “H” during normal operation).

This switch must be set to “L” once upon power up the evaluation board to reset the AK4495 and AK4118A.

**■ Board Control**

The AKD4495-SA can be controlled via a USB port with a PC. Connect J7 (USB) connector to a PC with USB cable. The control software is included in the AK4495-SA package. Refer to the “Control Software Manual” paragraph for operational sequence of the control software.

## 6. CONTROL SOFTWARE MANUAL

### ■ Evaluation Board and Control Software Settings

1. Set up the evaluation board as needed. According to the previous terms.
2. Connect the evaluation board and a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please disconnect the evaluation board once and reconnect it to the PC.
4. Insert the CD-ROM labeled “AKD4495 Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “akd4495-sa.exe” to open the control program.
6. Begin evaluation by following the procedure below.

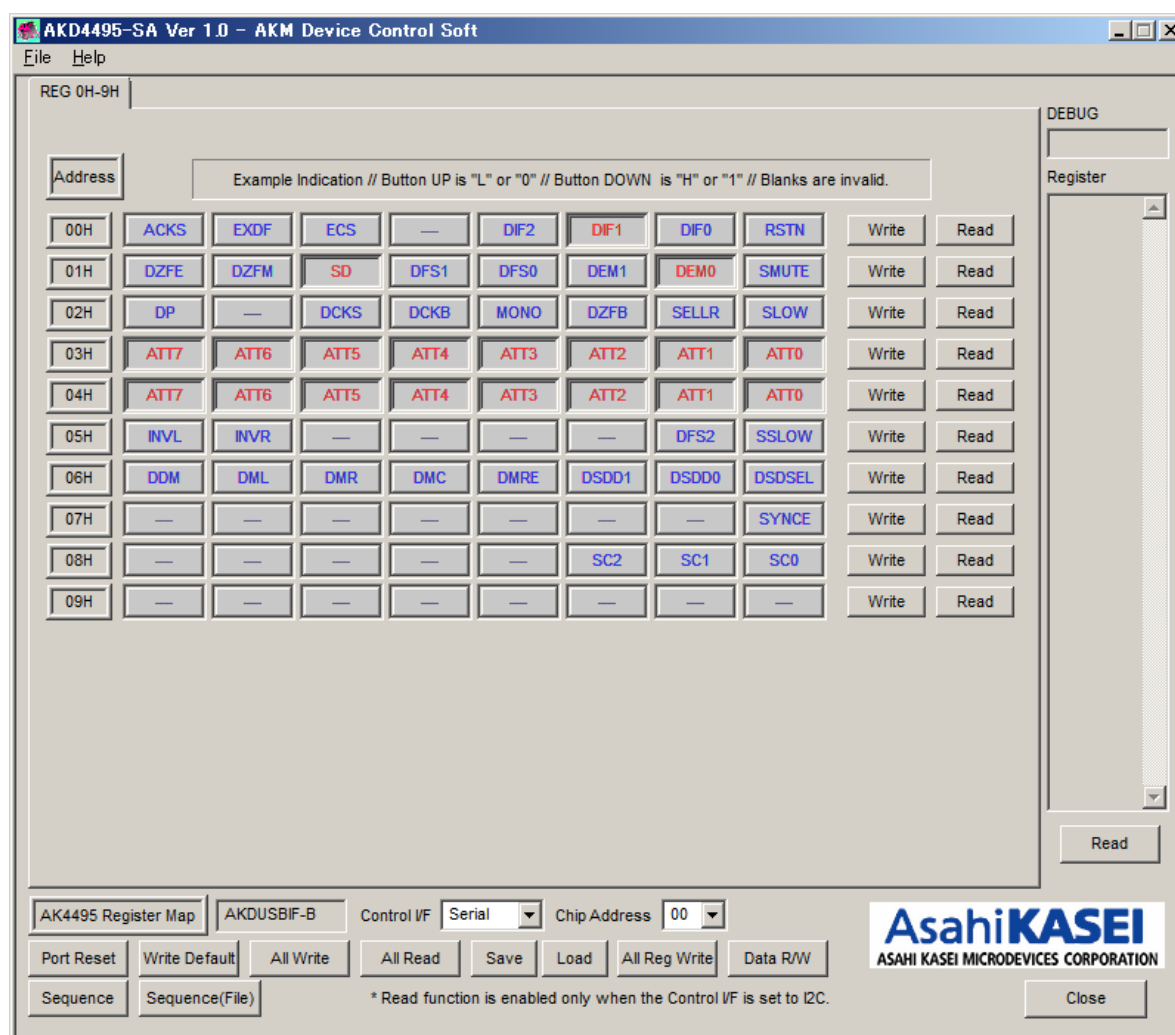


Figure 4. Control Software Window

## ■ Operation Overview

Register map is controlled by this control software.

Frequently used buttons such as the register initializing button “Write Default”, are located outside of the tab window. Refer to the “■ Dialog Boxes” section for details of each dialog box setting.

1. [Port Reset]: Resets the USB port of the main board.  
Click this button after the control software starts up when a PC is connected to J7 (USB) port of the AKD4495-SA.
2. [Write Default]: Initializes register values.  
Use this button to initialize the registers after the device is reset by hardware reset.
3. [All Write]: Executes all write commands of displayed registers.
4. [All Read]: Executes read commands for all registers displayed ([Note 5](#)).
5. [Save]: Saves current register settings as a file.
6. [Load]: Executes data write from a saved file.
7. [All Reg Write]: “All Reg Write” dialog box pops up.
8. [Data R/W]: “Data R/W” dialog box pops up.
9. [Sequence]: “Sequence” dialog box pops up.
10. [Sequence(File)]: “Sequence(File)” dialog box pops up.
11. [Read]: Reads current register settings and displays to the register area (on the right of the main window).  
This is different from [All Read] button as it does not reflect to the register map. It only displays register values in hexadecimal numbers ([Note 5](#)).

Note 5. [All Read] button and [Read] button are only available for “**I2C-bus Control Mode**” setting.

## ■ Tab Descriptions

### 1. [REG]: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.

Button Down indicates “1” and the bit name is shown in red (when read-only, the name is shown in dark red).

Button Up indicates “0” and the bit name is shown in blue (when read-only, the name is shown in gray).

Grayed out registers are read-only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

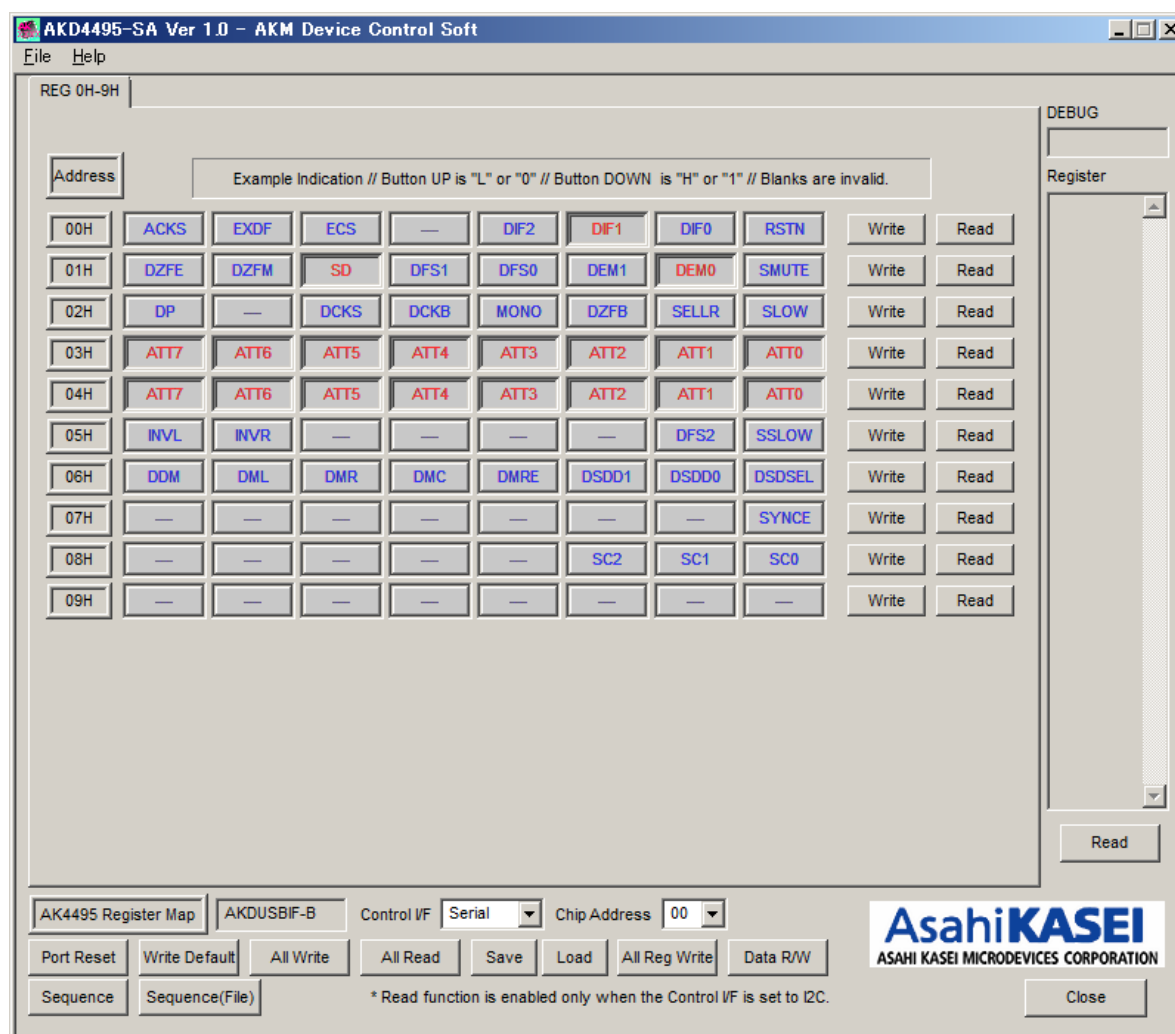


Figure 5. REG Window

### 1-1. [Write]: Data Write Dialog Box

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register name is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

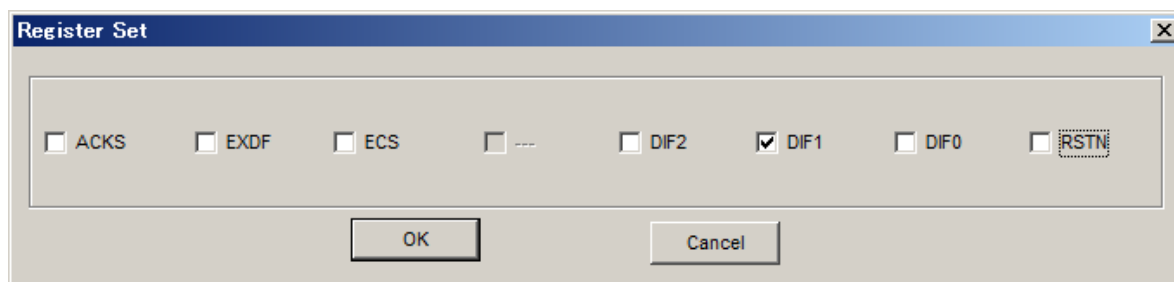


Figure 6. Register Set Window

### 1-2. [Read]: Data Read Dialog Box (I2C-bus Control Mode Only)

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.

Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).

Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray).

## ■ Dialog Boxes

### 1. [All Reg Write] : [All Register Write] Dialog Box

Click [All Reg Write] button in the main window to open register setting files.  
Register setting files saved by [SAVE] button can be applied.

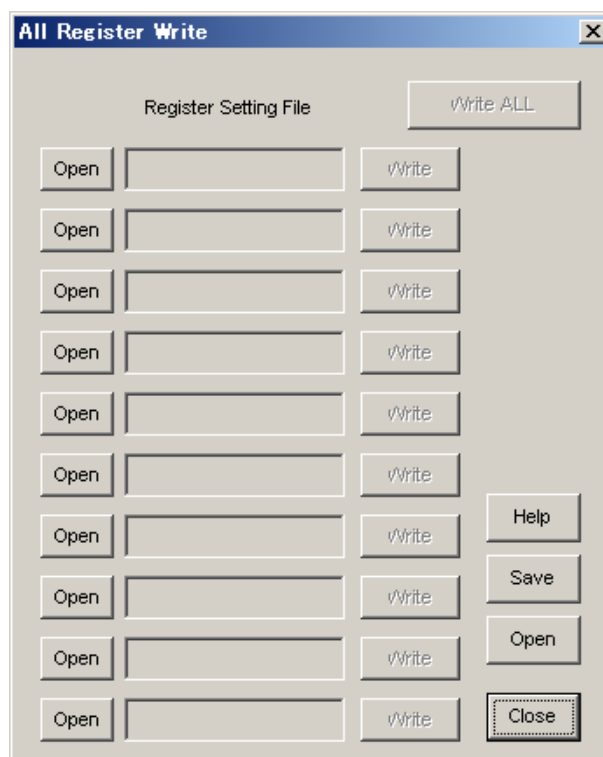


Figure 7. All Reg Write Window

- [Open (left)] : Open a register setting file (\*.akr).
- [Write] : Executes register writing.
- [Write All] : Executes all register writings.  
Writings are executed in descending order.
- [Help] : A help window pops up.
- [Save] : Saves register setting file assignment. The file name is "\*.mar".
- [Open (right)] : Open a register setting assignment file that is saved as "\*.mar".
- [Close] : Closes the dialog box and finishes this process.

### Operating Suggestions

- (1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "\*.mar" should be stored in the same folder.
- (2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

## 2. [Data R/W]: [Data R/W] Dialog Box

Click the [Data R/W] button in the main window to open the data read/write dialog box shown below.  
A data write is executed to specified address.

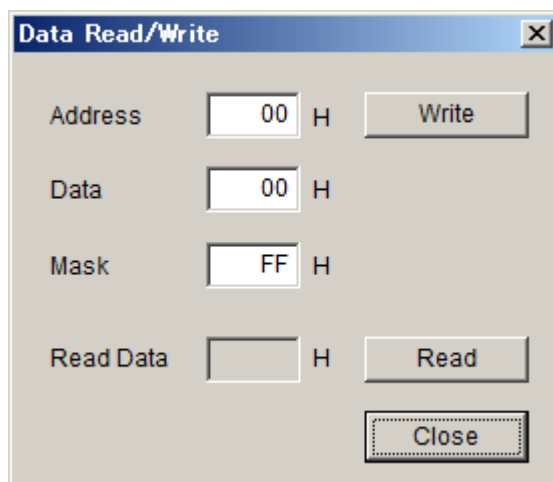


Figure 8. Data R/W Window

[Address] Box : Input write data address in hexadecimal numbers for data writing.

[Data] Box : Input start data in hexadecimal numbers.

[Mask] Box : Input mask data in hexadecimal numbers.

This value “ANDed” with the write data becomes the input data.

[Write] : Writes data to the address specified in “Address” box ([Note 6](#)).

[Read] : Reads data from the address specified by “Address” box.

The result will be shown in the Read Data Box in hexadecimal numbers ([Note 7](#)).

[Close] Button : Closes the dialog box.

Data write can be cancelled by this button instead of [Write] button.

Note 6. The register map will be updated after executing the [Write] command.

Note 7. [Read] button is only available for “**I2C-bus Control Mode**” setting.

### 3. [Sequence]: [Sequence] Dialog Box

Click the [Sequence] button to open register sequence setting dialog box shown below.  
Register sequence can be set in this dialog box.

|    | Address | Data | Mask | Interval | Select |    | Address | Data | Mask | Interval | Select |
|----|---------|------|------|----------|--------|----|---------|------|------|----------|--------|
| 1  | 00 H    | 00 H | FF H | 0 ms     | No_use | 16 | 00 H    | 00 H | FF H | 0 ms     | No_use |
| 2  | 00      | 00   | FF   | 0        | No_use | 17 | 00      | 00   | FF   | 0        | No_use |
| 3  | 00      | 00   | FF   | 0        | No_use | 18 | 00      | 00   | FF   | 0        | No_use |
| 4  | 00      | 00   | FF   | 0        | No_use | 19 | 00      | 00   | FF   | 0        | No_use |
| 5  | 00      | 00   | FF   | 0        | No_use | 20 | 00      | 00   | FF   | 0        | No_use |
| 6  | 00      | 00   | FF   | 0        | No_use | 21 | 00      | 00   | FF   | 0        | No_use |
| 7  | 00      | 00   | FF   | 0        | No_use | 22 | 00      | 00   | FF   | 0        | No_use |
| 8  | 00      | 00   | FF   | 0        | No_use | 23 | 00      | 00   | FF   | 0        | No_use |
| 9  | 00      | 00   | FF   | 0        | No_use | 24 | 00      | 00   | FF   | 0        | No_use |
| 10 | 00      | 00   | FF   | 0        | No_use | 25 | 00      | 00   | FF   | 0        | No_use |
| 11 | 00      | 00   | FF   | 0        | No_use |    |         |      |      |          |        |
| 12 | 00      | 00   | FF   | 0        | No_use |    |         |      |      |          |        |
| 13 | 00      | 00   | FF   | 0        | No_use |    |         |      |      |          |        |
| 14 | 00      | 00   | FF   | 0        | No_use |    |         |      |      |          |        |
| 15 | 00      | 00   | FF   | 0        | No_use |    |         |      |      |          |        |

Start Step: 1

Buttons: Start, Help, Save, Open, Close

Figure 9. Sequence Window

### Sequence Setting

Set register sequence according to the following process bellow.

#### (1) Select a command

Use [Select] pull-down box to choose commands.  
Corresponding boxes will be valid.

##### < Select Pull-down menu >

- No\_use : Not using this address
- Register : Register write
- Reg(Mask) : Register write (Masked)
- Interval : Takes an interval
- Stop : Pauses the sequence
- End : Ends the sequence

## (2) Input sequence

[Address] : Data address  
[Data] : Write data  
[Mask] : Mask  
The value in the [Data] box is ANDed with the value in the [Mask] box. This data becomes the actual input data.  
When Mask = 0x00, current setting is hold.  
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.  
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.  
Upper 4bit is hold to current setting.  
[ Interval ] : Interval time

Valid boxes for each process command are shown below.

· No\_use : None  
· Register : [Address], [Data], [Interval]  
· Reg(Mask) : [Address], [Data], [Mask], [Interval]  
· Interval : [Interval]  
· Stop : None  
· End : None

**Control Buttons**

Functions of Control Buttons are shown below.

[Start] Button : Executes the sequence  
[Help] Button : A help window pops up.  
[Save] Button : Saves sequence settings as a file. The file name is "\*.aks".  
[Open] Button : Open a sequence setting file "\*.aks".  
[Close] Button : Closes the dialog box and finish the process.

**Stop of the sequence**

When "Stop" is selected in the sequence, the process is paused. It starts again when the [Start] button is clicked. Restart step number is shown in the "Start Step" box. When executing the process until the end of sequence, the "Start Step" value will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.  
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

#### 4. [Sequence(File)]: [Sequence by \*.aks file] Dialog Box

Click the [Sequence(File)] button to open sequence setting file dialog box shown below.  
Files saved in the “Sequence setting dialog” can be applied in this dialog.

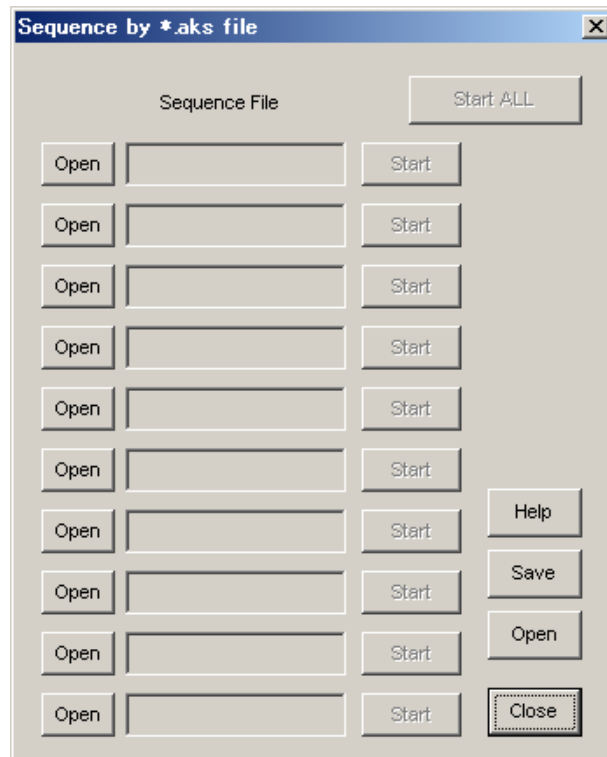


Figure 10. Sequence(File) Window

- [Open (left)] : Open a sequence setting file (\*.aks).
- [Start] : Executes the sequence setting.
- [Start All] : Executes all sequence settings.  
Sequences are executed in descending order.
- [Help] : A help window pops up.
- [Save] : Saves a sequence setting file assignment. The file name is “\*.mas”.
- [Open(right)] : Open a saved sequence setting file assignment “\*. mas”.
- [Close] : Closes the dialog box and finish the process.

#### Operating Suggestions

- (1) Files saved by the [Save] button and opened by the [Open] button on the right of the dialog “\*.mas” should be stored in the same folder.
- (2) When “Stop” is selected in the sequence the process will be paused and the message box shown below pops up. Click “OK” to continue the process.



Figure 11. Sequence Pause Window

## 7. Measurement Results

### [Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (44.1kHz), 256fs (96kHz), 128fs (192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD= DVDD=3.3V, VDDL/R=VREFHL/R=5V
- Interface : Internal DIR (44.1kHz, 96kHz, 192kHz)
- Temperature : Room
- Operational Amplifiers : OPA604

fs=44.1kHz

| Parameter | Input signal | Measurement filter | Results  |   |          |
|-----------|--------------|--------------------|----------|---|----------|
|           |              |                    | Lch      | / | Rch      |
| S/(N+D)   | 1kHz, 0dB    | 20kHz LPF          | 97.5 dB  | / | 97.4 dB  |
| DR        | 1kHz, -60dB  |                    | 113.3 dB | / | 113.4 dB |
|           |              | A-weighted         | 115.7 dB | / | 115.8 dB |
| S/N       | “0” data     | 20kHz LPF          | 113.1 dB | / | 113.2 dB |
|           |              | A-weighted         | 115.6 dB | / | 115.6 dB |

fs=96kHz

| Parameter | Input signal | Measurement filter | Results  |   |          |
|-----------|--------------|--------------------|----------|---|----------|
|           |              |                    | Lch      | / | Rch      |
| S/(N+D)   | 1kHz, 0dB    | 40kHz LPF          | 95.6 dB  | / | 96.1 dB  |
| DR        | 1kHz, -60dB  |                    | 105.9 dB | / | 106.3 dB |
|           |              | A-weighted         | 110.9 dB | / | 111.8 dB |
| S/N       | “0” data     | 40kHz LPF          | 108.9 dB | / | 108.9 dB |
|           |              | A-weighted         | 115.2 dB | / | 115.6 dB |

fs=192kHz

| Parameter | Input signal | Measurement filter | Results  |   |          |
|-----------|--------------|--------------------|----------|---|----------|
|           |              |                    | Lch      | / | Rch      |
| S/(N+D)   | 1kHz, 0dB    | 40kHz LPF          | 94.3 dB  | / | 95.7 dB  |
| DR        | 1kHz, -60dB  |                    | 106.5 dB | / | 105.9 dB |
|           |              | A-weighted         | 112.2 dB | / | 111.6 dB |
| S/N       | “0” data     | 40kHz LPF          | 108.8 dB | / | 108.9 dB |
|           |              | A-weighted         | 115.2 dB | / | 115.4 dB |

## Plots

(fs=44.1kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

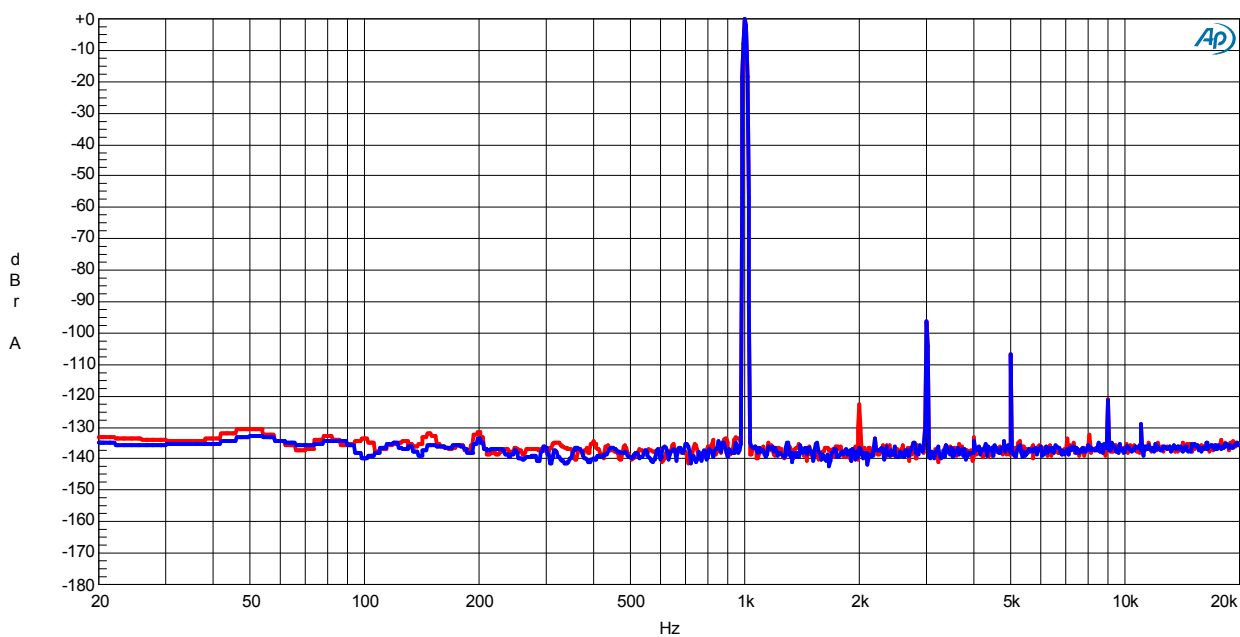


Figure 12. FFT (0dBFS Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

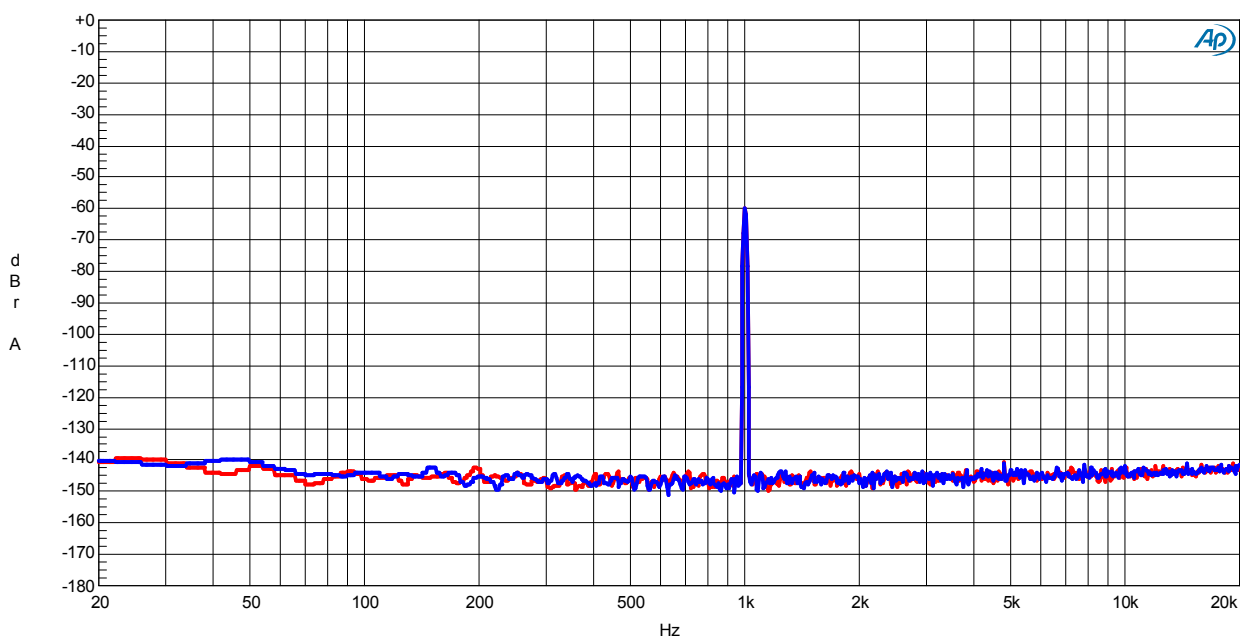


Figure 13. FFT (-60dBFS Input)

(fs=44.1kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

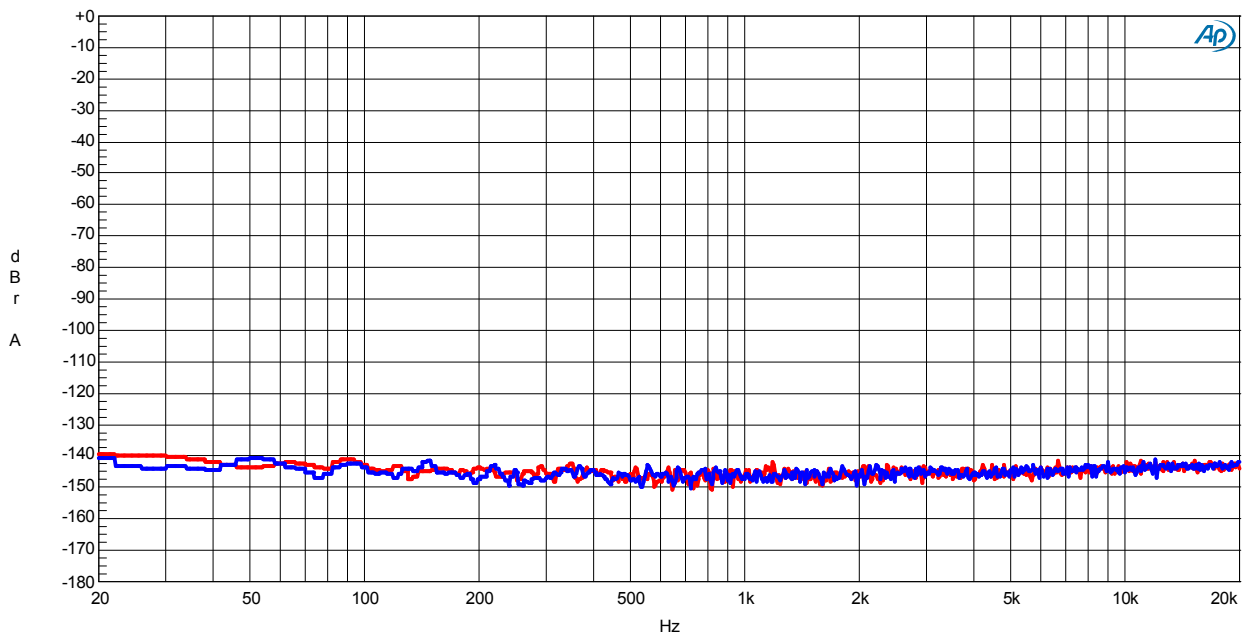


Figure 14. FFT (No Signal Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

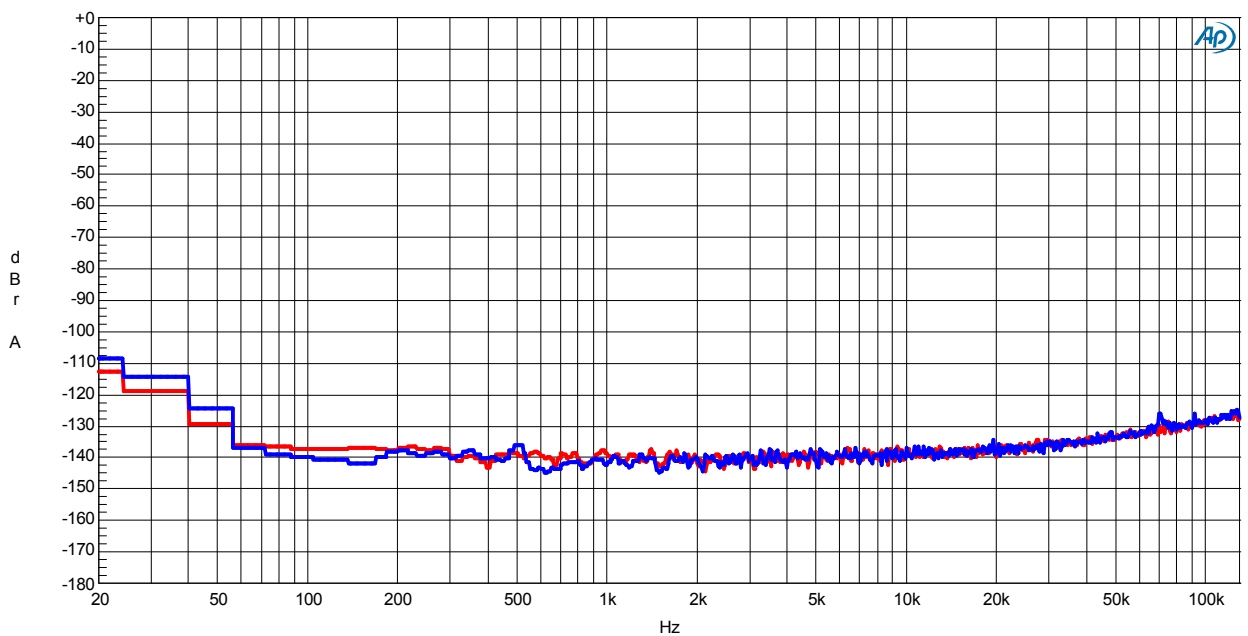


Figure 15. Out of Band Noise

(fs=44.1kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

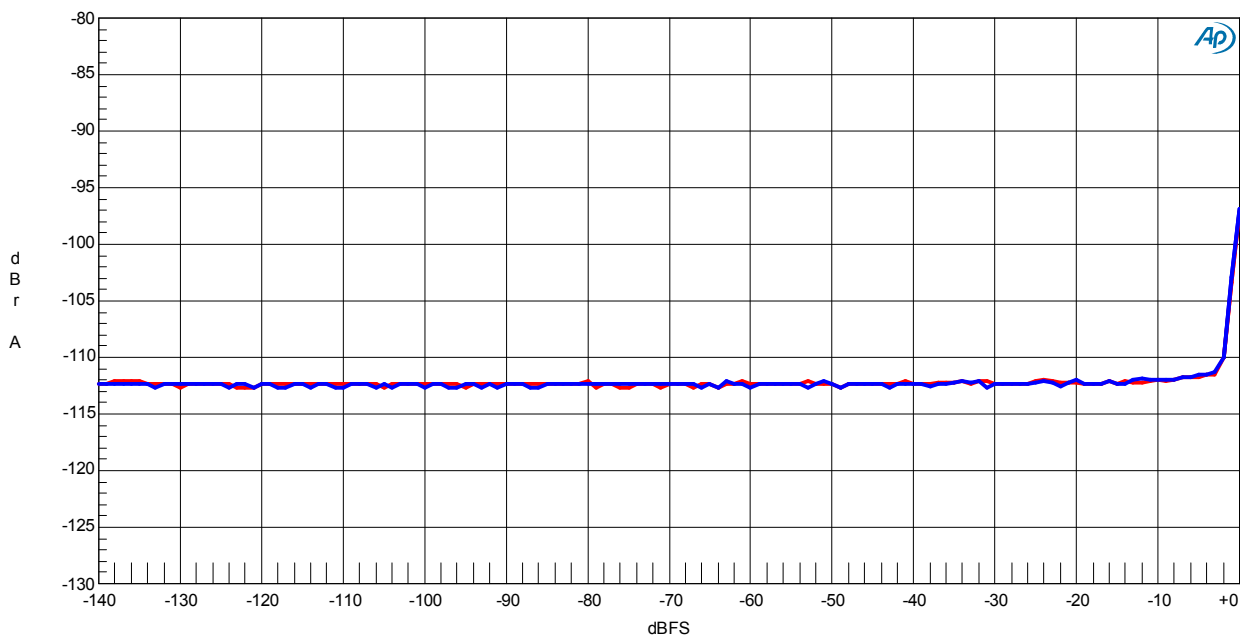


Figure 16. THD+N vs. Input Level

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

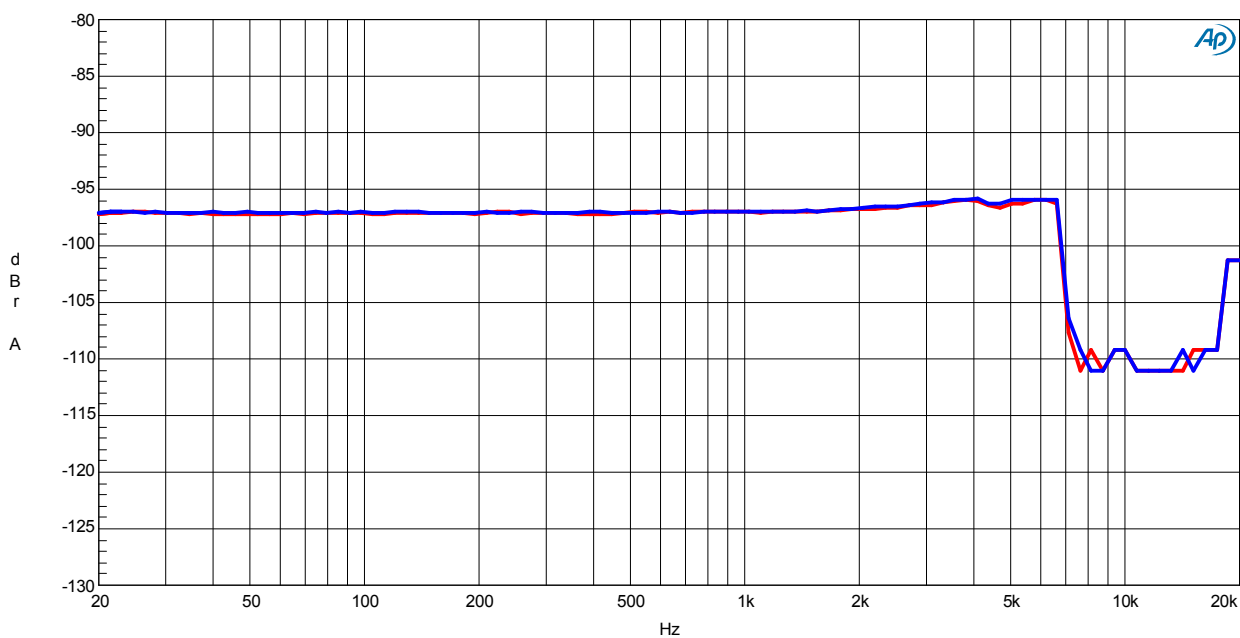


Figure 17. THD+N vs. Input Frequency

(fs=44.1kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

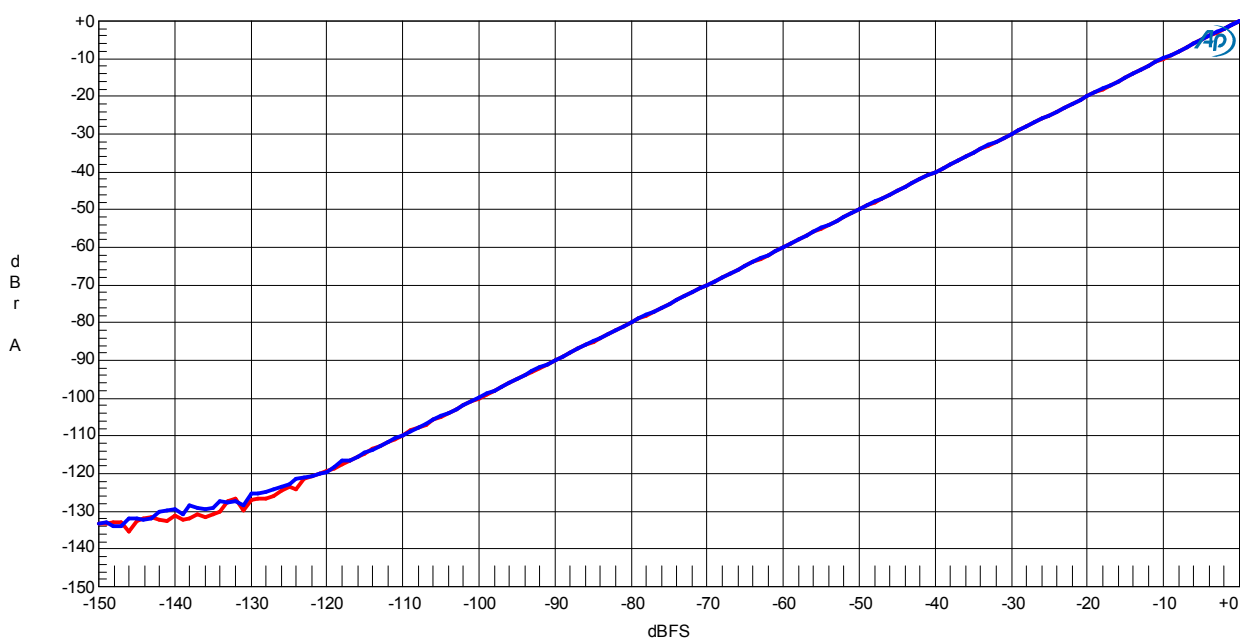


Figure 18. Linearity

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

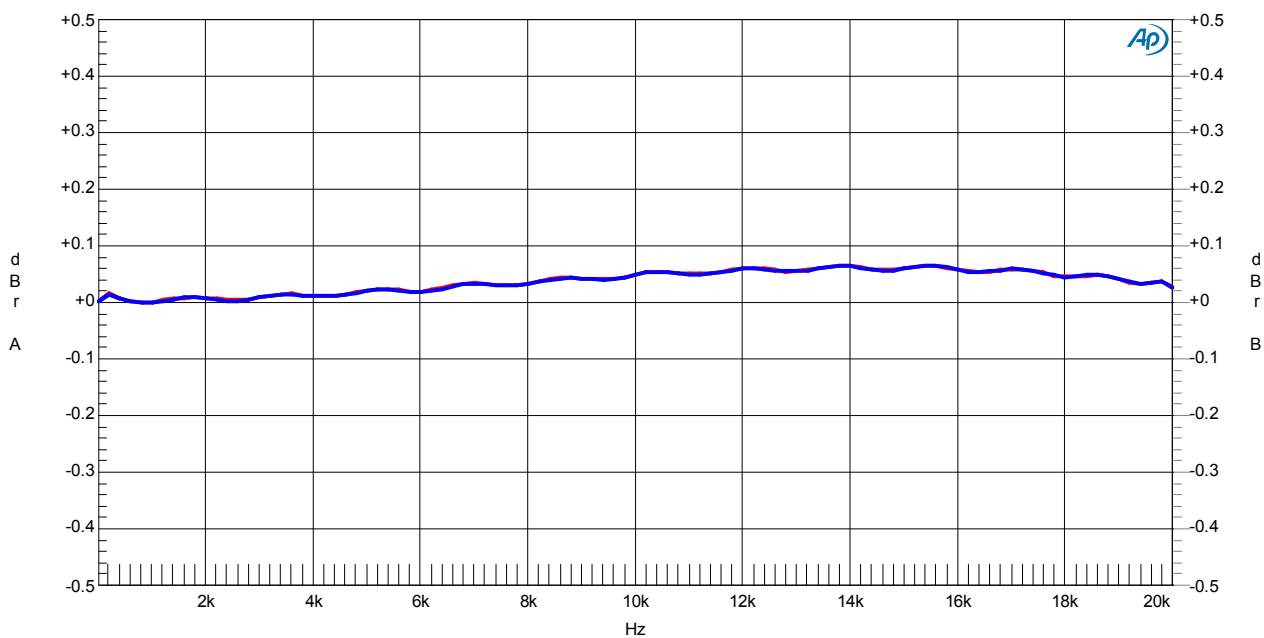


Figure 19. Frequency Response

(fs=44.1kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz

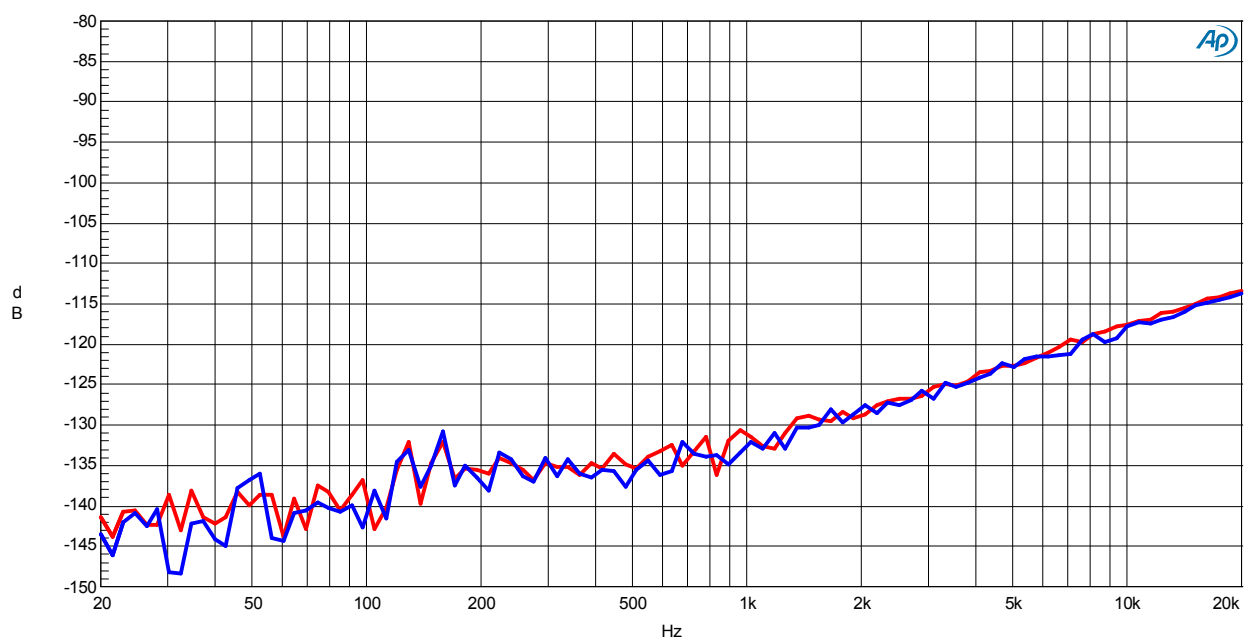


Figure 20. Crosstalk

(fs=96kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

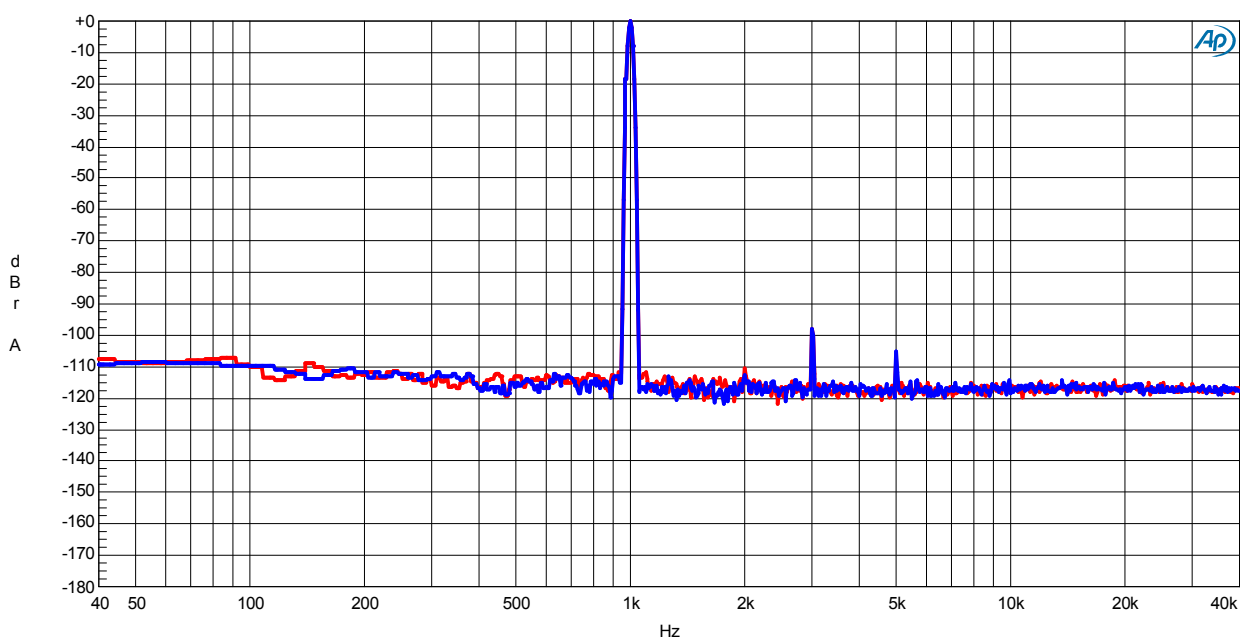


Figure 21. FFT (0dBFS Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

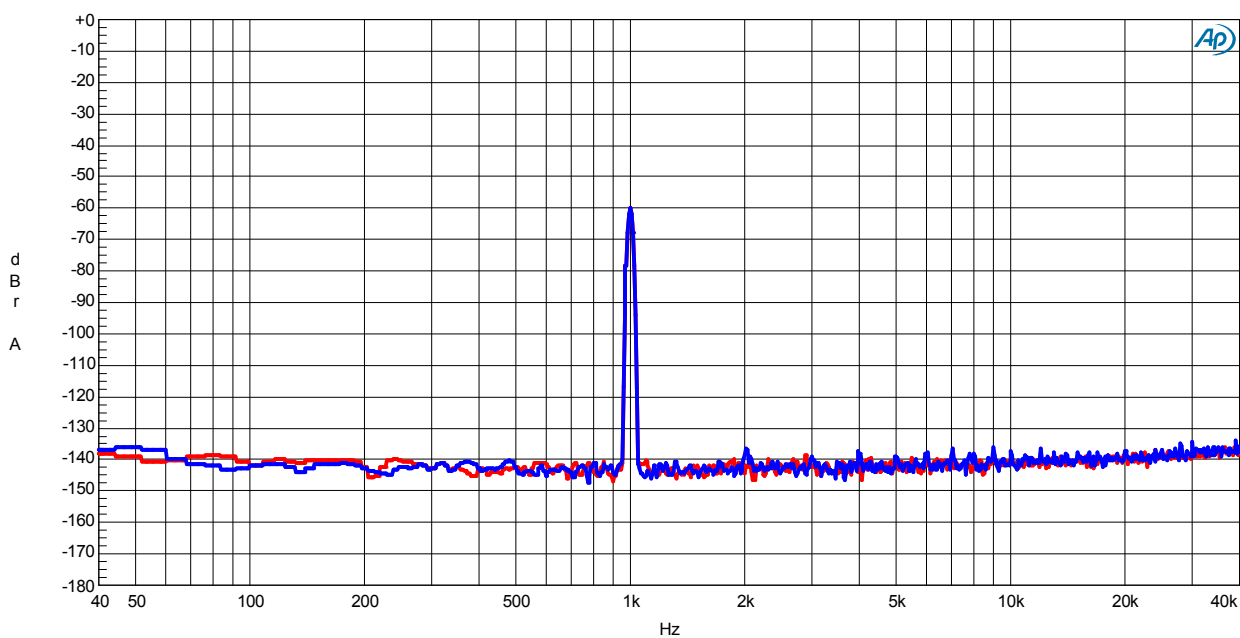


Figure 22. FFT (-60dBFS Input)

(fs=96kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

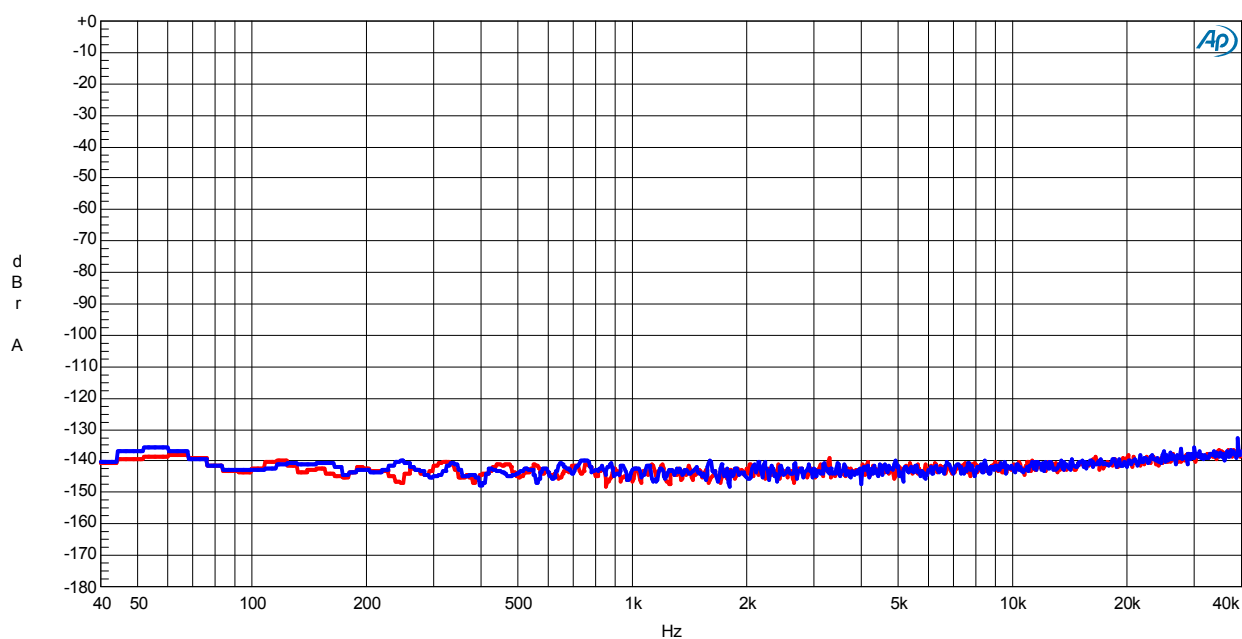


Figure 23. FFT (No Signal Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

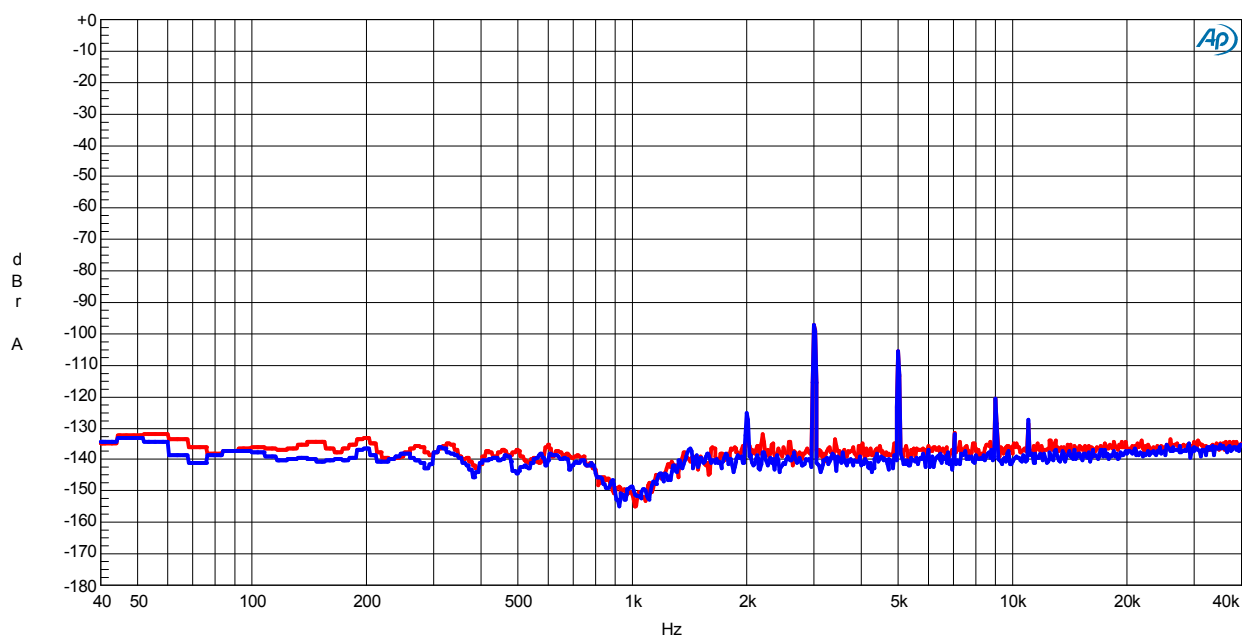


Figure 24. FFT (0dBFS Input, Notch)

(fs=96kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

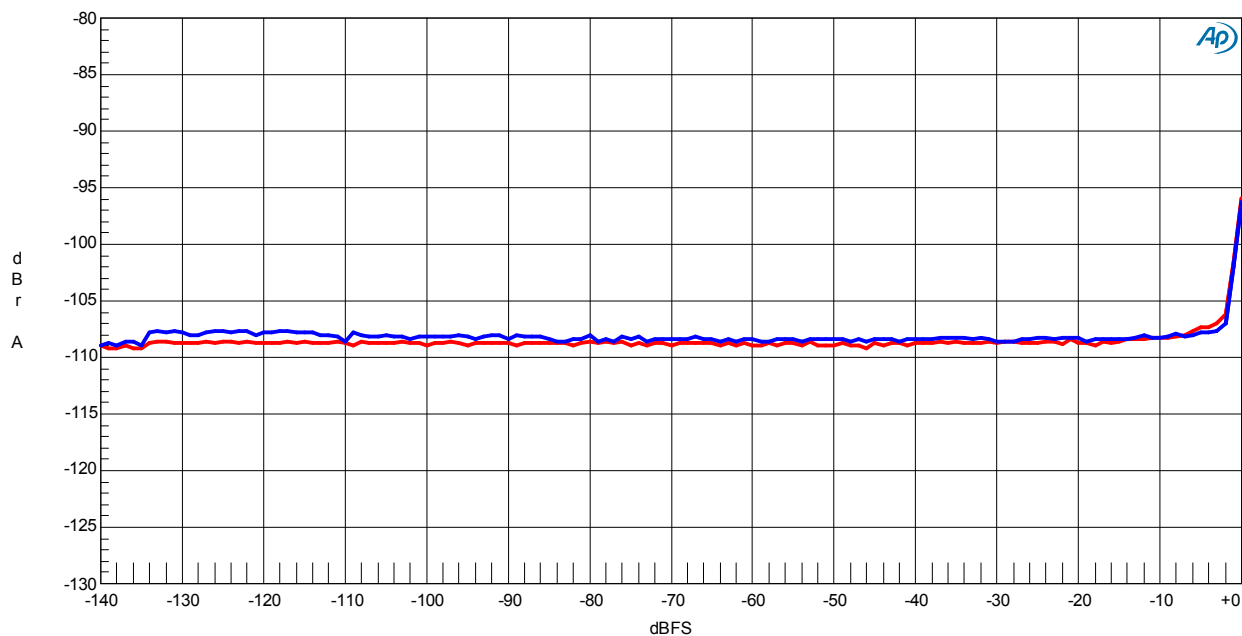


Figure 25. THD+N vs. Input Level

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

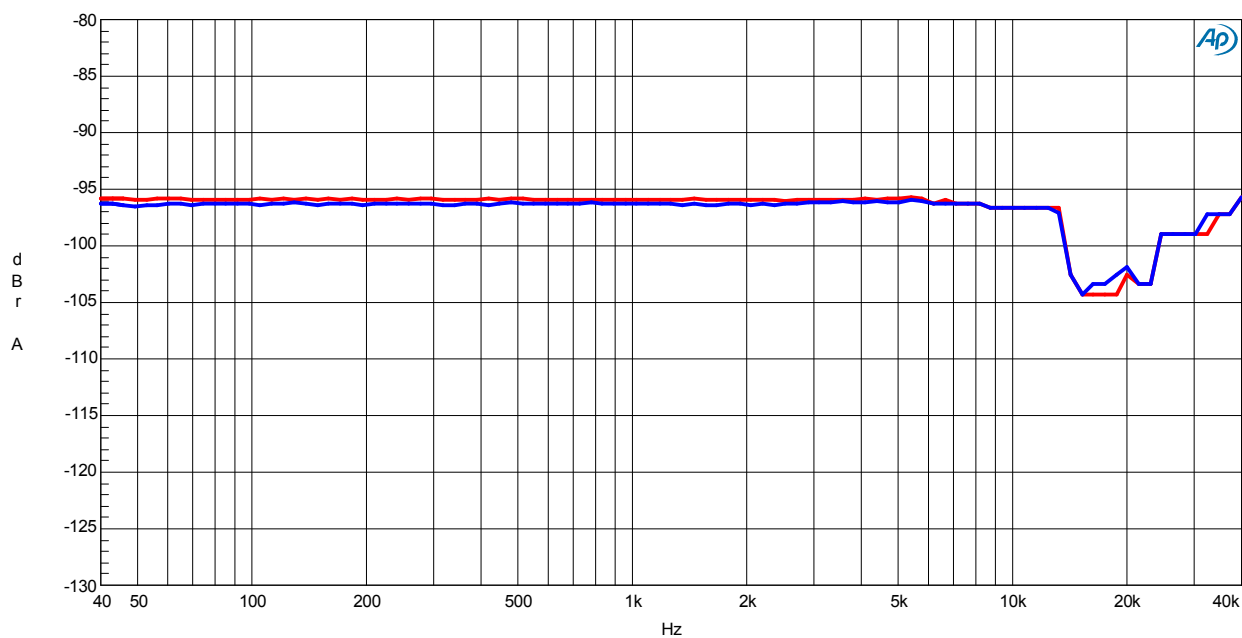


Figure 26. THD+N vs. Input Frequency

(fs=96kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

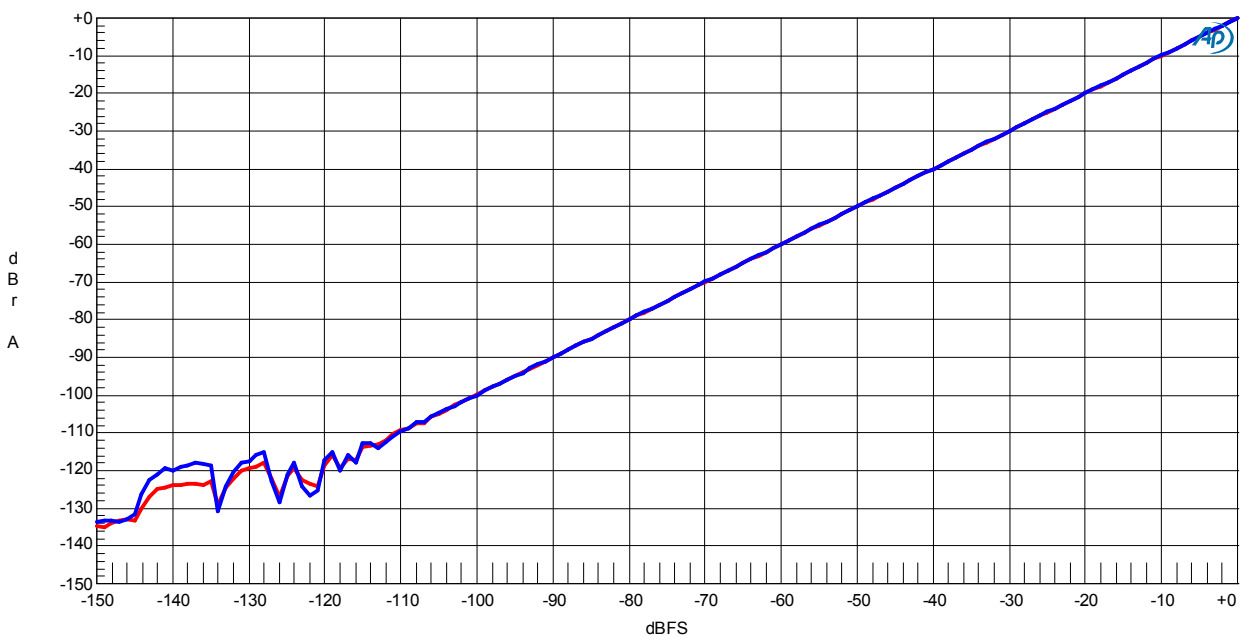


Figure 27. Linearity

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

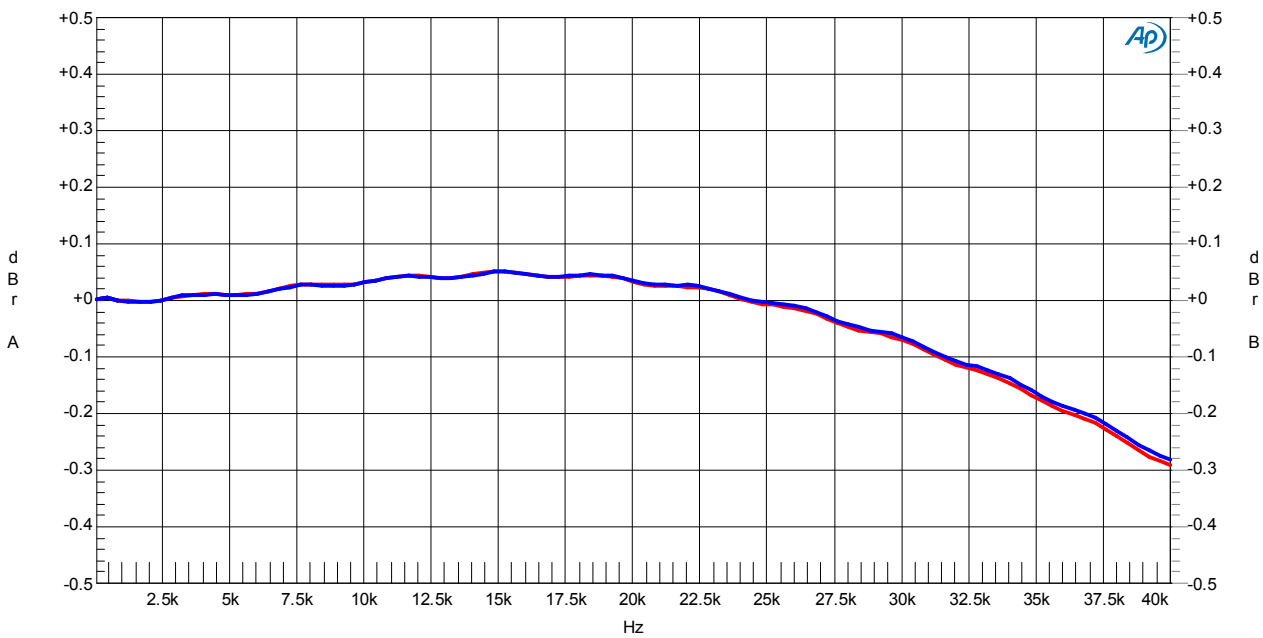


Figure 28. Frequency Response

(fs=96kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

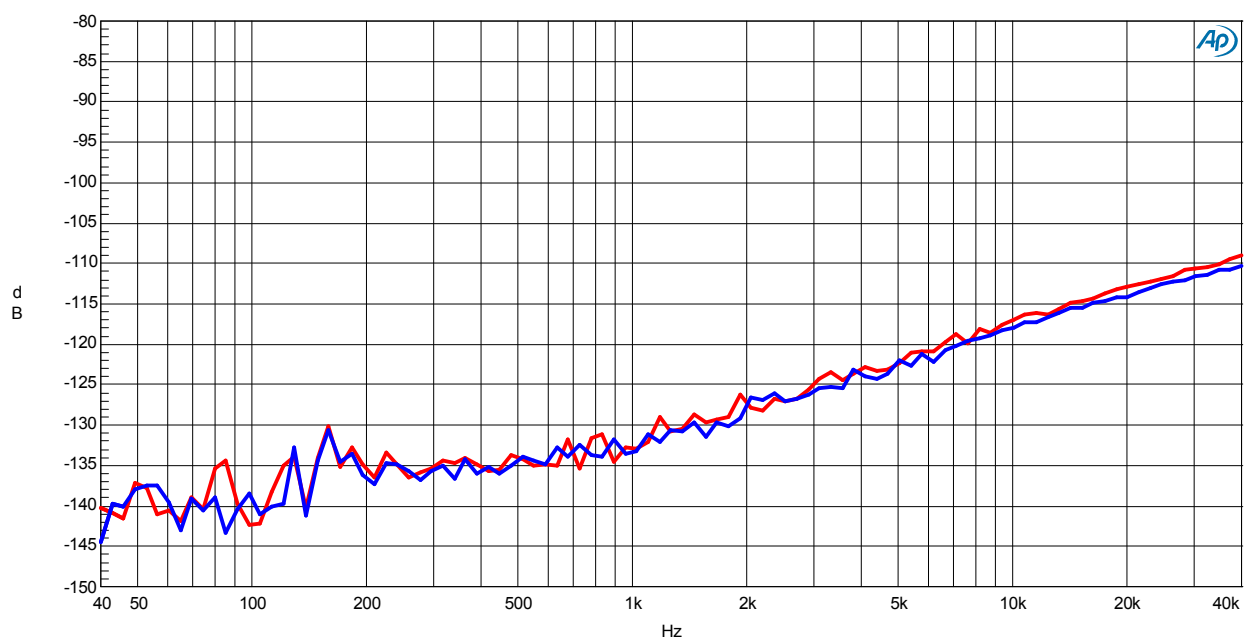


Figure 29. Crosstalk

(fs=192kHz)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

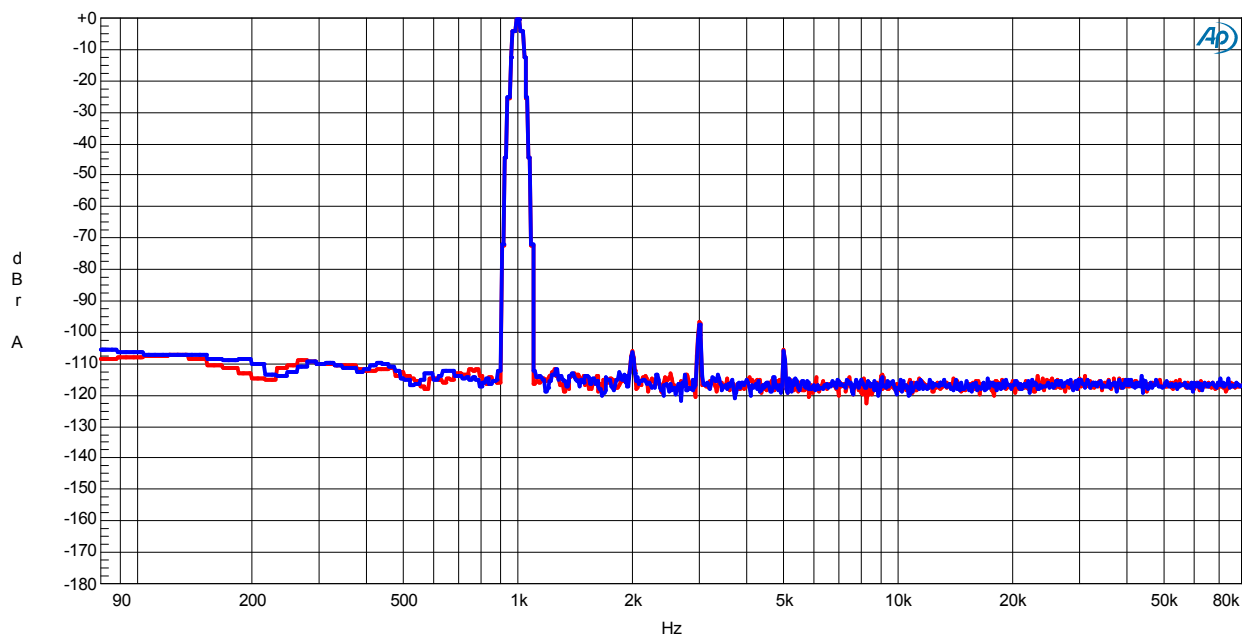


Figure 30. FFT (0dBFS Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

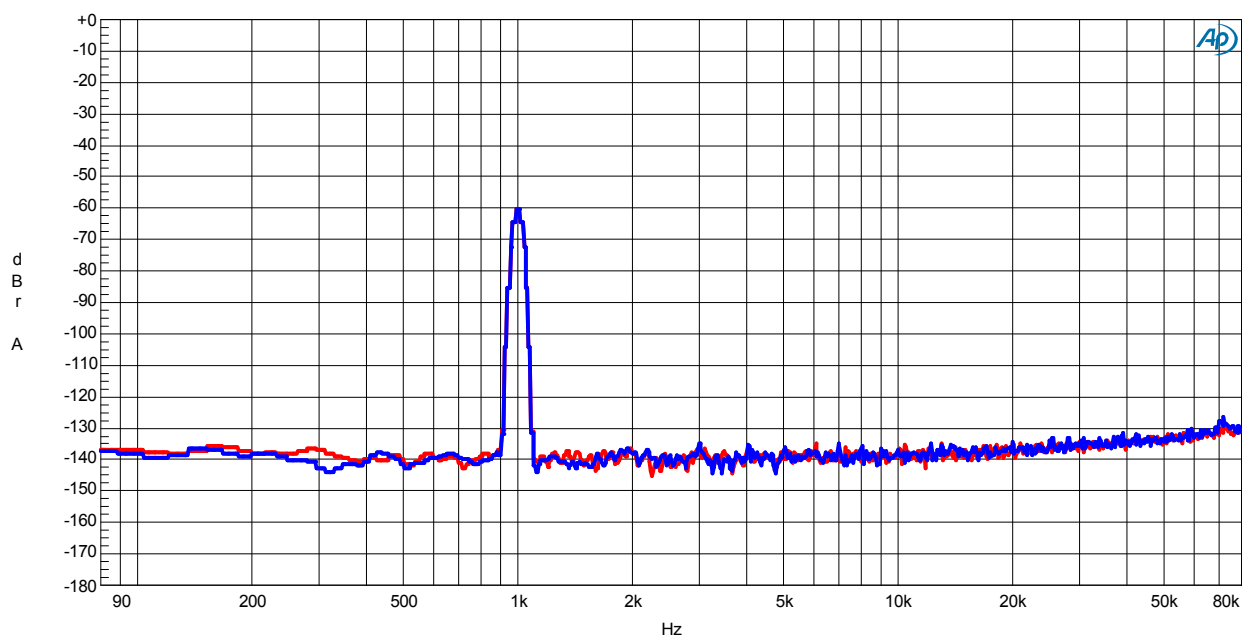


Figure 31. FFT (-60dBFS Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

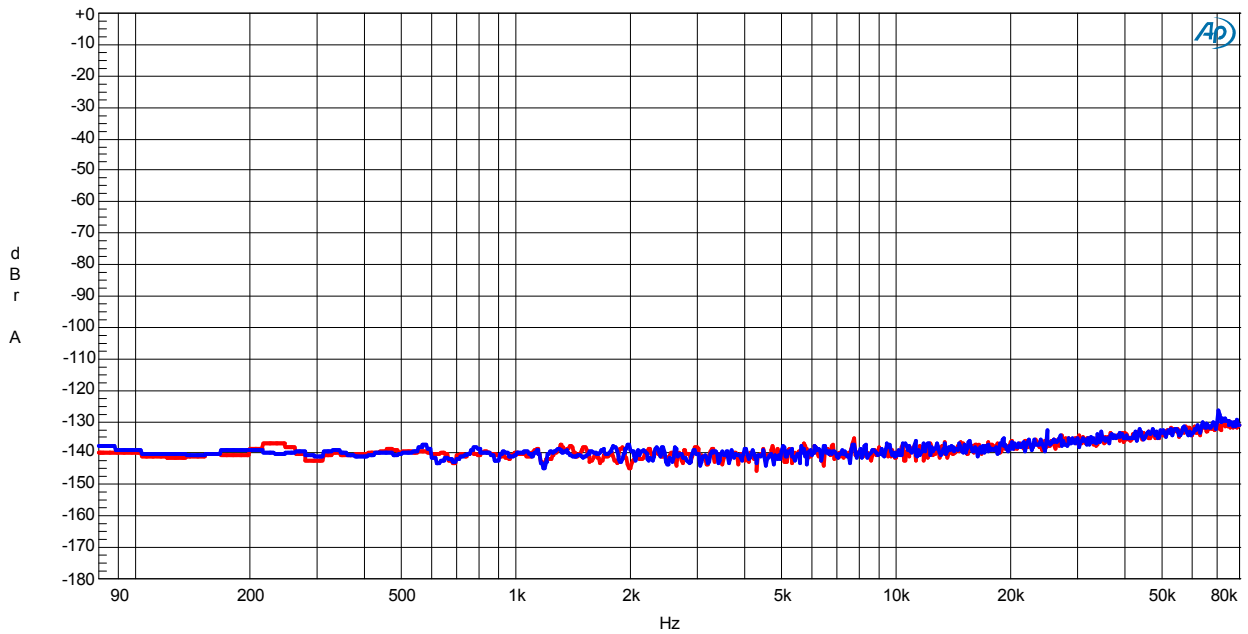


Figure 32. FFT (No Signal Input)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

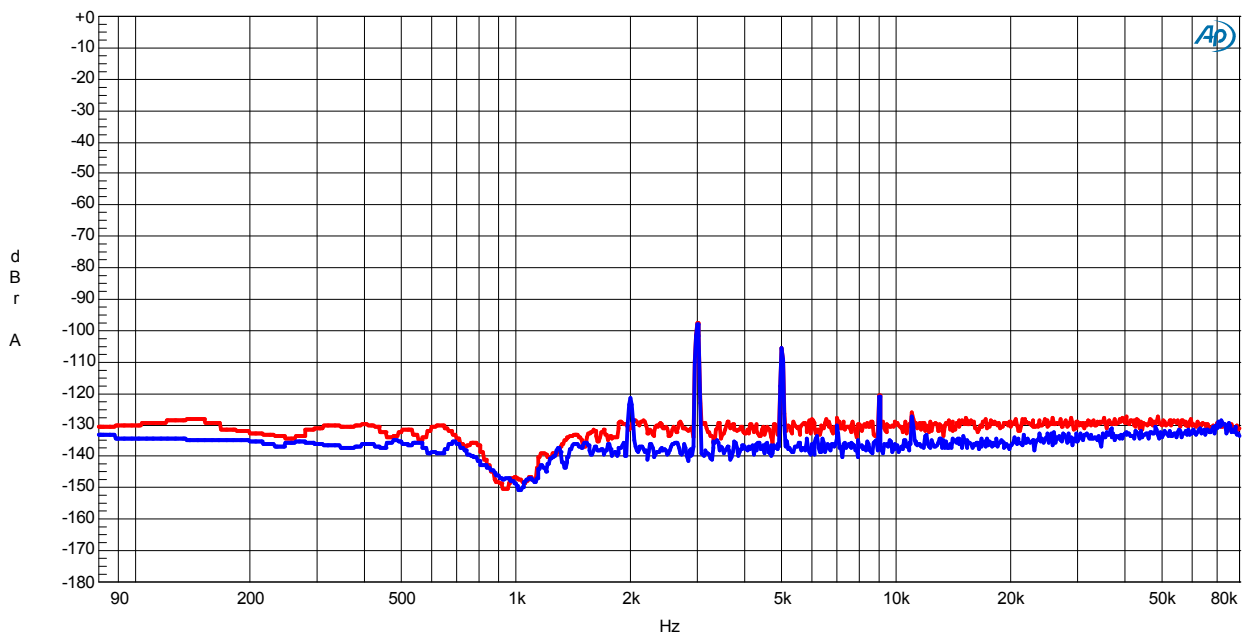


Figure 33. FFT (0dBFS Input, Notch)

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

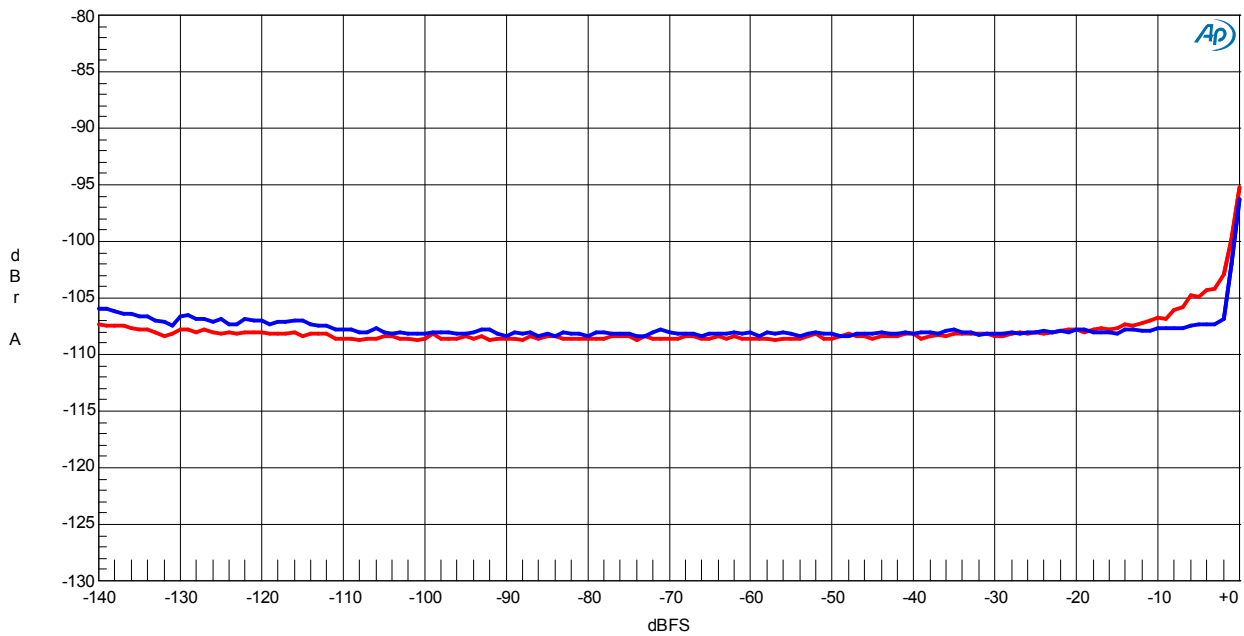


Figure 34. THD+N vs. Input Level

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

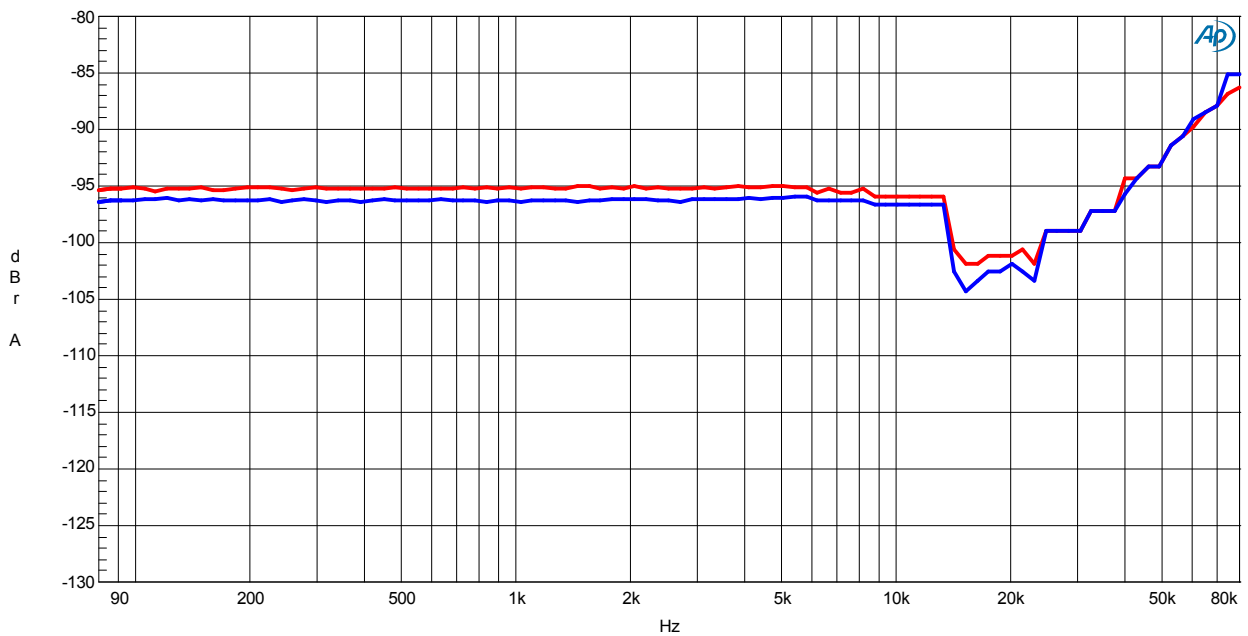


Figure 35. THD+N vs. Input Frequency

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

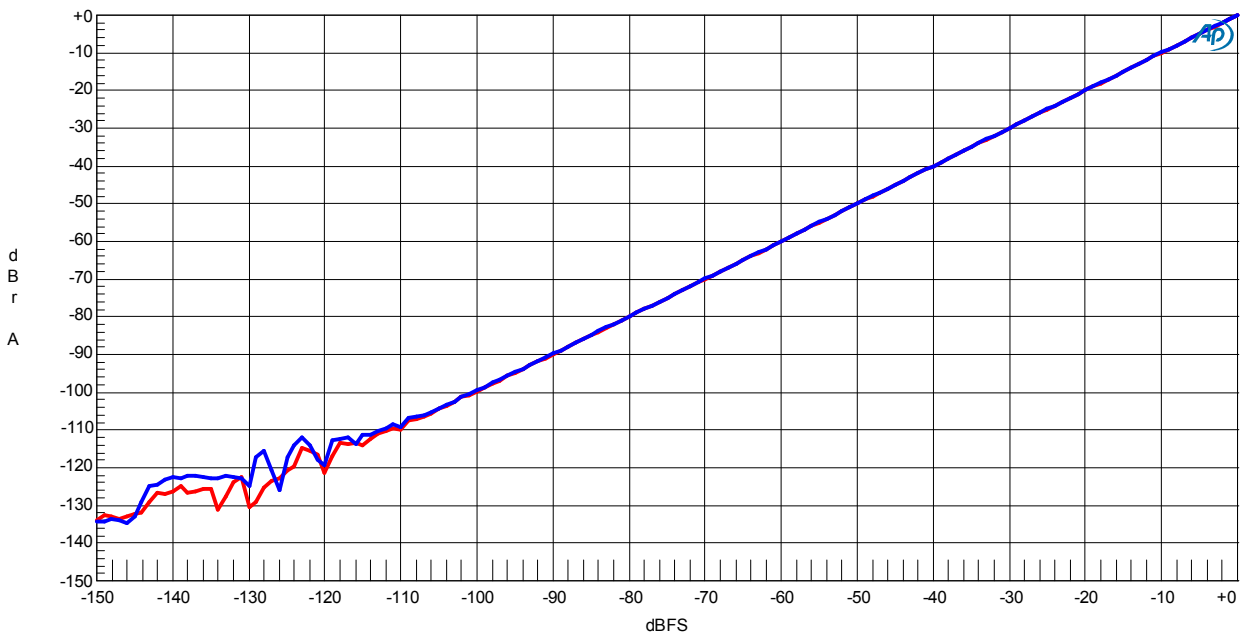


Figure 36. Linearity

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

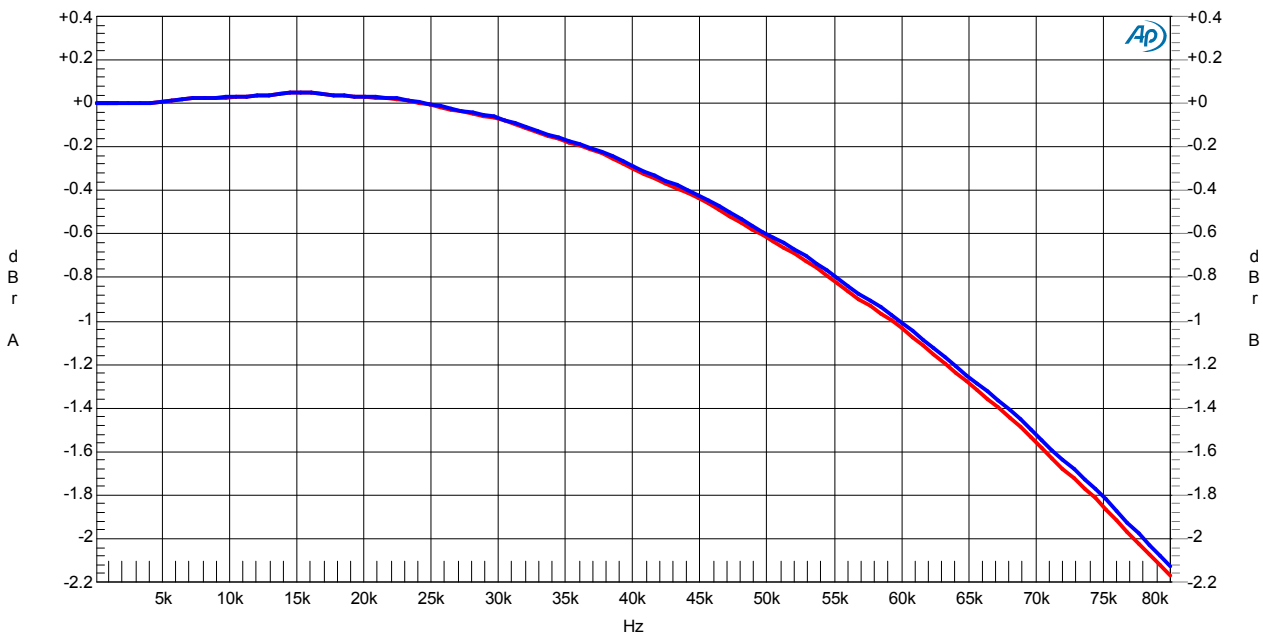


Figure 37. Frequency Response

AKM

AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

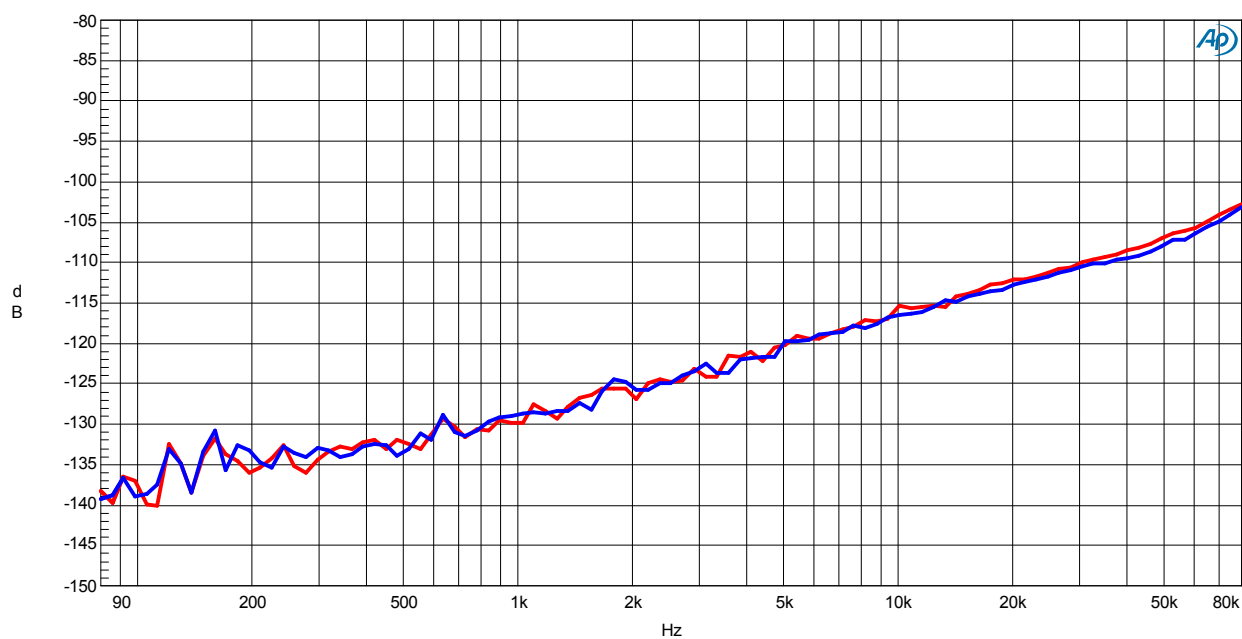


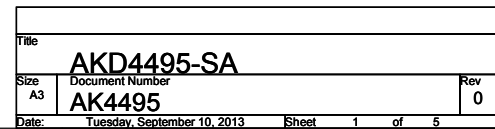
Figure 38. Crosstalk

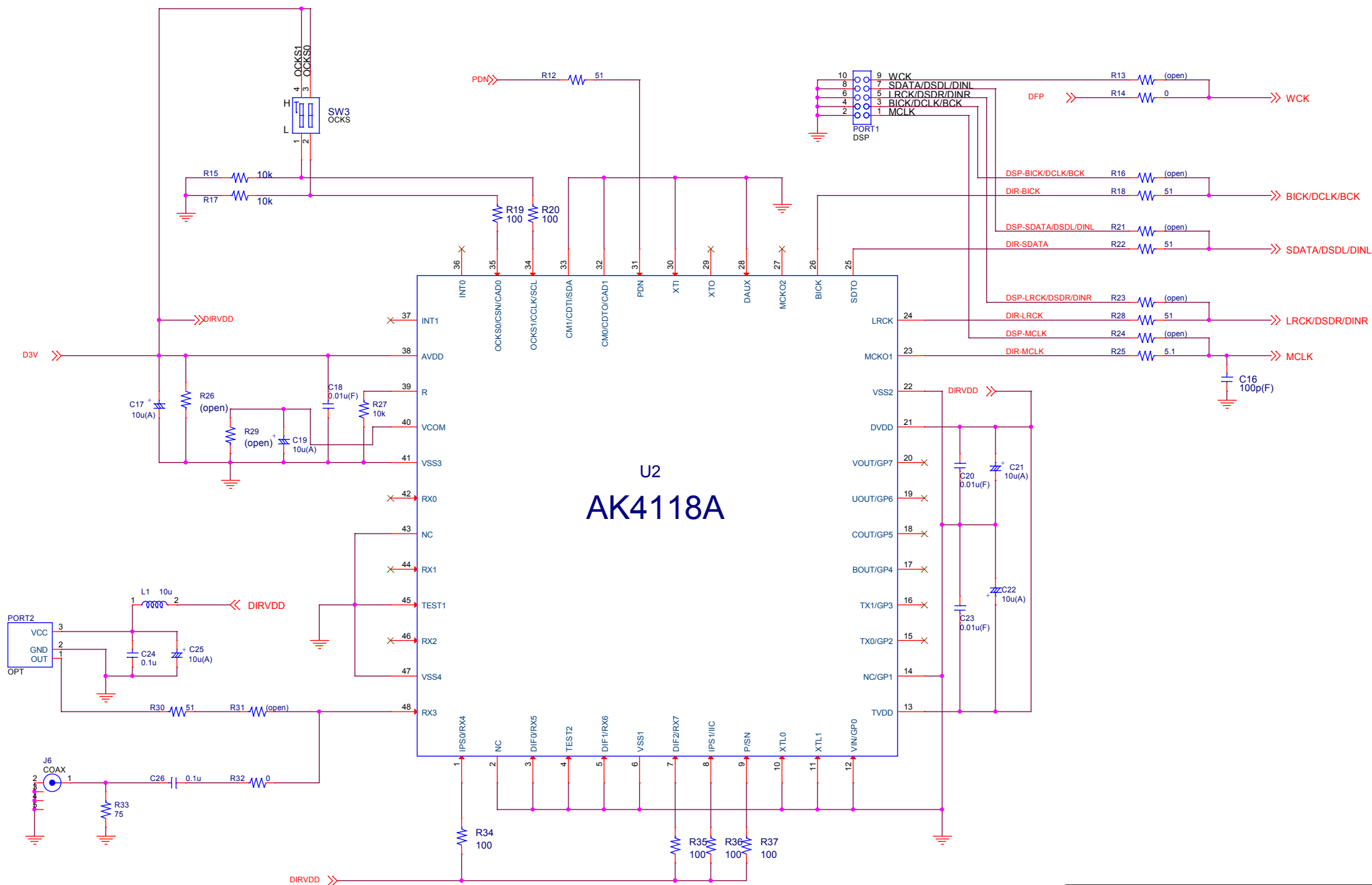
**8.Revision History**

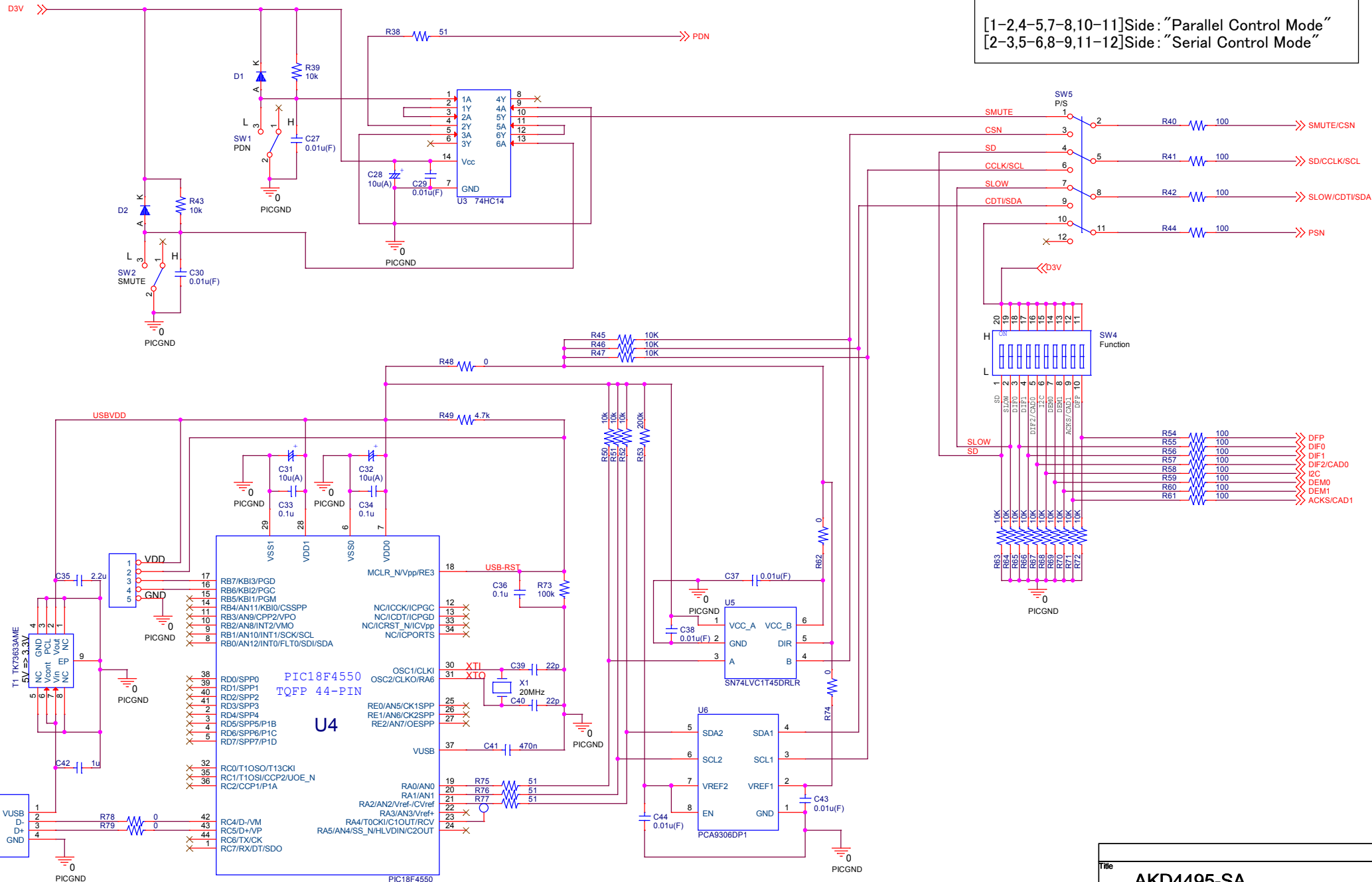
| Date<br>(YY/MM/DD) | Manual<br>Revision | Board<br>Revision | Reason        | Page | Contents |
|--------------------|--------------------|-------------------|---------------|------|----------|
| 13/09/13           | KM113800           | 0                 | First edition | -    |          |

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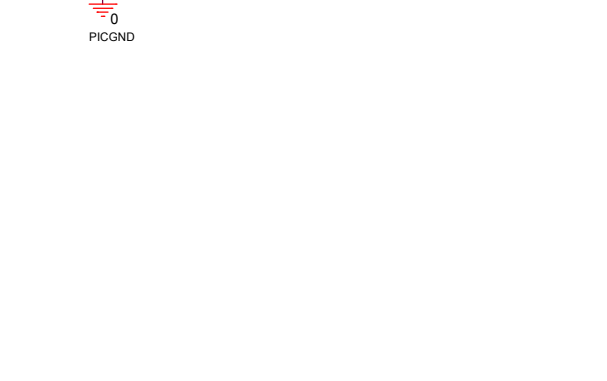
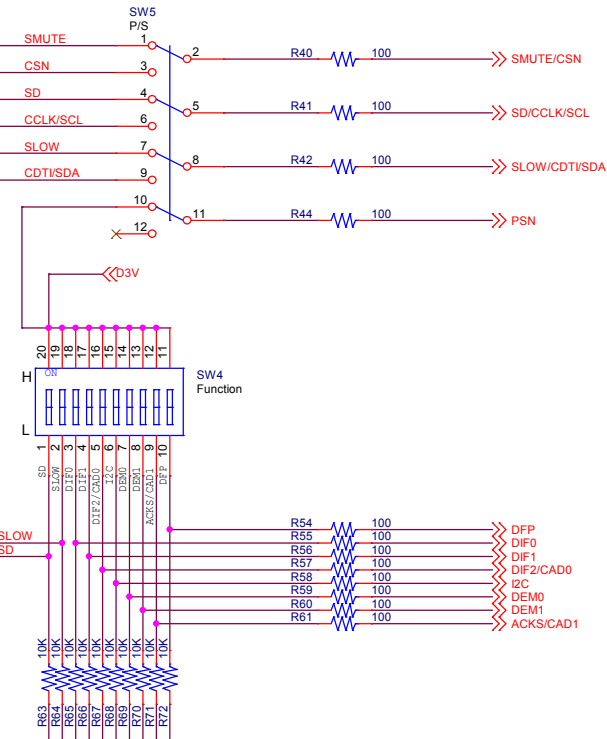






# SW5 Silk-Screen

[1-2,4-5,7-8,10-11]Side: "Parallel Control Mode"  
[2-3,5-6,8-9,11-12]Side: "Serial Control Mode"



|       |                             |                 |          |
|-------|-----------------------------|-----------------|----------|
| Title |                             | AKD4495-SA      |          |
| Size  | A3                          | Document Number | PIC & SW |
| Date  | Tuesday, September 10, 2013 | Sheet           | 3 of 5   |
| Rev   | 0                           |                 |          |

