ULTRAANALOG, INC.

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Application Note

AP02

Timing and Interface Requirements

for implementing

DAC D18400, DAC D20200, DAC D20400

family of D/A Converters for high performance audio applications

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DAC D18400 / DAC D20200 / DAC D20400

Application Note AP-02
Timing & Interface Requirements

The DAC D18400, DAC D20200, & DAC D20400 are Digital Audio D/A Converter Subsystems that include two complete *20 Bit D/A Converters, a stable bipolar reference, a serial CMOS/TTL compatible interface circuit and two distortion-suppressing output deglitcher amplifiers. This application note describes the digital timing and interface requirements for the DAC D18400, DAC D20200, & DAC D20400.
*18 bit for the DAC D18400

1. DIGITAL INPUT SIGNALS

A. Dynamic Timing and Control Signals

CLKL:
This is the bit clock that shifts left channel data into the left shift register. The active edge is the rising edge if CLKX is low or the falling edge if CLKX is high. For CLKL to be active, the $\overline{\text{LEFT}}$ signal must be low.

CLKR:
This is the bit clock that shifts right channel data into the right shift register. The active edge is the rising edge if CLKX is low or the falling edge if CLKX is high. For CLKR to be active, the RIGHT signal must be high.

DATAL:
The serial data for the left channel, from 16 to 32 bits, MSB first.

DATAR:
The serial data for the right channel, from 16 to 32 bits, MSB first.

$\overline{\text{LEFT}}$:
The gating input for CLKL active low, internal pull-down, DELAY = "0".

RIGHT:
The gating input for CLKR active high, internal pull-up, DELAY = "0".

WS/$\overline{\text{LOAD}}$: DELAY = "0".
Data for both channels is strobed from the 20 bit shift registers into the 20 bit parallel latches on one of the falling edge(s) as described;
- If (CLKL * CLKR) is logic 0, then data is strobed on the falling edge of WS/$\overline{\text{LOAD}}$.
- If (CLKL + CLKR) is logic 1 when WS/$\overline{\text{LOAD}}$ falls, then data is strobed with the next falling edge of CLKL or CLKR.

HOLD: (Independent signals for left and right channels)
The Hold control signal(s) independently freeze the output(s) of each DAC during the time that new data words are internally transferred and DAC "glitches" are settling. The Hold signal(s) control the output deglitcher mode by placing the deglitcher in the hold mode as logic "1". After the Hold signal(s) return to logic "0", the D/A Converter outputs will exponentially change to the new amplitude.
(Further information on the HOLD signal appears in section 5.)

B. Static Control Signals

The following five lines are set at fixed values (logic 1 or 0) in order to select the desired operating mode of the DAC D18400, DAC D20200, or DAC D20400.

(MSBX, DATAX):
These two lines are used to select the desired digital data coding.

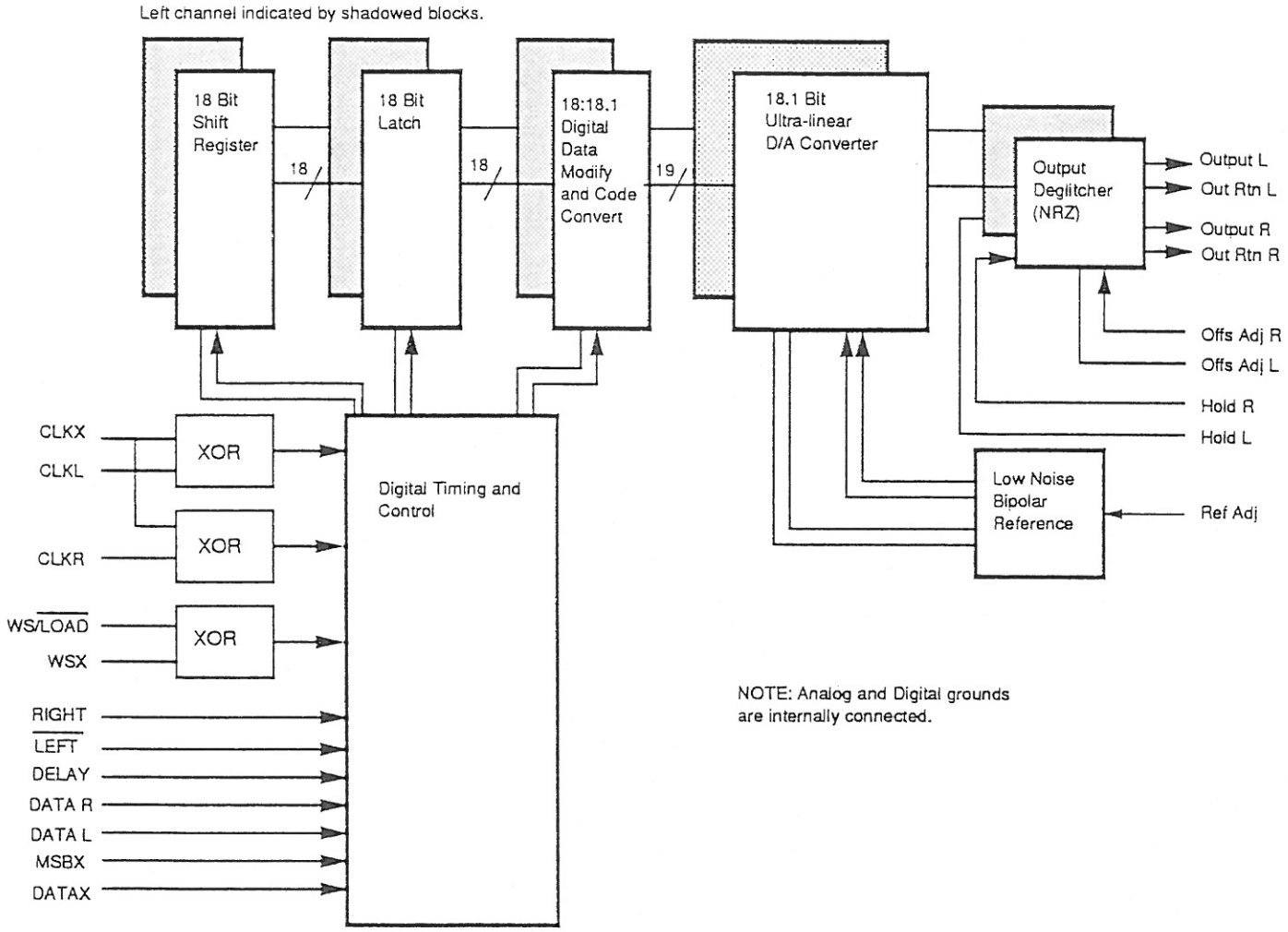
(0, 0) for Offset Binary.
(0, 1) for Complementary 2's Complement.
(1, 0) for 2's Complement.
(1, 1) for Complementary Offset Binary.

WSX:
This line determines which edge of the WS/$\overline{\text{LOAD}}$ signal is active. All timing diagrams assume that WSX=0. If WSX=1, the state of the WS/$\overline{\text{LOAD}}$ must be inverted in the diagrams.

CLKX:
This signal inverts the two clocks CLKL and CLKR. All timing diagrams assume CLKX=0. If CLKX=1, the state of the CLKL and CLKR must be inverted in the diagrams.

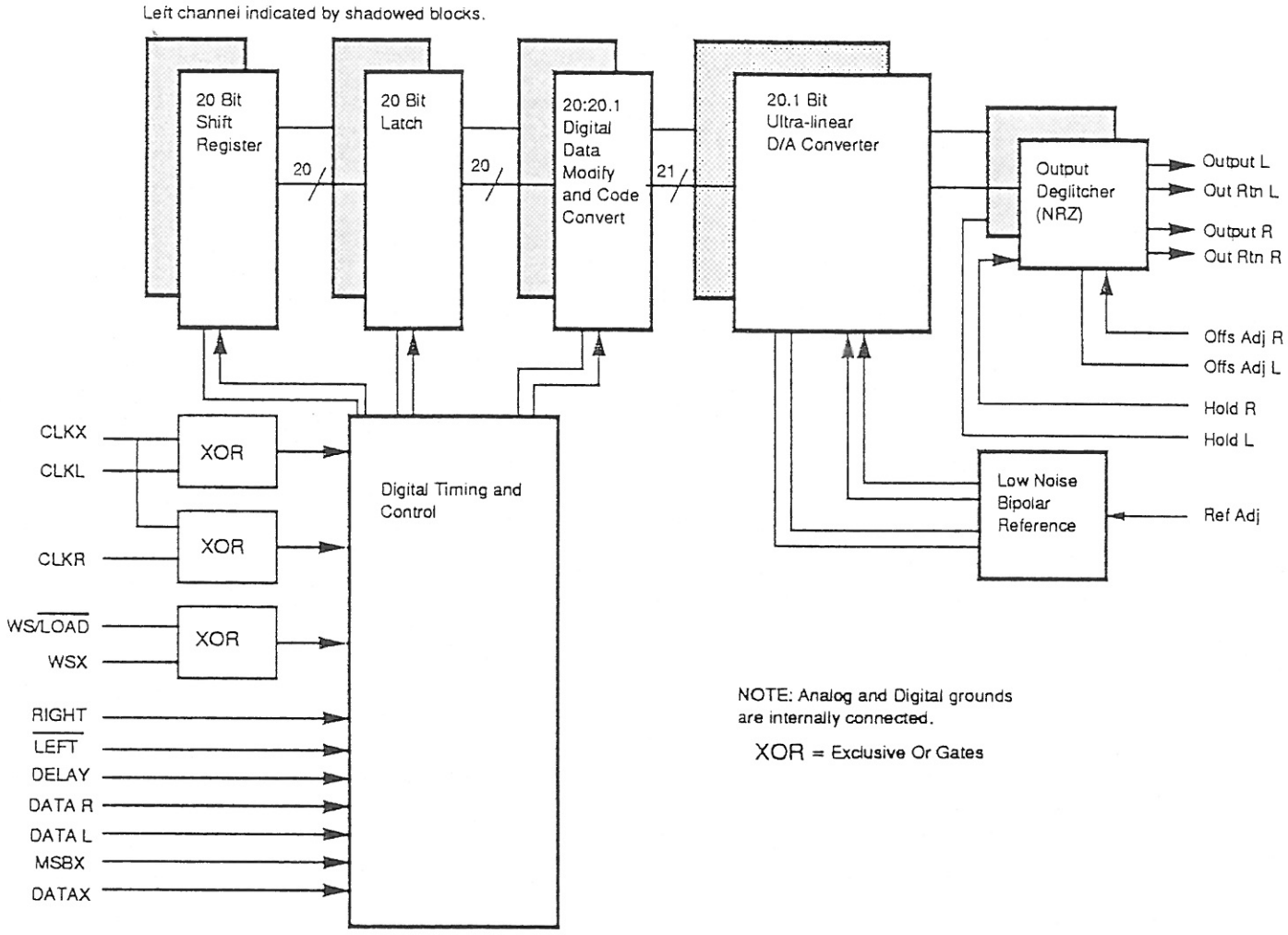
DELAY:
DELAY will cause the $\overline{\text{LEFT}}$, RIGHT and WS/$\overline{\text{LOAD}}$ to be delayed by one clock cycle inside the DAC D18400, DAC D20200, or DAC D20400.

2. DAC D18400 BLOCK DIAGRAM



XOR = Exclusive Or Gates

3. DAC D20200 & DAC D20400 BLOCK DIAGRAM



4. TIMING DIAGRAMS (For typical applications)

A number of possible timing configurations are presented.

	min		min	max
Tkl	25 ns	Tlsu	20 ns	
Tkh	25 ns	Tlho	0 ns	
Tdsu	20 ns	Tll	30 ns	
Tdho	0 ns	Thsu	5 ns	500 ns
		Thho	2 µS	

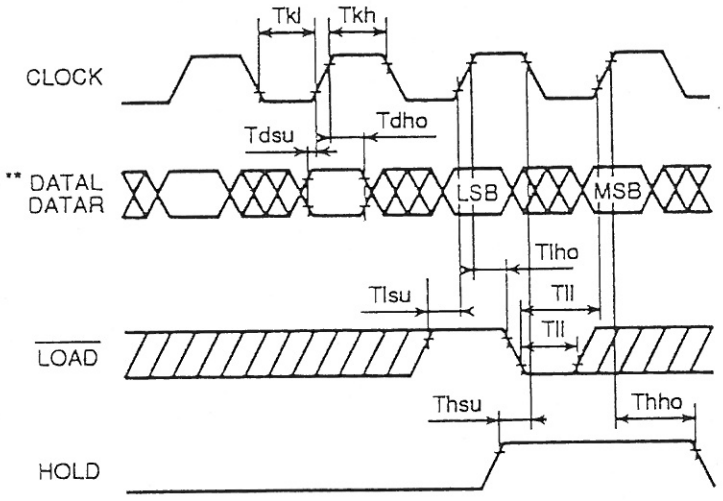
The optimum hold period, Thho, for the DAC D20200 is 2 µS.
The optimum hold period, Thho, for the DAC D18400 and DAC D20400 is 1.5µS.

4.1. Simultaneous.

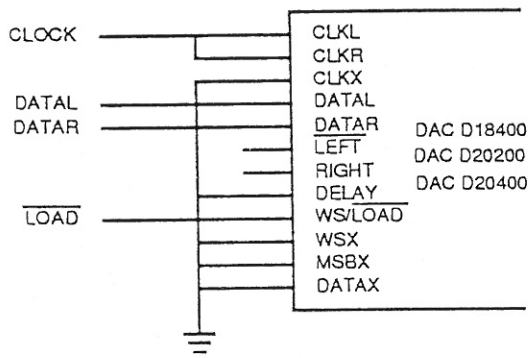
(For use with serial data circuits compatible with the industry standard, 16 Bit, PCM 56 manufactured by Burr Brown Corporation.)

In this application, the digital audio system applies left and right channel data simultaneously to the DATAL and DATAR inputs. A single clock is applied to both the CLKL and CLKR inputs. Data bits are loaded into an input shift register inside of the DAC D18400, DAC D20200, or DAC D20400 with each rising edge of the clock. The output of the shift register is then transferred to a parallel data register with the falling edge of the $\overline{\text{LOAD}}$ signal. Once data is transferred, the DAC D18400, DAC D20200 or DAC D20400 module converts the digital input data into an appropriate analog output voltage. During the period that the D/A converters are settling, the Hold signals place the output deglitchers into the "hold" mode thereby freezing the analog outputs. In most applications, an output filter will be used to remove the sampling frequency components found in the analog output waveform.

TIMING DIAGRAM:



CONNECTION DIAGRAM:



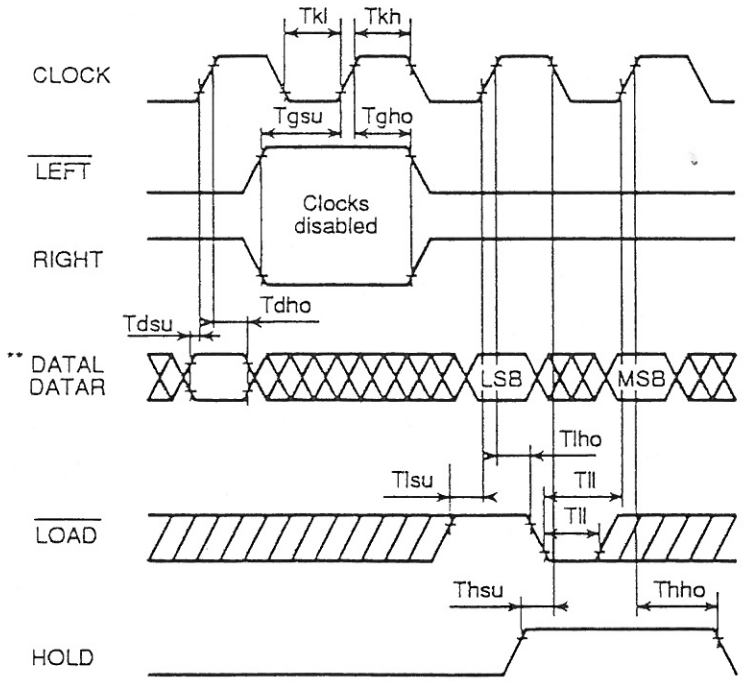
** The two data words are presented simultaneously. The MSB for each data word appears first and the LSB last.

4.2 Simultaneous / Continuous Clock / Gated.

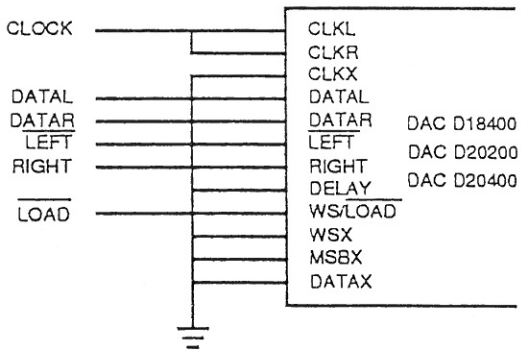
(This mode of operation satisfies certain applications that include the Motorola DSP56000 family of digital signal processors.)

In this application, the digital audio system applies left and right channel data simultaneously to the DATAL and DATAR inputs. A single *continuous* clock is applied to both the CLKL and CLKR inputs. Data bits are loaded into an input shift register with each rising edge of the clock. The output of the shift register is then transferred to a parallel data register with the falling edge of the LOAD signal, and the data is converted. The CLKL is disabled when the $\overline{\text{LEFT}}$ input becomes logic "1". The CLKR is disabled when the RIGHT becomes logic "0". During the period that the D/A converters are settling, the Hold signals place the output deglitchers into the "hold" mode thereby freezing the analog outputs.

TIMING DIAGRAM:



CONNECTION DIAGRAM:

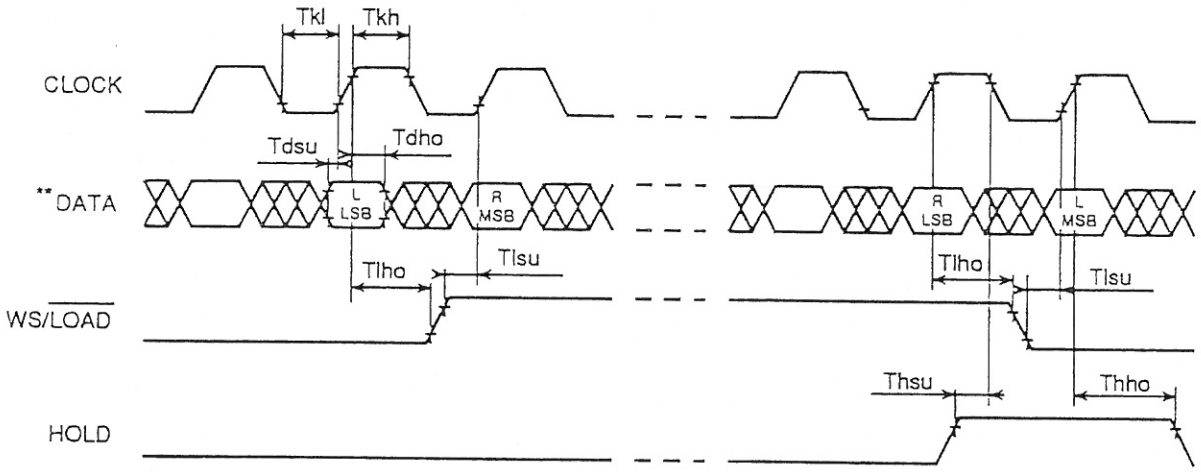


**The two data words are presented simultaneously. The MSB for each data word appears first and the LSB last.

4.3 Multiplexed.

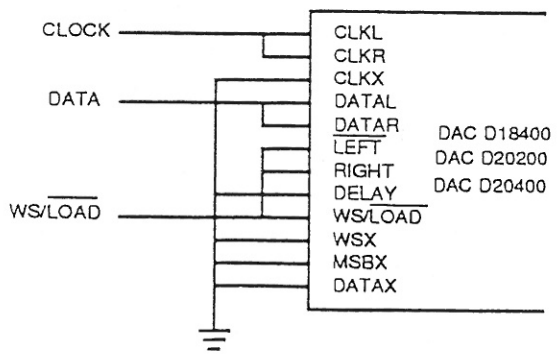
A single input data line provides multiplexed left and right channel data. Left channel data must appear first, followed by right channel data. The WS/$\overline{\text{LOAD}}$ control line allows left channel data to be clocked as logic "0" and right channel data to be clocked as logic "1". Data from both channels is transferred to parallel data registers on the falling edge of the WS/$\overline{\text{LOAD}}$ line and then converted. During the period that the D/A converters are settling, the Hold signals place the output deglitchers into the "hold" mode, thereby freezing the analog outputs.

TIMING DIAGRAM:



**The first data word is Left Channel with MSB first and LSB last. The next data word is Right Channel with MSB first and LSB last, etc.

CONNECTION DIAGRAM:



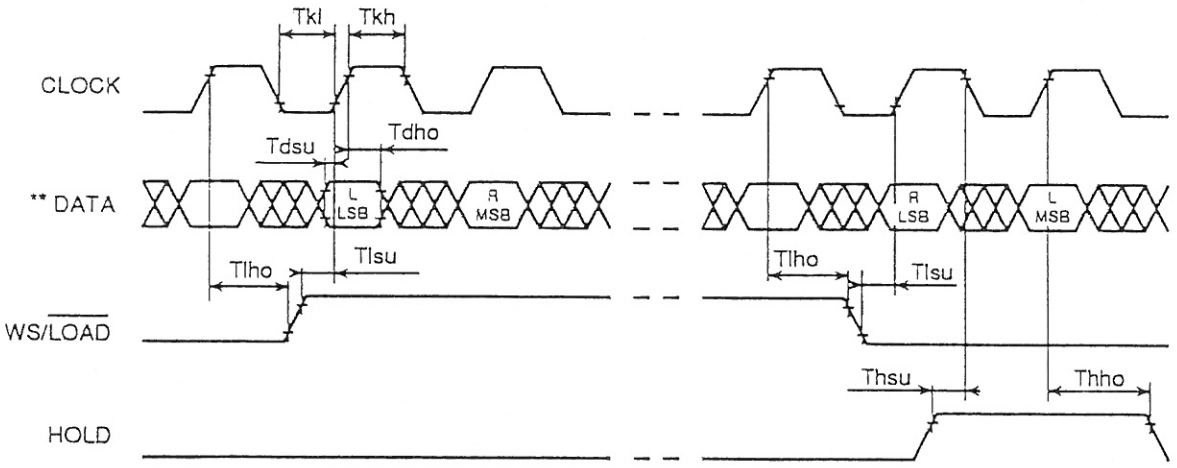
4.4 Multiplexed / Delay.

(For use with serial data circuits compatible with the industry standard Philips TDA-1541A D/A converter, when operated in the time multiplexed format.).

This operating mode is nearly identical to the Multiplexed mode described in section 3.3. The main difference is that the WS/$\overline{\text{LOAD}}$, $\overline{\text{LEFT}}$ and RIGHT control signals are internally delayed by one clock cycle. Therefore, the user must change the state of these inputs one clock cycle ahead of the desired time. Data is strobed from the *20 bit shift registers into the *20 bit parallel latches. Data transfer occurs with the falling edge of (CLKL + CLKR) which follows the rising edge of (CLKL + CLKR) which follows the falling edge of WS/$\overline{\text{LOAD}}$.

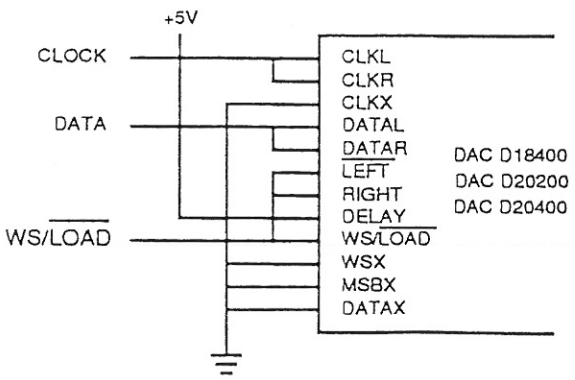
* 18 bits for the DAC D18400

TIMING DIAGRAM:



**The first data word is Left Channel with MSB first and LSB last. The next data word is Right Channel with MSB first and LSB last, etc.

CONNECTION DIAGRAM:

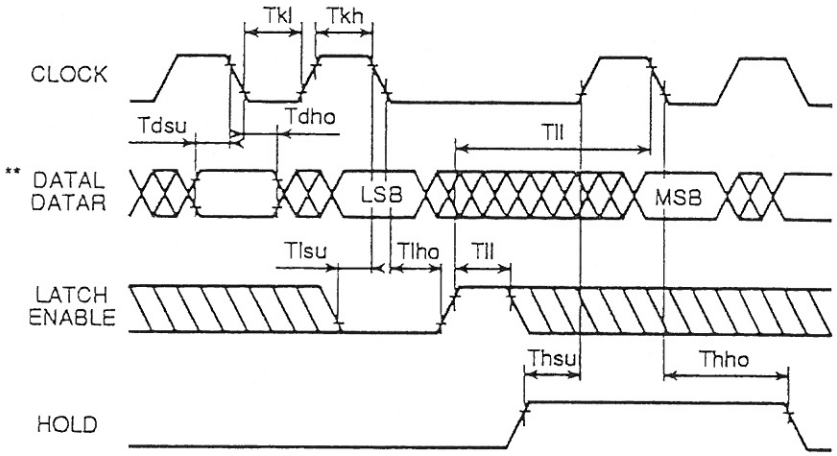


4.5 Simultaneous / Inverted Clock / Inverted WS/$\overline{\text{LOAD}}$.

(For use with serial data circuits compatible with the Philips TDA-1541A D/A converter, operated in the simultaneous mode.).

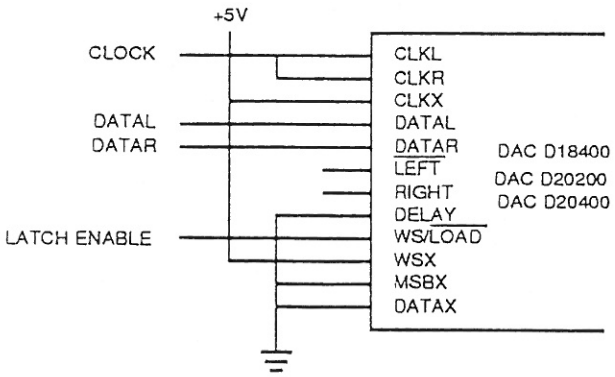
In this application, left and right channel data are received simultaneously on the DATAL and DATAR inputs. A single clock is applied to both the CLKL and CLKR inputs. Data bits are loaded into an input shift register with each falling edge of the clock, CLKX = "1". The digital data output of the shift register is then transferred to a parallel data register with the rising edge of the LATCH ENABLE (WS/$\overline{\text{LOAD}}$) signal and then converted. During the period that the D/A converters are settling, the Hold signals place the output deglitchers into the "hold" mode thereby freezing the analog outputs.

TIMING DIAGRAM:



**The two data words are presented simultaneously. The MSB for each data word appears first and the LSB last.

CONNECTION DIAGRAM:



5. Compatibility with the MOTOROLA DSP56000 family

UltraAnalog suggests using the asynchronous transmitter mode with a gated serial clock and a normal protocol. The clock should be inverted (CLKX=1) and 24 Bit words should be used. If the output flags are used, one DSP chip can be shared by both channels, or separate DSP chips can be connected to each channel. The maximum bit clock rate is 18MHz.

6. HOLD Signal (applications information).

The HOLD pulse width is optimally 2.0 µS wide for the DAC D20200 and 1.5µS wide for the DAC D18400 and DAC D20400. This width allows adequate settling time for the internal D/A converter circuitry. If the system application requires that the width of the HOLD pulse varies with sampling rate, or the pulse width can not be 2.0 µS wide for the DAC D20200 or 1.5µS wide for the DAC D18400 / DAC D20400 due to other system timing constraints, then 2.0 µS width should be considered the minimum HOLD period for the DAC D20200 and 1.5µS width for the DAC D18400 and DAC D20400. Further, as the HOLD period is increased, the output noise of the D/A converter will increase proportionally to the increase in HOLD period.

Another consideration for the HOLD signal is that it be "clean". Care must be taken to insure that digital noise is not allowed to contaminate this signal. One technique that insures the cleanliness of this signal is to generate a crystal clock powered from the "analog" power supply. This clock is applied to a CMOS divider, also powered by the "analog" power supply. The output of the divider is then applied to the HOLD inputs of the DAC D18400, DAC D20200, or DAC D20400. Then the clock is transmitted via a buffer, isolation transformer or an opto-isolator to the digital portion of the overall system. If the clock is isolated in this manner, then any noise that affects the clock by the digital system will not deteriorate the analog output signals. The jitter contained on the Hold signals must also be minimized. If jitter exceeds 100 ps., then the output D/A noise for high amplitude, high frequency signals will degrade. In certain cases, jitter may degrade the harmonic distortion performance of the product.

7. Power Supplies.

All of UltraAnalogs' D/A Converters require a ± 15 Volt linear-regulated supply and a + 5 Volt supply. The ± 15 Volt supply must have less than 5 mV peak - peak ripple and no transients. All of UltraAnalogs' D/A Converters exhibit very good immunity to DC power supply changes, however, like most analog / digital / analog circuitry, switching transients may create significant errors in the data conversion process. In this regard, transients that exist on digital ground in most systems must not be allowed to interfere with the D/A converter. The user should carefully design the overall power and grounding of the system to reduce the effects of noise caused by common "shared" grounds between the analog and digital portions of the system. UltraAnalog recommends connecting analog and digital grounds directly under the module, if possible.

8. External Offset and Gain Adjust.

Each channel of the DAC D18400, DAC D20200, or DAC D20400 has an external offset adjust input. If the user is not interested in fine-trimming the offset, then these two inputs should be connected to their respective output return pins. This will result in an output offset error of ± 5 mV, maximum. If it is desirable to reduce the output offset errors, the user may connect an external voltage source (either a voltage output D/A converter or an external trim potentiometer) to the offset adjust pins. The sensitivity of this adjustment is 1 mV/ 1 Volt. A single external gain (reference) adjust input is provided for both channels. By applying an external voltage source (either a voltage output D/A converter or an external trim potentiometer) to the reference adjust pin, the gain error of both channels may be reduced. With no external adjustment, the absolute gain error of both channels is ± 0.1%, maximum, and the channel - to - channel gain mismatch is ± 0.01%, maximum. The sensitivity of this adjustment is 0.013 % FSR/ Volt.