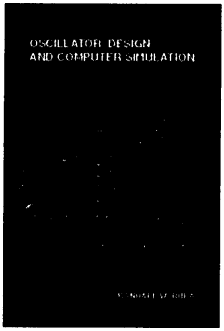

Oscillator Design and Computer Simulation

Randall W. Rhea

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This book covers the design of L-C, transmission line, quartz crystal and SAW oscillators. The unified approach presented can be used with a wide range of active devices and resonator types. Valuable to experienced engineers and those new to oscillator design. Topics include: limiting and starting, biasing, noise, analysis and oscillator fundamentals.

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by

Randall W. Rhea
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Contents

Preface

The engineer is often confused when faced with his/her first oscillator design. Other electrical engineering disciplines have evolved procedures for designing specific networks. A classic example is electrical filter design where many aspects have been reduced to cook-book simplicity With experience, the engineer develops a feel for the practical problems involved in filter design, and applies creative solutions to these problems. But the apprentice has many references with well-outlined approaches to the problems. For the RF and microwave oscillator apprentice, the approach is often less effective. Typically, the literature is searched for an oscillator type similar to that needed for the present requirement. Component values are modified and a prototype is constructed to complete the design. This approach is fraught with difficulty Lacking is an understanding of the fundamental principles involved. A large number of variables affect oscillator operation, and if the performance is inadequate, the apprentice is uncertain about a solution. Although much literature exists concerning oscillators, each reference typically addresses a specific oscillator type. A fundamental understanding of the concepts is all too often buried in pages of equations.

The purpose of this book is to demystify oscillator design and provide a practical reference on the design of RF and microwave oscillators. The thrust of the book is on concepts, a unified design approach to a variety of oscillators, and verification of the design via computer simulation. This is not a book of mathematics. Equations are included only when they contribute to fundamental understanding, determine component values, or predict oscillator performance.

Design begins with a linear approach. An active amplifier is cascaded with a passive frequency-selective resonator. The circuit small signal open-loop gain/phase (Bode) plot is considered. To form the oscillator, the loop is closed. Oscillation builds until limiting occurs which reduces the loop gain to unity The linear Bode plot describes many aspects of oscillator performance. The non linear characteristics of the loop amplifier are considered independently Together, these considerations predict nearly all aspects of oscillator behavior including the gain/phase oscillation margin, oscillation frequency, noise performance, start-up time, output level, harmonic level, and conditions conducive to spurious oscillation. This design approach is applied to a variety of oscillators using bipolar, JFET, MOSFET, and hybrid/MMIC active devices with L-C (inductor-capacitor), transmission line, SAW, and piezoelectric resonators.

If the amplifier and resonator were ideally simple, the mathematics involved for a complete linear solution would be simple. Accurate active-device models at RF and microwave frequencies are complex. Therefore, solving the equations for the loop, while not conceptually difficult, is typically tedious. The exact equations and techniques are different for each oscillator type, which discourages a unified design approach. Instead, why not leave the burden of computing the network responses to a general-purpose circuit simulation computer program? The accuracy and convenience of these programs is now mature. Dealing with a plethora of practical problems, such as component parasitics, is simple for a simulation program. The designer may ponder the concepts and solutions, while the computer handles the tedium of analysis. A unified approach to oscillator design is encouraged in this environment.

Most of the specific oscillator designs covered in this book are old friends of mine. Over 1 million units of a 300-MHz crystal controlled transmitter based on the Butler overtone oscillator with built-in frequency multiplier were constructed by Scientific-Atlanta, my former employer. Many other designs have been constructed by the thousands.

This is the second edition of a book originally published by Prentice Hall. This second edition includes significant updates and over 100 pages of new material. The new material includes remarks relating open loop oscillator theory to classical terminology It expands resonator theory to include additional L-C forms and popular ceramic loaded coaxial resonators. The material on negative resistance oscillators is substantially updated and expanded. Chapter 6 on computer aided techniques is rewritten to include recent advances and Spice-based oscillator analysis. A new Chapter 12 includes case studies of typical oscillator specifications and descriptions of the design procedures used to satisfy those requirements.

I would like to thank Larry McKinney of Scientific-Atlanta for thought-provoking discussions and sharing design experiences and data. I would also like to thank Crawford Patterson for layout and edit work on this second edition.

Randall W. Rhea
Stone Mountain, Georgia
January 2,1995

1

Analysis Fundamentals

For this section, we assume that networks are linear and time invariant. Time invariant signifies that the network is constant with time. Linear signifies the output is a linear function of the input. Doubling the input driving function doubles the resultant output. The network may be uniquely defined by a set of linear equations ***relating*** *port voltages and currents.*

1.1 Voltage Transfer Functions

Consider the network in Figure 1-1A terminated at the generator with R_g, terminated at the load with R_l, and driven from a voltage source E_g [1]. *Et* is the voltage across the load.

The quantity E_{avail} is the voltage across the load when all of the available power from the generator is transferred to the load.

$$E_{avail} = \sqrt{\frac{R_l}{R_g}} \frac{E_g}{2} \qquad 1.1$$

For the case of a null network with $R_l = R_g$,

$$E_{avail} = \frac{E_g}{2} \qquad 1.2$$

since one-half of E_g is dropped across R_g and one-half is dropped across R_l. For the case of a non-null network, dividing both sides of the equation 1.1 by *Et gives*

$$\frac{E_{avail}}{El} = \sqrt{\frac{Rl}{R_g}} \frac{E_g}{2E_l} \qquad 1.3$$

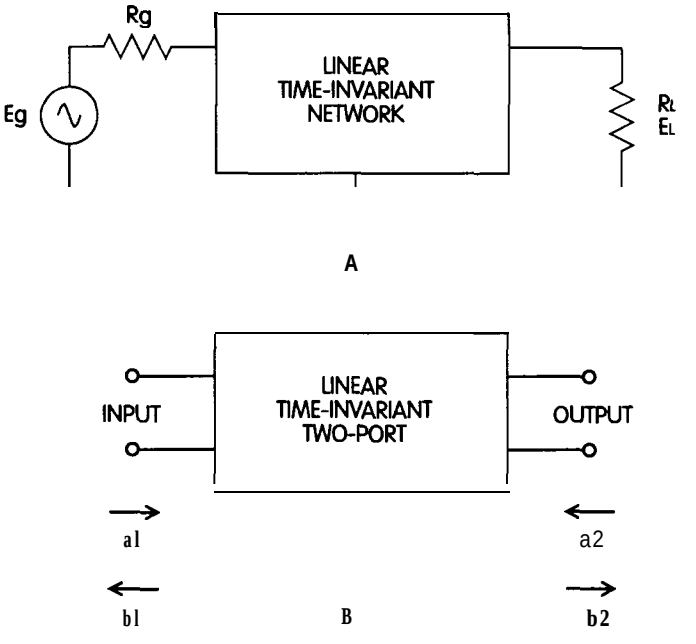


Figure l-l A linear, time-invariant network defined in terms of terminal voltages (A) and in terms of port incident and reflected waves (B).

We can then define the voltage transmission coefficient as the voltage across the load, E_l, divided by the maximum available voltage across the load E_{avail}, or

$$t = \frac{E_l}{E_{avail}} = \sqrt{\frac{R_g}{R_l}}\,\frac{2E_l}{E_g} \qquad 1.4$$

This voltage transmission coefficient is the "voltage gain" ratio. For the case with $R_g = R_l$, since $E_g = 2E_l$, the transmission coefficient is 1.

1.2 Power Transfer Functions

The power insertion loss is defined as

$$\frac{P_{null}}{P_l} = \left(\frac{R_l}{R_l + R_g}\right)^2 \left|\frac{E_g}{E_l}\right|^2 \qquad 1.5$$

where the voltages and resistances are defined as before, P_{null} is the power delivered to the load with a null network and P_l is the power delivered to the load with a network present. Figure l-2 depicts P_d as a function of R_l with a null network, E_g = 1.414 volts and R_g = 1 ohm. Notice the maximum power delivered to the load occurs with R_l = 1 ohm = R_g.

When R_l is not equal to R_g, a network such as an ideal transformer or a reactive matching network may re-establish maximum

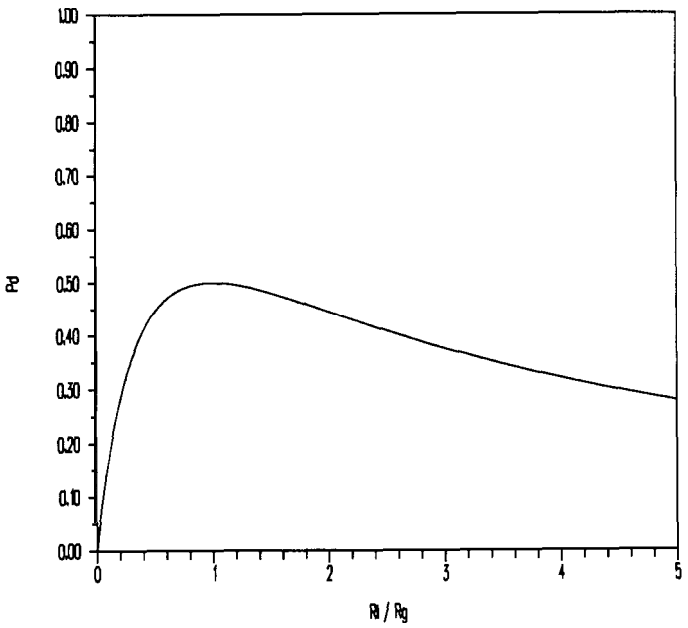


Figure 1-2 *Power delivered to the load versus the termination resistance ratio.*

power transfer. When inserted, this passive network may therefore result in more power being delivered to the load than when absent. The embarrassment of power "gain" from a passive device is avoided by an alternative definition, the power transfer function

$$\frac{P_{avail}}{P_l} = \frac{R_l}{4R_g}\left|\frac{E_g}{E_l}\right|^2 = \frac{1}{t^2} \qquad 1.6$$

where

$$P_{avail} = \frac{|E_g|^2}{4R_g} \qquad 1.7$$

When $R_l = R_g$, these definitions are identical.

1.3 Scattering Parameters

The networks depicted in Figure l-l may be uniquely described by a number of two-port parameter sets including *H*, *Y, Z, ABCD, S* and others which have been used for this purpose. Each have advantages and disadvantages for a given application. Carson [2] and Altman [3] consider network parameter sets in detail.

S-parameters have earned a prominent position in RF circuit design, analysis and measurement [4,5]. Other parameters, such as *Y, Z* and *H* parameters, require open or short circuits on ports during measurement. This poses serious practical difficulties for broadband high frequency measurement. Scattering parameters (S-parameters) are defined and measured with ports terminated in a reference impedance. Modern network analyzers are well suited for accurate measurement of *S*-parameters. S-parameters have the additional advantage that they relate directly to important system specifications such as gain and return loss.

As depicted in Figure 1-1B, two-port S-parameters are defined by considering a set of voltage waves. When a voltage wave from a source is incident on a network, a portion of the voltage wave is transmitted through the network, and a portion is reflected back

toward the source. Incident and reflected voltage waves may also be present at the output of the network. New variables are defined by dividing the voltage waves by the square root of the reference impedance. The square of the magnitude of these new variables may be viewed as traveling power waves.

$|a_1|^2 = incident$ *power wave at the network input* 1.8

$|b_1|^2 =$ *reflected power wave at the network input* 1.9

$|a_2|^2 =$ *incident power wave at the network output* 1.10

$|b_2|^2 =$ *reflected power wave at the network output* 1.11

These new variables and the network S-parameters are related by the expressions

$$b_1 = a_1S_{11} + a_2S_{12} \quad 1.12$$

$$b_2 = a_1S_{21} + a_2S_{22} \quad 1.13$$

$$S_{11} = \frac{b_1}{a_1}, a_2 = 0 \quad 1.14$$

$$S_{12} = \frac{b_1}{a_2}, a_1 = 0 \quad 1.15$$

$$S_{21} = \frac{b_2}{a_1}, a_2 = 0 \quad 1.16$$

$$S_{22} = \frac{b_2}{a_2}, a_1 = 0 \quad 1.17$$

Terminating the network with a load equal to the reference impedance forces $a_2 = 0$. Under these conditions.

$$S_{11} = \frac{b_1}{a_1} \quad 1.18$$

$$S_{21} = \frac{b_2}{a_1} \quad 1.19$$

S_{11} is then the network input reflection coefficient and S_{21} is the forward voltage transmission coefficient t of the network. When

the generator and load resistance are equal, the voltage transmission coefficient defined t earlier is equal to S_{21}. Terminating the network at the input with a load equal to the reference impedance and driving the network from the output port forces $a_1 = 0$. Under these conditions.

$$S_{22} = \frac{b_2}{a_2} \tag{1.20}$$

$$S_{12} = \frac{b_1}{a_2} \tag{1.21}$$

S_{22} is then the output reflection coefficient and S_{12} is the reverse transmission coefficient of the network.

The S-parameter coefficients defined above are linear ratios. The S-parameters also may be expressed as a decibel ratio.

Because S-parameters are voltage ratios, the two forms are related by the simple expressions

$$|S_{11}| = \textit{input reflection gain}\ (dB) = 20 \log |S_{11}| \tag{1.22}$$

$$|S_{22}| = \textit{output reflection gain}\ (dB) = 20 \log |S_{22}| \tag{1.23}$$

$$|S_{21}| = \textit{forward gain}\ (dB) = 20 \log |S_{21}| \tag{1.24}$$

$$|S_{12}| = \textit{reverse gain}\ (dB) = 20 \log |S_{12}| \tag{1.25}$$

To avoid confusion, in this book, the linear form of the scattering coefficients are referred to as C_{11}, C_{21}, C_{12} and C_{22}. The decibel form of S_{21} and S_{12} are often simply referred to as the forward and reverse gain. With equal generator and load resistance, S_{21} and S_{12} are equal to the power insertion gain defined earlier.

The reflection coefficients magnitudes, $|S_{11}|$ and $|S_{22}|$ are less than 1 for passive networks with positive resistance. Therefore, the decibel input and output reflection gains, $|S_{11}|$ and $|S_{22}|$, are negative numbers. Throughout this book, S_{11} and S_{22} are referred to as return losses, in agreement with standard industry convention. Therefore, the expressions above relating coefficients and the decibel forms should be negated for S_{11} and S_{22}.

Input *VSWR* and S_{11} are related by

$$VSWR = \frac{1 + |S_{11}|}{1 - |S_{11}|} \qquad 1.26$$

The output *VSWR* is related to S_{22} by an analogous equation. Table l-l relates various values of reflection coefficient, return loss, and *VSWR*.

The complex input impedance is related to the input reflection coefficients by the expression

$$Z_{input} = Z_o \frac{1 + S_{11}}{1 - S_{11}} \qquad 1.27$$

The output impedance is defined by an analogous equation using S_{22}.

Table l-l *Radially Scaled Reflection Coefficient Parameters*

S_{11} (dB)	C_{11}	VSWR	S_{11} (dB)	C_{11}	VSWR
40.0	0.0101	1.020	6.02	0.500	3.000
30.0	0.032	1.065	5.00	0.562	3.570
25.0	0.056	1.119	4.44	0.600	3.997
20.0	0.100	1.222	4.00	0.631	4.419
18.0	0.126	1.288	3.01	0.707	5.829
16.0	0.158	1.377	2.92	0.714	6.005
15.0	0.178	1.433	2.00	0.794	8.724
14.0	0.200	1.499	1.94	0.800	8.992
13.0	0.224	1.577	1.74	0.818	10.02
12.0	0.251	1.671	1.00	0.891	17.39
10.5	0.299	1.851	0.915	0.900	19.00
10.0	0.316	1.925	0.869	0.905	20.00
9.54	0.333	2.000	0.446	0.950	39.00
9.00	0.355	2.100	0.175	0.980	99.00
8.00	0.398	2.323	0.0873	0.990	199.0
7.00	0.447	2.615			

1.4 The Smith Chart

In 1939, Phillip H. Smith published an article describing a circular chart useful for graphing and solving problems associated with transmission systems [6]. Although the characteristics of transmission systems are defined by simple equations, prior to the advent of scientific calculators and computers, evaluation of these equations was best accomplished using graphical techniques. The Smith chart gained wide acceptance during an important developmental period of the microwave industry The chart has been applied to solve a wide variety of transmission system problems, many which are described in a book by Phillip Smith [7].

The design of broadband transmission systems using the Smith chart involves graphic constructions on the chart repeated for selected frequencies throughout the range on interest. Although a vast improvement over the use of a slide rule, the process is tedious except for single frequencies and useful primarily for training purposes. Modern interactive computer circuit simulation programs with high-speed tuning and optimization procedures are much more efficient. However, the Smith chart remains an important tool as an insightful display overlay for computer-generated data. An impedance Smith Chart with unity reflection coefficient radius is shown in Figure l-3.

The impedance Smith chart is a mapping of the impedance plane and the reflection coefficient. Therefore, the polar form of a reflection coefficient plotted on a Smith chart provides the corresponding impedance. All values on the chart are normalized to the reference impedance such as 50 ohms. The magnitude of the reflection coefficient is plotted as the distance from the center of the Smith chart. A perfect match plotted on a Smith chart is a vector of zero length (the reflection coefficient is zero) and is therefore located at the center of the chart which is $1+j0$, or 50 ohms. The radius of the standard Smith chart is unity Admittance Smith charts and compressed or expanded charts with other than unity radius at the circumference are available.

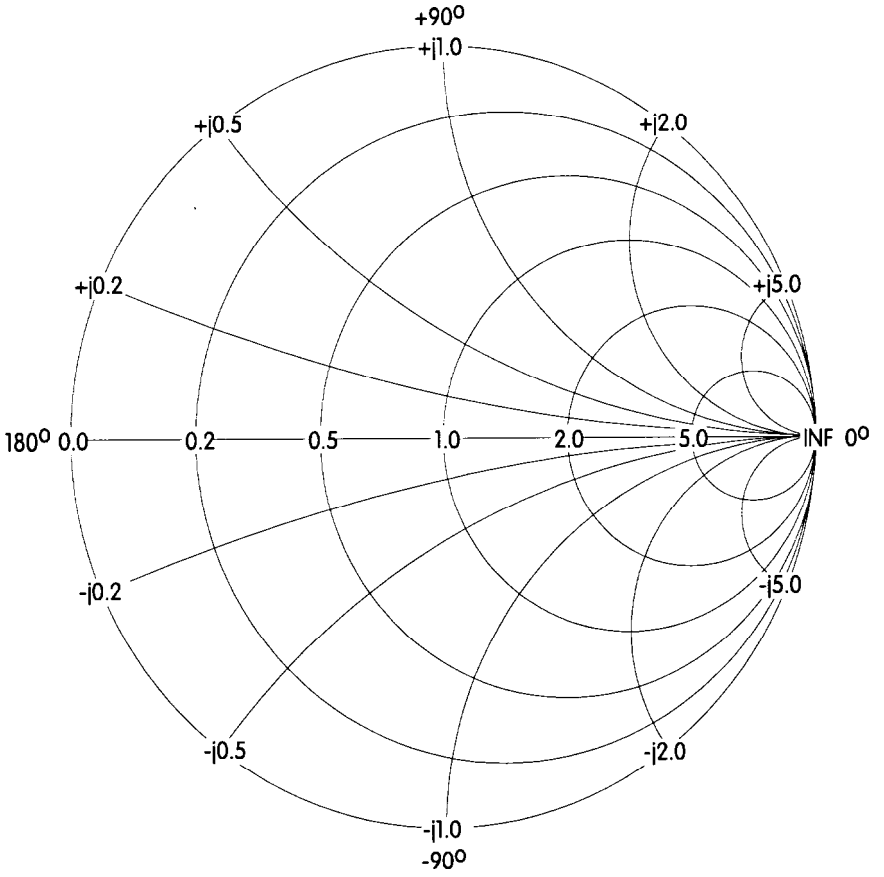


Figure 1-3 *Impedance Smith chart with unity reflection coefficient radius.*

Purely resistive impedances map to the only straight line of the chart with zero ohms on the left and infinite resistance on the right. Pure reactance is on the circumference. The complete circles with centers on the real axis are constant normalized resistance circles. Arcs rising upwards are constant normalized inductive reactance and descending arcs are constant normalized capacitive reactance.

High impedances are located on the right portion of the chart, low impedances on the left portion, inductive reactance in the upper half, and capacitive reactance in the lower half. The angle of the reflection coefficient is measured with respect to the real axis, with zero-degrees to the right of the center, 90^o straight up, and -90^o straight down. A vector of length 0.447 at 63.4' extends to the intersection of the unity real circle and unity inductive reactance are $1 + j1$, or $50 + j50$ when demoralized.

The impedance of a load as viewed through a length of lossless transmission line as depicted on a Smith chart rotates in a clockwise direction with constant radius as length of line or the frequency is increased. Transmission line loss causes the reflection coefficient to spiral inward.

1.5 Radially Scaled Parameters

The reflection coefficient, return loss *VSWR,* and impedance of a network port are dependent parameters. A given impedance, whether specified as a reflection coefficient or return loss, plots at the same point on the Smith chart. The magnitude of the parameter is a function of the length of a vector from the chart center to the plot point. Therefore, these parameters are referred to as radially scaled parameters. For a lossless network, the transmission characteristics are also dependent on these radially scaled parameters. The length of this vector is the voltage reflection coefficient, ρ, and is essentially the reflection scattering parameter of that port. The complex reflection coefficient at a given port is related to the impedance by

$$\rho = \frac{Z - Z_o}{Z + Z_o} \tag{1.28}$$

where Z is the port impedance and Z_o is the reference impedance. Then

$$RL_{dB} = -20 \log |\rho| \tag{1.29}$$

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \tag{1.30}$$

$$L_A = -10 \log (1 - |\rho|^2) \tag{1.31}$$

Table l-l includes representative values relating these radially scaled parameters.

1.6 Matching

Gain (or loss) is clearly an important parameter of a network. The definition of gain that will be used is the transducer power gain. The transducer power gain is defined as the power delivered to the load divided by the power available from the source.

$$G_t = \frac{P_{\text{del}}}{P_{\text{available}}} \tag{1.32}$$

The S-parameter data for the network is measured with a source and load equal to the reference impedance. The transducer power gain with the network inserted in a system with arbitrary source and load reflection coefficients is [5]

$$G_t = \frac{|C_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_{L\,1}{}^2)}{|(1 - C_{11}\Gamma_S)(1 - C_{22}\Gamma_L) - C_{21}C_{12}\Gamma_L\Gamma_S|^2} \tag{1.33}$$

where

Γ_S = reflection coefficient of the source 1.34

Γ_L = reflection coefficient of the load 1.35

If Γ_S and Γ_L are both zero, then

$$G_t = C_{21}{}^2 \tag{1.36}$$

or

$$G_t(\text{dB}) = 20 \log |C_{21}| = \text{IS21}| \tag{1.37}$$

Therefore, when a network is installed in a system with source and loads equal to the reference impedance, $|S_{21}|$ is the network transducer power gain in decibels.

Because C_{11} and C_{22} of a network are not in general zero, a portion of the available source power is reflected from the network input and is dissipated in the source. The insertion of a lossless matching network at the input (and/or output) of the network could increase the gain of the network. Shown in Figure l-3 is a two-port network with lossless matching networks inserted between the network and a source and load with the reference impedance.

Equation 1.22 gives the gain of the network in Figure l-4. To simplify equation 1.22, C_{12} may be assumed equal to zero. At higher frequencies, where C_{12} is larger in active devices, this assumption is less valid. The assumption is unnecessary in computer-assisted design but considerably simplifies manual and graphical design procedures. The assumption also allows factoring equation 1.22 into terms that provide insight into the design process. If $C_{12} = 0$, then

$$G_{tu} = \frac{1 - |\Gamma_S|^2}{|1 - C_{11}\Gamma_S|^2} \quad |C_{21}|^2 \quad \frac{1 - |\Gamma_L|^2}{|1 - C_{22}\Gamma_L|^2} \qquad 1.38$$

where

G_{tu} = unilateral transducer power gain 1.39

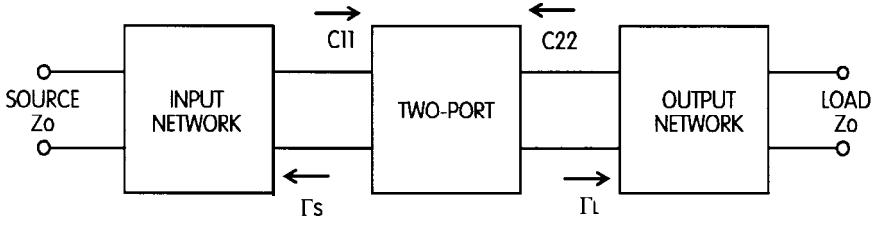


Figure 1-4 *Two-port defined by S-Parameters with lossless matching networks at the input and output.*

When both ports of the network are conjugately matched, and C_{12} = 0,

$$G_{u\,max} = \frac{1}{1-|C_{11}|^2} \quad |C_{21}|^2 \quad \frac{1}{1-|C_{22}|^2} \qquad 1.40$$

The first and third terms are indicative of the gain increase achievable by matching the input and output, respectively If C_{11} or C_{22} are much larger than zero, substantial gain improvement is achieved by matching. Matching not only increases the network gain, but reduces reflections from the network.

It is more desirable for network gain to flatten across a frequency band than minimum reflections. The lossless matching networks are designed to provide a better match at frequencies where the two-port gain is lower. By careful design of amplifier matching networks, it is frequently possible to achieve a gain response flat within fractions of a decibel over a bandwidth of more than an octave.

1.7 Broadband Amplifier Without Feedback

An example of 2 to 4 GHz amplifier design using the foregoing principles is considered next. An Avantek AT60585 bipolar transistor with the S-parameter data given in Table l-2 for the common-emitter configuration is used. This data is graphed in Figure 1-5. The transistor gain in decibels, S_{21}, is plotted on the left. The gain is 11.4 dB at 2 GHz and 5.8 dB at 4 GHz. The transistor input and output return loss plotted on a Smith chart are shown on the right in Figure l-5. The input impedance is less than 50 ohms and slightly inductive. The output impedance is greater than 50 ohms and capacitive. The markers may be used to discern the traces and read specific values (along the bottom of the screen).

As is typical, the transistor gain decreases with increasing frequency Using equation 1.29 and S_{11} and S_{22} from Table 1-2, the additional gain achievable at 4 GHz by matching both the input and output is 1.0 + 1.4 = 2.4 dB. The conjugately matched gain

Table 1-2 *S-Parameter Data for Avantek AT60585 Bipolar Transistor Biased at 8 V and 10 mA*

Freq (MHz)	C_{11} (ratio)	Angle (deg)	C_{21} (ratio)	Angle (deg)	C_{12} (ratio)	Angle (deg)	C_{22} (ratio)	Angle (deg)
2000	.41	174	3.70	66	.06	58	.53	-33
2500	.42	165	3.06	60	.072	58	.51	-35
3000	.44	155	2.56	51	.086	65	.50	-42
3500	.46	i45	2.23	42	.098	61	.50	-51
4000	.46	138	1.96	32	.114	59	.52	-59

should be 5.8 + 2.4 = 8.2 dB, assuming that C_{12} = 0. Therefore, an amplifier with 8 dB of gain is attempted.

Some practice or experience is helpful in selecting an appropriate topology for the input and output matching networks. The trick will be to match input at the transistor and output at the higher

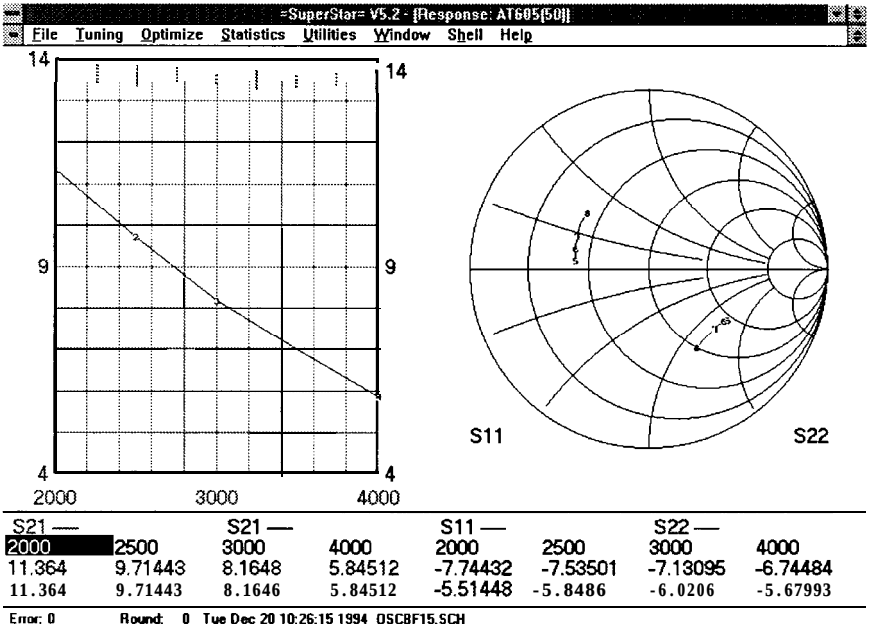
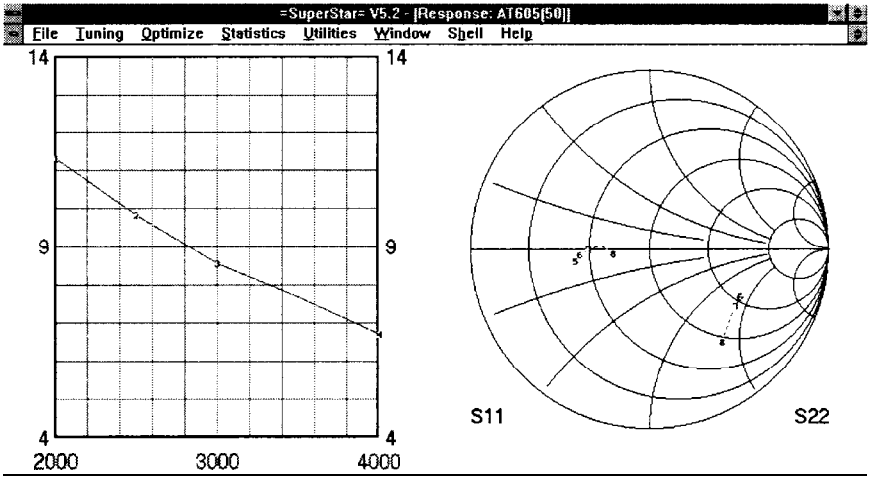


Figure 1-5 *S_{21}, S_{11} and S_{22} for an Avantek AT60585.*

frequencies to increase the gain, and to worsen the match at the lower frequencies to decrease the gain. First, placing a shunt capacitor at the input of the transistor rotates the 4 GHz end of the S_{11} trace toward the center of the Smith chart, improving the input match at 4 GHz and increasing the gain. By trying different values for the shunt capacitor, it was discovered that a value of 1 pF results in the maximum increase in gain. The results are shown in Figure 1-6. The gain at 4 GHz has been increased to 6.7 dB, up from 5.8 dB. The gain at 2 GHz was unaffected.

A shorted transmission line stub followed by a series transmission line are used to match the output. The values for this network were determined using optimization with the =SuperStar= computer program.

The results are shown in Figure 1-7. The flatness is within a few tenths of a decibel. Actual results should agree closely with these calculated results because the assumption that $C_{12} = 0$ is unnec-



S21 —		S21 —		S11 —		S22 —	
2000	2500	3000	4000	2000	2500	3000	4000
11.33	9.84261	8.56155	6.69843	-7.57962	-8.18934	-9.33818	-13.9332
11.33	9.84261	8.56155	6.69843	-4.84913	-4.86497	-4.80822	-3.66834

c.
1|

Figure 1-6 *Auantek AT60585 transistor responses with 1 pF shunt capacitance at the input.*

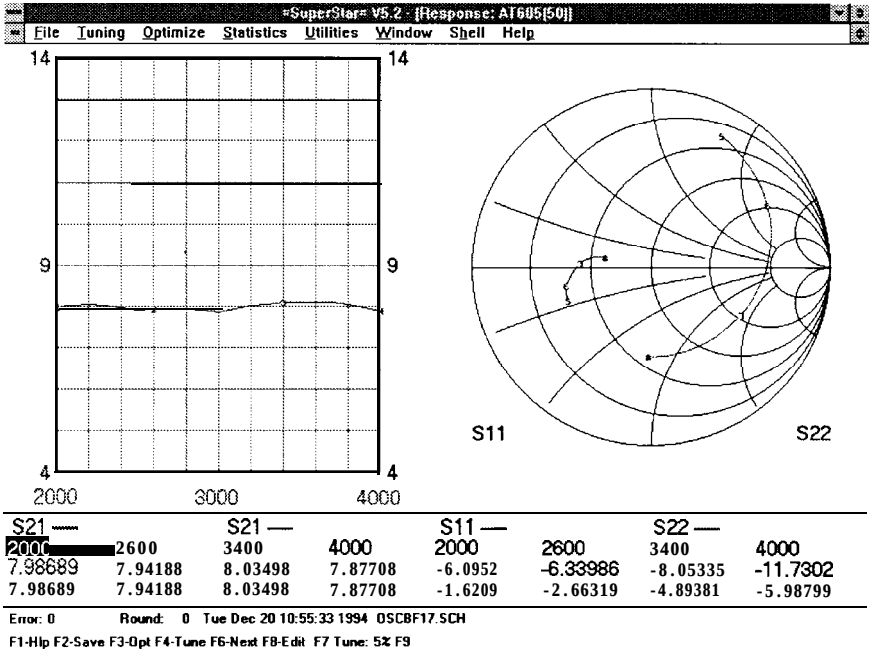


Figure 1-7 *Avantek AT60585 transistor with matching at the input and output.*

essary when computer simulation techniques are utilized. The schematic of the completed design is given in Figure 1-8.

1.8 Stability

The type of networks used at the input and output of an amplifier must be selected based on an additional criterion, stability The fact that C_{12} is not equal to zero represents a signal path from the transistor output to the input. This feedback path is an opportunity for oscillation to occur. The reflection coefficients presented to the transistor by the matching networks affect the stability of the amplifier. A stability factor, K, is

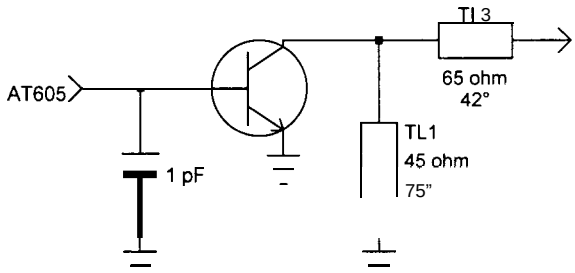


Figure 1-8 *Bipolar 2 - 4 GHz transistor amplifier with matching at the input and output optimized to flatten the gain.*

$$K = \frac{1 - |C_{11}|^2 - |C_{22}|^2 + |D|^2}{2\,|C_{12}|\,|C_{21}|} \qquad 1.41$$

where

$$D = C_{11}\,C_{22} - C_{12}\,C_{21} \qquad 1.42$$

When $K>1, C_{11}<1,$ and $C_{22}<1,$ the two-port is unconditionally stable. That means that the two-port is stable for all input and output loads with positive real components. To ensure stability, these conditions must be met both internally and at the input and output ports. Stability should be checked not only at the operating frequencies, but also at frequencies above and below the operating frequency

Stability circles may be used for a more detailed analysis. The load impedances of a network which ensures that $C_{11}<1$ are identified by a circle of radius *r* centered at C on a Smith chart. The output plane stability circle is

$$C_{out} = \frac{(C_{22} - D\,C_{11}^{*})^{*}}{|C_{22}|^2 - |D|^2} \qquad 1.43$$

$$r_{out} = \left| \frac{C_{12}\,C_{21}}{|C_{22}|^2 - |D|^2} \right| \qquad 1.44$$

This circle is the locus of loads for which $C_{11} = 1$. The region inside or outside the circle may be the stable region.

The input plane stability circle equations are the same as the output plane equations, with 1 and 2 in the subscripts interchanged. Reference [4] includes a more detailed tutorial on stability

1.9 Broadband Amplifier With Feedback

Achieving a flat frequency response by shaping the match of the input and output networks has the advantage that the gain at higher frequencies can exceed S_{21}. This advantage is especially useful at higher frequencies where gain is more expensive to achieve, so this technique is a common practice in microwave amplifier design. Unfortunately, this technique has several disadvantages:

(a) The match is necessarily poor at lower frequencies.

(b) The bandwidth of flat gain response is limited.

(c) Stability considerations are critical.

Another method of flattening the frequency response is to apply resistive negative feedback. This method overcomes the above disadvantages but the gain is less than the gain of the transistor at the highest frequency However, at UHF and lower frequencies, where transistor gain is naturally higher and less expensive, this disadvantage is less significant.

Amplifiers designed using negative feedback can possess wide bandwidth, excellent match, excellent stability, and excellent flatness. Consider the simple amplifier shown in Figure l-9. Shunt (collector to base) feedback and series (emitter) feedback are applied to an MRF901 transistor. S-parameter data for the transistor is given in Table l-3.

The results shown in Figure l-10 were computed using the =SuperStar= program. These results illustrate excellent gain flatness and match from low frequencies to 450 MHz. In practice,

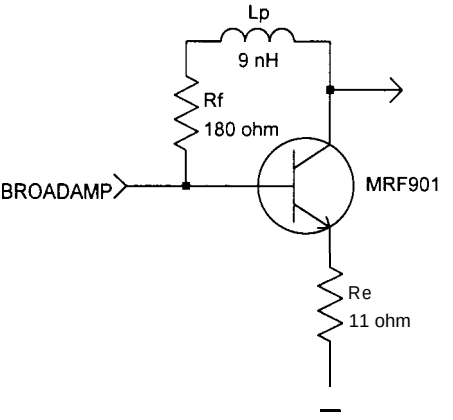


Figure 1-9 *Simple broadband amplifier using resistive series feedback in the emitter, R_e, and shunt feedback from collector to base, L_p and R_f.*

the low-frequency response is limited by the values of the input and output coupling capacitors.

The inductor, L_p, in series with the shunt feedback resistor is called a peaking inductor. It is used to extend the bandwidth of the amplifier. At higher frequencies, where the amplifier gain begins to fall because the open-loop transistor gain is falling, the reactance of the peaking inductor effectively reduces the shunt

Table 1-3 *S-Parameter Data for a Motorola MRF901 Transistor Biased at 10 V and 15 mA*

Freq (MHz)	C_{11} (ratio)	Angle (deg)	C_{21} (ratio)	Angle (deg)	C_{12} (ratio)	Angle (deg)	C_{22} (ratio)	Angle (deg)
50	.5	-23	24.0	160	.01	69	.90	-12
100	.51	-66	20.4	141	.02	63	.83	-22
200	.47	-112	14.5	119	.03	54	.63	-31
500	.50	-166	6.81	92	.05	57	.41	-35

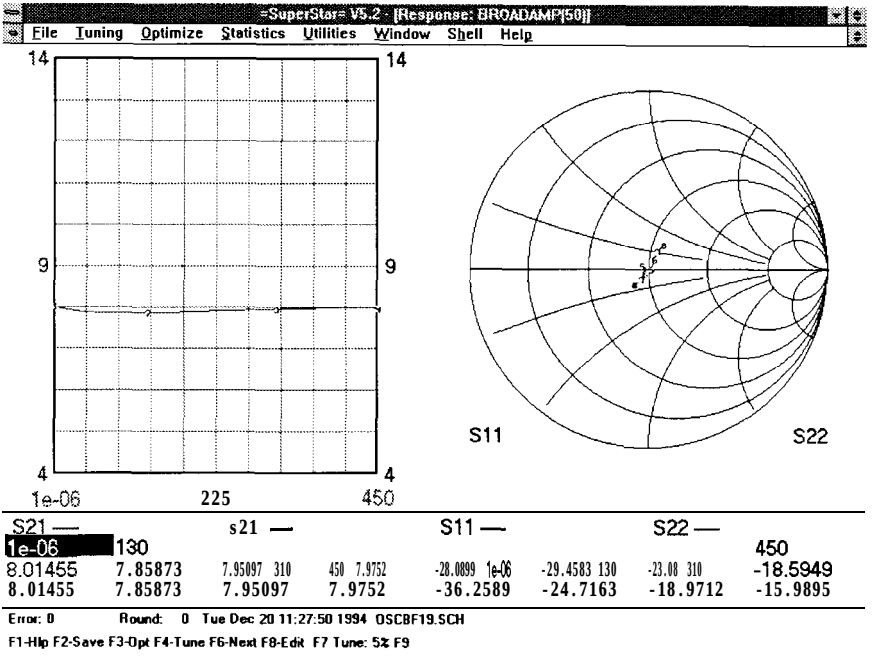


Figure 1-10 *Gain and match responses of the broadband amplifier with resistive feedback.*

feedback and extends the frequency response. A similar technique may be employed in the emitter by placing a capacitor in parallel with the emitter series feedback resistor. The match at these extended frequencies is not as good as the match at lower frequencies.

When the transistor open-loop gain is much greater than the gain with feedback, the gain with feedback is given by

$$G_f\,(\mathrm{dB}) = 20 \log\left[\frac{R_{fn}^2 - 1}{R_{fn} + 1}\right] \qquad 1.45$$

where

$$R_{fn} = \frac{R_f}{Z_o} \qquad 1.46$$

$$R_e = \frac{Z_o^2}{R_f} \quad 1.47$$

The shunt feedback resistor, R_f, reduces both the input and output impedance. The series feedback resistor, R_e, increases both the input and output impedance. As greater feedback is applied, the input and output impedances asymptotically approach the relation

$$Z_o = (R_f\ R_e)^{1/2} \quad 1.48$$

This expression, which indicates the proper relationship of R_f and R_e to achieve a desired Z_o, is most valid when the device input and output impedances are already near the desired Z_o. When the input and output impedances differ from Z_o, other values for R_f and R_e may yield a better match. For example, if both the input and output impedances are higher than Z_o, more shunt feedback (lower R_f) and less series feedback (lower R_e) will yield a better match.

In Figure l-11, the frequency response of MRF901 transistor amplifiers with a 50 ohm source and load is compared for differing values of shunt and series feedback. A peaking inductor is used, but not an emitter peaking capacitor. The peaking inductor values have been optimized to achieve the greatest possible bandwidth.

1.10 Component Parasitics

Components used in the construction of electronic networks are seldom as ideal as we would wish. An example is C_{12} not equal to zero for active devices. Even relatively simple components such as resistors, capacitors, and inductors have significant parasitics. Through UHF frequencies, some of the more important parasitics of passive components are

(a) Inductance of capacitor leads

(b) Self-capacitance of inductors

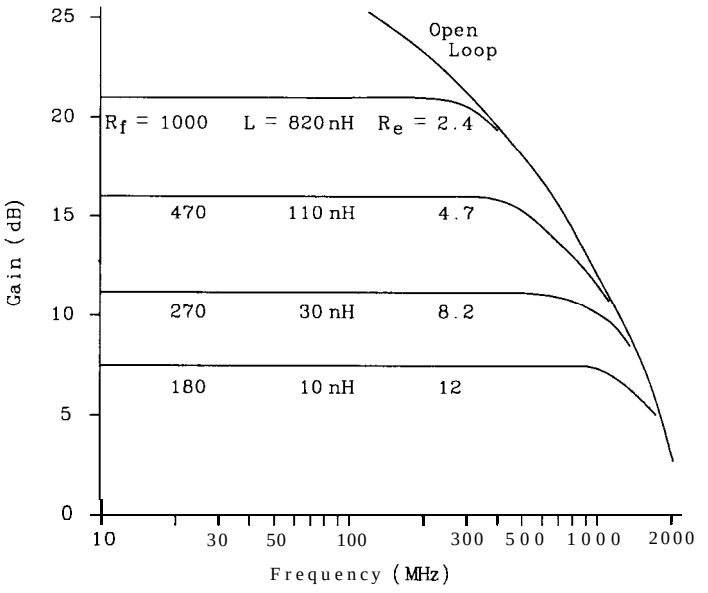


Figure 1-11 Closed *loop frequency response of a transistor amplifier with varying degrees of feedback applied.*

(c) Finite Q of inductors

(d) Coupling between inductors

Other parasitics may be significant as well, but an experienced high-frequency designer will consider the effects of these four parasitic types on every passive component used in the design. The importance of this cannot be over stressed. Countless hours of breadboard trouble shooting can be saved by considering these effects during the design.

The vast majority of design equations published in engineering literature do not include the effects of these parasitics because the resulting complexity would hopelessly reduce the usefulness of the expressions. This places RF and microwave design in the category of black magic, to be delved in only by those initiated in the art. Often, successful practitioners are simply those who have the experience of knowing which parasitics to worry about, what

to do about those, and which are insignificant in a given application.

Computer simulation programs offer a powerful tool for dealing with these effects. All parasitics are not included directly in computer program component models simply because the possibilities are endless. However, the designer can easily add to the network description parasitics appropriate for the components being used. In addition to simulating and identifying these effects, tuning and optimization in the computer program can assist in determining a remedy. Listed in Table l-4 are typical passive component parasitics for high frequencies. Reference [8] includes an entire chapter devoted to components and parasitics.

Table 1-4 *Typical Component Parasitic Effects at High Frequencies and Possible Remedies*

Parasitic Effects	Typical Values		Remedies
Capacitor lead inductance	Lead spacing	*L*	Use capacitors in parallel
	0.25 in.	9 nH	
	0.20 in.	8 nH	
	0.10 in.	4 nH	
	Leadless	1 nH	
Inductor self capacitance	Refer to Chapter 8		Use smaller diameter coil Use toroid Reduce required inductance
Inductor *Q*	Refer to Chapter 8		Increase inductor volume At lower frequencies use pot cores
inductor coupling	Varies significantly		Increase inductor spacing Reorient inductors Use toroids Use magnetic shielding

1.11 Amplifier With Parasitics

An approximate model for a 1/4-watt leaded carbon composition or film resistor is shown in Figure 1-12. For higher resistance values, the reactance of the lead inductance is less significant than the resistance. In this case, the parallel capacitance is important at higher frequencies. For lower resistance values and high frequencies, the reactance of the lead inductance is more significant.

Figure 1-13 shows the schematic of a simple 108 to 300 MHz amplifier similar to the amplifier in Figure 1-9, but using a 2N5179 transistor and feedback resistors with parasitics.

The results are shown in Figure 1-14. The solid traces in each case are with ideal resistors with no parasitics. On the upper left (LRF), the dashed response is with 9 nH of inductance added to the resistor R_f. Notice the gain is increased and the flatness is improved. The resistor parasitic inductance adds to the required peaking inductance and aids amplifier performance. At the upper right (CRF), the resistor parallel capacitance is added. The gain is reduced and the flatness is degraded. Therefore, inductance in the shunt feedback resistor is not a problem but capacitance degrades performance somewhat.

Next consider the effects of the same parasitics in the series feedback resistor, R_e. On the lower left (LRE) adding the resistor

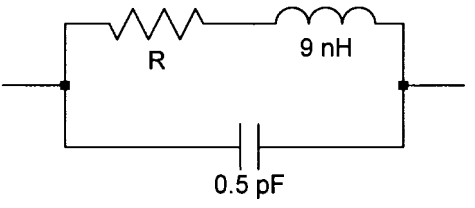


Figure 1-12 *Model of a l/4-watt composition or film resistor with first-order parasitics.*

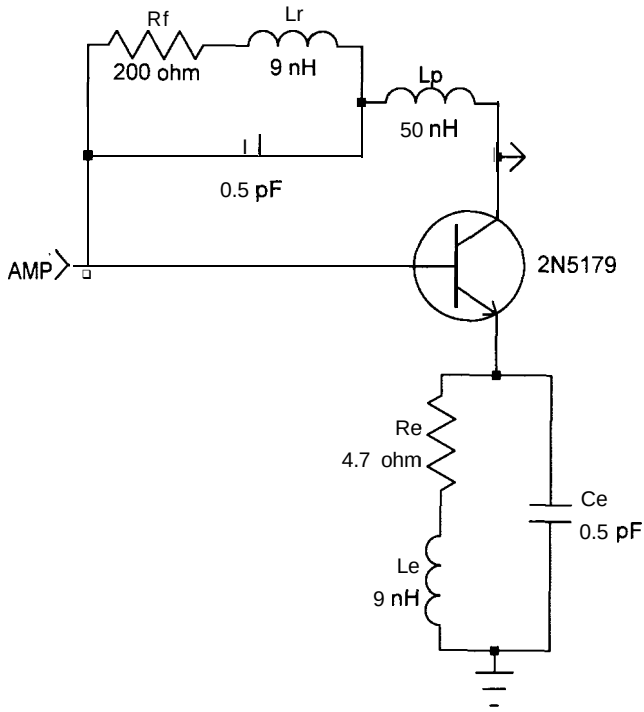


Figure ***1-13*** *Schematic of a broadband feedback amplifier with resistorparasitics included.*

inductance causes significant performance degradation. However, parasitic capacitance has no discernible effect in R_e (CRE).

Parasitic sensitivities are highest for capacitance in R_f because the resistor value is higher A small series reactance has little effect while parallel capacitance shunts the high resistance. On the other hand, the low resistance of R_e makes it extremely susceptible to small values of series inductive reactance but insensitive to parallel capacitive reactance.

The effect of emitter resistor inductance is reduced by smaller resistor length (such as 1/8 watt or chip resistors) or by using two or more resistors in parallel. Two resistors effectively reduce the

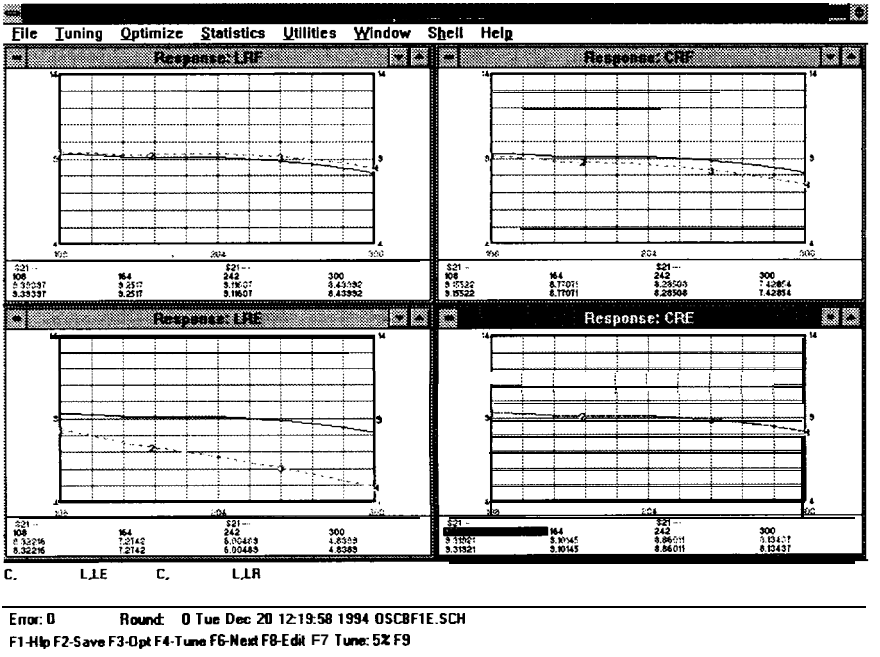


Figure 1-14 *Gain responses of the 2N5179 transistor amplifier with ideal elements (all solid traces). Dashed responses are with 9 nH inductance in Rf (LRF), 0.5 pF in Rf (CRF), 9 nH inductance in Re (LRE) and 0.5 pF in Re (CRE).*

lead inductance by a factor of 2. The increased parasitic capacitance is unimportant because it has little impact on the response.

Another potential problem is the lead inductance of the 2N5179 transistor. The emitter lead must be very short. A better solution would be to use a leadless form of this transistor.

These are but a few of the parasitic considerations with which the high-frequency designer must deal. Remember, it is very important to become habitual about considering these effects for every component. It has been the author's experience that designers readily find solutions to these problems once the problems are recognized.

1.12 References

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[2] Ralph S. Carson, *High-Frequency Amplifiers*, John Wiley & Sons, New York, 1982.

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[4] Application Note 95, S-Parameters-Circuit Analysis and Design, Hewlett-Packard, Palo Alto, CA, September 1968.

[5] Application Note 154, S-Parameter Design, Hewlett-Packard, Palo Alto, CA, April 1972.

[6] Philip H. Smith, Transmission Line Calculator, *Electronics*, Vol. 12, January 1944, p. 29.

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[8] Randall W. Rhea, *HF Filter Design and Computer Simulation*, Noble Publishing, Atlanta, 1994.

2

Oscillator Fundamentals

Two methods of oscillator analysis and design are considered in this book. One method involves the open-loop gain and phase response versus frequency. This Bode response [1] and nonlinear effects discussed later predict many aspects of oscillator performance. A second method considers the oscillator as a one-port with a negative real impedance to which a resonator is attached. The loop methodprovides a more complete and intuitive analysis while the negative resistance method is more suitable for broad tuning oscillators operating above several hundred megahertz.

The loop method is studied first. Consider the amplifier-resonator cascade in Figure 2-l. The cascade is driven by a source with a resistance of Z_o and is terminated in a load resistance of Z_o. The gain (forward) at a given frequency is

$$G_f = 20 \log |C_{21}| \qquad 2.1$$

where C_{21} is the magnitude of the forward-scattering parameter for the cascade at a given frequency The transmission phase at a given frequency is the angle of C21. If the cascade is matched at the input and output to Z_o the magnitudes of C_{11} and C_{22}, the input and output scattering parameters, are zero.

The gain-phase response for a typical cascade is given in Figure 2-2. The normal convention of the Bode response is to plot frequency on a logarithmic scale. Because oscillators typically operate over less than a decade of bandwidth, we will use a linear frequency scale. The curve on the left with a peak just above 100 MHz is the gain plotted on a scale of -20 to 20 dB. The S-shaped trace is the transmission phase plotted on a scale of -225^o to 225^o. Plotted on the right Smith chart are the cascade input return loss,

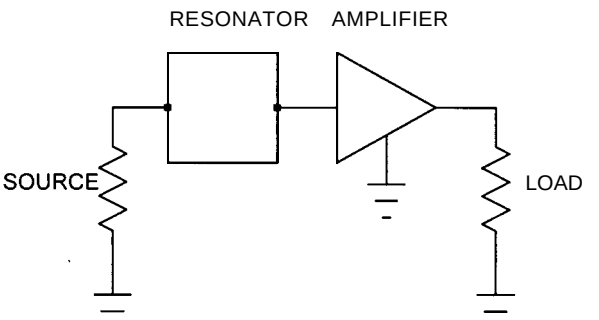

Figure 2-1 *Simple amplifier and resonator cascade and resulting open-loop Bode response.*

S11, (left of chart center) and the output return loss, S22, (right of chart center).

The cascade transmission phase is zero-degrees at 100 MHz (marker numbers 3 and 7). The gain at this frequency is 12.7 dB. The gain in excess of zero decibels at the phase zero crossing is referred to as the gain margin. When the output of the cascade is connected to the input, any initial signal at the frequency of zero-degree phase shift is amplified and continually increases in level. When the signal reaches a sufficiently high level, amplifier nonlinearities reduce the gain and the level stabilizes with unity network gain. Noise or power-on transients readily provide this initial signal.

Oscillation occurs at the frequency of a zero-degree phase shift. Limiting may modify the phase response and shift the oscillation frequency from the open-loop value. It is shown later that for a well-designed oscillator, this effect is small. A very important practical aspect of this analysis method is that the open-loop Bode response is readily measured with a network analyzer, allowing verification of the oscillator design prior to closing the loop.

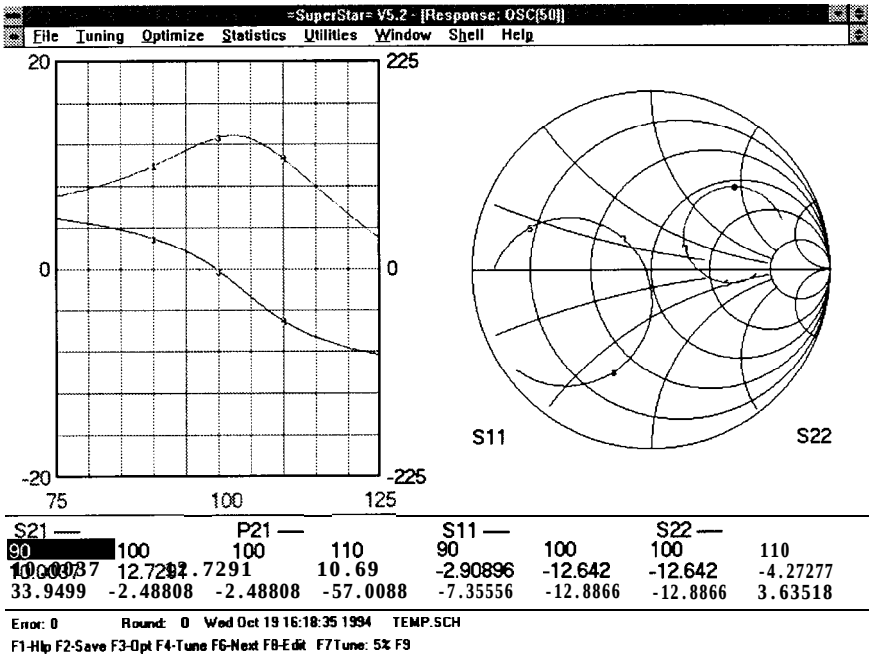

Figure 2-2 *Open-loop transmission gain and phase (left) and input and output match (right) of a resonator-amplifier cascade.*

2.1 An Example

Figure 2-3 shows the schematic of the cascade used to compute the open-loop response given in Figure 2-2. A pi-network resonator is cascaded with a common-emitter 2N5179 bipolar NPN transistor amplifier. R_c is the collector DC load resistance and R_b provides base bias. R_f is an RF feedback resistor which is decoupled for biasing through a 1000 pF capacitor. The output 1000 pF capacitor is used for DC decoupling of the collector and base when the oscillator is finally formed by connecting the output to the input.

A characteristic of well-designed oscillators is a gain peak near the phase zero crossing frequency A second desirable characteristic is a phase-zero-crossing near the maximum phase slope.

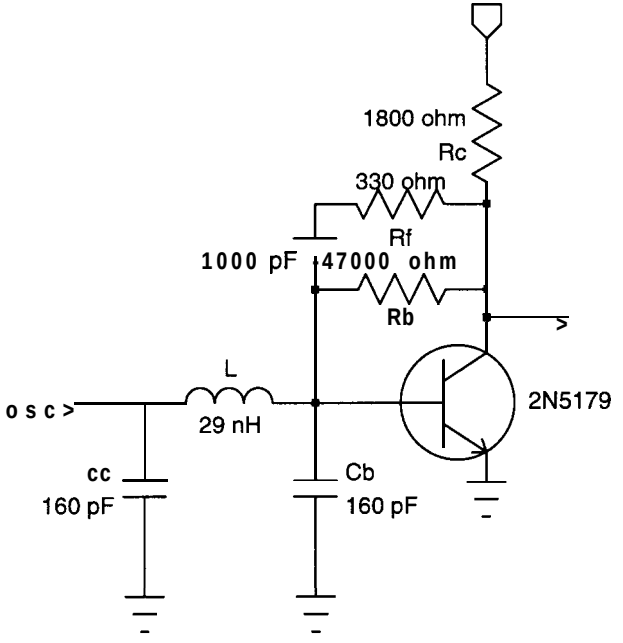

Figure 2-3 ***Schematic of a 100 MHz example oscillator.***

These criteria are approximately satisfied in this example with the gain peak and maximum phase slope occurring near 102 MHz. The gain margin is large for this example, ensuring that variations in production transistor parameters, passive component tolerances, and temperature effects are unlikely to prevent oscillation.

2.2 Mismatch

The input and output scattering parameters for the cascade, C_{11} and C_{22}, are plotted on the Smith chart in Figure 2-2. Marker 7 is at the phase zero crossing frequency of 100 MHz. C_{11} is 0.24 at 133^0 and C_{22} is 0.23 at 40^0. When the cascade input and output impedances are not equal to Z_o, the mismatch results in an analyzed gain that differs from the maximum available gain. If

the input and output impedances are equal to each other and real, but not equal to Z_o, then in the analysis, Z_o may be readjusted to obtain a correct analysis. The gain and phase are then accurately modeled. To simplify measurement of the Bode response, it is generally desirable to design the oscillator network so that the input and output impedances are equal to the impedance of available measurement equipment, typically 50 or 75 ohms.

For this first' example, C_{22} is not exactly equal to Z_o, and the calculated and displayed loop gain is less than it would be if the output were matched [2]. When the output of this cascade is connected to the input to form the oscillator, the mismatch will reduce the loop gain below the maximum available value.

If the amplifier reverse isolation is adequate, C_{12} may be assumed zero. The loop gain, with the output driving the input, may then be derived from equation 1.38.

$$G_{\text{open loop}} = \frac{1-|C_{22}|^2}{|1-C_{11}C_{22}|^2}\ C_{21}{}^2\ \frac{1-|C_{11}|^2}{|1-C_{11}C_{22}|^2} \qquad 2.2$$

where

C_{11} = cascade input reflection coefficient 2.3

C_{22} = cascade output reflection coefficient 2.4

$\Gamma_S = C_{22}$ 2.5

$\Gamma_L = C_{11}$ 2.6

For this example,

$$G = 0.851 \times 18.66 \times 0.847 = 13.45 = 11.3 \text{ dB} \qquad 2.7$$

In this case the mismatch reduces the open-loop gain by 1.4 to 11.3 dB. Because feedback is often employed in the amplifier, the assumption that $C_{12}=0$ may not be valid. In this case, equation 2.2 only approximately represents the open-loop gain with the cascade terminating itself The best policy is to design the cascade for at least a reasonable match at both the input and output. The cascade may include matching networks at the input and

output but this level of complexity is typically not required or justified.

2.3 Relation to Classic Oscillator Theory

The open-loop concept of oscillator design is often met with considerable skepticism by engineers familiar with classic oscillator terminology For comfort consider Figure 2-4A where the oscillator cascade is drawn with only the RF components. Next, the circuit is redrawn in Figure 2-4B with the output connected to the input and the ground floated. In Figure 2-4C the emitter is selected as the ground reference point. Notice the configuration is the familiar common-emitter Pierce oscillator. In Figure 2-4D the circuit is again redrawn, this time with the base

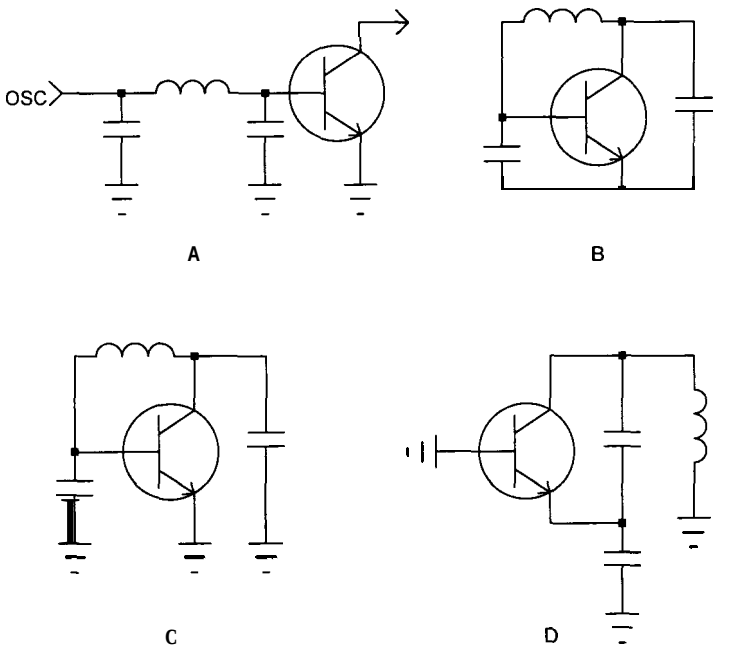

Figure 2-4 *Various definitions of the loop oscillator based on the selected ground reference point.*

selected as ground reference. The result is the familiar common-base Colpitts. These open-loop, Pierce and Colpitts oscillators are in fact the same oscillator!

2.4 Loaded *Q*

The oscillator loaded Q is a critical parameter. The loaded Q is a direct indication of many oscillator performance parameters. A high loaded Q

(a) Reduces phase noise

(b) Reduces frequency drift

(c) Isolates performance from active-device variation

Phase noise is inversely proportional to the square of the loaded Q [4]. Drift is reduced because the resonator solely determines the oscillation frequency in high-Q designs. Isolating the resonator from active device reactances reduces the effect of temperature. Many oscillator designs have low loaded Qs. The phase noise and long-term stability of these designs are far from optimum. An oscillator with a low loaded Q is often the root problem even though designers offer imaginative and esoteric descriptions of the problem. Noise is discussed further in Chapter 4.

The open-loop loaded Q of a cascade is

$$Q_l = \frac{f_o}{BW_{3dB}} \tag{2.8}$$

For the 100 MHz example the loaded Q is approximately 5.2. The loaded Q in terms of the phase slope is

$$Q_l = 0.5 f_o \frac{d\varphi}{df} \tag{2.9}$$

where φ is in radians or

$$\text{"} = \frac{\pi f_o}{360} \frac{d\varphi}{df} \tag{2.10}$$

where φ is in degrees.

When the phase zero crossing does not occur at maximum phase slope, the loaded Q should be calculated using one of the latter two equations instead of using the amplitude response bandwidth. The loaded Q is less than optimum in that situation. If the phase zero crossing occurs at maximum phase slope, the first equation for loaded Q may be used.

2.5 L-C Resonator Configurations

In the previous example a 3-element pi network was used for the cascade resonator. If the resonator is considered to be a simple filter it becomes apparent that a large variety of structures can serve as a resonator. In fact all lowpass, highpass and bandpass structures have the potential to serve as a resonator. Shown in Figure 2-5 are several such structures. The element values given assume a resonant frequency of approximately 100 MHz, a loaded Q of 6.9 and 50 ohm terminations.

LC1 and LC2 are basic series and parallel resonators. At resonance, the reactance of the series inductor and series capacitor cancel, and if the components are lossless, the network essentially vanishes. For equal source and load terminations maximum power transfer occurs. LC1 is capacitive below resonance and inductive above resonance. Both conditions impede signal transmission. Transmission phase shift is zero at resonance. The parallel resonator behaves in a dual fashion with maximum transmission and zero phase shift at resonance.

The loaded Q of the series resonator terminated at the source and load in R_o is

$$Q_l = \frac{\omega L_1}{2 R_o} \qquad 2.11$$

The loaded Q of the doubly-terminated parallel resonator is

$$Q_l = \frac{2 R_o}{\omega L_2} \qquad 2.12$$

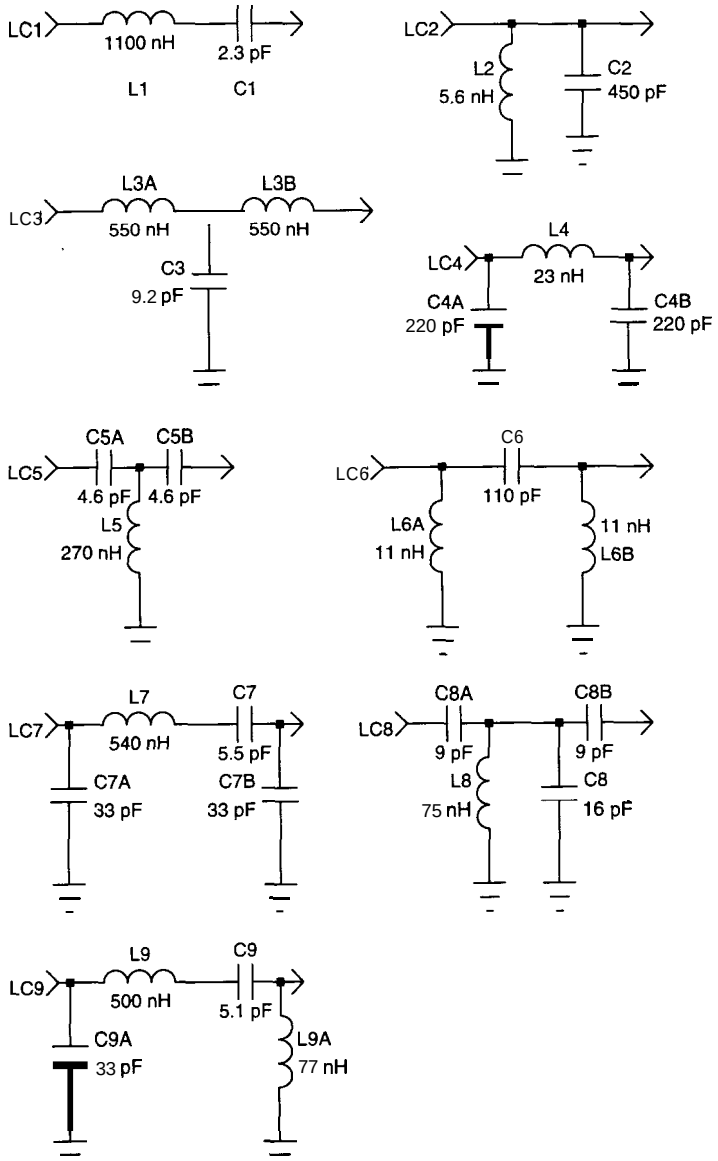

Figure 2-5 L-C resonator structures with a resonant frequency of 100 MHz and a loaded Q of 6.9 when terminated in 50 ohms.

The difficulty with the simple series and parallel resonator is extreme element values with 50 ohm terminations as the loaded Q is increased. Notice in Figure 2-5 that the series inductor, L_1, is 1100 nH and the shunt inductor, L_2, is 5.6 nH. If a higher loaded Q is desired the values become even more extreme.

LC3 through LC6 are three element resonators. LC1 and LC2 are bandpass structures. LC3 and LC4 are lowpass and LC5 and LC6 are highpass structures. At high loaded Q (6.9 in this case), the lowpass and highpass structures have responses which are similar to bandpass, at least near the resonant frequency A potential hazard of lowpass and highpass structures is that signal transmission with only small attenuation may occur over a broad band of frequencies. Unless care is exercised, additional reactances in the oscillator circuit for biasing and decoupling may cause an additional transmission phase zero and result in ambiguous oscillation frequencies. The three element forms do offer more reasonable element values. LC3 and LC5 have large but moderated inductance values and LC4 and LC6 have small but moderated element values.

Resonator LC3 is analyzed by converting each series inductor and termination resistance combination to a parallel equivalent. The resulting two shunt inductors and two shunt resistors for a parallel resonant circuit. The loaded Q for LC3 is then

$$Q_l = \frac{X_l}{R_o} \qquad 2.13$$

where X_l is the reactance of *L3A* or ***B. The*** reactance of the resonating capacitor, C_3, is then

$$X_{C3} = \frac{R_o^2 + X_l^2}{2X_l} \qquad 2.14$$

Element values for the simple and three element resonators are unique. Only one set of values satisfy a given loaded Q and termination resistance.

Although values for the three element resonators are more moderate than the simple resonators, as the loaded Q is increased

further, even those values become impractical. Lower termination resistance moderates values in LC1, 3 and 5 while higher termination resistance moderates values in LC2, 4, and 6. This is the basis for remarks often found in oscillator literature such as "a FET transistor is more suitable because the higher impedances load the parallel resonator lightly and provide higher Q." In the author's view this represents a narrow perspective on oscillator design. We should learn an important lesson from filter design theory. How are narrowband filters (high loaded *Q*) constructed with reasonable element values and 50 ohm terminations? The answer is found in the use of coupling elements.

C7A and B in the four element resonator LC7 are examples of coupling elements. At 100 MHz the shunt 33 pF capacitors are approximately 50 ohms of reactance which are in parallel with the terminations. The resulting series equivalent R-C networks and the input and output are 25 ohms resistance and 25 ohms reactance (the reactance of a 66 pF capacitor). The effective termination resistance is halved and the required resonator series inductor, L7, for a given loaded Q is half the inductance of the simple series resonator LC1. Two series capacitors of 66 pF each increase the resonating capacitor from approximately twice the simple resonator capacitance of 2.3 pF (4.6 pF) to 5.5 pF. Increasing the coupling capacitors would further reduce the required inductance to achieve a given loaded Q. Thus the four element coupled resonators provide a degree of freedom in element values.

For the LC7 series resonator (shunt-C coupled series resonator), the effective capacitance which resonates with the series inductor is

$$C_e = \frac{1}{\frac{1}{C_7} + \frac{2C_{7A}(\omega_o R_o)^2}{(\omega_o R_o C_{7A})^2 + 1}} \qquad 2.15$$

where

C_7 = series resonator capacitor 2.16

C_{7A} = shunt coupling capacitor 2.17

R_o = input and output load resistance 2.18

The required inductance to resonate at f_o is then

$$L_7 = \frac{1}{\omega_o{}^2 C_e} \tag{2.19}$$

The loaded Q of the LC7 resonator is a function of the shunt coupling capacitors. The reactance required for a given loaded Q is approximately

$$X_{C7A} = R_o\left(\frac{2R_oQ_e}{X_l} - 1\right)^{-1/2} \tag{2.20}$$

where

$$Q_e = \frac{1}{\frac{1}{\&l} - \frac{1}{Qu}} \tag{2.21}$$

and Qu is ***inductor unloaded Q.***

For LC8 (top-C-coupled parallel resonator) the effective resonating capacitor is

$$C_e = C_8 + \frac{2C_{8A}}{(\omega_o R_o C_{8A})^2 + 1} \tag{2.22}$$

The top-C coupled resonator in Figure 2-4 requires series coupling reactances of approximately

$$X_{8A} = \left(\frac{2R_oQ_e}{B_{L8}} - R_o^2\right)^{1/2} \tag{2.23}$$

where

B_{L8} = admittance of the shunt inductor 2.24

The coupling elements may be inductors or mixed, as discussed in the series resonator case above.

2.6 L-C Resonator Phase Shift

The transmission phase shift at resonance (maximum transmission and maximum phase slope) of the simple resonators is zero degrees. The transmission phase shift of the three element resonators at resonance is 180^o.

The four element coupled resonators also provide a degree of freedom in transmission phase shift at resonance. For example, with LC7, for a given Q, smaller values of shunt capacitance lead to larger series inductance up the the value of inductance for the simple resonator. At this extreme, the transmission phase approaches zero-degrees. Large values of shunt capacitance decrease the series inductance and the transmission phase approaches -180^o at resonance. The LC8 resonator has a transmission phase shift of zero-degrees for large C8A and B and $+180^o$ for small C8A and B. The designer therefor has available resonators of arbitrary transmission phase at resonance!

2.7 Resonators as Matching Networks

The element values of the resonators in Figure 2-5 are symmetric with respect to the input and output. If the elements are lossless (high unloaded Q), at resonance the input impedance is purely resistive and equal to the termination resistance. If the termination resistance is 50 ohms the input resistance is 50 ohms and if the termination resistance is 1000 ohms the input resistance is 1000 ohms. Although the resonant frequency shifts with termination resistance for the three and four element resonators, at resonance the input impedance equals the termination resistance.

Earlier it was stated that one oscillator design goal was a matched cascade input and output impedance. The resonator behavior described above naturally maintains this criteria provided the cascade amplifier is matched at the input and output. If the amplifier input and output impedance are not matched, it is often possible to use the resonator as a matching device by perturbing the symmetry of a three or four element resonator. This is

preferred to adding matching networks because the number of elements and the possibility of introducing additional resonances are minimized.

For example, consider resonator LC7 cascaded with an amplifier with an input resistance of 200 ohms and an output resistance of 50 ohms. The resonator is terminated in 200 ohms. The input resistance looking into the resonator would be 200 ohms if LC7 were symmetric. When C_{7A} is reduced to approximately 20 pF, LC7 acts as a matching network with an input resistance of 50 ohms, therefore matching the cascade input and output impedance. The resonators are also capable of absorbing termination reactance by adjustment of resonator reactances.

2.8 Resonator Voltage

In an earlier section we listed desirable attributes of high loaded Q. However, there are fundamental limitations to the maximum loaded Q. As the cascade loaded Q approaches the unloaded Q of components in the resonator the resonator insertion loss approaches infinity The insertion loss for the resonator is

$$IL = -20 \log\left(\frac{Q_u - Q_l}{Q_u}\right) \qquad 2.25$$

where ***IL*** is a positive decibel number. ***IL*** is therefore equal to $-S_{21}$ dB. For example, if Q_u = 100 and Q_l = 21.5, ***IL = 2.1*** dB. If the cascade amplifier has adequate gain then significant loss can be tolerated in the resonator. Nevertheless, the loaded Q can not exceed the component unloaded Q.

A second factor which may limit the maximum loaded Q is resonator voltage. This is particularly a problem with high-power oscillators and oscillators with varactor tuning elements. The voltage at resonance across the shunt inductor and capacitor in LC8, the top-C coupled parallel resonator, is given by

$$V_r = \frac{V_s}{R_o - jX_{C8A}\left(\frac{2R_o}{R_o^2 + X_{C8A}^2} + \frac{B_{L8}}{Q_u}\right)^{-1}} \qquad 2.26$$

where V_s is source voltage into R_o ohms and B_{L8} is the admittance of the shunt inductor.

The insertion loss, Q_l and V_r versus X_s are given in Figure 2-6 for Q_u = 200, R_o =50 ohms, V_s = 0.707 V_{rms} (+10 dBm,) and B_{L8} = .01 mhos. Notice with only 0.707 volts drive the resonator voltage reaches 5 V_{rms} or 14.1 $V_{p\text{-}p}$ at Q_l/Q_u = 0.5! The insertion loss at Q_l/Q_u = 0.5 is 6.02 dB. A varactor used for C8 would be driven

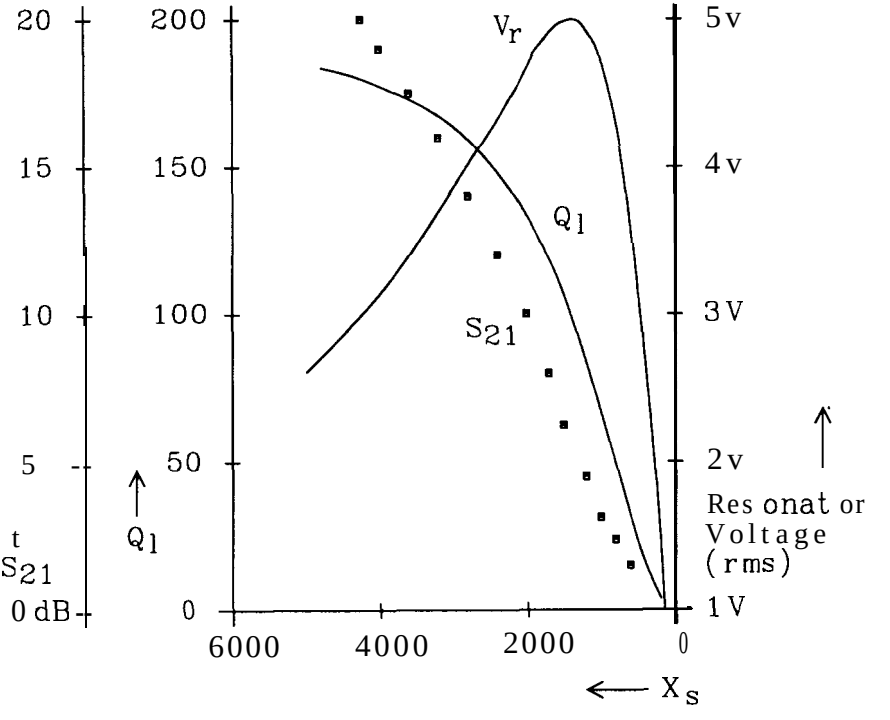

Figure 2-6 *Insertion loss, loaded Q and resonator voltage as a function of the coupling reactance in top-C coupled parallel resonators.*

into heavy forward conduction and perhaps even reverse breakdown by the RF voltage. Since this significantly degrades resonator unloaded Q and increases loss, limiting in the cascade occurs in the resonator instead of the amplifier, an intolerable situation leading to erratic tuning and poor stability

The varactor may be decoupled from the resonator by placing a very small capacitor in series with the varactor, therefore dropping most of the voltage across the series capacitor. However, the varactor now has much less ability to shift the oscillation frequency Thus, we face a fundamental tradeoff; high loaded Q results in high resonator voltage and impedes broadband varactor tuning. Keep in mind that broad tuning and high Q are not inherently impossible. The problem is resonator voltage. When tuning elements are not effected by high voltage, such as with mechanically tuned capacitors and cavities, broad tuning and high Q are possible. A wonderful example is the venerable Hewlett-Packard model HP608 signal source.

2.9 Transmission Line Resonators

Over limited bandwidth there are important lumped (L-C) and distributed (transmission-line) equivalences. For example, a shunt inductor may be replaced with a shorted transmission line stub. The equivalent inductive reactance of a shorted stub less than 90^o long is

$$X_l = Z_o \tan \theta_e \qquad 2.27$$

where

$$\theta_e = \text{electrical length of the stub} \qquad 2.28$$

$$Z_o = \text{characteristic impedance of the line} \qquad 2.29$$

Similarly, an open stub less than 90^o long may replace a capacitor. The equivalent capacitive reactance is

$$X_c = Z_o \tan \theta_e \qquad 2.30$$

The reactance of inductors and capacitors vary linearly with frequency over the entire frequency range for which component parasitics are not a problem. From the above expressions we see the reactance of transmission line stubs are trigonometric functions of frequency which are linear and therefore simulate lumped reactance when the electrical length is short. The error is about 1% at 10^o and 10% at 30^o. The reactance is predicted accurately by the above equations for any length less than 90^o. It is not absolutely necessary that the reactance varies linearly with frequency unless the oscillator is to be tuned over a wide frequency range. Electrical lengths of 45^o or even 60^o are sometimes used. However, as the length approaches 90^o, the reactance approaches infinity Unlike lumped elements, transmission line elements do not have unique solutions for Z_o and θ_e. For example, 50 ohms of inductive reactance is simulated with a 50 ohm shorted stub 45^o long or a 100 ohm shorted stub 26.56' long.

The equations above describe the equivalence between a single lumped and a distributed element. A distributed element also may serve as an equivalent to an L-C pair. A high-impedance transmission line which is 180^o long at f_o behaves like a series L-C resonator at f_o with an inductive reactance given by

$$X_l = \frac{\pi Z_o}{2} \qquad 2.31$$

Likewise, a transmission line shorted stub which is 90^o long at f_o behaves like a parallel L-C resonator at f_o with an inductive reactance given by

$$X_l = \frac{4Z_o}{\pi} \qquad 2.32$$

Shown in Figure 2-7 are various transmission line resonators with a resonant frequency of 100 MHz and a loaded Q of 5.2 when terminated in 50 ohms. TL1 and TL2 are analogous to LC1 and LC2 and are a direct implementation of the above equations. Notice the extreme values of line impedance. This is a direct carry-over of the extreme L-C values for these simple resonator forms. As with the L-C resonators, the transmission line imped-

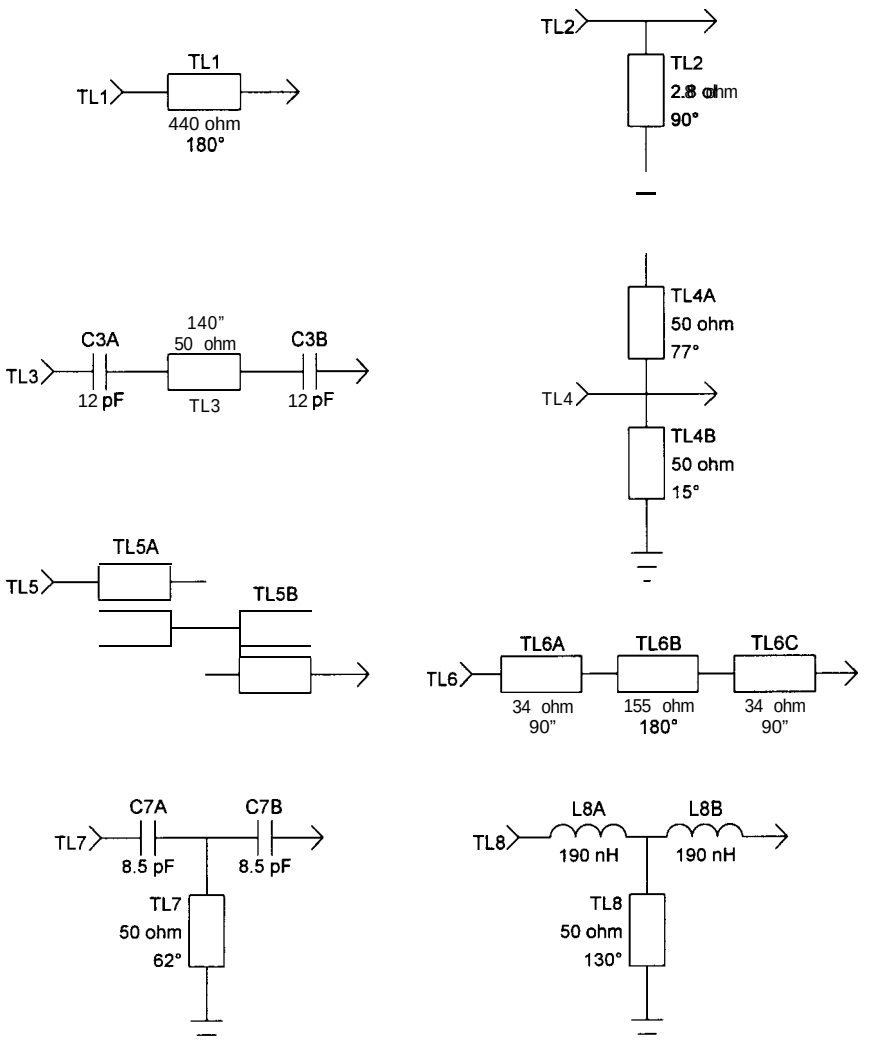

Figure 2-7 *Transmission line structures with a resonant frequency of 100 MHz and a loaded Q of 5.2 when terminated in 50 ohms.*

ance values are moderated by lower termination resistance for the series resonator and higher termination resistance for the shunt resonator.

Again, as with the L-C resonators, the solution is to use coupling techniques. Examples are given as TL3 through TL8 in Figure 2-7. Most of these examples use transmission lines with a characteristic impedance of 50 ohms. However, transmission line resonator solutions are typically not unique and alternative resonators with either higher or lower line impedance are possible.

End coupling capacitances are used in TL3. 12 pF is far too much capacitance to realize as a gap in microstrip and lumped elements would be used. At higher microwave frequencies a gap becomes feasible. The capacitive loading shortens the required transmission line electrical length at the resonant frequency In this case the line length is approximately 140^o. For higher loaded Q the end capacitors must be smaller and transmission line shortening is reduced.

The end-coupling capacitors as a function of Q are

$$C_c = \frac{1}{\omega_o Z_o}\left(\frac{4Q_l}{\pi} - 1\right)^{-1/2} \qquad 2.33$$

The required length of the transmission line for resonance is

$$\theta_e = 180^o - \tan^{-1} 2\omega_o Z_o C_c \qquad 2.34$$

assuming the Z_o of the resonator transmission line equals the input and output load resistance. In practice, the resonator may be higher or lower in impedance if the coupling capacitors and resonator length are adjusted. This technique may be used to shift slightly the location of the phase zero crossing on the phase slope, particularly for lower Qs.

In TL4 a shunt resonator is tapped to increase the loaded Q for the moderate 50 ohm line impedance. The total electrical length of the two sections is somewhat greater than 90^o because of termination loading.

Coupled transmission line elements are used in TL5. Each of the two coupled sections are 90^o long so that the continuous middle line is a total of 180^o long. The coupled transmission line sections are defined by their even and odd mode impedances, in this case 72 and 35 ohms respectively The line widths may be equal and are similar to 50 ohm lines because $\sqrt{72 \times 35}$ is approximately 50. Additional information on coupled lines, and other lumped/distributed equivalents, is given in ***HF Filter Design and Computer Simulation*** [3].

TL6 is a stepped-impedance transmission line resonator. Line TL6B is a high-impedance resonator which is approximately 180^o long. To moderate the line impedance, low-impedance sections TL6A and TL6C act as transformers to reduce the termination resistance presented to the resonator. In this case the coupling sections are 90^o long and transform the 50 ohm terminations to 23 ohms with no reactive component so the resonator section is 180^o long. To conserve space shorter coupling sections may be used. For a given loaded Q, shorter coupling sections must have a lower impedance and they introduce inductive reactance which causes a small increase in the length of the resonator line.

TL7 and TL8 are shorted stub resonators with capacitive and inductive coupling respectively TL7 is analogous to LC8 in Figure 2-5. The reactance coupled to the resonators causes the capacitive-coupled resonator to be less than 90^o long and the inductive coupled resonator to be greater than 90^o long.

2.10 Re-entrance

Oscillators constructed with transmission line elements or resonators have re-entrant modes. For example, a half-wavelength resonator is also resonant at approximately odd multiples of the fundamental frequency The open-loop cascade gain and phase should be examined at these higher resonances. If necessary, lumped reactive elements may be added to reduce the cascade gain to less than 0 dB above the desired oscillation frequency

2.11 Quartz Crystal Resonators

A quartz crystal resonator is a thin slice of quartz with conducting electrodes on opposing sides [6]. Applying a voltage across the crystal displaces the surfaces, and vice versa. The quartz is stiff, and the crystal has natural mechanical resonant frequencies which depend on the orientation of the slice in relation to the crystal lattice (cut). Although there are many crystal cuts, the most common cut for high-frequency application is AT FT-243 crystals, in common use during World War II, had spring-loaded thick metal plates pressing against each side of the quartz slice. These crystals could be disassembled and the quartz etched to reduce the resonant frequency Drawing a graphite pencil mark on the quartz lowered the resonant frequency Modern quartz crystals use electrodes plated directly onto the quartz disk.

Quartz crystals have very desirable characteristics as oscillator resonators. The natural oscillation frequency is very stable. In addition, the resonance has a very high Q. Qs from 10,000 to several hundred thousand are readily obtained. Qs of 2 million are achievable. Crystals of high performance can be mass produced for a few dollars. The crystal merits of high Q and stability are also its principal limitations. It is difficult to tune (pull) a crystal oscillator.

Quartz crystal resonators are available for frequencies as low as 1 kHz. The practical frequency range for fundamental-mode AT-cut crystals is 0.6 to 20 MHz. Crystals for fundamental frequencies higher than 20 to 30 MHz are very thin and therefore fragile. Crystals are used at higher frequencies by operation at odd harmonics (overtones) of the fundamental frequency Ninth-overtone crystals are used up to about 200 MHz, the practical upper limit of crystal oscillators.

It is possible to extend the maximum operating frequency and still maintain adequate mechanical strength by surrounding a very thin quartz disk with a thicker concentric outer support ring integral to the quartz. This structure is manufactured by chemical etching techniques [7]. Due to the resulting shape, the resulting structure is referred to as inverted mesa.

A simplified electrical equivalent circuit for the quartz crystal is given in Figure 2-8. C_o is the capacitance formed by the electrodes separated by the quartz dielectric. It is static and may be measured at any frequency well below resonance. R_m, L_m and C_m are the motional parameters of the crystal. L_m and C_m resonate at the series resonant frequency of the crystal. R_m is associated with the loss of the resonator. The model in Figure 2-8 represents one oscillation mode. A more complex model can represent a crystal through as many overtones modes as desired. For the sake of simplicity, this simple model is usually employed and different values are used to model fundamental or overtone modes. Spurious resonances occur at frequencies near the desired resonance. In a high-quality crystal, the motional resistance of spurious modes are at least two or three times the primary resonance resistance and the spurious modes may be ignored.

Crystal manufactures can provide specific data on model parameters. Nominal values are a function of the fundamental frequency and the overtone being used. The manufacturer has some control over parameter values. Typical fundamental-mode values are

$$C_o = 3 \text{ to } 8 \text{ pF} \tag{2.35}$$

$$\text{Cm} = 0.004C_o \tag{2.36}$$

$$L_m = \frac{1}{(2\pi f_s)^2 C_m} \tag{2.37}$$

$$R_m = 400 \text{ ohms at 1 MHz to 20 ohms at 20 MHz} \tag{2.38}$$

where

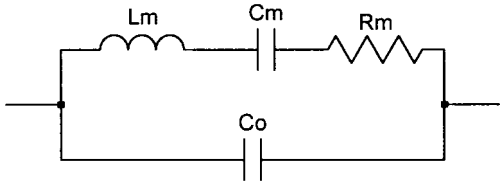

***Figure 2-8** Lumped R-L-C model for a quartz crystal.*

f_s = series resonant frequency 2.39

For overtone crystals

$$C_0 = 3 \text{ to } 8 \text{ pF} \quad (2.40)$$

$$C_m = \frac{C_{m\,\text{fund}}}{\text{overtone}^2} \quad (2.41)$$

$$L_m = \frac{1}{(2\pi f_s)^2 C_m} \quad (2.42)$$

R_m = 35 ohms for third overtone 2.43

= 55 ohms for fifth overtone 2.44

= 90 ohms for seventh overtone 2.45

= 150 ohms for ninth overtone 2.46

The parameters may be determined by measuring S_{21} versus frequency with a high-quality scalar or vector network analyzer. The crystal is inserted in series in the transmission path. A response similar to Figure 2-9 should be observed. The crystal Q is very high. Careful tuning of the analyzer center frequency and a narrow scan width are required. The peak transmission point occurs at the series resonant frequency, f_s. *The* insertion loss at

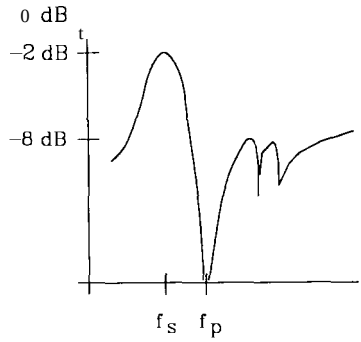

Figure 2-9 *Insertion loss response of a quartz crystal resonator.*

series resonance is *IL*. The transmission zero just above f_s in frequency is the parallel resonance, f_p. First, C_o is obtained by measuring the capacitance at a low frequency, such as 1 kHz. Then

$$C_m = C_0 \left[\left(\frac{f_p}{f_s} \right)^2 \frac{f_p}{f_s} - 1 \right] \qquad 2.47$$

$$L_m = \frac{1}{(2\pi f_s)^2 C_m} \qquad 2.48$$

$$R_m = 2Z_0 \left[10^{IL/20} - 1 \right] \qquad 2.49$$

where

Z_0= transmission measurement system impedance 2.50

2.12 Crystal Dissipation

Over-excitation of a quartz crystal causes a long-term change of the crystal parameters (aging). Although the change is small, generally a few parts per million, in some applications it is significant. For best aging, crystal dissipation in the circuit should be less than 20 μW [8]. Severe over excitation can crack the quartz crystal. For AT cuts, to avoid damaging the crystal, the dissipation should be less than 2 mW, below 1 MHz and above 10 MHz, and less than 5 mW from 1 to 10 MHz.

The dissipation may be computed by E^2/R_m, where *E* is the rms voltage across the crystal exactly at series resonance. A more precise measurement method is to place a small resistance in series with the crystal and find the current based on the voltage drop across the added resistance. The dissipation is then calculated by I^2R_m.

2.13 Pulling Crystal Oscillators

The long-term stability and close-in phase noise performance of crystal oscillators is superior to L-C and cavity oscillators but tuning more than a fraction of a percent of the resonant frequency is difficult. L-C oscillators, while less stable and noisier, are readily tuned a octave or more in frequency For frequencies up to about 100 MHz, there are not many alternatives between these two extremes. The primary limitation is C_o. If it were not for C_o, crystal oscillators could be pulled much further. The pulling range for fundamental-mode crystals is approximately

$$F_{\text{pull}} = \left(\frac{C_o + C_m}{C_o} \right)^{1/2} \qquad 2.51$$

Since C_m is nominally about $0.004C_o$, the pull range is about 1.002, or 0.2%. The pulling range for overtone-mode crystals is

$$F_{\text{pull overtone}} = 1 + \frac{F_{\text{pull}} - 1}{\text{overtone}^2} \qquad 2.52$$

A typical ninth overtone crystal pulling range is 1.000025. This is only 25 ppm!

Shown in Figure 2-10 is a crystal resonator with a series pulling capacitor, C_t. Disregarding C_o, the pulling capacitor in series with the motional capacitance reduces the net effective series capacitance, increasing the series resonant frequency In Figure 2-11 the transmission of such a network with a very large value of C_t is shown as the solid trace. In this case fs is $10\,\text{MHz}$, R_m is 30

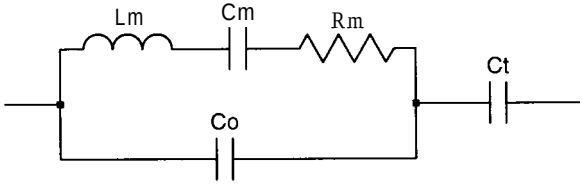

Figure 2-10 *Quartz resonator model with pulling capacitor.*

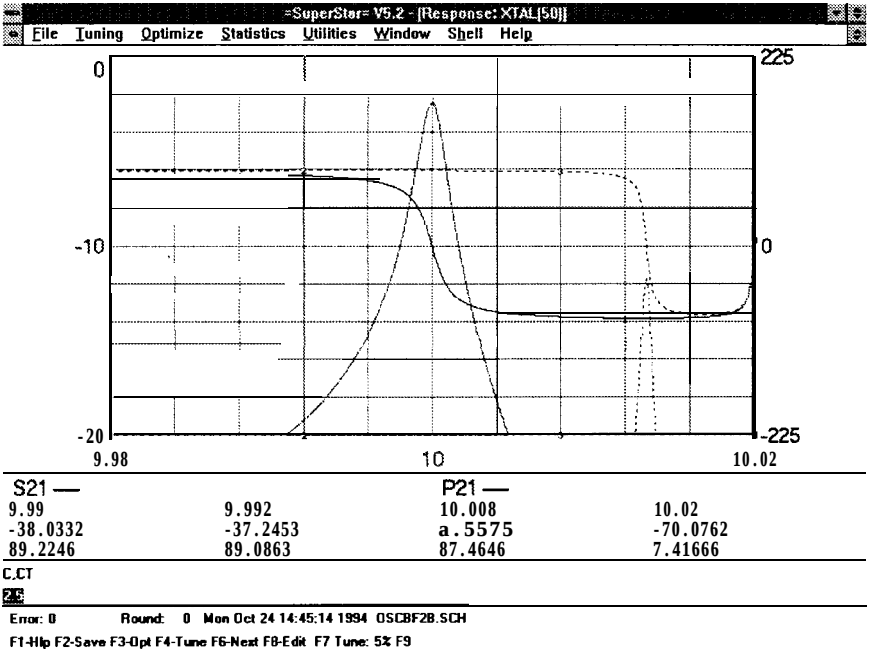

Figure 2-11 *Transmission gain and phase response of a 10 MHz quartz resonator before (solid) and after (dashed) pulling with a 2.5 pF series capacitor.*

ohms, C_o is 5 pF and C_m is 0.02 pF. The gain curve peaks and the transmission phase is zero at series resonance. The insertion loss is 2.5 dB. The transmission phase is again zero at parallel resonance just above 10.016 MHz but the transmission gain is very low. The dotted curve in Figure 2-11 is the network response with C_t at 2.5 pF. Decreasing C_t from a large value to 2.5 pF has pulled the frequency up about 13 kHz. The gain is reduced to about -12 dB. If C_t is further reduced to pull the frequency higher, the gain rapidly falls as the frequency approaches parallel resonance. This parallel resonance, caused by C_o resonating with a net inductive reactance of the motional arm above series resonance, is the limiting factor in crystal pullability

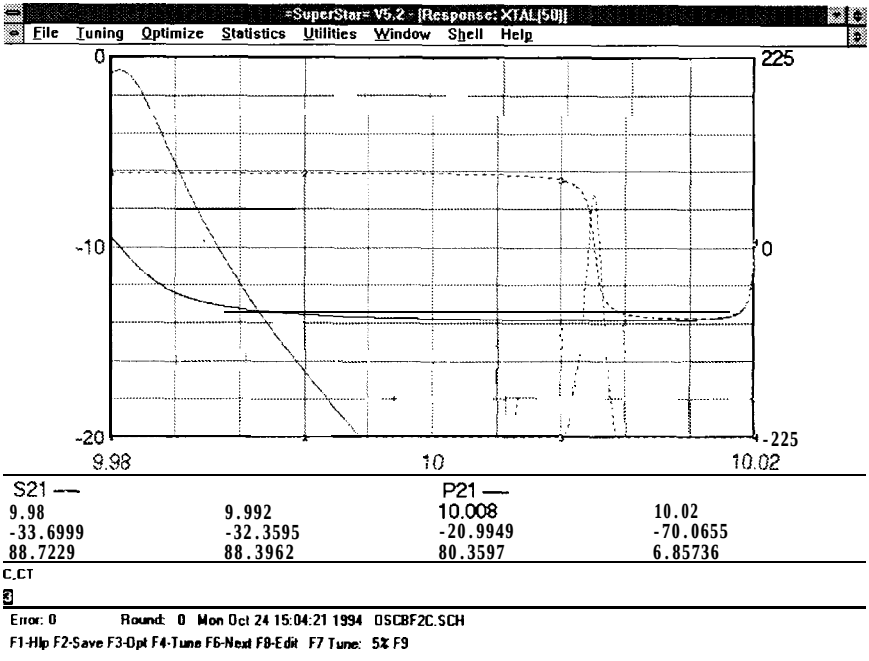

Figure 2-12 *Quartz resonator pulling with a 33 μH series inductor and a 32 pF series capacitor (solid) or a 3 pF series capacitor (dashed).*

If C_t is replaced with a series L-C, the crystal frequency can be pulled both below and above the series resonance. For example, if a 33-μH inductor is used with a nominal 7.7 pF capacitor, they resonate at 10 MHz and the crystal is unpulled. If C_t is decreased, the net reactance is capacitive and the crystal is pulled higher. If C_t is increased, the net reactance is inductive and the crystal is pulled lower. In Figure 2-12 the response is shown for an L-C pulling network with C_t at 32 and 3 pF. The inductor, L_t, is 33 μH. The amount of pulling down in frequency is determined by the value of the pulling inductor. L_t must be less than the value that resonates with C_o; otherwise, C_t, L_t and C_o form a new series resonant path which bypasses the crystal motional elements. If

this occurs, the new resonator becomes entirely L-C and crystal control is lost.

In Figure 2-13 an inductor is placed in parallel with C_o. L_o resonates with C_o at f_s. Because the Q of the L_o-C_o combination is much lower than the Q of the crystal, L_o effectively cancels the reactance of C_o for a broad frequency range around f_s. In Figure 2-14 the response of this network is shown with L_t equal to 33 μH and C_t from 80 to 2.7 pF. Notice the absence of the parallel resonance and that the gain is flat across the entire frequency range tuned by Ct. This configuration does have excellent pulling characteristics. However, the inductor values in this and the previous network are large. Inductor parasitic capacitance can create additional resonances that cause erratic behavior. Also, the farther a crystal is pulled, the more dependent the operating frequency becomes on the L-C pulling elements, eliminating the purpose of using a crystal.

2.14 Ceramic Piezoelectric Resonators

Piezoelectric resonators constructed from ceramic materials are now available for the HF frequency range. These devices bridge the gap in Q_u and stability between L-C and quartz crystal resonators. The electrical model is the same as the quartz crystal

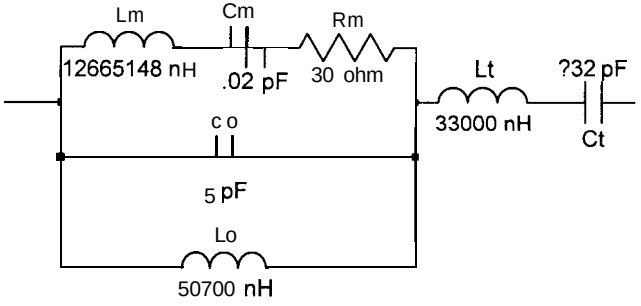

Figure 2-13 *Quartz resonator model for pulling above and below f_o using a series inductor and a compensation inductor in parallel with C_o.*

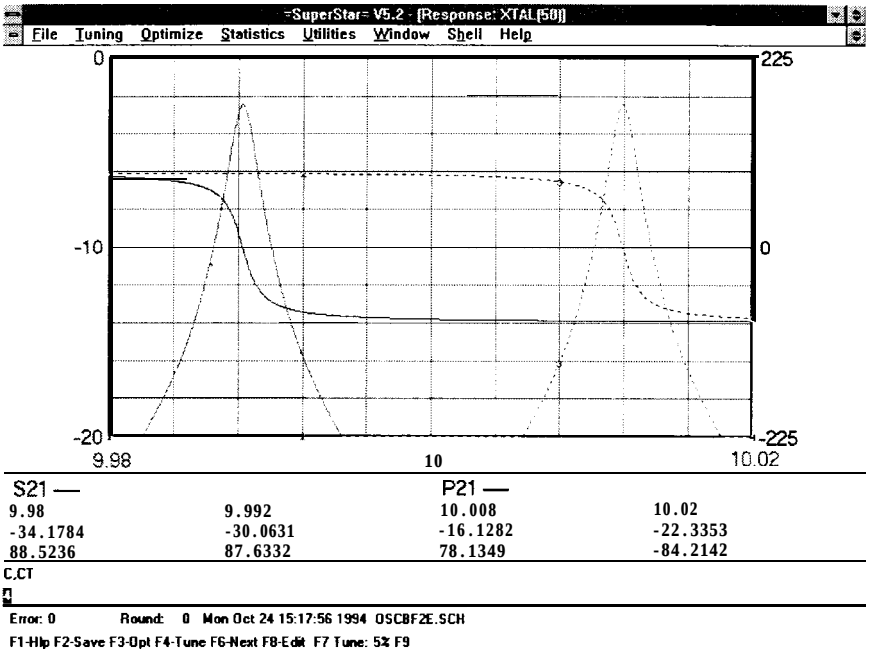

Figure 2-14 *Transmission gain and phase for a pulled quartz resonator with* C_o *compensation.* C_t *tuned from 80* pF *(solid) to 4* pF *(dashed).*

and is shown in Figure 2-8. Typical values for a 4 MHz ceramic resonator are

$$R_m = 6 \text{ ohms} \tag{2.53}$$

$$L_m = 0.3 \text{ mH} \tag{2.54}$$

$$C_m = 5.3 \text{ pF} \tag{2.55}$$

$$C_o = 42 \text{ pF} \tag{2.56}$$

The unloaded series resonant Q is about 1200 for this unit. The ratio of C_o/C_m is much smaller than an AT-cut quartz crystal, so the pullability is better. As might be expected, the stability is less than the quartz crystal.

2.15 SAW Resonators

The surface acoustic wave resonator (SAWR) is a high-Q resonator similar in some aspects to the quartz crystal resonator [9]. Interdigitized metal fingers are engraved on the surface of piezoelectric substrate. Y- cut quartz is often used. The interdigitized transducer launches and detects surface acoustic waves on the substrate. When the excited frequency is equal to V_s/p, where V_s is the propagation velocity and p is the interdigital period, the waves generated by each finger are in phase. This is the center frequency of the SAWR.

SAWRs used in oscillators have two forms, two-port and two-terminal. The two-port form has an input and an output, which are interchangeable, and a ground. The two-terminal form is similar to a quartz crystal resonator in that it has two terminals. Each form is available in two types. The RP type two-port form has approximately 180^o degrees of transmission phase shift at resonance and the RS type has approximately zero-degree phase shift at resonance. The selection is made during manufacture by the way the interdigital fingers are connected to the port terminals. Electrical models for the RP SAWR is given in Figure 2-15A and the RS type in Figure 2-15B. If the SAWR two-port is connected internally so that the ports are driven in parallel, the two-terminal forms are created. The models are given in Figure 2-15C and D. SAWRs on quartz are practical from 250 to 1200 MHz. Designs as low as 50 MHz and as high as 1500 are feasible. The frequency range of SAWR satisfies a real need, since quartz crystals are commonly available only to 200 MHz. SAWR unloaded Qs are nominally 12,000 at 350 MHz and 6000 at 1000 MHz. Typical model parameter values are

$$R_m = 120 \text{ ohms} \tag{2.57}$$

$$L_m = \frac{Q_u R_m}{2\pi f_s} \tag{2.58}$$

$$C_m = \frac{1}{(2\pi f_s)^2 L_m} \tag{2.59}$$

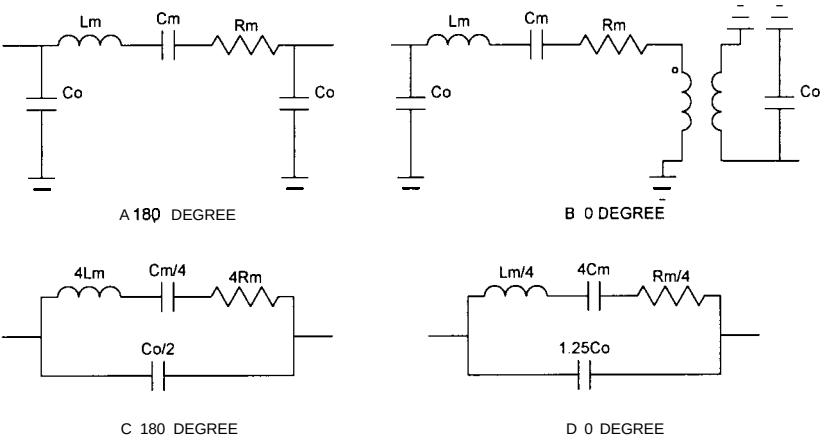

Figure 2-15 *Two-port* SAW *resonators (A&B) and two-terminal SAWRs (C&D).*

$$C_o = 2.5 \text{ pF at 200 MHz} \qquad 2.60$$

$$= 1.1 \text{ pF at 1200 MHz} \qquad 2.61$$

Typical manufacturing tolerances for SAWRs is f150 ppm. The frequency shift with a ±50° Celsius temperature range is about 80 ppm. The aging characteristics of high-quality SAWRs are about 1 to 10 ppm per year. Each of these stability parameters is substantially better than with L-C resonators but approximately an order of magnitude worse than high-quality quartz crystals. The SAWR is capable of safe operation at much higher power levels than quartz crystals and therefore the ultimate noise performance, well removed from the carrier, can be better than crystal oscillators. Typical power dissipation limits are +30 dBm at 250 MHz and +18 dBm at 1000 MHz.

2.16 Multiple Resonators

Thus far we have considered oscillator design using a single resonator as the frequency-selective phase shift network and we

have identified loaded Q as the critical parameter for high-performance oscillator design. For the single resonator, Q as defined by the loop gain response is related to the phase slope. Furthermore, since it is not the loop gain response but the phase slope that is an indication of oscillator stability and phase noise performance, it is best to define the unloaded Q in terms of the phase slope. The phase slope, $d\phi/d\omega$, is the definition of group delay Since the group delay, t_d, is

$$t_d = \frac{-d\varphi}{d\omega} \qquad 2.62$$

then

$$Q_l = \frac{\omega t_d}{2} \qquad 2.63$$

Group delay is a more convenient measure of loaded Q because manual computation of the phase slope from phase versus frequency data, or manual computation of the 3-dB bandwidth from the amplitude response, is unnecessary.

Recall that a primary limitation of high loaded-Q oscillator design is the insertion loss encountered as the loaded Q approaches the unloaded Q. The goal for high-performance resonator design is therefore to achieve the greatest possible group delay for a given acceptable resonator loss. That requirement can be more optimally achieved by the use of multiple resonators. Consider the conventional top-C coupled single-section resonator in Figure 2-16A and a proposed dual-section resonator in Figure 2-16B. The capacitor unloaded Q is infinite and the inductor an unloaded Q is 100.

Shown in Figure 2-17 are the transmission gain and group delay response for these two resonator configurations. Component values have been optimized for maximum group delay with a maximum insertion loss of 10 dB. Smaller coupling capacitors result in higher group delay but loss greater than 10 dB.

The resulting group delay at resonance is 213 nS which corresponds to a loaded Q of 67. If the values are readjusted for greater

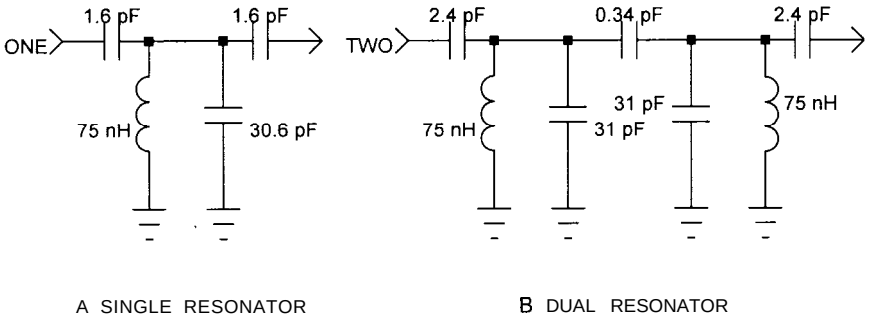

Figure 2-16 *Conventional single section top-C coupled resonators (A) and a dual-section resonator (B).*

loaded Q, the insertion loss increases. For a 10 dB loss, this is the maximum loaded Q for a single resonator.

The schematic for a dual resonator is given in Figure 2-17B. Using the same component unloaded Qs as those of the single resonator, the components in the dual resonator were optimized for maximum group delay again with a 10 dB maximum insertion loss. The resulting component values are shown in Figure 2-17B and the response in Figure 2-18. The group delay at resonance has increased to 293 nS which corresponds to a loaded Q of 92, a factor of 1.37 higher than with the single resonator. The absolute phase at f_o is different; however, the maximum phase slope (group delay) occurs at f_o, so the total resonator and amplifier phase is adjusted in the oscillator design to achieve a zero-degree phase shift at f_o.

For three resonators, the loaded Q is approximately 107. As the number of resonators increases beyond two or three, the advantage of additional resonators diminishes. Also, as the number of resonators increases, the possibility of phase ambiguities increases. As long as the loop gain is below 0 dB for the additional phase zero crossings, frequency oscillation ambiguities do not exist.

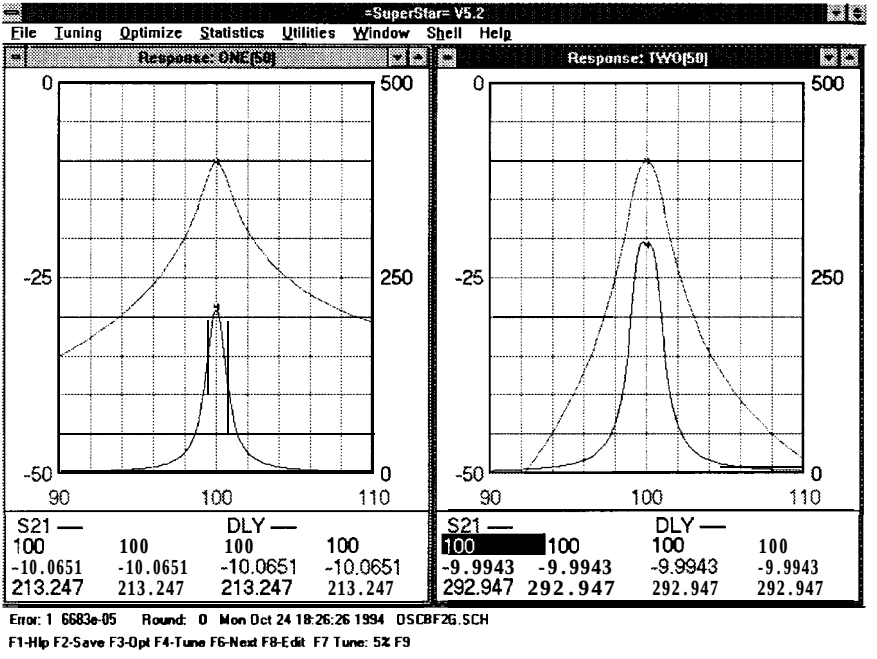

Figure 2-17 *Transmission gain and group delay responses of a single section resonator (left) and a dual section resonator (right).*

2.17 **Phase**

The phase shift of many L-C and transmission line resonators is near 180^{o}. Common-emitter amplifiers and popular Darlington MMIC amplifiers have a transmission phase shift of 180^{o} at frequencies well below the device F_t. The net phase shift of the cascade is therefore very near zero-degrees.

At higher frequencies, and for other cascade configurations, we may not be so fortunate. It is not necessary for the gain peak to occur at exactly zero-degrees phase shift, although this is a good design goal. In addition, the maximum phase slope should occur at the phase zero crossing. For example, if the entire phase response in Figure 2-2 is shifted down a division, the zero crossing occurs at a lower frequency and the phase slope is less steep. That

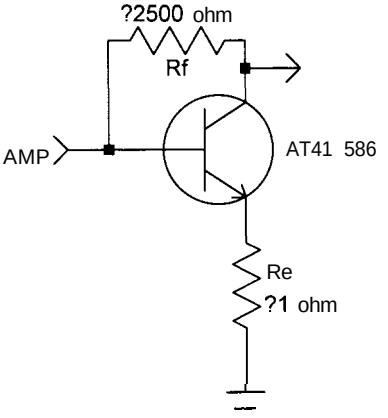

Figure 2-18 *Common-emitter bipolar amplifier with series resistive feedback (R_e) and shunt feedback (R_f).*

reduces the long-term stability (drift) and short-term stability (noise) performance of the oscillator.

One of the more important tools for controlling phase is resonator selection. Previously we discussed how the four element L-C resonators are used to obtain an arbitrary phase shift at resonance. For fixed frequency and narrow tuning VCOs this is often the only phase control required. However, the cascade transmission phase of a VCO which tunes over a broad bandwidth may change with frequency This is caused by active device transmission phase variation with frequency and by changes in the resonator characteristics with frequency

The 180^o low-frequency transmission phase shift of common-emitter bipolar amplifiers decreases with increasing frequency This variation is troublesome when designing high-frequency oscillators. For octave bandwidth VCO above several hundred megahertz the problem may become so severe that we abandon open-loop cascade oscillator design in favor of one-port negative-resistance oscillator design. More about this later.

First we'll discuss methods of improving the phase characteristics of amplifiers. The schematic of a common-emitter AT41586 bipolar amplifier with resistive series (R_e) and shunt (R_f) feedback is given in Figure 2-18. For simplicity, bias components are absent. The resistive values shown introduce little feedback and the circuit characteristics are defined by the device S-parameters. The transmission gain and phase are given in Figure 2-19.

The transmission gain (left grid) and phase (right grid) for the amplifier shown in Figure 2-18 are given in Figure 2-19. The solid traces are with small R_e and large R_f which is little feedback. At low frequencies the open loop gain exceeds 24 dB and the phase shift is near 180^o. At higher frequencies the gain and phase shift drop off significantly For this AT41586 the phase shift has dropped to 90^o by 1 GHz.

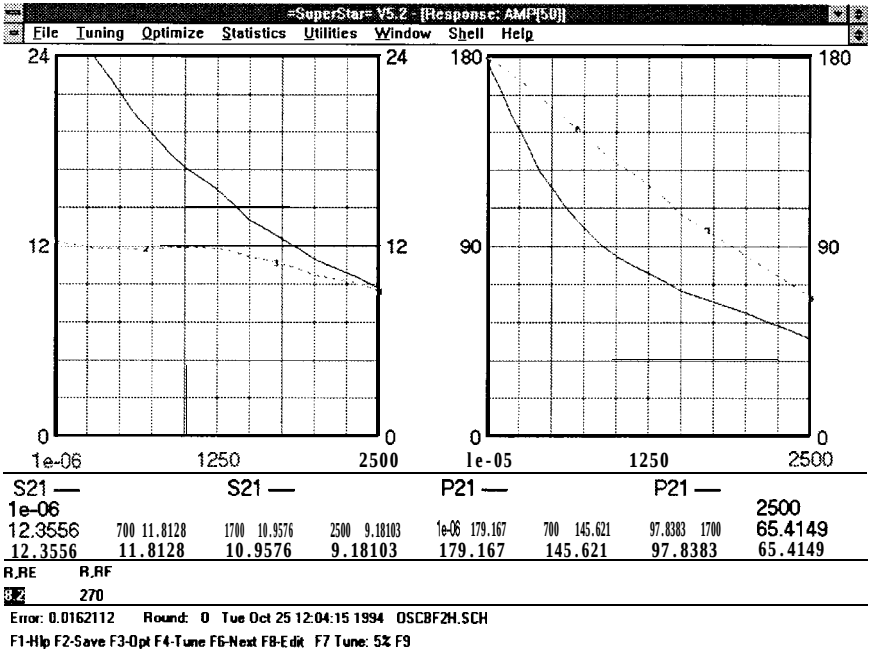

Figure 2-19 *Transmission gain (left) and phase (right) of a simple common-emitter bipolar amplifier without feedback (solid) and with feedback (dashed).*

The dashed responses in Figure 2-19 are with R_e increased to 8.2 ohms and R_f decreased to 270 ohms. This negative feedback limits the low frequency gain to approximately 12 dB and therefore flattens the gain response with frequency The reduced low frequency gain reduces the likelihood of spurious oscillations. The feedback also provides a more ideal phase response with less phase roll-off. The phase shift is held within 90^o up to nearly 2 GHz.

Higher-frequency transistors inherently have phase shifts closer to 180^o through higher frequencies. These devices also work well with feedback because their higher gain. MMICs, such as the Avantek MSA0235, push the 140^o phase shift to over 800 MHz. Eventually, the cause is lost and other techniques are required. For example, a phase shift network or short transmission line may be added to the active amplifier and a zero-degree phase resonator is used. Caution is advised when adding delay to reach a zero- degree phase shift. It is possible to create a cascade with more than one phase zero crossing. As long as the gain is less than 0 dB for the undesired phase zero crossings, there should be no problem. Otherwise, the network may oscillate at an undesired frequency

2.18 Negative Resistance Analysis

Thus far our analysis of oscillators has been based on the open-loop Bode response. A second method of analysis is based on modeling the oscillator as a one-port with a negative resistance. When a simple series or parallel resonator is connected to this port, the oscillation level builds until limiting reduces the net resistance to zero ohms.

The negative resistance analysis method is useful at microwave frequencies where the phase shift of an amplifier/resonator cascade becomes difficult to manage. The negative resistance method is useful for the analysis of grounded-collector tuned-base and grounded-base tuned emitter VCOs which are popular in UHF and microwave applications [10].

Although the negative resistance analysis characterizes the conditions leading to oscillation and predicts the oscillation frequency accurately, the author's experience is that relating the results of the analysis to the noise performance of the oscillator is unreliable. This is a controversial position to take because of the existence of a paper by K. Kurokawa which contains a rigorous analysis of the noise performance of the negative resistance oscillator [11] . An article by S. Hamilton [12] is also an excellent reference on negative resistance oscillators and noise performance. We will return to this subject later.

Consider the simple model in Figure 2-20 of a negative resistance oscillator. The right portion of the model, consisting of the negative resistance and the series capacitance, represents the active device. A typical active device circuit which can develop negative resistance, R_n, is given shortly The effective reactance can be positive or negative and in series or parallel with the negative resistance. The reactance is typically series capacitance for bipolar grounded-collector tuned-base oscillators and parallel inductance for bipolar grounded-base tuned-emitter oscillators.

The added external series-resonator consists of L_{ext} and C_{ext}. R_{ext} is the loss resistance resulting from the finite resonator Q. The simplest form of this oscillator is constructed by eliminating C_{ext} and choosing L_{ext} to resonate with C_{eff} at the desired operating frequency This is the lowest loaded Q configuration. In the

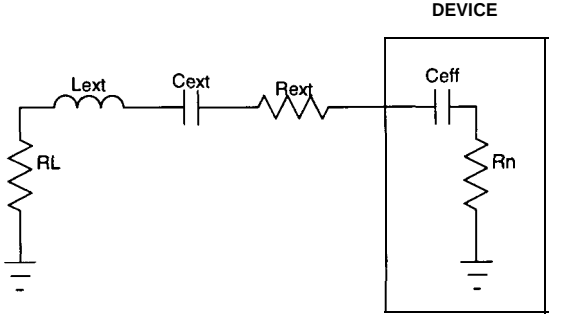

Figure 2-20 Negative resistance oscillator model.

popular VCO, C_{ext} is the tuning varactor. R_l in the model is the external load into which the output power is fed.

When power is applied to the circuit, the negative resistance developed by the active device overcomes the output loading and resonator loss resistance, $R_l + R_{ext}$. **The** signal level builds until nonlinearities in the active device reduce the negative resistance to exactly balance the total loss resistance.

The schematic of a simple bipolar negative resistance oscillator is given in Figure 2-21. R_{b1}, R_{b2} and R_e are bias resistors. The addition of an emitter capacitor, C_e, increases the negative resistance and increases C_{eff}, both of which are beneficial. C_e plays a critical role in the performance of the common-collector negative-resistance oscillator.

For the final analysis procedure we look into the transistor base through the resonator. To form the oscillator the left side of L_e is typically grounded. A 50 ohm load resistor may be connected in series with L_B provided the transistor negative resistance exceeds 50 ohms. The characteristic impedance of the analysis is

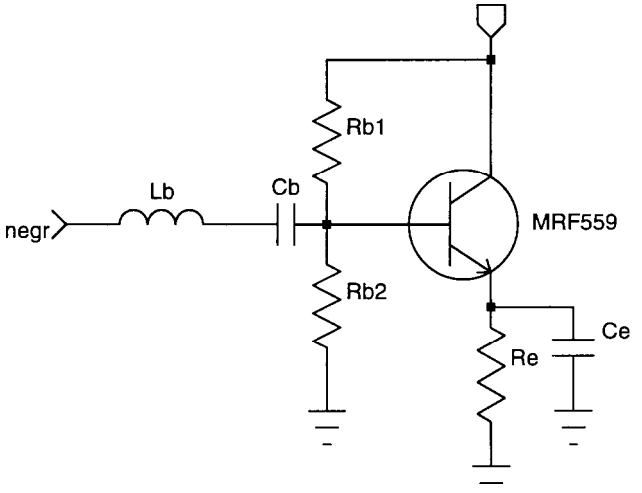

Figure 2-21 Simple series mode negative resistance oscillator.

the oscillator load resistance, R_l. It is common practice to take output power by tapping the resonator inductor, ***Lb.*** This reduces the loading. If the magnitude of the negative resistance developed by the transistor is greater than 50 ohms plus the resonator finite-Q loss resistance, the load could be connected directly in series with the resonator. This is very heavy loading and is seldom used except in the case of power oscillators.

The feedback in this circuit which develops the negative resistance is internal to the bipolar transistor. Microwave transistors have low internal junction capacities and may not work as well as lower-frequency or power transistors. When the internal junction capacities are considered, this circuit resembles a common-collector Clapp oscillator.

When looking into the base of the transistor through the external resonator, a net negative resistance results in an input reflection coefficient magnitude greater than 1. The frequency of oscillation is where the net reactance of ***Lb,*** C_b, and C_{eff} is zero. This results in an angle of the input reflection coefficient of zero or 180^o.

The oscillation frequency is determined by looking into the transistor through the resonator. However, characterization of the active portion of the oscillator without the resonator is an important step in the design. This is done by looking directly into the base without the resonator. The input reflection coefficient magnitude and phase for a common-collector MRF559 bipolar transistor are given in columns 2 and 3 of Table 2-1. A characteristic impedance of 50 ohms is used. An external emitter capacitance of 1.5 pF and emitter resistance of 180 ohms are added to ground. The transistor is biased at 10 volts and 25 mA. The reflection coefficients and input resistance and reactance were found using the =SuperStar= circuit simulation program.

Columns 4 and 5 contain the negative resistance and reactance, which are related to the complex reflection coefficient by

$$Z_n = Z_o \frac{1 + C_{11}}{1 - C_{11}} \qquad 2.64$$

where

Table 2-1 *Negative resistance parameters of a common-collector MRF559 bipolar transistor with 1.5-pF emitter capacitance and 180 emitter resistance*

Freq	C_{11}	Angle(deg)	$R_n(\Omega)$	$X_{eff}(\Omega)$	C_{eff}(pF)
300	1.020	-20.2	-15.9	-280.2	1.89
525	1.121	-32.6	-35.0	-164.2	1.85
750	1.247	-44.6	-35.6	-112.4	1.89
975	1.411	-66.6	-26.5	-69.2	2.36
1200	1.565	-86.2	-22.3	-48.1	2.76

$$Z_n = R_n + jX_{\text{eff}} \qquad 2.65$$

The effective series capacitance in column 6 was computed from the reactance, X_{eff}. The fact that C_{eff} is nearly constant over most of the frequency range when a series model is assumed suggests that the assumption of a series model is correct. If the transistor were better modeled as a parallel configuration, the computed parallel capacitance would be nearly constant with frequency The series transistor model justifies the use of a series resonator to complete the oscillator design.

If a different reference impedance were chosen for the analysis, C_{11} would have a different value. However, R_n and C_{eff} would compute to the same values. This is a necessary result. How could the measurement impedance looking into the base affect the actual values of the physical circuit? An important variation on this circuit is the use of a transmission line in place of L_e. In this case, the analysis is easier to interpret when the analysis impedance is much less than the transmission line impedance.

Knowledge of the value of C_{eff} is important. The oscillation frequency is the resonant frequency of L_e and C_e in series with C_{eff}. If the capacitance C_e is chosen larger than C_{eff}, the net capacitance is due largely to C_{eff}, and C_e has little effect. The unsuspecting designer wonders why the tuning range is less and operating frequency is higher than expected.

The value of C_{eff} is generally determined once for each transistor type and it is unnecessary to compute R_n and C_{eff} from C_{11} each time an oscillator is designed. The analysis is done by looking through the resonator and making certain that C_{11} is sufficiently greater than unity across the tuning range to allow for device and temperature variations.

A critical parameter which strongly effects both C_{eff} and R_n is the added emitter capacitance C_e. The effect of this parameter is studied next.

2.19 Emitter Capacitance in Negative-R Oscillators

Bipolar common-collector negative resistance oscillator performance is enhanced by the addition of capacitance to ground at the emitter. This is particularly important when high gain-frequency bandwidth devices are used and when operating at lower frequencies. The data for the MRF559 transistor given in Table 2-1 includes 1.5 pF of added emitter capacitance.

The first step when designing the common-collector negative resistance oscillator is to examine R_n and X_{eff} (from which C_{eff} can be found) versus C_e. This is done by looking into the base without the resonator present and tuning C_e. Figure 2-22 is a 3-D plot of the R_n versus frequency (from the center to the right) and versus values of C_e (from the center towards the back).

Notice at the lowest frequency (left edge of the surface) that increasing capacitance to 10 pF results in increased negative resistance. At the highest frequency, the negative resistance reaches a maximum magnitude when C_e is approximately 6 pF. From this we conclude the optimum value of C_e increases with decreasing frequency

Shown in Figure 2-23 is a plot of the input reactance, X_{in}, as a function of frequency and emitter capacitance. Notice the front right edge of the surface (constant 10 pF for C_e) tends to smaller capacitive reactance with increasing frequency. This results naturally since the reactance of a capacitor decreases with increasing frequency.

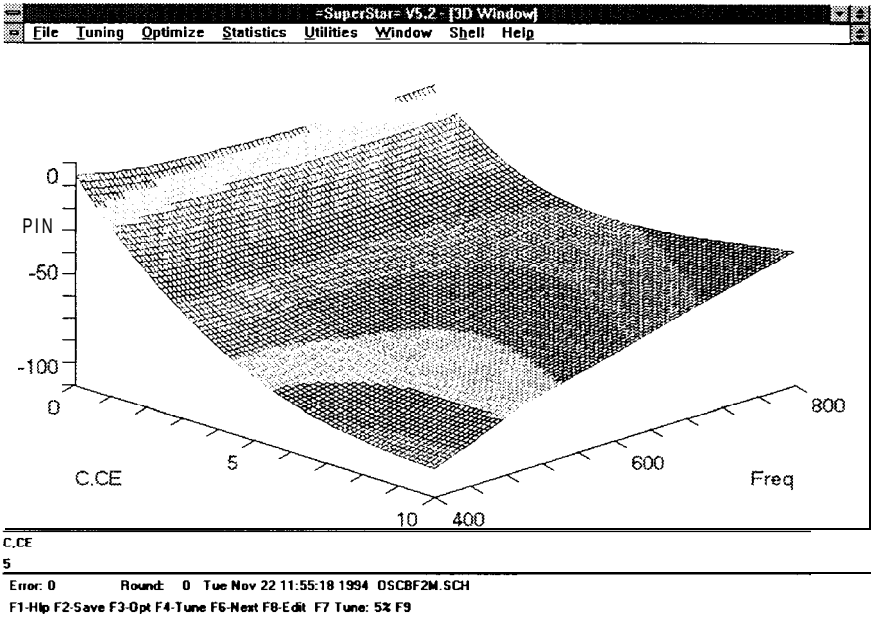

Figure 2-22 3-D *plot of* R_n *versus frequency (to the right) and* C_e *(to the back).*

Also notice at all points along the frequency axis that increasing C_e decreases the magnitude of the capacitive reactance. Lower capacitive reactance corresponds to larger values of capacitance. Therefore larger values of C_e result in larger C_{eff}. This is desirable because for a given resonator larger C_{eff} tends to isolate the active device from oscillator performance and increases the tuning range.

From Figure 2-23 we conclude we should use the largest value of C_e consistent with developing adequate negative resistance. Higher gain-bandwidth transistors have less internal junction capacitance and often require larger values of C_e to keep C_{eff} from being troublingly small, particularly at operating frequencies below 10% of the device F_t. Aggressive use of high C_e is complicated by inductance present in the capacitance to ground.

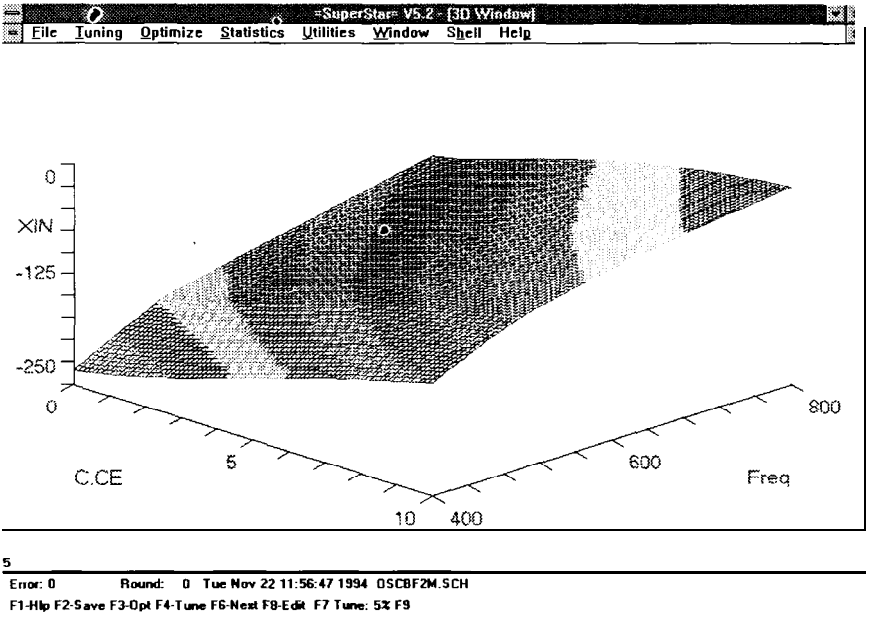

Figure 2-23 3-D plot of R_n versus frequency (to the right) and C_e (to the back).

Just as C_e plays a critical role in the design of common-collector negative resistance oscillators, inductance in series with the base of the common-base negative resistance oscillator is critical. The first step in the design of these oscillators involves examining the reflection coefficient looking in the emitter while adjusting inductance from the base to ground. The reactance in series with the negative resistance is positive and therefore inductive. The fact that it is inductive helps avoid the limitation of the tuning range caused by C_{eff} in the common-collector configuration. However the author's experience is that the common-collector configuration is somewhat less tricky to design.

2.20 Looking Through the Resonator

As we have seen, the input impedance of the common-collector bipolar negative resistance oscillator consists of a series negative resistance and a capacitive input reactance. The first step in the design involved evaluating this input impedance with the device properly configured and added capacitance at the emitter.

The next step involves adding the resonator and again looking at the input impedance but now through this resonator. The external inductor in series with the external capacitance, Cext, and the effective internal capacitance, Ceff, form a series circuit which resonates at the oscillation frequency Looking through the resonator, the input impedance is resistive with a net reactance of zero. For oscillation to occur, a linear analysis must yield a negative real component of the impedance. As the oscillation level builds, device non linearities reduce the device negative resistance until its magnitude equals the positive resistance in the input series circuit loop.

A plot of the input resistance and reactance of an oscillator similar to that shown in Figure 2-21 is given in Figure 2-24. The flatter curve is the input resistance with a scale of -100 to 100 ohms (left vertical axis). For this particular oscillator the resistance ranges from -28 ohms at 500 MHz to -9 ohms at 1000 MHz. The input reactance is given as the curves with greater slope. The scale on the left is -250 to 250 ohms. The solid trace to the right is with a series external capacitance of 1 pF and the dashed curve on the left is with this capacitor tuned to 6 pF. With 1 pF external capacitance the reactance is zero and the oscillation frequency is at 940 MHz, marker #3. With 6 pF external capacitance the oscillation frequency is 570 MHz, marker #2. For the analysis the inductor is specified with an unloaded Q of 90. The loss resistance associated with this finite Q is included in the analysis and the net negative resistance is -28 ohms at 570 MHz and -12 ohms at 940 MHz.

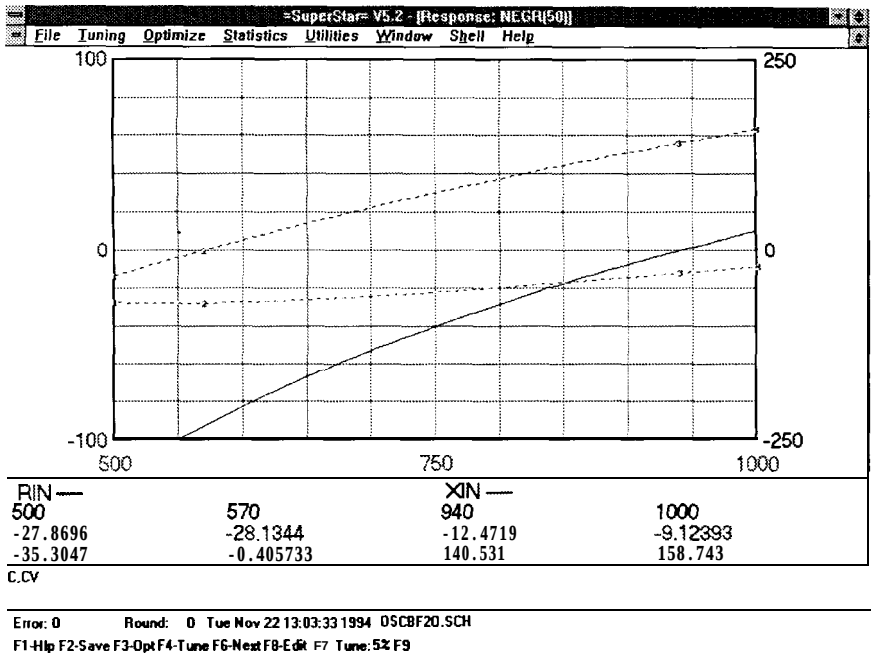

Figure 2-24 *Plot of the input resistance (flatter curve) and reactance (sloped curve) of a negative resistance oscillator looking through the resonator.*

2.21 Negative Resistance Oscillator Noise

In the Hamilton reference, the negative resistance oscillator minimum loaded Q is defined without C_{ext} and C_{eff} resonates with L_{ext} at the operating frequency The minimum value of L_{ext} is referred to as *L. The* minimum loaded Q, Q_d, is

$$Q_d = \frac{1}{2\pi f C_{eff} \mid R_n \mid} \qquad \textbf{2.66}$$

For the MRF559 circuit depicted in Table 2-1, Q_d at 750 MHz is approximately 3.2.

When C_{ext} is reduced, and L_{ext} is therefore increased, the loaded Q is improved. The loaded Q is

$$Q_l = \frac{2\pi f L_{ext}}{R_l} \qquad 2.67$$

The equation given by Hamilton is in a different form, based on the ratio of L_e to L, but is essentially equivalent. Hamilton refers to the loaded Q as Q_{ext}.

The problem here is that as the circuit is lightly loaded, R_l approaches zero, the loaded Q approaches infinity, and the circuit becomes free of noise. This is clearly a dilemma. The astute reader observes that the resonator loss resistance is missing from Hamilton's expression, and that if it were included, the lightly loaded Q approaches the unloaded Q of the resonator.

Because this resonator is a one-port the coupling techniques used to construct high-Q two-port transmission resonators are difficult to apply Increasing the loaded Q of this series resonator involves increasing L_{ext} and decreasing C_{ext}. Ultimately unrealizable values are required. At UHF and higher frequencies it is difficult to realize loaded Qs higher than about 5. In any case, negative resistance oscillators are not recommended when noise performance is the limiting factor. This may not be a severe limitation for broadband VCO design because varactor modulation noise, as discussed in a subsequent chapter, generally limits the noise performance of these oscillators. It has been observed that an impedance transformation, by using a transformer between the resonator and the transistor base, improves the loaded Q.

2.22 Negative Conductance Oscillators

The common collector negative resistance oscillator model introduced in Section 2.18 operates in a series resonant mode. The device small signal input port reflection coefficient may be plotted on an impedance Smith chart with a negative normalizing resistance. If the reflection coefficient is measured with increasing incident signal level the device becomes non-linear and the

reflection coefficient begins to change. When the device behaves in an ideal series resonant mode as the incident signal level increases the magnitude of the negative resistance decreases but the reactance does not change. The locus of plotted reflection coefficient data with increasing incident signal level moves along constant reactance arcs on the Smith chart. This configuration is referred to as open circuit stable because if the device port is left open the circuit does not oscillate.

Consider the simple oscillator schematic in Figure 2-25 which utilizes a common base bipolar configuration. The resonator consists of L_e and C_e connected to the emitter. The common collector configuration given in Figure 2-21 uses emitter capaci-

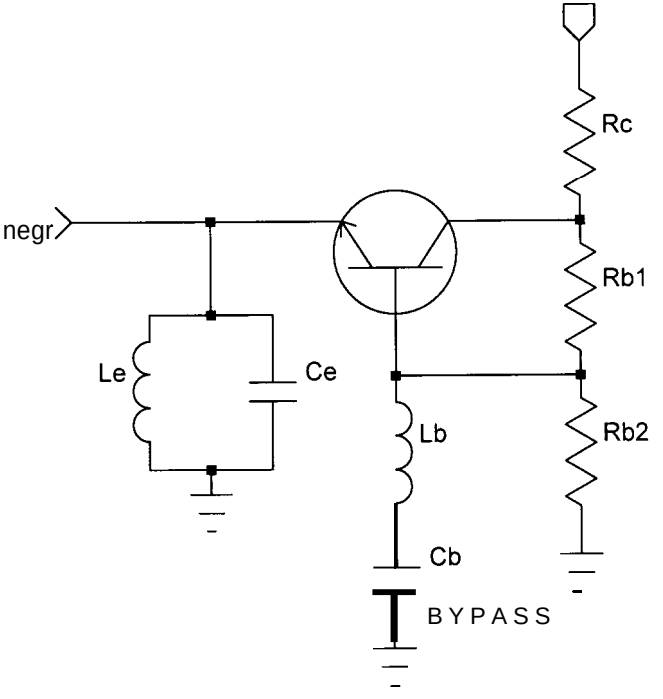

Figure 2-25 *Simple parallel resonant mode negative resistance (conductance) oscillator.*

tance to control the negative resistance developed at the base. The inductor L_b in the base of the circuit in Figure 2-25 serves a similar function for the common base configuration. Capacitor C_b is a bypass capacitor.

When the reflection coefficient of this configuration is observed versus increasing incident signal level the locus of points moves along constant susceptance arcs on an admittance Smith chart normalized with a negative conductance. Given in Figure 2-26 are common base emitter input characteristics of a microwave bipolar transistor at 1.6 GHz and 2.6 GHz plotted on an imped-

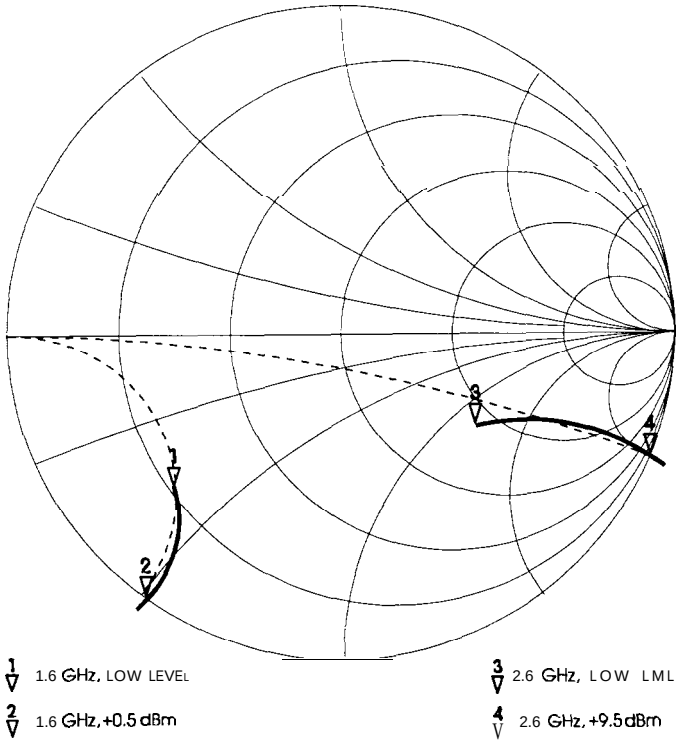

Figure 2-26 *Reflection coefficient at the emitter of a common base negative conductance oscillator with increasing incident signal level. (Courtesy of Larry McKinney of Scientific-Atlanta).*

ance Smith chart with a normalized resistance of -50 ohms. No external inductance is added and the base inductance is only ground path inductance. The dashed lines are arcs of constant susceptance lifted from an admittance Smith chart.

Marker number 1 is at 1.6 GHz at low incident input level. Marker number 2 is with the incident signal level at +0.5 dBm. At this level the device has become sufficiently non-linear that the negative conductance is zero mhos. Because the locus of points lies nearly on a constant susceptance arc the frequency suffers only limited shift as the oscillation level builds to a final steady state level. Marker number 3 is at 2.6 GHz and low incident input level. The negative conductance is zero mhos at marker number 4 with an incident signal level of +9.5 dBm.

Since the locus of points follow very nearly arcs of constant susceptance the operating mode is parallel resonant. This configuration is short circuit stable and oscillation does not occur with a short on the emitter.

Given on the left in Figure 2-27 is the input reflection coefficient of a common base negative conductance oscillator plotted on an impedance Smith chart with a normalizing resistance of -50 ohms. The circuit configuration is similar to Figure 2-25 where the refection coefficient is measured across a parallel resonant circuit on the emitter. On the right is the same reflection coefficient plotted on a polar chart with a circumference of 2 and normalized with +50 ohms. Marker number 1 is at 500 MHz. Resonance and oscillation occur at marker 2 at 710 MHz. The input reflection coefficient crosses the circumference of the Smith chart and the unity circle on the polar chart by marker number 3 at 860 MHz.

Careful examination of Figure 2-25 reveals a potential problem. The oscillator resonator at the emitter is capacitive above the desired resonant frequency At these frequencies the circuit behaves like the negative resistance oscillator shown in Figure 2-21 and develops negative resistance at the base. The inductor L_b (which assists in developing negative conductance at the emitter) then series resonates with the base bypass capacitor forming a

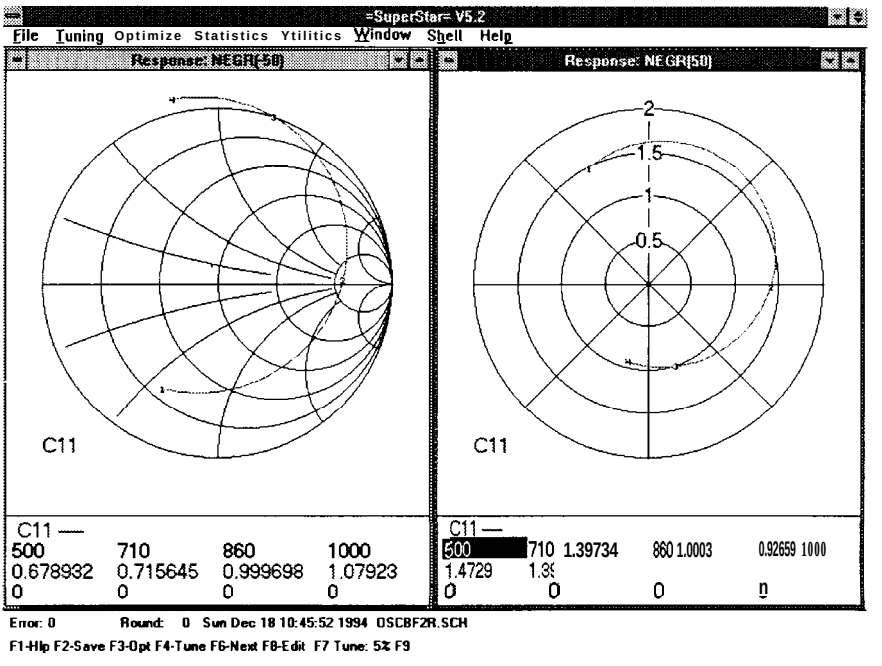

Figure 2-27 *Input reflection coefficient of a common base negative conductance oscillator configuration plotted on an impedance Smith chart normalized to -50 ohms (left) and on a polar chart with radius greater than unity and normalized with +50 ohms.*

second oscillation mode. Therefore the bypass capacitor must be carefully selected to insure that the base series resonant frequency occurs at a frequency where there is no negative resistance at the base, otherwise severe spurious modes will exist.

This completes the discussion in this chapter of topics specific to negative resistance and conductance oscillator design. Additional examples of these oscillators are given in Chapter 9.

2.23 Stability Factor and Oscillator Design

The objective of negative resistance oscillator design is to develop negative resistance at the port of an active device. When a passive resonator, such as a series L-C circuit, is placed at the port the net loop resistance is less than zero and oscillation builds. From the viewpoint of amplifier design, negative resistance at an amplifier port signifies the circuit is unstable. A passive load with a positive resistance can result in oscillation. Therefore oscillation based on a reflection coefficient greater than unity is related to amplifier instability

However, it is important to recognize that the previous method of oscillator design which utilizes an amplifier resonator cascade relies on a stable amplifier section. Oscillation is induced when the output is connected to the input. If the open loop amplifier is unstable at one or both ports the phenomena controlling the oscillation frequency and other characteristics is uncertain. Therefore, the amplifier should be designed with the same care used to insure that any amplifier is stable. Stable bipolar amplifiers can be built in common emitter, common collector or common base configuration. However, the common emitter form is generally more stable and is preferred unless a specific reason suggests otherwise. The poorer stability of the common-base and common-collector forms is why they work well as "unstable" negative resistance oscillators.

The importance of stability considerations in amplifier resonator cascade oscillators is illustrated by the schematic of a proposed tuned emitter amplifier resonator cascade in Figure 2-28. Biasing and decoupling elements are eliminated for simplicity The common-emitter amplifier with resistive series (27 ohm) and shunt (270 ohm) feedback has 180^{o} transmission phase shift and the transformer inserts an additional 180^{o} phase shift. The L-C network at the emitter is an effective bypass at the series resonant frequency with a resultant gain peak and phase zero crossing. The effective resistance presented to the series resonator is low and the loaded Q of the cascade is high. This is the basis of the high-performance Driscoll oscillator studied in Chapter 11 where a quartz crystal is used as the series resonator.

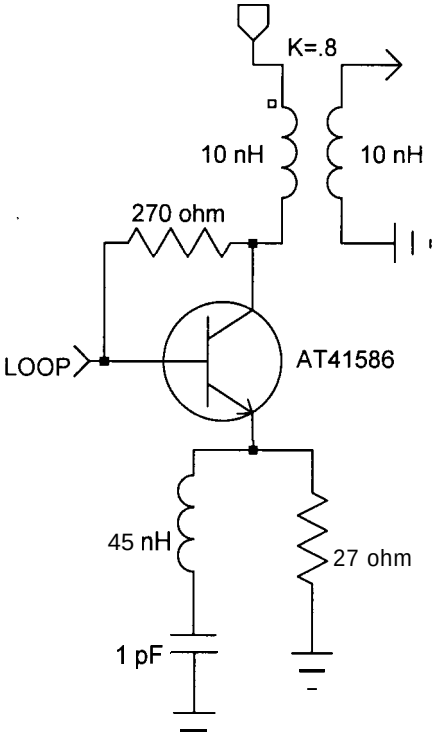

Figure 2-28 *Tuned emitter amplifier resonator cascade for a proposed oscillator.*

However, notice that below resonance the net reactance of the series L-C is capacitive which results in a negative resistance at the input of the cascade. Extreme care must be exercised to insure that the transformer and biasing components do not offer the opportunity for instability at the device base or collector.

2.24 Output Coupling

Thus far, the oscillator has been studied ignoring loading effects. The oscillator is formed by connecting the cascade output back to

the input or by grounding the port where the reflection coefficient was viewed. The question arises: How is output taken from the oscillator? A number of techniques are available.

An obvious and analytically rigorous method is to insert a directional coupler or power splitter in the closed loop. For greatest output power, a low coupling value can be used. For loops with a high gain margin, the coupled arm can be used to close the loop, and the majority of power is delivered to the load.

Directional couplers are generally more complex than is required to couple energy from the oscillator. A more economical method is to couple power by connecting a capacitor or inductor from an appropriate point in the circuit to the load. The Bode response analysis is modified to include the coupling element and the load. The degree of coupling is controlled by the reactance of the coupling element. When the coupling element and load are added to the analysis, the effects of output coupling on the gain margin is naturally included.

Consider the simple series reactor and load network on the left in Figure 2-29. This network represents the coupling element and the load. For small values of coupling reactance (a large capacitor or a small inductor), the reactance has little effect and the load is effectively connected directly to the circuit. This is referred to as tight coupling. For high-impedance loads, such as a buffer amplifier, this works well. For a 50 ohm load, the loading may reduce the gain margin, perhaps even below unity gain. This tight coupling also causes oscillator performance parameters to be heavily dependent on load characteristics and changes.

On the right in Figure 2-29, the effective parallel resistance, R_p, and reactance, X_p, which load the cascade are shown. Increasing the coupling reactance, X_s, reduces the resistive loading on the cascade by increasing R_p. The parallel and series values are related by

$$R_p = \frac{R_s^2 + X_s^2}{R_s} \qquad 2.68$$

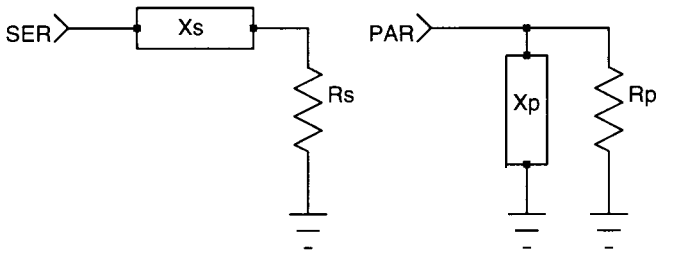

Figure 2-29 Series-to-parallel network conversion valid for a given frequency.

$$X_p = \frac{R_s^2 + X_s^2}{X_s} \qquad 2.69$$

and

$$R_s = \frac{X_p^2 R_p}{R_p^2 + X_p^2} \qquad 2.70$$

$$X_s = \frac{R_p^2 X_p}{R_p^2 + X_p^2} \qquad 2.71$$

The coupling reactances in the equations above may be inductive or capacitive. A series coupling reactance equal to the load resistance results in a parallel load resistance of twice the load resistance. A coupling reactance of three times the load resistance results in a parallel load resistance of 10 times the load resistance.

The degree of loading on the cascade by the coupling network is dependent on the impedance level at the coupled location. For example, an effective 500 ohm load at a circuit location with an impedance level of 50 ohms has a minimal effect on the gain margin or loaded Q. On the other hand, the same load across the resonator, where the impedance level is high, may have a considerable effect.

Power may be extracted from any point in the oscillator. In general, higher power levels but poorer harmonic performance is achieved when energy is coupled at the collector of bipolar oscillators. Lower output levels with excellent harmonic performance are available by light coupling directly from the resonator. These issues are further illustrated in Chapter 3, Limiting and Starting.

2.25 Pulling

The impedance of the load coupled to the oscillator effects the output level and oscillation frequency Variation of the output frequency with load changes is referred to as pulling. Pulling can be examined directly by computer simulation or direct measurement by varying the load impedance while observing the cascade phase response, the reflection coefficient or the actual oscillation frequency

Load variations in a given system typically depend on tolerances and extreme changes are avoidable. Pulling is typically specified for a load with a given return loss magnitude at any angle. A return loss magnitude of 12 dB (VSWR=1.671) is commonly used to define a pulling specification.

In a 50 ohm system a 12 dB return loss corresponds to complex impedances of 29.9, 44.1 - j23.6, 83.5, and 44.1 + j23.6 ohms at return loss angles of $-180^o, -90^o, 0^o$ and 90^o degrees respectively This range of impedances is achieved by rotating a 29.9 or 83.5 ohm termination through a variable length of 50 ohm transmission line.

This technique is illustrated in Figure 2-30. The input resistance and reactance are plotted for a negative resistance oscillator similar to that in Figure 2-21. A 29.9 ohm load resistor terminates a 50 ohm transmission line which is 25 wavelengths long at 750 MHz. This 12 dB return loss (referenced to 50 ohms) is coupled to the oscillator emitter through a 1 pF coupling capacitor (solid traces) and a 6.8 pF coupling capacitor (dashed traces). The peridicity of the traces illustrates the effect of the varying return

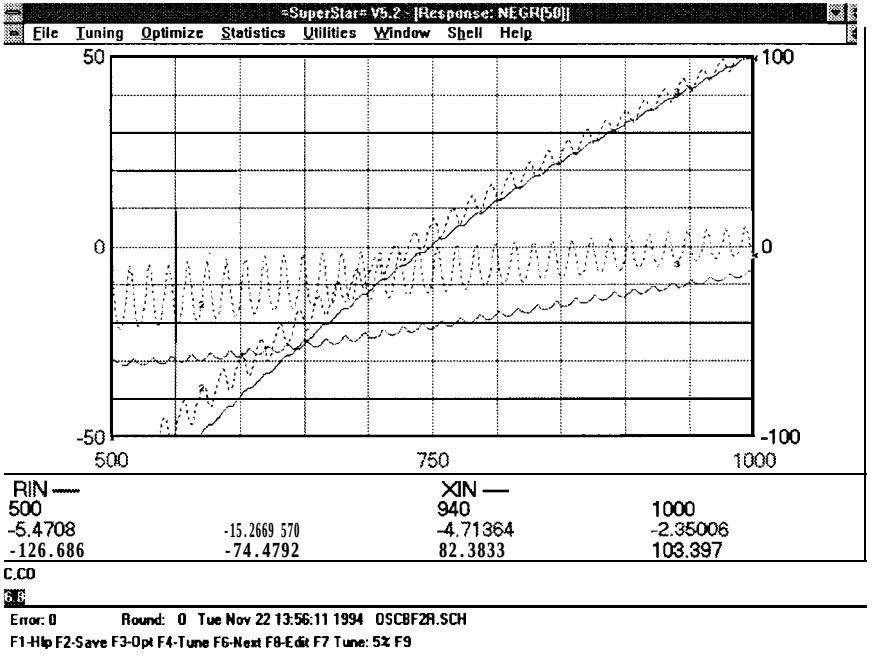

Figure 2-30 *Load pulling effects on the input resistance of a negative resistance oscillator with light coupling (solid) and heavy coupling (dashed).*

loss phase which rotates versus frequency for the long length of transmission line.

The 1 pF capacitor at the emitter is light coupling. The negative resistance and input reactance are only slightly perturbed. When this load is coupled to the oscillator emitter through a 6.8 pF capacitance the coupling is tight. At higher frequencies the resistance is not negative at some load phases. Oscillation could not occur with these load conditions. The tight coupling case also reveals significant frequency pulling with load variation.

2.26 Pushing

Ideally, the oscillation frequency and amplitude are independent of the supply voltages. Supply voltages generally drift with time, temperature, and load variations. In addition, noise on the supply lines causes significant FM and AM modulation to an oscillator which is unduly affected by the supply voltage. Pushing is measured simply by manual adjustment of the supply voltage and observing the resulting frequency and amplitude variation. For example, a measured frequency sensitivity to supply voltage might be 10 kHz/volt. A supply voltage ripple of 0.5 mV peak at 120 Hz would then result in a peak phase deviation of

$$\theta_p = 2\sim 10{,}000\ \frac{0.5\text{x}10^{-3}}{120} = 0.262 \text{ rad} \qquad 2.72$$

This results in a modulation level for the 120-Hz sidebands of

$$L(f_m) = 20 \log \frac{0.262}{2} = -17.7 \text{ dBc} \qquad 2.73$$

Filtering the supply voltage reduces this problem, but a more ideal solution is an oscillator design with higher loaded Q. Higher loaded Q isolates the resonant circuit from active-device junction capacitance variation due to supply changes. The total reactance loading the resonator is often a function of several different parameters of a device. Therefore, some oscillator designs, or certain operating voltages for a given design, may have a low-frequency sensitivity to the supply voltage. It is good practice to adjust the supply voltage of the design prototype manually and observe what happens to the oscillation frequency and amplitude.

2.27 References

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3

Limiting and Starting

Thus far, oscillator design has been considered assuming linear operation of the active device. Many aspects of oscillator performance are predicted by these linear design considerations. In this chapter the nonlinear aspects of the design are considered. This allows prediction of most remaining oscillator performance parameters.

3.1 Limiting

Assuming that oscillation criteria is satisfied, an oscillator is formed by connecting the output of the resonator-amplifier cascade to the input. Oscillations then build up until the excess loop gain is lost because of limiting in the active device. Limiting occurs when the transistor is driven into saturation and/or cutoff during a portion of the waveform cycle. If the excess loop gain is small, the required limiting is slight, waveforms are nearly sinusoidal, and nearly-class-A operation conditions exist. The linear design considerations and parameters have the greatest validity in this situation. If the excess loop gain is large, and AGC or other form of external limiting is not applied, the active device may remain saturated or cut off over a significant portion of the waveform period. This results in class-C operation conditions. This is normally undesirable, except in the design of high-efficiency, high-output power oscillators.

3.2 Amplitude and Frequency Stability

For near-class-A operation, if limiting is due to cutoff, the oscillation amplitude is proportional to the emitter bias current. If limiting is due to saturation, the amplitude is proportional to the quiescent dc collector-emitter voltage [l]. These parameters may be established with nearly any desired degree of stability by the selection of bias network type and complexity Because the output level and gain of the cascade amplifier are dependent on the supply voltage and bias conditions, changes in the supply voltage and temperature affect the output level. Otherwise, the steady-state output level is relatively constant.

In a well-designed near-class-A oscillator, the frequency is determined primarily by the resonator. As the loaded Q is increased, the active-device reactances become less significant in determining the oscillation frequency Changes in these parameters from device to device, with temperature and with supply voltage, have less effect. A simple test of how well the active-device reactances are isolated from the resonator is to observe the operating frequency as the supply voltage(s) is varied. Only small changes in the operating frequency should be observed.

The temperature characteristics of resonators are sometimes compensated by adding a component, usually a capacitor, with known temperature characteristics. The temperature characteristics of an L-C resonator alone are much simpler functions of temperature than the combined characteristics of the resonator-amplifier cascade. The prospects for successful frequency compensation of the temperature characteristics are therefore much better for high-Q, near-class-A oscillators.

Designers of class-C power amplifiers are aware of the fact that the large-signal two-port parameters of devices are significantly different from the small-signal two-port parameters. In Table 3-l the class-A (15 V and 80 mA) and class-C (13.6 V and P_o = 1 W) parallel input and output impedances for a 2N3948 at 300 MHz are given [2]. The significant shift of resonator loading caused by these parameter changes during class-C operation causes frequency pulling. High loaded Q reduces, but does not completely

Table 3-1 *Class-A and Class-C Transistor Parameters*

Parameter	Class-A	Class-C
Rin	*9* ohms	38 ohms
Xin	0.012 uH	21 pF
Rout	199 ohms	92 ohms
X out	4.6 pF	5.0 pF
Gf	12.4 dB	8.2 dB

eliminate, these effects. In the case of high-efficiency power oscillators, resonator losses must be kept low. This requires lower loaded Qs, which aggravates the problem. The resonator circulating current causes dissipation in the loss resistance of resonator components. The resulting component temperature rise may cause frequency drift as the oscillator warms up after turn-on. This problem is most significant with higher power levels and when frequency stability requirements are critical. For all these reasons, the designer of high-efficiency power oscillators should expect some shift in the oscillation frequency as predicted by analysis of the linear phase-zero-crossing frequency

The highly nonlinear conditions of oscillators with heavy limiting also cause the active device to act as a mixer. This may allow noise at baseband and harmonics of the carrier frequency to modulate the carrier and appear as noise sidebands around the carrier. The high-collector base voltage swing “pumps” the collector-base capacitance. This tends to create effective negative circuit resistance at harmonics of the fundamental oscillation frequency This phenomenon is used to advantage in parametric amplifiers but may increase the output level of harmonics in oscillators. If this problem is severe, the greatest output level may occur at a harmonic of the fundamental frequency

3.3 Class-A Operation

Except for the case of high-efficiency power oscillators, the design goal is therefore to ensure near-class-A operation. The simplest method of ensuring near-class-A operation is to design the resonator amplifier cascade with small excess loop gain. The problem

with this approach is ensuring that the loop gain does not fall below unity with temperature, device, loading, or other circuit changes. A second problem is that starting in an oscillator with low loop gain is slower.

A second solution is to apply AGC to the circuit. The output is sampled and a dc voltage proportional to the oscillator output level is developed. This dc voltage controls the bias of the loop amplifier, regulating the gain at the minimum value necessary for oscillation.

A third solution involves adding a second active stage with well-behaved limiting characteristics which is isolated from the resonator. For example, a differential amplifier acts as a limiter without saturating the transistors. Antiparallel diodes may be used in a similar fashion. Reference [3] contains an example of the latter for a two-transistor 20 MHz Pierce crystal oscillator.

The fourth solution involves applying feedback to the amplifier. This approach

(a) Uses a minimum of additional components

(b) Establishes a stable and flat gain versus frequency

(c) Improves amplifier linearity

(d) Reduces amplifier phase shift

(e) Reduces effects of device parameter variations

(f) Improves the amplifier input and output match

AGC and isolated limiting are good choices for more critical applications. The feedback approach, with its many desirable characteristics, makes it a good choice for cost-driven or less critical applications.

3.4 Near-Class-A Example

Shown in Figure 3-l is a block diagram for a 20 MHz oscillator. The amplifier is a Motorola MWA110 hybrid amplifier. The resonator is a series inductor-capacitor decoupled from the input

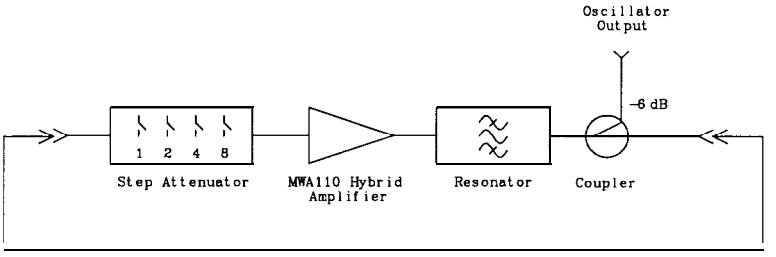

Figure 3-1 *Block diagram for a 20 MHz near-class-A oscillator example.*

and output via shunt 1000 pF capacitors, as shown in Figure 3-2. The lead inductance of 1000 pF capacitors would be significant at 20 MHz, so leadless capacitors were used.

The measured small-signal gain and phase shift through 200 MHz for the MWA110 amplifier with a 13.6-volt supply voltage and a 1000 ohm external decoupling resistor is given in Figure 3-3. The gain and phase shift at the desired operating frequency of 20 MHz is approximately 12 dB and 160^{o}. The measured insertion loss and phase shift of the resonator are given in Figure 3-4. The inductor was tuned until the phase shift of the resonator was 180^{o} at 20 MHz. Notice that the phase shift at resonance, as defined by the peak of the amplitude response, is approximately -165^{o}. The loaded Q is approximately 36. The insertion loss of

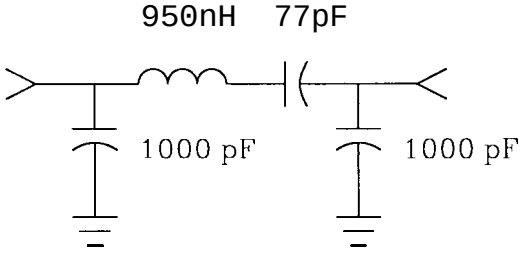

Figure 3-2 *Resonator used in the 20 MHz oscillator example.*

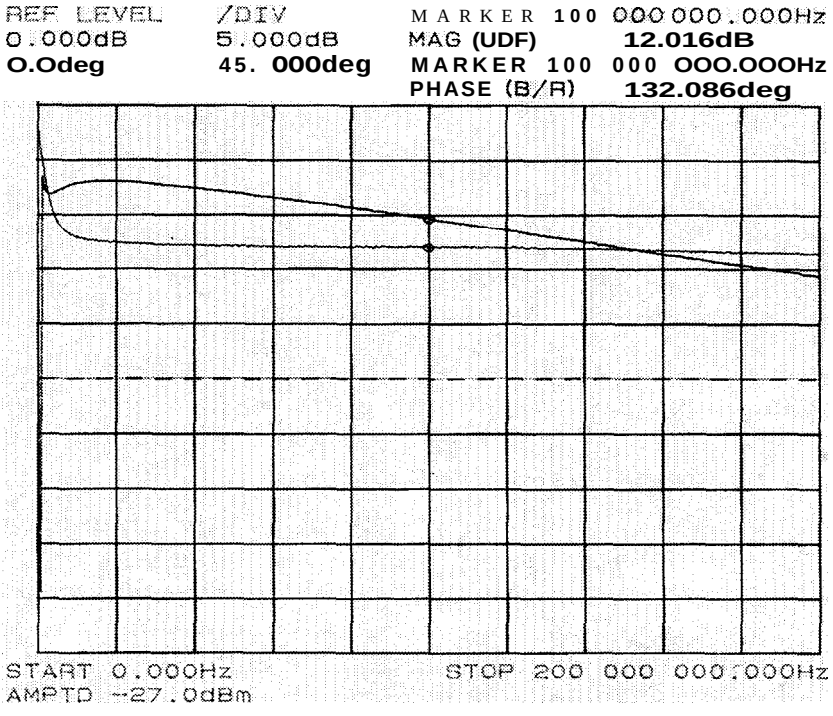

Figure 3-3 Measured gain and phase response through 200 MHz for the MWAllO amplifier used in the loop oscillator example.

2.7 dB at resonance is the result of a component unloaded Q of approximately 140.

The output is taken by a broadband ferrite 6 dB coupler. The coupled port has a measured loss relative to the input of 6.5 dB and a through-port loss of 1.5 dB with only a few degrees of phase shift at 20 MHz. A step attenuator is included within the cascade to test the effects of loop gain on oscillator behavior. The step attenuator is switchable from 0 though 15 dB of attenuation in 1 dB steps. The phase shift is only a few degrees. The open-loop gain and phase shift for the cascaded MWAllO and resonator is given in Figure 3-5. The open-loop gain peaks near 10 dB at 19.9

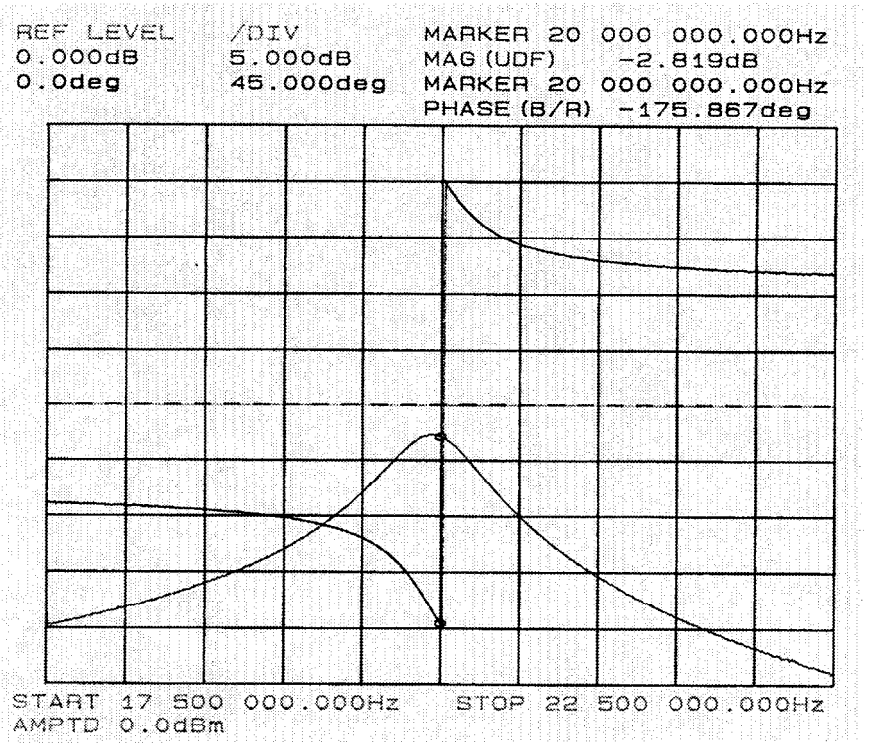

Figure 3-4 *Measured gain and phase response of the resonator used in the loop oscillator example. The resonator is terminated on the imput and output with 50 ohms.*

MHz just below the marker frequency The gain peak and maximum phase slope are nearly coincident in frequency, but zero-degree phase shift occurs somewhat lower at 19.85 MHz. The open-loop gain is approximately 9 dB at the phase zero crossing. Fifteen degrees less phase shift would be more optimum, but the phase slope at the phase zero crossing is not far below the maximum value.

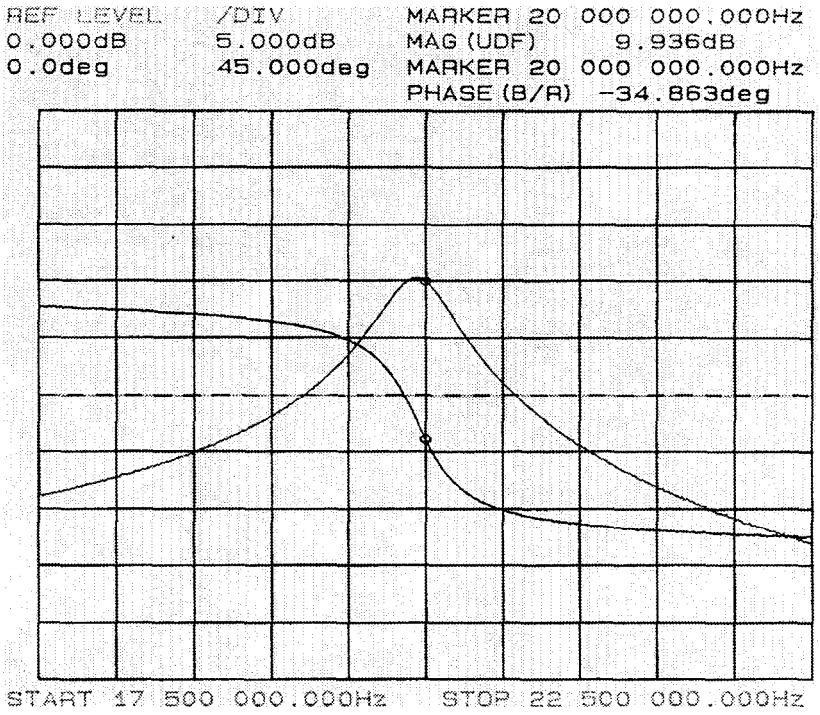

Figure 3-5 *Measured gain and phase response of the MWA110 and resonator cascade.*

3.5 Predicting Output Level

The limiting phenomenon in oscillators is similar to amplifier limiting. Amplifier output saturation is generally measured with a generator or matched amplifier driver. The "driver" in the oscillator case is often the oscillator tank, with reactances that are capable of high peak currents during nonlinear operation. However, the limiting characteristics of amplifiers and oscillators with small loop gain are similar enough to allow reasonably accurate prediction of oscillator output power by studying the output saturation characteristics of the open-loop resonator amplifier cascade.

Given in Figure 3-6 is the measured output power and gain versus input power for the MWA110 unit used in these tests. The MWA110 is a moderate-gain hybrid with a low output-level capability The manufacturer specifies the typical 1 dB gain compression level as -2.5 dBm [4]. *The* 1 dB gain compression of the measured unit, as determined from Figure 3-6, is 1 dBm, which is not unreasonably different from the typical specification. Somewhat disconcerting, however, is the fact that the gain at moderate signal levels is approximately 1 dB above the low-signal gain. This sometimes results from bias shifting caused by the input signal level and is generally undesirable in class-A amplifiers. The gain was measured using a network analyzer to avoid contributions to the output power from harmonics of the input frequency

Predicting the output level of the oscillator based on the open-loop gain margin and the amplifier saturation characteristics is dis-

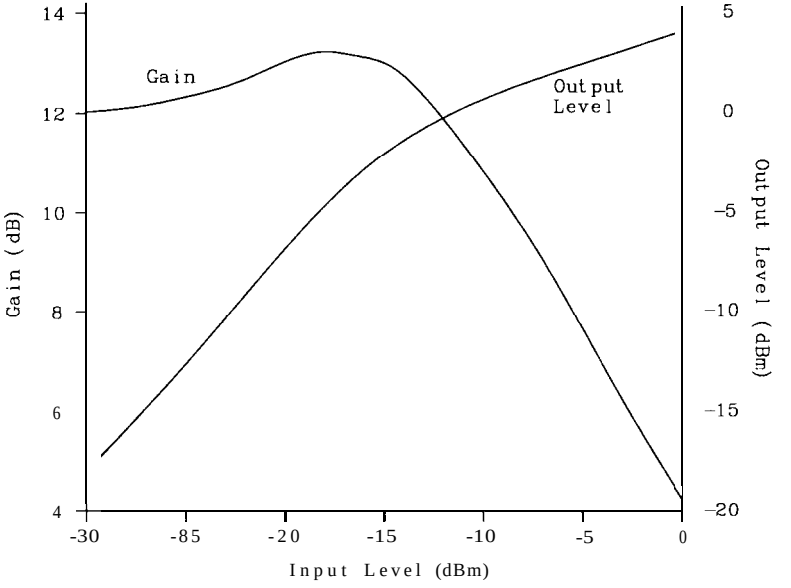

Figure 3-6 *Measured signal gain and output power vs. input power for the MWA110 amplifier.*

cussed next. The loop gain is adjusted with the step attenuator in the cascade, as shown in Figure 3-l. With the step attenuator set to 0 dB, recall that the loop gain is approximately 9 dB at the phase zero crossing minus 1.5 dB for the through-port loss of the directional coupler, or 7.5 dB. The cascade output is connected to the cascade input via a short coaxial jumper. The spectrum of the resulting oscillator taken at the coupler output with the step attenuator set to 1 dB is given in Figure 3-7. With 1 dB in the step attenuator, the loop gain is 6.5 dB. Therefore, approximately 6.5 dB of gain compression is needed in the amplifier. The output level of the MWA110 with 6.5 dB gain compression is approximately 3 dBm. The output is taken through the resonator and the coupler, which represents 9.2 dB of loss relative to the MWA110 output. The expected output level is then - 6.2 dBm.

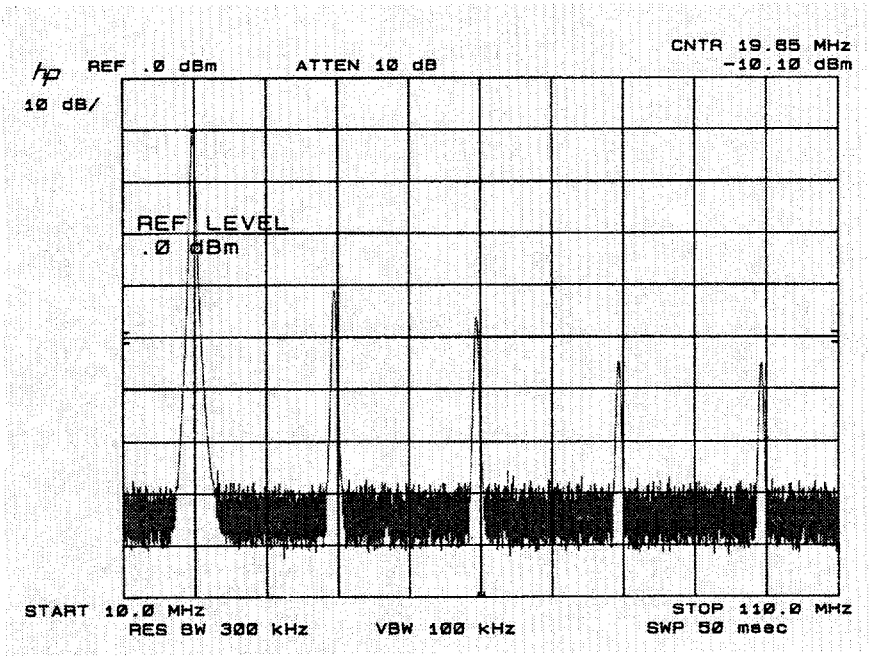

Figure 3-7 *Output spectrum of the oscillator configuration in Figure 3-l with the step attenuator set to 1 dB.*

The resulting oscillator output spectrum with the attenuator set to 6 dB is given in Figure 3-8. The required gain compression is 1.5 dB when the step attenuator is set to 6 dB. This corresponds to an MWA110 output level of 1 dBm, or -8.2 dBm at the coupler output. The measured fundamental output levels with 1dB and 6 dB attenuator settings, as read from Figures 3-7 and 3-8, are -10.1 and -13.7 dBm, respectively The differences in the predicted and measured output levels are probably a result of differences in limiting characteristics for the MWA110 when driving the reactive resonator load or a 50 ohm load.

When the coupler is moved from the resonator output to the output of the MWA110, the measured oscillator output spectrum is given in Figure 3-9. For this measurement the step attenuator

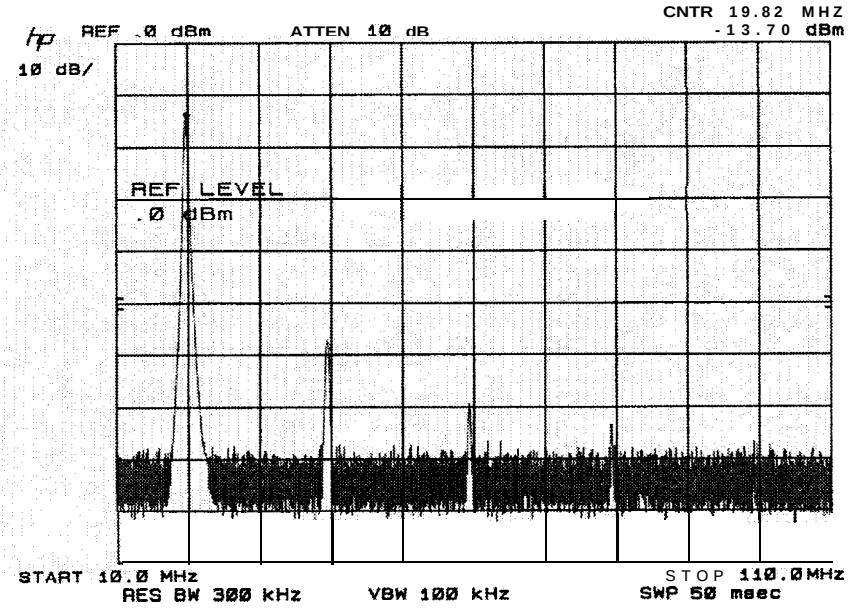

Figure 3-8 *Output spectrum of the oscillator configuration in Figure* 3-1 *with the step attenuator set to* 6*dB.*

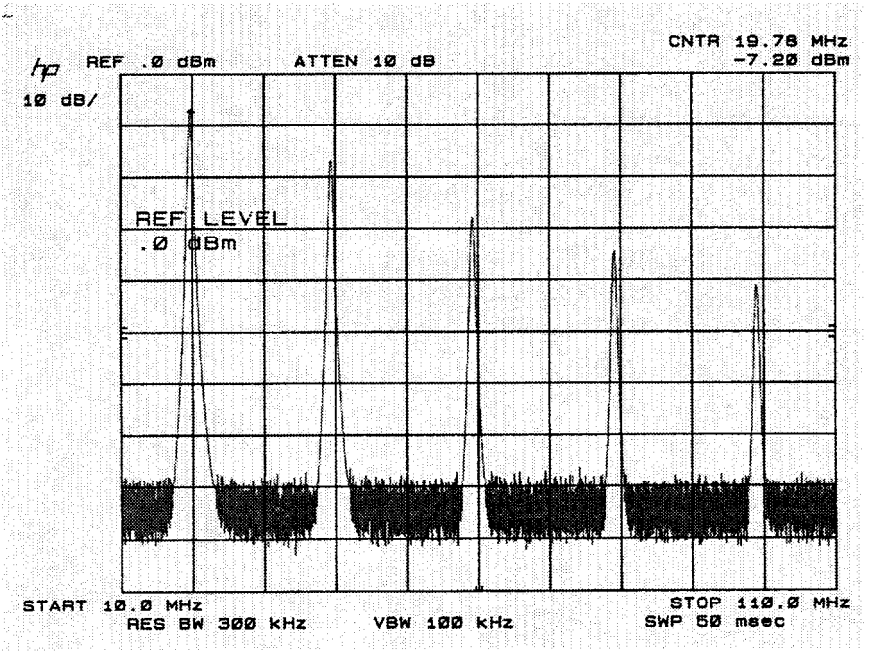

Figure 3-9 Output spectrum of the oscillator with the coupler moved to the output of the MWAllO.

is set to *6* dB. The fundamental output power is -7.2 dBm. This is closer in agreement with a predicted output level of -5.5 dBm.

In Figure 3-10 the output spectrum is given for the loop connected through the coupled port of the coupler. The additional loss associated with using the coupled port instead of the through port is compensated for by removing the step attenuator. This allows taking the output via the through port of the coupler, which results in greater output power. A block diagram of this configuration is given in Figure 3-11. With a 6.5 dB coupler loss, 2.5 dB of gain compression is needed. From Figure 3-6 the expected MWA110 output level is 2dBm. With 1.5 dB through loss for the coupler, the expected oscillator output level is 0.5 dBm. This is in excellent agreement with the measured output power of -0.9 dBm. In the latter two configurations, the resonator is isolated from the

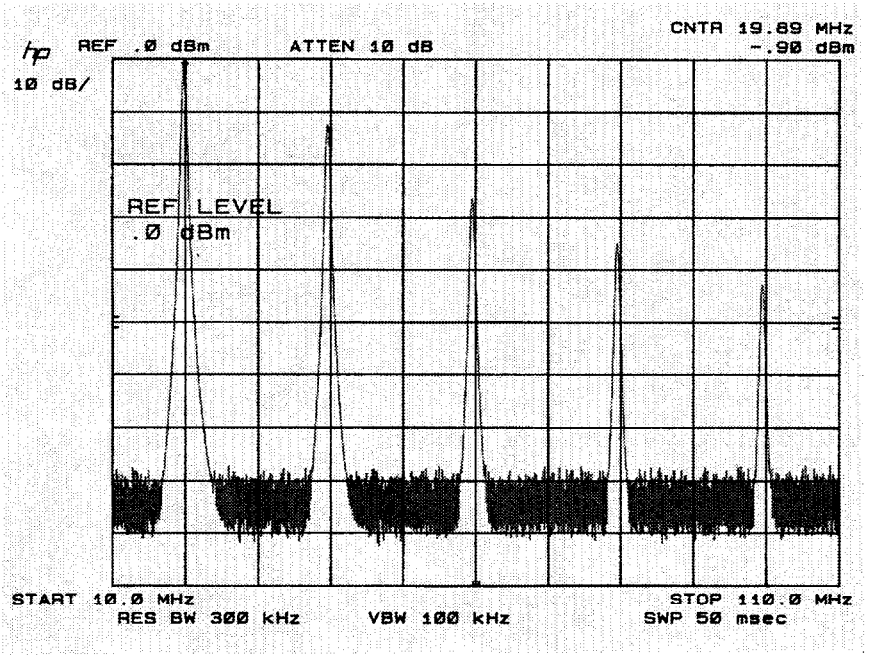

Figure 3-10 *Spectrum of the oscillator with the output taken from the through port of the coupler.*

MWA110 via the coupler. This is probably responsible for the much closer agreement of the predicted and actual output levels.

These are approximate but simple and effective methods of estimating the approximate output power of oscillators. A coupler is used in this example to take output power. The simplest coupling method is to connect the hybrid output directly to the resonator and couple out with a capacitor or inductor. Capacitive coupling is the most economical, while inductive coupling results in less harmonic content in the output.

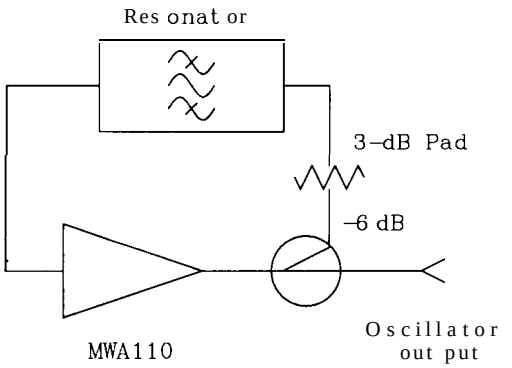

Figure 3-11 *Oscillator configuration with the output taken from the through port of the coupler.*

3.6 Output Harmonic Content

The resonator has a significant effect on harmonic currents. Therefore, accurate prediction, based on amplifier harmonic content, of oscillator harmonic content is difficult. Although not rigorous, certain considerations are useful to the designer wishing to minimize harmonic levels in the oscillator output. First of all, oscillators with large excess gain require hard limiting to absorb the excess gain. This increases the harmonic content in the resulting waveforms. This effect is illustrated in Figure 3-12. The output level and second harmonic output of the oscillator configuration in Figure 3-l are plotted versus the step attenuator setting. Recall that a step attenuator setting of 1 dB corresponds to a loop gain of approximately 6.5 dB. Therefore, with the step attenuator at 7 dB, the gain margin has fallen to 0.5 dB, and the output power is low. As expected, the second harmonic level decreases with less loop gain. In fact, spectrum plots at each step attenuator setting show that decreasing loop gain decreases the level of all harmonics, at least through the fifth harmonic. This is suggested by observing the output spectrums in Figures 3-7 and 3-8 for attenuator settings of 1 and 6 dB, respectively

However, the point at which the output is coupled is often more significant than the loop gain. Consider Figures 3-8 and 3-9.

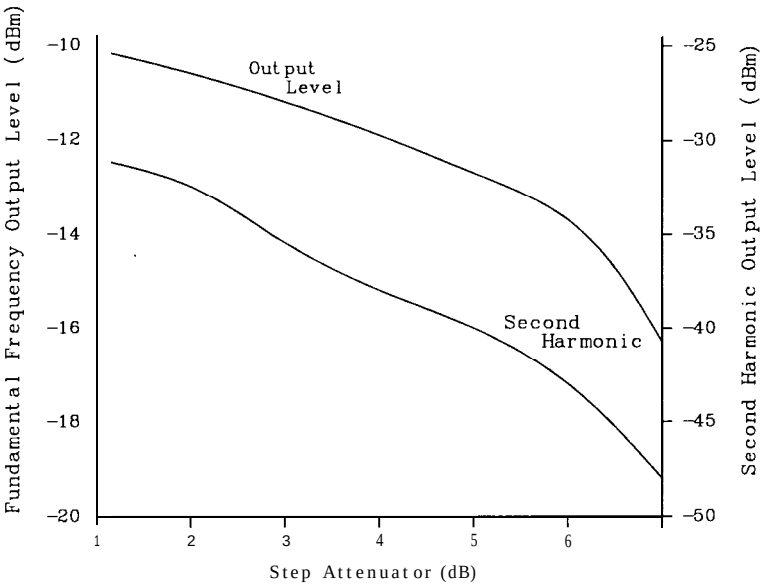

Figure 3-12 ***Measured fundamental output level and harmonic output vs step attenuator setting amplifier for the oscillator configuration in Figure*** 3-1.

Both spectrums are with the step attenuator set at 6 dB. However, in Figure 3-8 the output coupler is located after the resonator, while in Figure 3-9 the coupler is located directly at the output of the MWA110. In the former case, the oscillator resonator, which is in essence a bandpass filter, is used to filter the resulting output spectrum. Although the fundamental output level is reduced, the harmonic performance is improved dramatically When coupling directly to the resonator, care should be exercised so that variations of the load are not reflected back into the resonator, and therefore affect the operating frequency or loop gain. Using a high-impedance buffer amplifier, which therefore loads the resonator more lightly, may improve oscillator stability Using a higher reactance coupling element also improves oscillator stability This also reduces the output power level, and the trade-off should be made based on the relative importance of

stability and output power requirements. Biasing the oscillator for a greater power level and decreasing the coupling improves load stability and short-term stability (phase noise). However, a higher power level increases resonator component dissipation and therefore increases the warm-up drift.

The reactance of a coupling capacitor decreases with increasing frequency, This tends to couple harmonic energy to the output. Inductive output coupling has the opposite effect and tends to reduce harmonic output. Capacitive coupling is more economic, and the effect mentioned above is insignificant when using low coupling reactance.

3.7 Class-C Power Oscillators

When high output power is required, and stability and noise are of less concern, the oscillator may be designed for class-C operation. Shown in Figure 3-13 is a 1680 MHz radiosonde oscillator [5]. This oscillator has an output power of 2 watts with an efficiency of nearly 30%. The bias is very "stiff." There is no collector resistor and the emitter resistance is only 7.8 ohms. High peak currents, limited primarily by the transistor, flow for a small fraction of the waveform period, but supply substantial power to the tank. An exponential taper transmission line is used

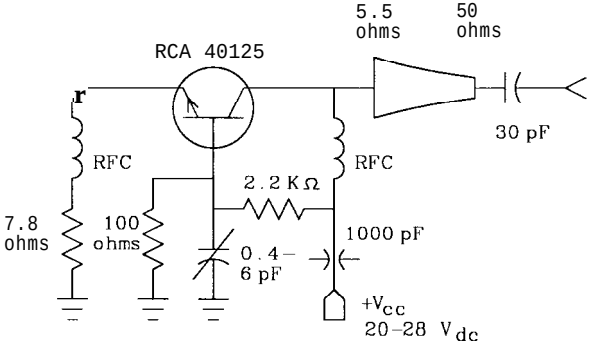

Figure 3-13 *High-power class-C L-band oscillator.*

in this oscillator to couple the collector to the 50 ohm output. C_1 resonates the transistor lead inductance to provide a very low base impedance.

The stiff bias is characteristic of class-C oscillators, as opposed to substantial collector resistance and heavy shunt and series feedback typical in near-class-A oscillators. The initial dc bias current in a class-C power oscillator is typically a fraction of the average current flowing after oscillation begins.

Because the requirement is for substantial output power, output coupling is tight, as opposed to the near-class-A design, where coupling is generally loose to improve stability and noise performance. The output in class-C designs is often conjugately matched to provide maximum power transfer. The output matching network is designed using typical class-C amplifier techniques [6].

3.8 Starting

Oscillation in the resonator amplifier cascade requires the cascade to provide its own input signal. What causes the cascade to start? Starting in a well-designed oscillator is not a problem. In fact, the process is very repeatable.

When power is applied to the cascade, large voltage changes in the bias network result in voltage changes in the resonator network. These voltage changes excite the natural frequency of the resonator and signal buildup can begin. The time constants of the bias network are generally such that the signal developed in the resonator is small; however, the excess loop gain continuously increases the level until limiting occurs.

If bias transients did not start oscillation, cascade noise would. Natural thermal noise in the cascade is bandlimited by the resonator. The resulting colored noise is amplified by excess loop gain and ultimately starts oscillation.

3.9 StartingTime

The time required to reach a steady-state oscillation level is a function of the excess gain and cascade input to output delay. Reference [7] derives an expression for buildup time, but the cascade delay is incorrectly stated to be the oscillation period. The cascade delay, primarily from the resonator, is a function of resonator Q and the oscillation period (frequency). For a single resonator

$$t_d = \frac{2Q_l}{\omega} \qquad 3.1$$

Figure 3-14 is a schematic of an oscillator similar to the oscillator in Figure 3-l. The coupler splitter has been removed and the output is taken via a 100 pF capacitor. Vcc is 12.5 V switched at a 1 kHz rate. The measured cascade open-loop gain with Vcc equal to 12.5 *Vdc* is approximately 10 dB. Shown in Figure 3-15 is Vcc and the output waveform into the 50 ohm load with the loop output connected to the loop input via a short coaxial jumper. Figure 3-16 shows the same waveforms, but with a 6-dB pad inserted in the loop output-to-loop input jumper. Without the 6 dB pad, the output is within 3 dB of the steady-state value in

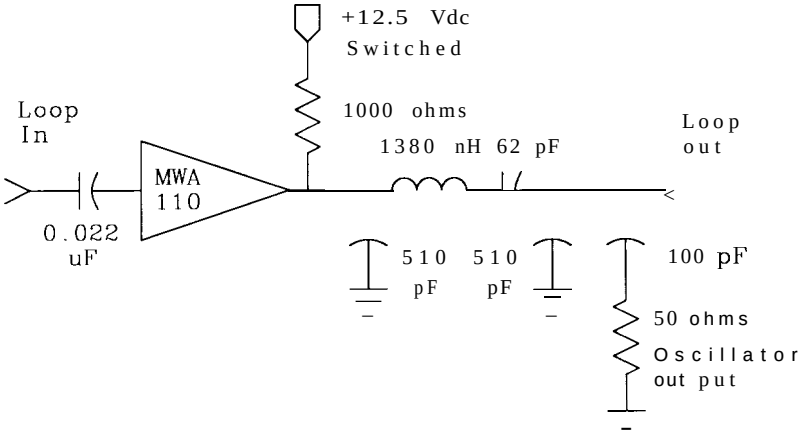

Figure 3-14 A ***20*** *MHz oscillator studied for starting characteristics.*

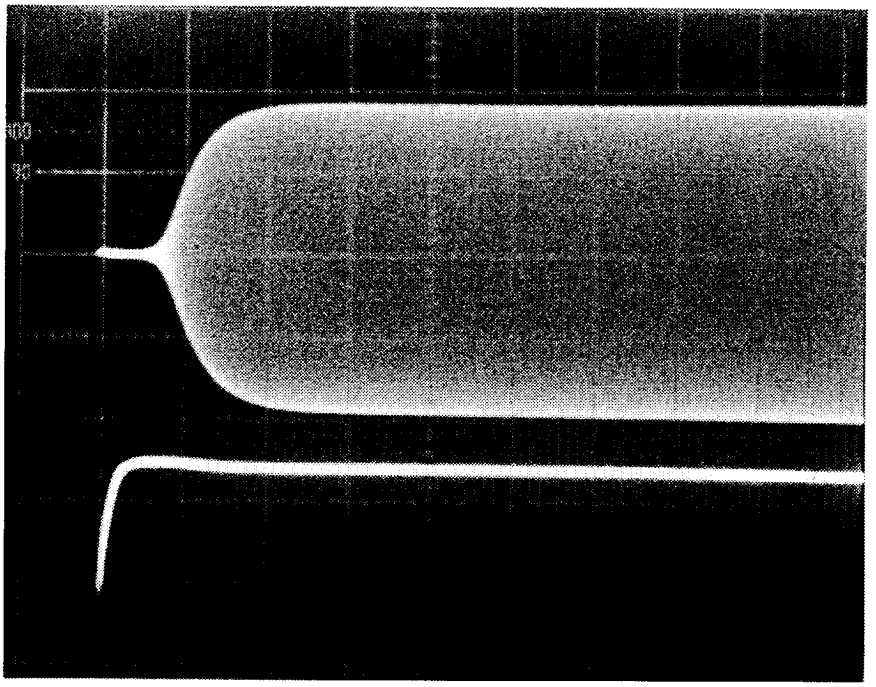

Figure 3-15 *Oscillator starting waveform (upper trace) with 10 dB loop gain. The switched supply voltage is the lower trace.*

approximately 1 μS. With the 6 dB pad, the time required is approximately 8 μS. The delay of this resonator is approximately 250 nS, so steadystate is reached in about 8 times the delay for 10 dB loop gain and about 32 times the delay with 4 dB of loop gain. The waveforms shown in Figure 3-16 were recorded with an oscilloscope triggered on the switched V_{cc}. The fact that the output waveform starting edge is without jitter illustrates that starting is predictable and repeatable.

For an extremely high-Q oscillator, such as a crystal oscillator, starting times can be very long. Not only are high-Q oscillators hard to pull in frequency and therefore FM modulate, but they are also difficult to AM modulate at high rates. Using the expression above for delay as a function of loaded Q, a crystal oscillator

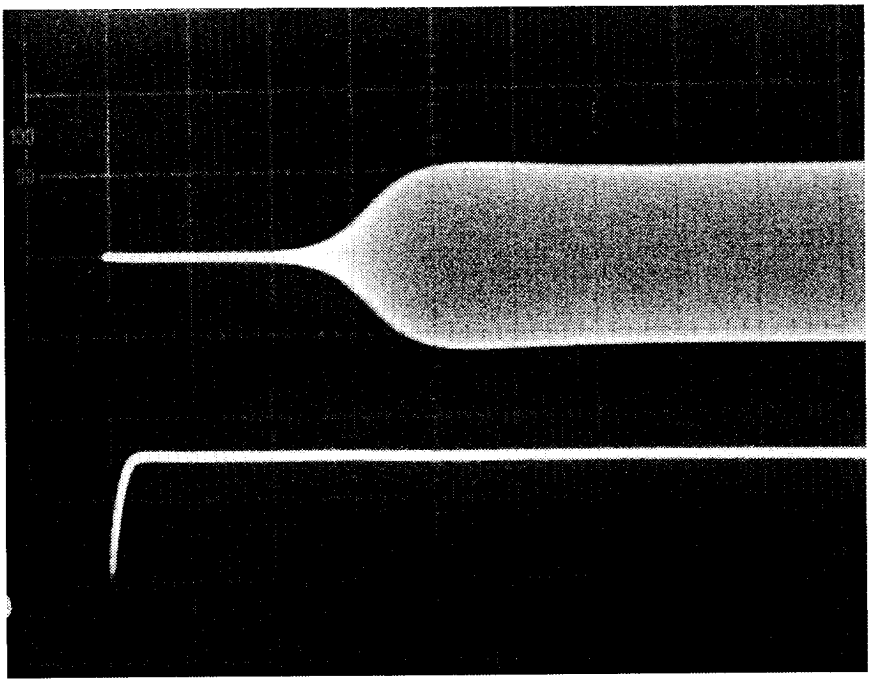

Figure 3-16 *Oscillator starting waveform (upper trace) with 4-dB loop gain. The switched supply voltage is the lower trace.*

with a frequency of 20 MHz, 4 dB loop gain, and a loaded Q of 50,000 requires approximately 25 mS to reach a near-steadystate output level.

3.10 Bias Time Constant

Oscillations cannot occur until the amplifier is biased in the active region. The time required for the bias network to reach steady-state can be greater than oscillation buildup time. This can significantly lengthen start-up time. The type of bias network, and the value of coupling and decoupling capacitors, affect the bias network time constant. This particular oscillator design, using a hybrid amplifier, has a short time constant. Discrete

transistor oscillators, with large bias resistances and decoupling capacitors, often have long time constants.

Bias time constant effects on starting are circumvented when *Vcc* is continuously applied and the RF signal path is switched. If the switching network supplies a steady resonator inductor current or resonator capacitor voltage prior to closing the loop, the starting phase of the oscillator can be controlled.

3.11 Frequency Effects of Limiting

As limiting occurs, the load presented to the resonator by the active device changes. Therefore, the operating frequency is expected to be a function of the degree of limiting, and thus the loop gain. These effects are minimized by a high loaded Q. Consider the resonator in Figure 3-2. The loaded Q increases with increasing shunt capacitors. With sufficiently large shunt capacitors, shifts in the reactance presented to the resonator caused by limiting effects in the active device have no effect on the operating frequency In this case, with a loaded Q of approximately 36, the shunt capacitors are 1000 pF each. High-frequency transistors have junction capacitances of only a few picofarads. Even substantial changes in these capacitances due to limiting will have only a small effect on the operating frequency of a high-Q near-class-A oscillator.

Table 3-2 *Operating Frequency versus Step Attenuator*

Attenuator (dB)	Frequency (MHz)
0	19.792
1	19.793
2	19.789
3	19.781
4	19.779
5	19.772
6	19.770
7	19.767

The operating frequency, measured with a digital frequency counter, of the oscillator in Figure 3-l with various step attenuator settings is given in Table 3-2. The operating frequency with 7 dB in the step attenuator, and therefore little limiting, is only 25 kHz different from the operating frequency with 0 dB attenuation, which is 7.5 dB of gain compression. This 25 kHz shift is only 0.13% of the operating frequency Also notice that the operating frequency is in excellent agreement with the oscillation frequency predicted by the zero-degree phase shift frequency, over the entire range of gain compression tested here.

3.12 References

[l] James F. Gibbons, *Semiconductor Electronics,* McGraw-Hill, New York, 1966, p. 593.

[2] Roy Hejhall, Systematizing RF Power Amplifier Design, *Motorola RF Data Manual,* Motorola, Phoenix, AZ, 1983, p. S-13. Also Motorola Application Note AN- 282A.

[3] Robert J. Matthys, *Crystal Oscillator Circuits,* John Wiley & Sons, New York, 1983, p. 131.

[4] *Motorola RF Device Data,* 3rd edition, MWA110/ MWA120/ MWA130 DC-400 MHz Wideband General-Purpose Hybrid Amplifiers, Motorola, Phoenix, AZ, 1983, pp. 5-88 to 5-95.

[5] Gregory Hodowanec, Microwave Transistor Oscillators, *Microwave Journal,* June 1984, pp. 39-42,62.

[6] Reference [2], pp. 8-13 to 8-16. Note AN-282A.

[7] Reference [l], pp. 579-580.

4

Noise

An ideal oscillator output voltage is described mathematically as a pure sine wave of constant frequency and amplitude. A real oscillator output voltage is expressed as

$$v(t) = [1 + n(t)] \cos [\omega_0(t) + \varphi(t)] \quad 4.1$$

with random processes

$$n(t) = \text{amplitude noise modulation} \quad 4.2$$

$$\varphi(t) = \text{phase noise modulation} \quad 4.3$$

In well-designed oscillators, amplitude noise is less signifcant than phase noise, and will not be considered further [1].

The phase noise performance of oscillators has become increasingly important because communications channels have become closer spaced and more heavily loaded, data transmission systems often require low phase noise, military EW and CCC systems are more sophisticated, and higher frequencies are being used by a variety of systems [2]. Broadband voltage-controlled oscillators used in electronically tuned PLL applications, which are now common, are inherently noisy.

4.1 Single-Sideband Phase Noise

Phase noise performance is described by various terms in both the frequency and time domains. In the frequency domain, the phase noise modulation creates continuous spectra sidebands, which generally decrease in level with increasing frequency offsets, *fm*, from the carrier. This common form of phase noise

description is the single-sideband (SSB) phase noise, L(fm). The units are dBc/Hz, or decibels below the carrier in l-Hz bandwidth.

4.2 Amplifier Noise

Before considering the phase noise of an oscillator, let us review the phase noise of an amplifier. Shown in Figure 4-l is the asymptotic power spectral density $S\varphi(fm)$ of the phase modulation term $\varphi(t)$ for an amplifier. For large offsets [3]

$$S\varphi(f_m) = \frac{FkT}{P_s} \tag{4.4}$$

where

F = amplifier thermal noise factor (4.5)

k = Boltzmann's constant = $1.38x10^{-23}$ J/K (4.6)

T = temperature ^{o}K (4.7)

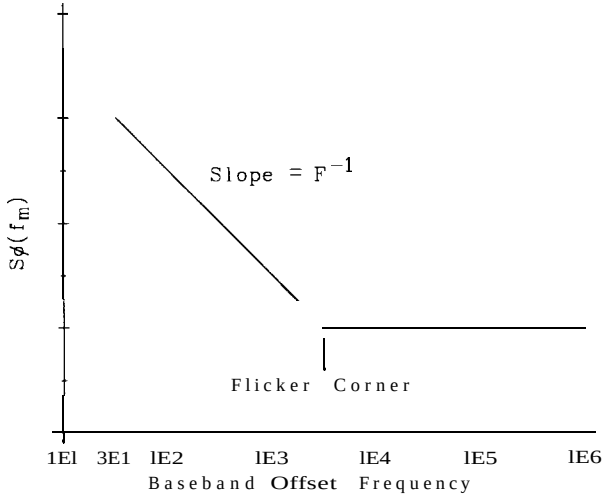

Figure 4-1 *Amplifier noise as a function of baseband frequency.*

Ps = amplifier input power level 4.8

At 290°K, $kT = 4.00 \times 10^{-21}$. Expressed in decibel terms we have

$$S\varphi(f_m) = -174(\text{dBm}) + \text{F(dB)} - P_s(\text{dBm}) \quad 4.9$$

4.3 Amplifier Flicker Noise

At lower frequencies, device flicker noise is significant. Unlike flat thermal noise, flicker noise power decreases with increasing offset frequencies with a slope of 10 dB per decade. The offset frequency at which the noise including flicker is 3 dB higher than the flat noise is the flicker corner frequency In-circuit flicker corner frequencies for active devices typically range from a few kilohertz to as high as several megahertz. Reference [2] suggests a rule-of-thumb flicker value of -120 dBc/Hz at l-Hz offset for bipolar transistors. This relates to a flicker corner frequency of 10 kHz for a flat thermal noise floor of -160 dBm/Hz or 262 kHz for a flat thermal noise floor of -174 dBm/Hz.

Unfortunately, manufacturers seldom characterize RF and microwave devices for flicker noise. One exception is the Motorola 2N4957 family of bipolar transistors [4]. Figure 3 in that reference gives the noise figure of the 2N5829 biased at Vce = 10 volts and I_c = 1 mA with a source resistance of 150 ohms versus frequency The noise figure is flat at 2.3 dB from 100 kHz to 600 MHz. At frequencies below 100 kHz the noise figure rises. At approximately 5 kHz the noise figure has risen 3 dB higher than the floor value, suggesting a flicker corner of 5 kHz.

Flicker noise is device dependent and varies considerably among bipolar, JFET, GaAs, and other devices. GaAsFET devices may have very high flicker corner frequencies resulting in significantly degraded phase-noise performance. The author has experienced flicker corner frequencies as high as 6 MHz in GaAsFET devices. Much work needs to be done on understanding and characterizing the flicker noise performance of active devices used at RF and microwave frequencies.

4.4 Oscillator Noise

An oscillator is formed by cascading the amplifier with a resonator and closing the loop. In a benchmark letter [5], D. B. Leeson summarized the phase noise characteristics of such an oscillator. At baseband frequencies within the resonator half-bandwidth, phase perturbations at the oscillator input due to noise or parameter variations result in a frequency shift at the output. Therefore, the SSB phase noise has a slope of f^{-3} (30 dB/decade) at offset frequencies below the flicker corner and a slope of f^{-2} at offsets greater than the flicker corner and less than the resonator half-bandwidth, $f_o/2Q$. Above the resonator half-bandwidth, the SSB phase noise floor is flat. Noise in a buffer amplifier outside the oscillator loop adds flat thermal noise. The buffer amplifier adds flicker phase noise if the buffer flicker corner frequency is greater than the resonator half-bandwidth. The asymptotic phase noise versus offset frequency of the oscillator formed by the cascade of a resonator and amplifier is given in Figure 4-2.

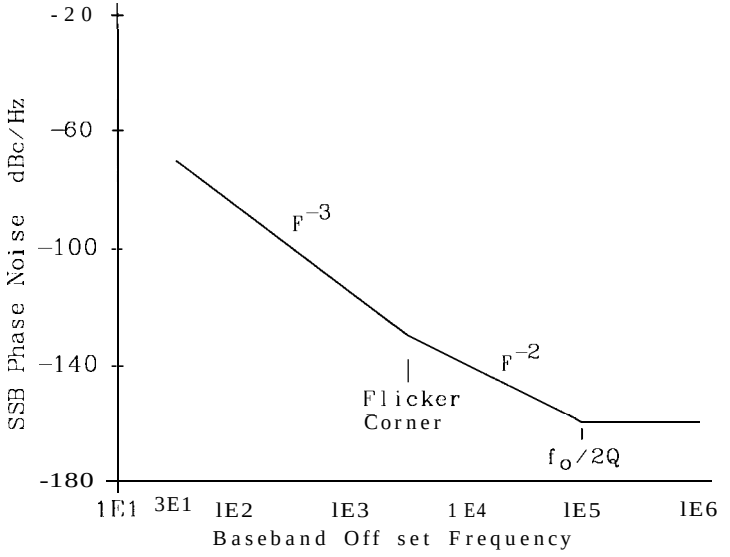

Figure 4-2 *Oscillator SSB phase noise as a function of baseband frequency.*

The expression for oscillator SSB phase noise (dBc/Hz) from Leeson, with a term for flicker noise, is

$$L(f_m) = 10 \log\left[\frac{1}{2}\left(\left(\frac{f_o}{2Q_l f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\left(\frac{FkT}{P_s}\right)\right] \qquad 4.10$$

$L(f_m)$ may be measured directly with a spectrum analyzer whose phase noise performance is better than the measured oscillator at the desired offset frequency The measurement bandwidth is usually greater than 1 Hz, such as 1 kHz, so the actual noise is reduced from the measured noise by 10 $\log_{10}(\mathrm{BW})$.

A photograph taken from a spectrum analyzer of the SSB phase noise versus offset frequency for a broadband VCO tuned to 755 MHz is shown in Figure 4-3. Notice that the phase noise spectrum is symmetrical about the carrier frequency The appearance, response and width of the spectrum near the center

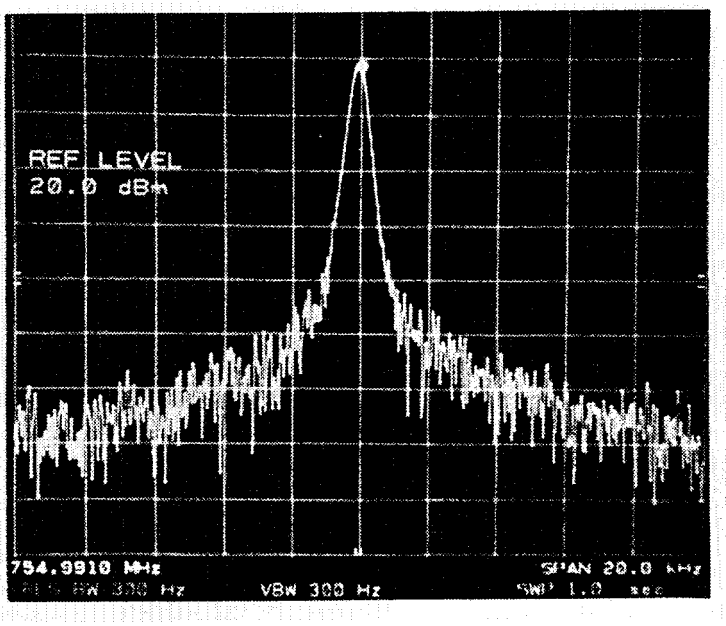

Figure 4-3 *Photograph of spectrum analyzer display of SSB phase noise of a VCO tuned to 755 MHz.*

frequency (down to approximately 40 dB) is a result of the selected 300-Hz analyzer IF resolution bandwidth. The SSB phase noise accumulated in this bandwidth and then displayed by the spectrum analyzer is 10 log10(300) or approximately 25 dB higher than the normally specified dBc/Hz value. In Figure 4-3 the span is 20 kHz, or 2 kHz per division. For measurements taken with an analyzer with Gaussian IF filters and an envelope detector, the noise is 2.5 dB worse than indicated [6]. Additional video filtering with the analyzer averages the displayed noise peaks and valleys. Therefore, the SSB phase noise performance shown in Figure 4-3 at 6 kHz offset is approximately -62-25+2.5 dB or -84.5 dBc/Hz.

4.5 Oscillator Noise Nomograph

Given in Figure 4-4 is a nomograph for finding the SSB phase noise of an oscillator. The far left scale is the oscillator signal power level in dBm minus the cascade amplifier noise figure in decibels. Given a circuit operating temperature of 290^{o} Kelvin, these two factors establish the phase noise floor at offsets greater than $f_o/2Q$, so the floor is included on the left scale.

The second factor which establishes oscillator phase noise performance is the carrier frequency, f_o, divided by two times the loaded Q. The frequency unit for f_o on the nomograph is megahertz. $f_o/2Q$ is the offset frequency at which the SSB phase noise breaks from the noise floor and rises toward the carrier at a rate of 20 dB/decade. For high Q oscillators at low carrier frequencies (such as quartz crystal oscillators) the break occurs at relatively low offsets so the decreasing noise at increasing offset is observed to level onto the floor at offsets below one megahertz. With moderate and low Q microwave oscillators the break occurs above one megahertz offset and the noise is seen to continuously decrease with increasing offset.

A straight line from the power minus the NF through $f_o/2Q$ extends to the pivot bar on the nomograph. A straight line from the pivot point through the desired offset frequency in kilohertz,

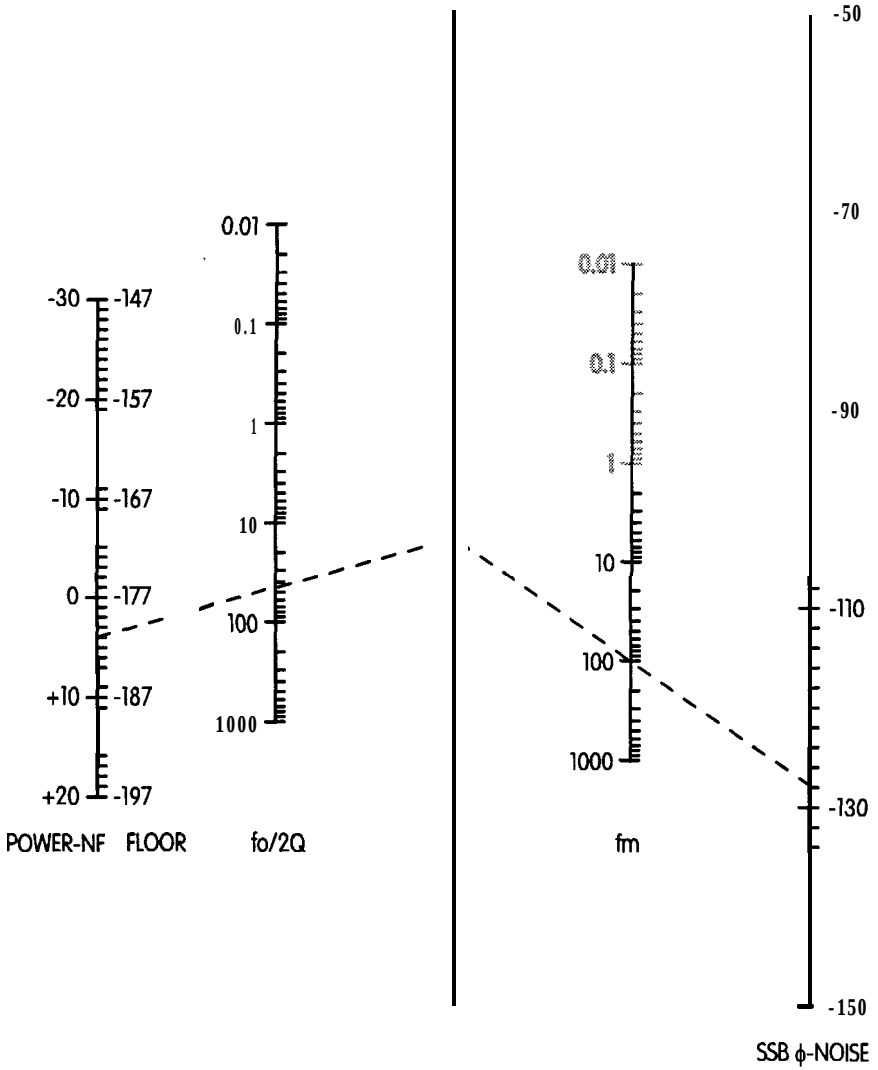

***Figure** 4-4 SSB ϕ-noise versus the power (dBm) minus the NF (dB), the carrier frequency (MHZ over 2 times the loaded Q and the baseband offset frequency, fm,(KHz). The example is for a power of +9 dBm and a NF of 5 dB, a carrier frequency of 900 MHz and a loaded Q of 10 (fo/2Q=45), and an offset of 100 KHz. The nomograph is valid for fc < fm < fo/2Q.*

fm, intersects the far right scale to find the SSB phase noise for the oscillator at that offset.

The nomograph does not include flicker noise. Therefore the estimation is only valid for offset frequencies greater than the flicker corner,fc. Offset frequencies of 1 KHz and lower are grayed in Figure 4-4 as a caution because the flicker corner is seldom this low. In fact it may be much higher. The estimated noise may be corrected by adding 10 dB additional noise per decade less than f_c. The nomograph does not consider that the phase noise asymptotically approaches the noise floor. Therefore the estimation is only valid if $f_m < f_o/2Q$. At higher offsets the oscillator phase noise approaches the floor value on the left scale.

4.6 Residual Phase and Frequency Modulation

If an unmodulated oscillator is detected with a sensitive phase demodulator, the detector output voltage is the residual phase modulation. It is sometimes referred to as incidental phase modulation. The demodulated baseband output is normally limited to a specific range of frequencies, for example from 50 to 3000 Hz. These demodulated baseband frequencies are related to the undetected carrier offset frequencies. The baseband frequencies of interest are a function of the type of system involved. The baseband frequencies of interest for voice communication systems are about 50 to 3000 Hz, for Doppler radar are 1 Hz to 10 MHz, for FM mobile are 10 to 100 kHz, for QPSK are subhertz to 100 Hz, and for navigation systems are subhertz to 10 Hz [2]. These offset frequencies limits are obviously just general guidelines.

The frequency-domain power spectral density of the phase noise term, $\varphi(t)$, is $S\varphi(f_m)$. If

$$\int_{fa}^{\infty} S\varphi(f_m) < 1 \text{ rad}^2 \qquad 4.11$$

the square of the residual rms phase modulation is

$$\Delta\varphi^2 = 2\int_{f_a}^{f_b} L(f_m)\, df_m \text{rms} \qquad 4.12$$

If an unmodulated oscillator is detected with a sensitive frequency demodulator, the detector output voltage is the residual frequency modulation. It is sometimes referred to as incidental frequency modulation. Again, subject to the limitation that the total value of the integrated phase noise is $< 1\ \text{rad}^2$, the square of the residual rms frequency modulation is

$$\Delta f^2 = 2\int_{f_a}^{f_b} f_m^2 L(f_m)\, df_m \text{rms} \qquad 4.13$$

The SSB phase noise versus offset frequency uniquely defines the residual phase and frequency modulation. Unless the slope of the SSB phase noise is known, the SSB phase noise is not uniquely defined by the residual phase or frequency modulation. Therefore, SSB phase noise is a more complete characterization of phase noise performance. For this reason, and because it is readily observed and measured with a spectrum analyzer, SSB phase noise is commonly used to characterize phase noise performance. The residual phase or frequency modulation of a system is of interest because it relates directly to the ultimate postdetection SIN ratio in PM and FM systems.

In an FM system with a high predetection C/N ratio, the ultimate postdetection S/N ratio, ignoring improvement by emphasis and deemphasis, is directly related to the square of the ratio of the signal rms frequency deviation to the residual rms frequency modulation. That is,

$$\frac{S}{N} = 10 \log\left[\frac{\text{rms deviation}^2}{\Delta f^2}\right] \qquad 4.14$$

4.7 Varactor Modulation Phase Noise

Oscillators are often electronically tuned using a voltage- or current-dependent reactive element such as a varactor in the resonator. Any internal or external noise voltages impressed on this element tunes the resonator frequency, effectively FM modulating the oscillator. We refer to this as varactor modulation noise. In the author's experience, the effective noise resistance, R_{enr}, of silicon hyperabrupt varactors ranges from 1 to 10 K ohms. R_{enr} is seldom if ever specified and is therefore determined empirically The thermal noise in this resistance modulates the varactor capacitance, adding phase noise. The equivalent noise voltage modulating the varactor is given by Nyquist's equation

$$Vn = \sqrt{4kTR_{enr}} \text{ volts /root hertz} \qquad 4.15$$

This expression for the equivalent noise voltage assumes that no external resistance is noise modulating the varactor. If the varactor is driven from a source with a high source resistance, thermal noise in the source resistance may be greater than the internal varactor resistance. Because noise from these two resistances is uncorrelated, the total noise voltage is the square root of the sum of the squared voltages.

The peak phase deviation in 1 Hz bandwidth which results from the varactor noise resistance is

$$\theta_d = \frac{\sqrt{2}K_v V_n}{f_m} \qquad 4.16$$

where K_v is the VCO gain constant in hertz/volt. The resulting SSB phase noise (dBc/Hz) is

$$L(fm) = 20 \log \frac{\theta_d}{2} \qquad 4.17$$

The total SSB phase noise of a varactor-controlled oscillator is the power sum of this varactor modulation phase noise and the oscillator phase noise discussed previously

Varactor modulation noise is most significant in broadband high-frequency VCOs because the VCO gain constant is large. For

example, if a varactor tunes an oscillator 1000 MHz with a 10 volt control voltage change, the VCO gain constant is 100 MHz/volt. Even a small noise voltage produces a large frequency modulation. Varactor modulation noise may be reduced by using a frequency tuning range no larger than necessary, using a varactor with a larger required voltage change for a given capacitor ratio, or by switching ranges so that the tuning range for each switch position is less.

A chart for quick reference showing the SSB phase noise contribution from varactor modulation is given in Figure 4-5. The SSB phase noise is given for an effective noise resistance of 3300 ohms and VCO gain constants of 1000 to 0.001 MHz/volt.

Varactor modulation noise is a different phenomenon than oscillator loaded Q reduction because ofvaractor Q. It is true that varactor unloaded Q often reduces the oscillator loaded Q and therefore reduces phase noise performance. However, in broadband high frequency oscillators where varactor noise modulation is prevalent, a higher-Q varactor may increase phase noise if it has a higher effective noise resistance.

Broad tuning per se is not a limiting factor of phase noise performance. By using a mechanically tuned capacitor or cavity, varactor modulation noise is avoided, the resonator may be tuned over a broad range, and the loaded Q may be very high.

4.8 Buffer Amplifiers

Leeson's oscillator phase noise equation indicates that phase noise performance improves with higher-power operation. For the sake of simplicity and performance, a medium-power oscillator followed by a passive pad for load isolation is suitable for many applications. This approach uses fewer active devices, is easier to tune, and may give better phase noise performance than that of a low level oscillator followed by a buffer amplifier. The use of a buffer amplifier is unavoidable in certain applications. Crystal oscillators are operated at a low power level for best aging characteristics. Oscillators with varactor tuning elements

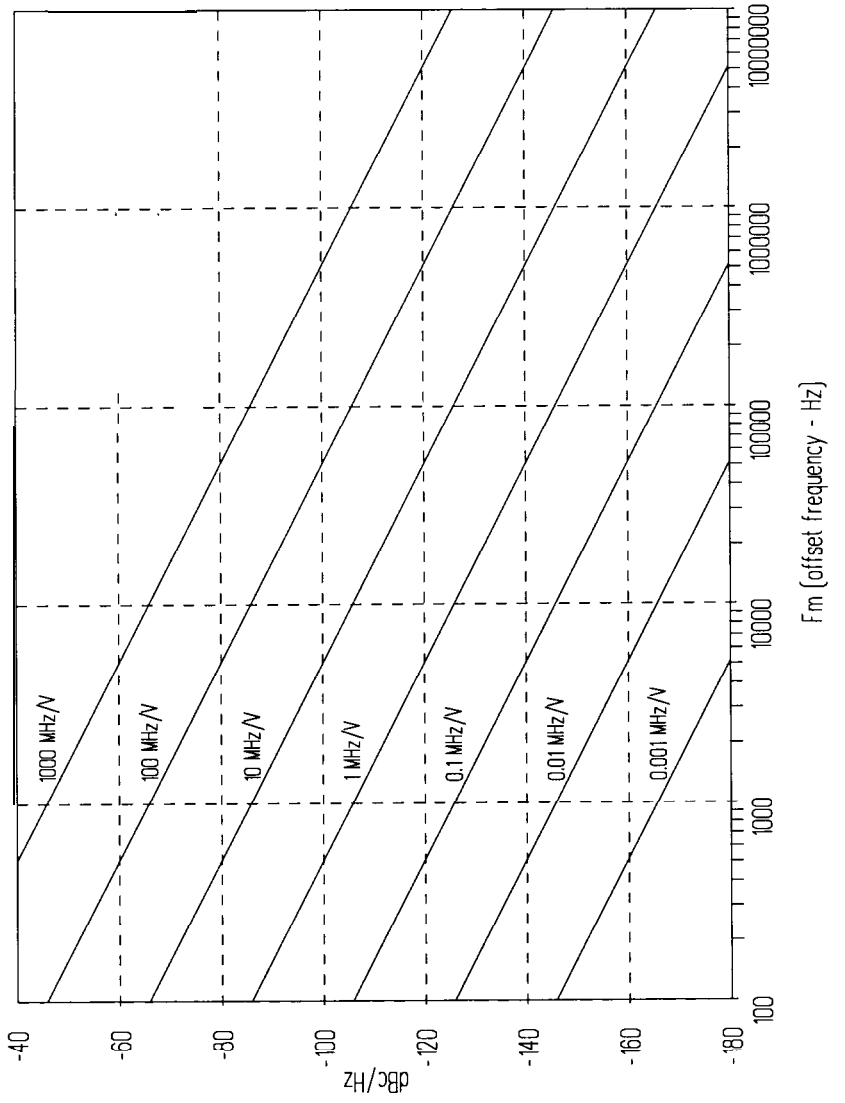

Figure 4-5 *Varactor modulation contribution to oscillator SSB phase noise. Curves are for a nominal varactor effective noise resistance of 3300 ohms with VCO gain constants of 1000 to 0.001 MHz/ volt.*

may require low operating levels to avoid large voltages across the varactor.

A buffer amplifier degrades phase noise performance if its thermal noise, referenced to the input, exceeds the oscillator output phase noise at a given offset frequency This condition is most likely at large offset frequencies and low oscillator power level. The buffer amplifier thermal noise floor referenced to the input in 1 Hz of bandwidth (watts/hertz) is

$$Ni=FkT \qquad 4.18$$

An asymptotic phase noise response for a typical oscillator/buffer cascade is given in Figure 4-6.

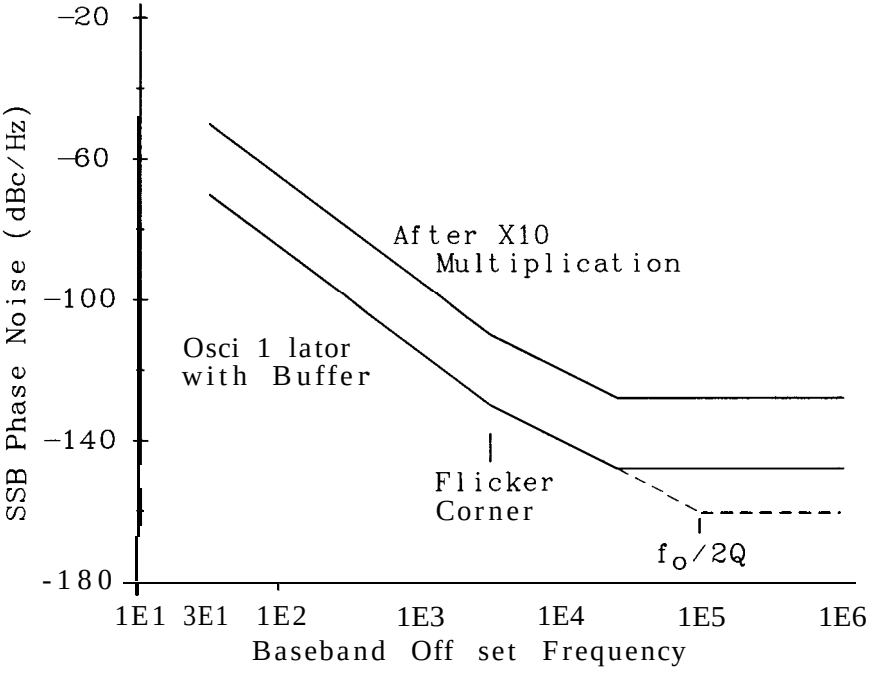

Figure 4-6 *Oscillator SSB phase noise after a buffer amplifier (lower trace) and frequency multiplication (upper trace).*

4.9 Frequency Multiplication

Frequency multiplication of the output of an oscillator with non-linear resistive (diode) or reactive (varactor) devices results in increased SSB phase noise at the higher output frequency

$$L(fm)Nfo = N^2 L(f_m) f_o + A \qquad 4.19$$

where

N = multiplication factor 4.20

A = additive term 4.21

For well-behaved multipliers, the additive factor, *A*, is between 0 and 3 dB. The additive factor for nonlinear resistance multipliers such as diode ring doublers is very low and can generally be ignored. The additive factor for varactor and step-recovery diode multipliers is larger and is frequently dependent on the power level.

Because the SSB phase noise performance of the fundamental oscillator increases as the square of the carrier frequency and the phase noise increases as the square of the frequency multiplication factor, it is tempting to assume that there is no difference in the phase noise performance of a multiplied low-frequency oscillator and a direct high-frequency oscillator. However, the direct high-frequency oscillator ultimate phase noise at large offset frequencies reaches the FkT/P_s limit, whereas the floor of the multiplied low-frequency oscillator rises by N^2. The SSB phase noise after frequency multiplication by 10 is shown in Figure 4-6.

4.10 Discrete Sidebands

The oscillator output frequency spectrum considered thus far is continuous. A typical output spectrum also includes discrete components at specific offset frequencies. Often present are harmonics of the 60 Hz power-line frequency An oscillator can be modulated at 60 Hz by ripple on the dc supply lines or by

magnetic fields, frequently from transformers. Inductors with cylindrical magnetic cores, whether used in the resonator or for bypassing, are susceptible to magnetic fields.

The VCO control voltage in PLL applications has ripple components at the fundamental and harmonics of the phase detector reference frequency These components modulate the VCO and create discrete sidebands at harmonics of the reference frequency Narrow-loop bandwidths tend to filter out the reference frequency sidebands, while wide-loop bandwidths result in greater sideband levels.

4.11 Power Supply Noise

Noise on the dc supply voltages to an oscillator can AM and FM modulate the output. The effects of power supply noise are reduced by designing the oscillator so that the operation frequency is relatively insensitive to the supply voltage. This can easily be tested by adjusting the dc supply voltages and observing changes in the operating frequency Further improvement can be realized by isolating the oscillator from power supply noise using voltage regulators.

A common component in electronic circuits and systems is the bipolar monolithic voltage regulator. These devices are available in a variety of forms from several manufacturers. They are simple to use, small, and inexpensive. Unfortunately, many have unpredictable and erratic noise performance. A significant broadband noise component superimposed on the dc output voltage may erratically appear and disappear over a time span of minutes. A good oscillator design tends to suppress this noise, but a random and unpredictable drift or jump of a few or several decibels in the SSB phase noise of the oscillator may be observed. The author avoids their use in oscillator design. At least a device with specified output noise performance should be selected. Zener diodes are also noisy but are generally less erratic. With additional R-C filtering, they are a better selection than inexpensive monolithic voltage regulators.

Because the average current drain of a typical oscillator is fairly small, simple series resistance and shunt capacitance filtering of the dc supply is often adequate. The small current drain allows a fairly large resistance, which therefore provides good filtering of supply noise, particularly at frequencies above 60 Hz. The supply to a buffer amplifier requires less filtering and can be through a separate line.

For critical applications, where R-C filtering is inadequate, a simple discrete transistor regulator serves well. Many of the performance requirements of monolithic voltage regulators, such as low differential voltage, accurate voltage value and low-temperature drift are unnecessary and a single transistor regulator usually suffices.

4.12 Low-Noise Design Suggestions

Let us summarize some of the techniques involved in low-noise oscillator design. First of all, it is necessary to determine if phase noise performance is limited primarily by varactor modulation or by oscillator noise. If the oscillator is to be varactor tuned, Leeson's equation and the varactor modulation equation are evaluated to determine which noise contribution is more significant. The nomographs in Figures 4-4 and 4-5 are helpful in making this determination. The conclusion may be verified by measuring the phase noise performance with the varactor and with the varactor replaced with a fixed or mechanically tuned capacitor.

If the phase noise performance is limited primarily by varactor modulation, the following steps are taken:

(a) Reduce the tuning range for a given varactor voltage change. If the tuning range exceeds the necessary value, it may be reduced by series or parallel capacitance with the varactor, or a varactor with a smaller tuning ratio.

(b) Range switch the oscillator. Breaking the tuning range into smaller ranges reduces the VCO gain constant. Switching may be mechanical or PIN diode.

(c) Select a different varactor. The internal noise voltage varies between varactor types, When the phase noise is varactor modulation limited, varactor Q is not the criterion. Empirical testing is required for varactor selection.

Some workers suggest using two varactors; one for coarse tuning whose voltage is switched, and one for fine tuning. However, even with a clean applied voltage, varactor resistance noise modulates the coarse tuning varactor. Range switching with fixed reactors must be used, such as PIN switching of capacitors or inductors. Dual-range varactors accomplish nothing.

If the phase noise performance is limited by Leeson's equation, these steps may be taken:

(a) Increase the loaded Q of the oscillator. The importance of this cannot be over emphasized. Oscillator designs with loaded Qs of only 2 or 3 are common even when component unloaded Qs are high. When phase noise or long-term stability is important, the loaded Q of an oscillator design should be 50 to 70% of the component unloaded Q [7].

(b) Utilize components with higher unloaded Qs. Higher unloaded Qs allow designs with higher loaded Q. Cavities, SAWs, DSOs, and crystals have high unloaded Qs.

(c) Run the oscillator at higher power levels. This improves phase noise at all offset frequencies.

(d) Select a device with a low flicker corner frequency and use a circuit design which minimizes flicker noise. An unbypassed emitter resistance of 10 to 30 ohms may reduce flicker noise by as much as 40 dB [8].

(e) Select a device and a circuit topology with a low noise figure. The cascade amplifier is designed using the same techniques employed for low-noise amplifiers. The source impedance presented to the transistor should be optimum and the emitter should be directly grounded (this of course contrasts with the flicker design goal above).

(f) Absorb excess loop gain via AGC or well-behaved limiting such as encountered in differential amplifiers instead of via saturation. Heavy saturation can dampen resonator Q, increase noise due to AM-to-PM conversion, and up-convert noise at baseband frequencies to noise sidebands on the carrier frequency

Authors sometimes state a preference for a JFET, or a particular bipolar configuration, because the high impedance obtained loads the resonator less and affords a higher Q. These concepts are based on a restricted viewpoint. Via inductive taps or coupling elements, resonator loaded Q is independent of source and load impedances. Otherwise, how could narrow filters (high loaded Q) be constructed for 50 transmission systems?

Similarly, claims are sometimes made that oscillators constructed from transmission line resonators have lower noise. Certainly TEM, TE and TM mode cavity oscillators can achieve high unloaded Qs, but this is due to larger resonator size. The unloaded Q of both L-C and transmission line resonators increase with increased physical size. The maximum size of inductors is restricted due to increased winding capacitance which lowers the maximum practical operating frequency Transmission line structures can be constructed physically larger and therefore with higher unloaded Q before parasitic modeing is significant. However, for a given size, transmission line structures have no unloaded Q advantage over L-C structures. For example, through several hundred megahertz, resonators constructed using semirigid 0.141-inch-OD Teflon coax have lower Q than those of equivalent- sized L-C resonators.

The maximum expected unloaded Qs for several resonator forms [9,10] at 100,300,1000, and 3000 MHz are given in Table 4-l.

4.13 Typical Oscillator Noise Performance

The SSB phase noise versus offset frequency for several different types of oscillators is given in Figure 4-7. Curve 1 is calculated data for a 100 MHz L-C resonator, MRF901 transistor oscillator.

Table 41 *Best Unloaded Qs of Typical Transmission Lines*

	Frequency (MHz)			
	100	300	1000	3000
CONSTRUCTION		Unloaded Qs		
0.5-in.-OD 50 Ω, air coax	480	840	1500	2600
0.141 -in-OD 50 Ω, PTFE	120	200	360	600
0.062-in-thick 50-Ω microstrip, PTFE glass microfiber	130	200	330	440
0.025-in.-thick 50-Ω microstrip, alumina	20	40	70	120
0.30-in.-OD coil, 260 nH, L/D=2, 10 turns	350			
0.07-in.-OD coil, 13 nH, L/D=2, 5 turns	80	140	260	

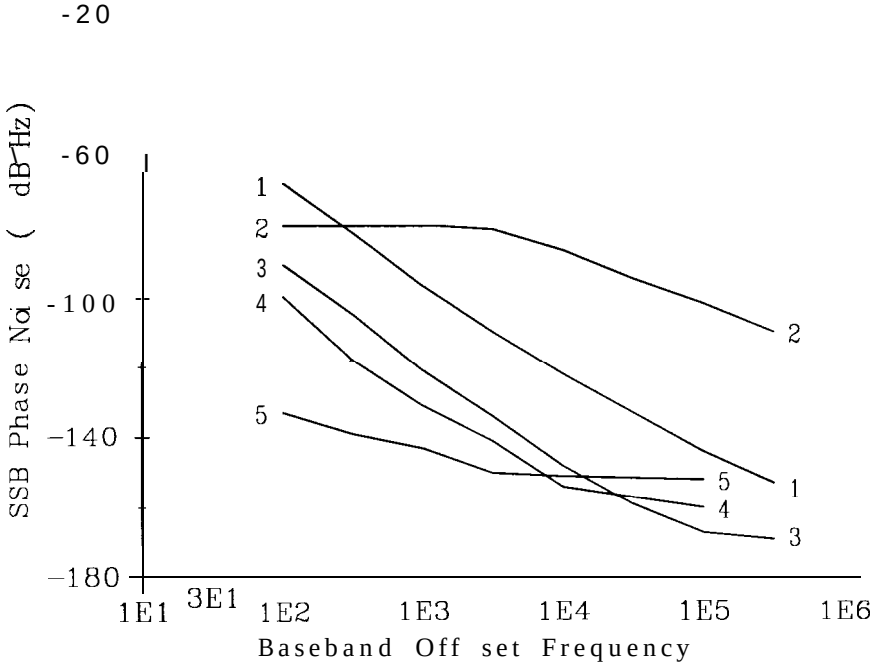

Figure 4-7 *SSB phase noise of five different oscillator types.*

A loaded Q of 15, a power level of 8 dBm, and a flicker corner of 10 kHz are assumed. A varactor provides a 10 MHz tuning bandwidth. Noise is predominatelyvaractor modulation noise for offset frequencies above 50 kHz. The ultimate noise floor is reached at offsets greater than 1 MHz.

Curve 2 is measured data for a 600 to 900 MHz VCO running at 750 MHz and phase locked to a crystal reference. The VCO type is the negative resistance UHF VCO studied in Chapter 9. This unit uses a 2N5109 and provides approximately 10 dBm tapped from the resonating transmission line. The phase noise above 3 kHz is predominately varactor modulation noise. Below 3 kHz, the phase-locked loop improves the phase noise. The phase noise below 3 kHz in this case is phase detector noise, at the reference frequency, multiplied up to 750 MHz. The flat (or nearly flat) SSB phase noise below the loop bandwidth is typical of phase-locked oscillators.

Curve 3 is the calculated SSB phase noise of a 5.5 MHz fixed or mechanically tuned L-C Clapp oscillator using a 2N4416 JFET transistor. A loaded Q of 35 and a flicker corner frequency of 10 kHz are assumed. The ultimate SSB phase noise is approximately -170 dBm and is reached by 100 kHz. The lower phase noise of the 5.5 MHz oscillator as compared to the 100 MHz oscillator illustrates the advantages of a higher Q and lower operating frequency

Curves 4 and 5 are measured data for a high-performance Driscoll oscillator type, discussed in Chapter 11. Curve 4 is for an oscillator using a 4 MHz ceramic resonator with a series resistance of 5.4 ohms and an unloaded Q of 1560. Curve 5 is for an oscillator using a fundamental-mode 4 MHz quartz crystal resonator with a series resistance of 22 ohms and an unloaded Q of 154,000. The input transistor is biased at $Vce = 9$ volts and $I_c =$ 15 mA. The output transistor is biased at 1.5 mA.

The relatively low value of series resistance for these resonators does not take full advantage of the Driscoll oscillator. However, this crystal oscillator, with an inexpensive quartz resonator, illus-

trates the marvelous noise performance available in crystal oscillators.

4.14 References

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[2] Phase Noise, *RF & Microwave Phase Noise Seminar,* Publication 59558136, Hewlett-Packard, Palo Alto, CA, p. 4.

[3] Reference [2]. pp. 13-14.

[4] *Small-Signal Transistor Data*, Motorola Semiconductor Products Div., Phoenix, AZ, 1983, pp. 7-20.

[5] D. B. Leeson, A Simple Model of Feedback Oscillator Noise Spectrum, *Proceedings of the IEEE,* February 1966, pp. 329-330.

[6] Application Note 150-4, Spectrum Analysis...Noise Measurements, Spectrum Analyzer Series, Hewlett-Packard, Palo Alto, CA, January 1973, pp. 7-11.

[7] J. K. A. Everard, Minimum Sideband Noise in Oscillators, *40th Annual Frequency Control Symposium, IEEE,* 1986, pp. 336-339.

[8] Ulrich L. Rohde, *Digital PLL Frequency Synthesizers,* Prentice Hall, Englewood Cliffs, NJ, 1983, p. 78.

[9] *=TLINE= Operation Manual,* Eagleware Corporation, Stone Mountain, GA, 1987, p. 3-8.

[10] *Reference Data for Radio Engineers,* 6th ed., Howard W. Sams, Indianapolis, IN, 1975, p. 6-4.

5

Biasing

A complete and rigorous description of biasing techniques, including all temperature and leakage effects, for bipolar, JFET, dual-gate FE?: and hybrid devices, is beyond the scope of this chapter: Except in rare applications, such as calibrated output-level oscillators, the bias schemes given here provide a more than adequate degree of bias ***point*** *definition and stability. An active bipolar bias network is given as the final bias example. Resorting to even this modest level of bias network complexity is seldom required.*

5.1 Bipolar Transistor Biasing

The bipolar junction transistor is biased in the active region with the base-emitter junction forward biased and the base-collector junction reverse biased. The base-emitter voltage is approximately 0.6 volt but increases with a decrease in temperature and with increasing current.

The required base current is the collector current divided by β. β increases with an increase in temperature. β is typically 30 to 80 for RF and microwave transistors at room temperature. Greater variation in β, even for devices of the same type, is frequently encountered. β is also a function of collector current. It has a broad maximum at a current that is optimum for highest gain. β drops off at lower current. Operation at currents less than the maximum gain current is often used to reduce transistor noise. β drops off more quickly above the maximum gain current. Device data sheets normally specify expected β for various operating conditions.

Saturation occurs when the base drive exceeds the current necessary to pull the collector voltage down to the saturation voltage, generally about 0.3 volt. The saturation voltage increases with an increase in collector current. Cutoff occurs when the base-emitter junction is reverse biased. When this occurs, the collector voltage rises to the supply voltage.

Important parameters for bipolar transistor selection are the upper frequency range, noise performance, the intended operating power range, β, and the maximum current, voltage, and dissipation ratings. Although these parameters vary from device to device, manufacturing and selection techniques now provide reasonably consistent devices. The bias network must provide the necessary stabilization of the quiescent bias point with temperature and device-to-device variations.

Several different bipolar bias networks are outlined next. All bias networks except one require a single supply The NPN configuration is assumed, but if PNP transistors are used, the supply polarity may be reversed.

Several biasing schemes are given because bipolar CE, CC, or CB configurations are simpler if the appropriate biasing scheme is selected. At low frequencies this may reduce part count. At RF and microwave frequencies, where the parasitics of certain components such as the emitter resistor are significant, bias scheme selection may be critical to circuit performance.

5.2 **Simple Feedback Biasing**

The schematic of this configuration is given in Figure 5-l. The base bias current for this circuit is derived from the collector voltage minus the base voltage [1]. An increase in transistor β which increases the collector current also reduces the collector voltage, therefore decreasing base bias current. This self-regulating action guarantees that the quiescent bias point is in the active region. For $\beta>1$ and V_{be} = 0.6 volt (silicon)

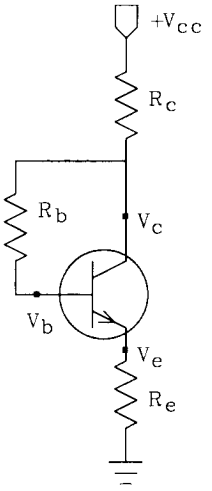

Figure 5-1 *Simple feedback biasing.*

$$R_c = \frac{V_{cc} - V_c}{I_c} \tag{5.1}$$

and

$$R_b = \beta \frac{V_c - 0.6 - I_c R_e}{I_c} \tag{5.2}$$

The transistor collector-emitter voltage is

$$V_{ce} = V_c - I_c R_e \tag{5.3}$$

This configuration may be used without R_e. This is particularly useful for very high frequency applications where emitter lead inductance is significant. When R_e is not used, the emitter is directly grounded.

R_e provides series feedback which flattens the amplifier frequency response and increases the CE input and output impedance. When used in conjunction with shunt feedback from the collector to the base, excellent control of the input impedance, output impedance, and flatness may be obtained [2].

5.3 One-Battery Biasing

The simple feedback bias network guarantees that biasing is in the active region. However, the bias point is a strong function of β. The bias point is more stable with the more complex one-battery bias [3] network shown in Figure 5-2. The equations below are used to establish the desired Ic and V_{ce}. For $\beta>1$, $I_c \sim I_e$. For best stability, because Vbe is a function of temperature, $V_e > V_{be}$. Ve is normally 10% to 20% of Vcc.

$$R_e = \frac{V_e}{I_c} \qquad 5.4$$

$$R_C = \frac{V_{cc} - V_{ce} - V_e}{I_c} \qquad 5.5$$

$$V_b = V_e + V_{be} \approx V_e + 0.6 \qquad 5.6$$

Selecting $I_{R2} = 10I_b = 10I_c/\beta$, we have

$$R_2 = \frac{\beta V_b}{10 I_c} \qquad 5.7$$

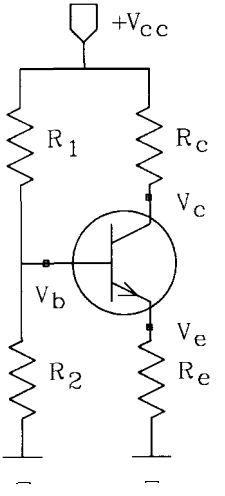

Figure 5-2 ***One-battery biasing.***

and

$$R_1 = \frac{\beta\,(V_{cc} - V_b)}{11 I_c} \qquad 5.8$$

The ***Re*** that results is generally greater than is desired for RF feedback use. R_e is therefore often bypassed with a capacitor. If a smaller effective RF value of R_e is desired, R_e is bypassed with a capacitor in' series with the desired resistance.

5.4 CC Negative Supply Biasing

The bias network shown in Figure 5-3 is an excellent choice when a common-collector configuration is required. It uses a negative supply for an NPN bipolar transistor. The collector is directly grounded, which is convenient for high-power applications. In the expressions below, voltages and currents are represented by their absolute values.

$$V_e = V_{ce} \qquad 5.9$$

$$R_e = \frac{V_{ee} - V_e}{I_e} \qquad 5.10$$

The base voltage is less negative than V_e by 0.6 volt for silicon.

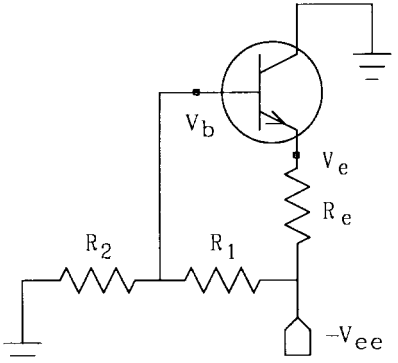

Figure 5-3 ***Negative supply common-collector biasing.***

$$Vb = Ve - 0.6 \tag{5.11}$$

If $I_{R2} = 10I_e/\beta$, then

$$R_2 = \frac{\beta V_b}{10I_e} \tag{5.12}$$

and

$$R_1 = \frac{\beta(V_{ee} - V_b)}{11I_e} \tag{5.13}$$

5.5 Dual Supply Biasing

This bias scheme, shown in Figure 5-4, uses only two resistors and is very stable. It is an excellent choice for grounded base configurations when both supply polarities are available. The base is grounded directly or through a small resistance. Assuming that $I_e \sim I_c$,

$$Vc = Vce - 0.6 \tag{5.14}$$

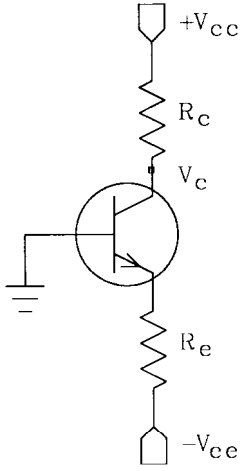

Figure 5-4 *Dual-supply biasing.*

$$R_e = \frac{V_{ee} - 0.6}{I_e} \quad 5.15$$

$$R_c = \frac{V_{cc} - V_c}{I_c} \quad 5.16$$

Except for high-power applications, Re tends to be large, which is consistent with typical common-base oscillator requirements. For high-power applications, a choke is placed in series with Re. Similarly, if a higher collector load resistance is required, a choke is placed in series with the collector resistance.

5.6 JFET Biasing

Junction field-effect transistor [4] device-to-device parameter variation is generally greater than for bipolar junction transistors. Some very simple JFET bias schemes exist which are suitable for many applications. With these schemes, active bias is guaranteed, but the device operating bias point may vary over a wide range from device to device. The supply polarities given are for n-channel JFETs. The supply polarity for p-channel devices is reversed. The following two bias networks for JFETs are depicted as common-source configurations.

5.7 Grounded Source

One simple scheme is to dc ground the gate and source. The drain current that flows is *Idss* and is somewhat independent of the drain-source voltage, when Vds is greater than V_p, the pinch-off voltage. V_p is generally a few volts. Idss in a typical RF JFET varies over an order of magnitude range from device to device. Device selection allows tighter specification of I_{dss}. I_{dss} decreases with increasing temperature. This simple bias scheme is shown in Figure 5-5.

$$I_d = I_{dss} \quad 5.17$$

$$V_d = V_{ds} = V_{dd} - I_d R_d \quad 5.18$$

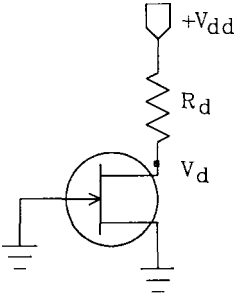

Figure 5-5 Grounded source biasing.

Since the gate current is nearly zero, the gate may be dc grounded through a large resistance to retain a high input impedance.

5.8 Self-Bias

The self-bias scheme shown in Figure 5-6 develops a negative gate-source voltage equal to the voltage dropped in the source resistor, Rs. Increasing source current develops greater negative gate-source bias which inhibits the increasing source current. This scheme therefore provides a degree of bias stabilization. The resulting drain current, Id, is less than Idss.

A desired V_{gs} is selected by examining the transfer characteristic curve, Id versus Vgs, or the output characteristic curves, Id versus Vgs, published or measured for the device. A formula relating Id to Idss, and V_{gs} and V_p is [5]

$$I_d = I_{dss}\left(\frac{1 - V_{gs}}{V_p}\right)^2 \qquad 5.19$$

Then

$$R_s = \frac{I_d}{V_{gs}} \qquad 5.20$$

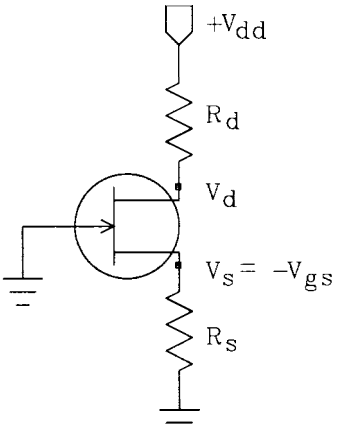

Figure 5-6 *JFET self-biasing.*

$$Rd = \frac{Vdd - Vds - Vs}{I_d} \qquad 5.21$$

Rs may be bypassed with a capacitor to increase the ac circuit gain. If necessary, an RF choke may be placed in series with Rd to increase the bias impedance loading the drain. Since the gate current is nearly zero, *Rg* may be large to retain a high input impedance, or an RF choke may be used.

5.9 Dual-gate FET

A typical bias network for a dual-gate FET is shown in Figure 5-7. The biasing strategy is similar to the self-bias JFET scheme except that two gates are biased and the self-bias developed in the source is supplemented with fixed applied bias to the gates. The design begins by selecting the desired gate l-to-source voltage, V_{g1s}, and the desired gate 2-to-source voltage, V_{g2s}. V_{g1s} and V_{g2s} are specified with the published RF parameter data for the device [6]. If $V_{g1}=V_{g2}$, then R_2 is replaced with a choke. If V_{g1} is negative with respect to V_{g2}, then V_{g1} and V_{g2} terminals are reversed for bias component connections.

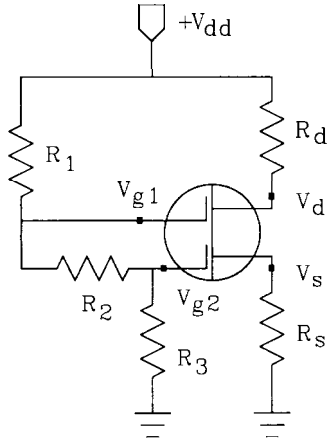

Figure 5-7 *Dual-gate FET biasing.*

V_{ds} and I_d are also selected based on the values used when measuring the published RF data. The following equations assume that Rs is 4 times Rd. This results in a large degree of bias stabilization. A typical value of R_3 is 33,000 ohms.

$$R_d = \frac{0.2(V_{dd} - V_{ds})}{I_d} \qquad 5.22$$

$$R_s = 4R_d \qquad 5.23$$

$$V_s = R_s I_d \qquad 5.24$$

$$V_{g1} = V_{g1s} + V_s \qquad 5.25$$

$$V_{g2} = V_{g2s} + V_s \qquad 5.26$$

$$R_2 = \frac{V_{g2}R_3}{V_{g1}} - R_3 \qquad 5.27$$

$$R_1 = \frac{V_d R_3}{V_{g1}} - \frac{V_{g2}R_3}{V_{g1}} \qquad 5.28$$

5.10 Active Bipolar Biasing

When a high level of bias stability is required, the bias network in Figure 5-8 may be used [7]. This network provides a high degree of bias stability even though the emitter is directly grounded. Direct grounding is an advantage for UHF and microwave applications.

Notice that Q_2 is a PNP transistor for a positive power supply The voltage drop across Ra is selected to be several times *Vbe,* 0.6 volt, so temperature variation of Vbe has minimal effect. V_{Ra} must be greater than *Vc* + 0.6 volt. Then

$$V_r = V_{cc} - V_{Ra} - 0.6 \tag{5.29}$$

$$R_a = \frac{V_{Ra}}{I_{\hat{e}}} \tag{5.30}$$

Assuming that the β of Q_2 > 10, we select $R_1 = 10Ra;$ then

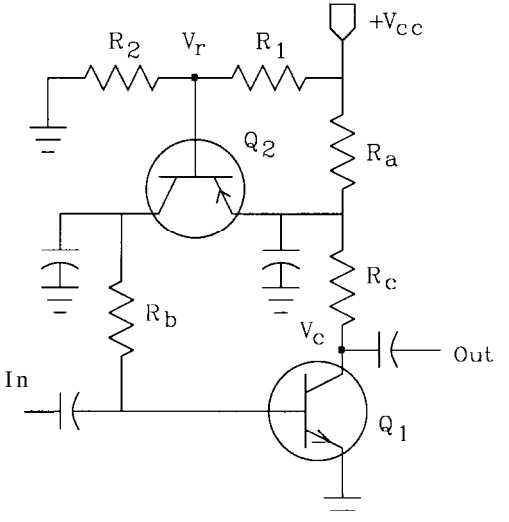

Figure 5-8 *Active bipolar biasing.*

$$R_2 = \frac{R_1 V_r}{V_{cc} - V_r} \qquad 5.31$$

$$R_c = \frac{V_r + 0.6 - V_c}{I_c} \qquad 5.32$$

Finally, R_b should be as large as possible, but

$$R_b < \frac{\beta(V_r - 0.6)}{I_c} \qquad 5.33$$

This condition must be met for the lowest β encountered with Q_1.

Extreme care must be used with bypass capacitor selection to ensure that the signal path loop formed by the oscillator and bias devices do not form a spurious low-frequency oscillator. The base of Q_2 should not be bypassed: otherwise, Q_2 may oscillate.

5.11 Hybrid Biasing

Commercially available hybrid and MMIC amplifiers generally have much of the biasing circuitry built in. Bias network design consists of selecting the appropriate output supply resistor and including a choke if the resistance is sufficiently low to load the output. Input and output coupling capacitors are often required to avoid shorting the internal bias voltages. The best practice is to consult the device data sheet for biasing requirements. When Vd and Id are specified, then

$$R_d = \frac{V_{cc} - V_d}{I_d} \qquad 5.34$$

where Vcc is the supply voltage. The dissipation in Rd is

$$P_{Rd} = I_d^2 R_d \qquad 5.35$$

If R_d is less than a few hundred ohms, an RF choke may be placed in series with R_d to reduce output loading.

5.12 References

[1] James F. Gibbons, *Semiconductor Electronics,* McGraw-Hill, New York, 1966, pp. 453-454.

[2] Wes Hayward and Doug DeMaw, *Solid State Design for the Radio Amateur,* American Radio Relay League, Newington, CT, 1977, pp. 188-190.

[3] Reference [1], pp. 448-449.

[4] FET Biasing, *FET Data Book,* Siliconix, 1986, pp. 7-12 to 7-19. Reprinted from *Electronic Design,* May 24, 1970.

[5] FETs in Balanced Mixers, Reference [4], pp. 7-55 to 7-64.

[6] *Motorola RF Device Data,* Motorola, 3rd ed., MRF966 N-Channel Dual-Gate GaAsFET Transistor, Motorola, Phoenix, AZ, pp. 6-2 to 6-11.

[7] Reference [2], p. 12.

6

Computer Techniques

Historically, the analysis of oscillator circuits involved the selection of a particular topology and then finding symbolic equations for that topology. Once the symbolic equations were found, evaluating which circuit element values satisfied the oscillation criteria required little computational effort. Abundant technical literature exists with symbolic equations for various oscillator structures. This technique was appropriate in a day when numeric tools were the slide rule and paper and pencil. Unfortunately, each time the engineer wishes to investigate a new oscillator topology the symbolic equations must be found. The symbolic approach is efficient for designing oscillators of one type but oppresses exploration of alternative and therefore perhaps more optimum structures.

The advent of economic numeric power in digital desktop computers offers another approach. This approach liberates the engineer by allowing rapid exploration of alternative designs and critical evaluation of new ideas before committed to hardware. The primary tool for this approach is the general purpose circuit simulator which frees the engineer from all numeric process tedium and which requires only a description of the proposed design to the simulator. This description may be modified as easily as editing a short file or editing a schematic. Element values are tuned or even optimized while the user observes circuit responses on the computer display in real-time.

This simulation approach is essentially topology independent and the procedure is identical regardless of the specific resonator technology or the type of active device used. Therefor the approach is equally applicable for quartz-crystal oscillators using

bipolar transistors or transmission-line oscillators using a GaAs-FET transistor. Two fundamentally different analysis criteria are used for all oscillator types as introduced in Chapter 2. Open-loop gain/phase Bode response analysis is used primarily for high-stability oscillators. Negative-resistance analysis is used for broad bandwidth VCOs. The use of computers for both analysis criteria are introduced and illustrated in this chapter. Additional oscillator case studies are then considered using these techniques in the following chapters.

6.1 Oscillator Simulation

We will use three different computer programs. The first is a high-speed real-time frequency-domain linear circuit simulator, =SuperStar= Professional, from Eagleware Corporation [1]. This simulator uses a number of unique techniques and algorithms such as node elimination, element classes and output classes to achieve extreme execution speed [2]. Other popular linear simulators may be used to perform the analysis described in the remainder of this book except execution is much slower.

Ideally the oscillator is designed, a prototype is constructed which confirms all specifications are achieved, and production is begun. In practice this rarely happens at RF frequencies. Necessary design simplifications, component tolerance and parasitics, dissipation, distributed element discontinuities, package modes, radiation and measurement error all result in discrepancies between the desired and measured responses. Prior to the advent of digital computer simulation, the prototype was tweaked and rebuilt until the desired performance was achieved. Computer simulation with a program such as =SuperStar= Professional allows quick design verification. Many perturbing effects may be corrected before the prototype is constructed, saving substantial time and cost.

6.2 Simple Resonator Example

Consider the simple shunt-C coupled series resonator shown in Figure 6-l. The shunt-coupling capacitors are 47 pF and the series-resonator capacitor is 2 pF. An unloaded Q of 1000 is used for all capacitors. The resonator inductor is 1340 nH with an unloaded Q of 120. This resonator circuit is described to the =SuperStar= Professional simulator by simply drawing a schematic using the Eagleware program =SCHEMAX= [1], which was also used to generate Figure 6-1. Alternatively the circuit may be described by using the text editor built into =SuperStar= Professional to enter the text net list shown in Table 6-l. The CIRCUIT block in the net list is used to specify element models, provide element values and connect elements between user selected node numbers. In this example the ground node is zero, the input is node 1 and the output is node 3. The line

IND 12 L=?1340 Q=?120

specifies a 1340 nH inductor with an unloaded Q of 120, and is connected between nodes 1 and 2. The "?" in front of certain element values indicates these values are available for tuning or optimization. The DEF2P statement in the CIRCUIT block defines a two-port for display with 1 as the input node and 3 as the output node. In this case we have given the two-port the name RESONATE.

The WINDOW block specifies the two-port which is to be displayed, how that two-port is terminated and what response data

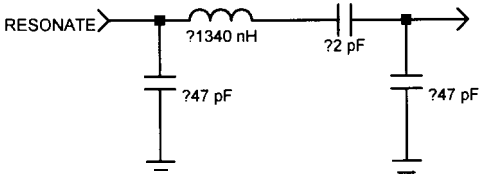

Figure 6-l *Simple circuit example of a shunt-C coupled series resonator.*

Table 6-l *=SuperStar= circuit file for the simple shunt-C coupled resonator*

```
CIRCUIT
CAP 1 0 C=?47 Q=?1OOO
IND 1 2 L=?1340 Q=?120
CAP 2 3 C=?2  Q=?I 000
CAP 3 0 C=?47 Q=? 1000
DEF2P 1 3 RESONATE
WINDOW
RESONATE(50,50)
GPH S21 -20 0
GPH P21 -225 225
SMH S11
FREQ
SWP 90 110 101
MARKER 95 100 105 11095 100 105 110
```

to display The first line after the WINDOW block title specifies this Window should display the responses of circuit RESONATE terminated at the input and output in 50 ohms. GPH specifies a rectangular grid with a linear frequency scale. SMH specifies a Smith chart grid. S21 on the GPH line requests a plot of the S-parameter forward transmission coefficient magnitude on the rectangular grid with a decibel vertical scale. The numbers -20 and zero specify the vertical axis scale minimum is -20 dB and the maximum value is zero dB. P21 requests a plot of the phase of the forward S-parameter from -225 to 225 degrees (45 degrees per division). S11 on the SMH line requests a plot of the input S-parameter reflection coefficient on the Smith chart grid. If the resonator circuit is described by drawing a schematic in =SCHEMAX= this same WINDOW block is entered in a text section of the =SCHEMAX= program. The FREQ section of the WINDOW block specifies the type of frequency sweep, the sweep range and the number analysis frequencies. SWP 90 110 101 specifies a sweep from 90 to 110 MHz with 101 points which is every 200 KHz. The MARKER section of the WINDOW block specifies the initial frequencies for markers on the responses. If the resonator circuit is described by drawing a schematic in =SCHEMAX= this same WINDOW block is entered in a text

section of the =SCHEMAX= program. Appendix A summarizes =SuperStar= codes for models and commands used in oscillator circuit files listed in the remainder of this book.

When the user exits the test or schematic editor, =SuperStar= Professional translates this description and then computes and displays the requested responses as shown in Figure 6-2. The solid traces are responses with the initial element values. The dashed responses are with tuned or optimized elements values as displayed on a row near the bottom of the screen. These element values are tuned by simply tapping on the up and down arrow keys. The left and right arrow keys select the value to tune. Alternatively an element value may be selected and a specific value typed from the keyboard.

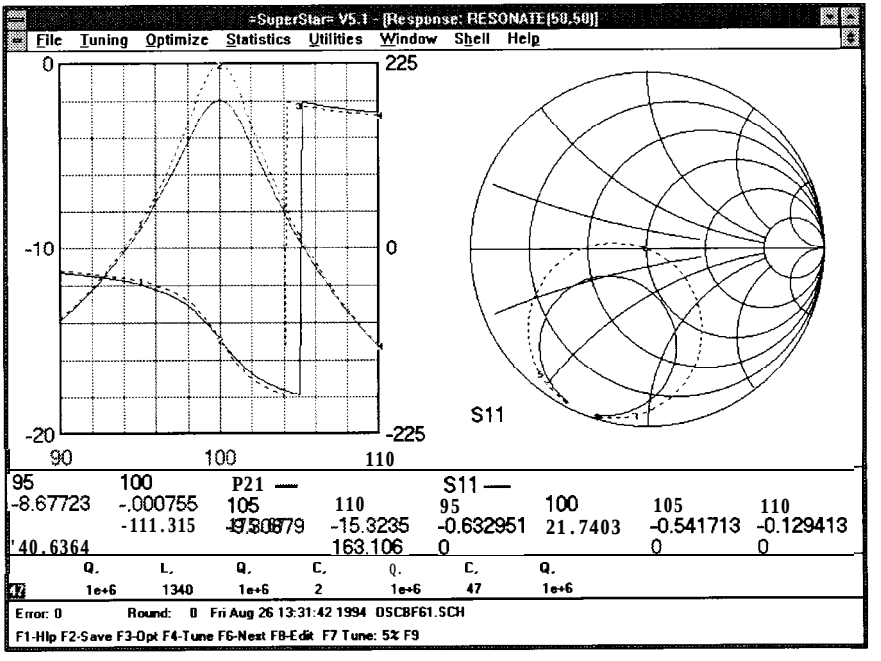

Figure 6-2 *Computed responses of the simple shunt-C coupled resonator with finite Q components (solid) and infinite Q components (dashed).*

Markers provide digital read-out of the specified output parameters near the bottom of the screen. The markers track with the dashed responses and the digital values update as element values are tuned. The markers are tuned to desired frequencies by clicking on the desired marker frequency read-out and tapping the up and down arrow keys. As the arrow keys are tapped the selected marker frequency steps through each frequency sweep point specified in the FREQ block.

The dashed responses in Figure 6-2 are with the unloaded Q of all elements tuned very high, 1 million. Marker number 3 at 100 MHz is near the resonant frequency where the resonant frequency is defined as maximum transmission or minimum reflection. Notice with high unloaded Q the insertion loss is nearly zero and the input impedance is near the center of the Smith chart and is thus 50 + j0. How can a purely reactive resonator have a purely resistive input impedance? Basically, resonator inductive and capacitance reactance cancel and the load termination resistance is presented to the input. A simple calculation reveals that the resonant frequency of the 1340 nH inductor and 2 pF series capacitor is 97.2 MHz. Since resonance is near 100 MHz it is clear the coupling capacitors effect the resonant frequency

The transmission phase shift at resonance is approximately -11 1^{o}. As the shunt coupling capacitors are reduced the resonator loaded Q is reduced, the insertion loss is reduced for a given component unloaded Q and the phase shift approaches zero-degrees. Minimum loaded Q occurs with the coupling capacitors removed and is equal to the series inductive or capacitive reactance divided by the sum of the termination resistance. As the coupling capacitor values are increased the resonator loaded Q increases, the insertion loss increases and the transmission phase shift approaches -180^{o}.

Notice from the solid traces, that with finite element unloaded Q, the input impedance is not 50 ohms at the resonant frequency It is not purely resistive at any frequency but the resistive component of the impedance is always less than 50 ohms. Finite inductor Q may be modeled as series resistance. With resistance in series with the inductor, it is reasonable to expect the input

resistance might increase. In fact, transformation properties of this resonator circuit result in a decrease in the input resistance with finite unloaded Q. Simulators allow us to tune element values for this and other resonators to obtain immediate visual feedback of circuit behavior. This simple circuit is unintuitive, imagine the importance of simulation for more complex circuits.

6.3 Oscillator Synthesis

The second program we will use is =OSCILLATOR= [1] which has two functions; to assist with creating an initial oscillator circuit and to estimate the oscillator phase noise performance. =OSCILLATOR= creates 16 different L-C, transmission line, SAW and quartz crystal oscillators. These oscillators are outlined in Appendix B. Once an oscillator type is selected, =OSCILLATOR= finds RF and bias element values, displays a schematic of the proposed oscillator and write a =SuperStar= text or =SCHEMAX= file. Then, =SuperStar= is used to display oscillator responses and tune or optimize element values. At this point the user may change not only the element values but also the topology if desired.

6.3.1 Synthesis Example

Given in Figure 6-3 is the main =OSCILLATOR= screen for one of the 16 types, a shunt-C coupled resonator with an MMIC amplifier. The desired maximum and minimum operating frequencies are entered at the upper left. The desired operating voltage and current for the active device and the supply voltage are entered at the lower left.

The device is characterized by S-parameter data stored in a standard ASCII file. The name of the file with the S-parameter data is also entered at the lower left. The selected device is a Mini-Circuits MAR3 biased at 5 volts and 35 mA. S-parameter data provided by the manufacturer is given in Table 6-2. The line

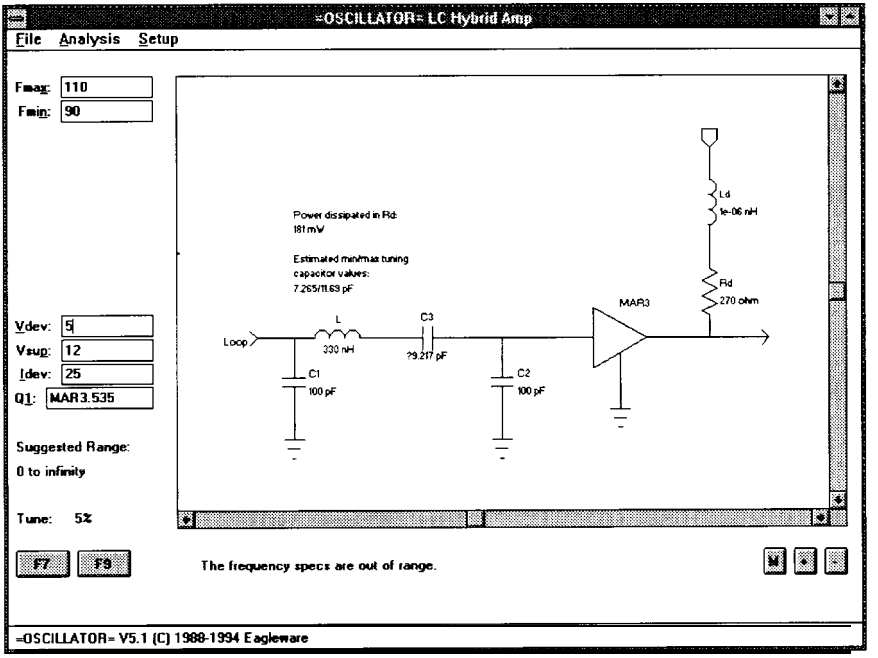

Figure 6-3 *=OSCILLATOR= program screen for a 100 MHz shunt-C coupled resonator oscillator using a Mini-Circuits MMIC amplifier.*

Table 6-2 *S-parameter data file format. This data is for a Mini-Circuits MAR3 MMIC amplifier*

```
#MHZ
!          S11          S21          S12          S22
!FREQ    MAG   ANG    MAG   ANG    MAG   ANG    MAG   ANG
 100     .07   172   4.47   174    .12     1    .15   -11
 500     .06   156   4.37   152    .12     5    .16   -45
1000     .05   146   4.22   128    .13    10    .18   -88
1500     .04   172   3.89   103    .14    12    .21  -120
2000     .06   173   3.35    83    .18    11    .25  -142
2500     .17   175   3.27    59    .19     5    .26  -173
3000     .24   157   2.85    38    .20     0    .25   168
3500     .32   140   2.45    21    .21    -6    .25   152
4000     .39   124   2.11     3    .22   -14    .25   138
```

MHZ specifies megahertz as the units of the frequency in the first column. The lines beginning with "!" are comment lines used to identify the data following the frequency which are the magnitude and angle of the polar S-parameters normalized to typically 50 ohms.

The resonator designed by =OSCILLATOR= uses a smaller L-C ratio and larger coupling capacitors than the previous shunt-C coupled resonator. The supply resistor, Rd, is sufficiently large that a decoupling inductor is not required, therefor ***Ld*** is a null component. Once =OSCILLATOR= finds appropriate element values and displays a schematic on screen it writes a text circuit file or schematic for the =SuperStar= simulator.

6.3.2 Analysis of the Example

The simulator text circuit file written by =OSCILLATOR= is given in Table 6-3. We chose to couple power out at the output of the MAR3 MMIC amplifier. Therefore a 100 pF capacitor and a 50 ohm resistor are manually added to the circuit file (nodes 5 and 6) to simulate coupling power to a 50 ohm load. The unloaded Q of the resonator inductor is 90.

The transmission gain (S21) and phase and input and output S-parameters as computed and displayed by =SuperStar= are given as the solid traces in Figure 6-4. There is ample loop gain and S11 andS22 are relatively well matched. However the phase zero crossing is approximately 0.6 MHz low and the phase zero crossing is slightly off the maximum phase slope.

6.3.3 Optimization of the Example

An OPT optimization section was added to the circuit file as shown at the bottom of Table 6-3. The desired optimization frequency of 100 MHz is bracketed by specifying 99.9 to 100.1 MHz. The optimization goals are an open loop gain, S21, of at least 6 dB, loop phase equal to zero, and matches of 16 dB return loss or better. In Chapter 2 we discovered unloaded Q is propor-

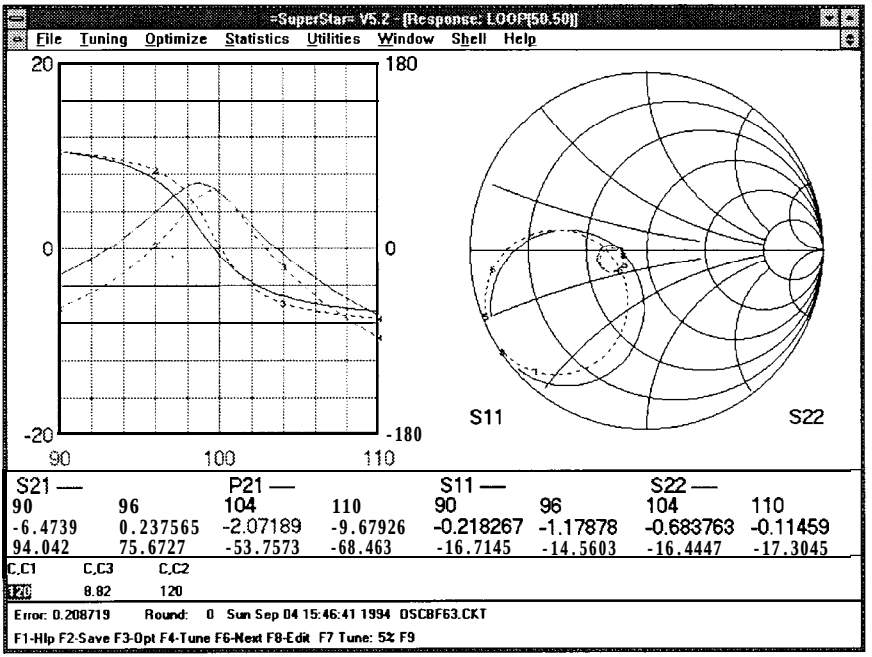

Figure 6-4 Computed responses of the MMIC oscillator as designed by =OSCILLATOR= (solid) and after optimization in =SuperStar= (dashed) to improve the loaded Q.

tional to group-delay Although not displayed in Figure 6-4, the initial group delay of this cascade is approximately 50 nS. To improve the loaded Q the group-delay optimization goal is specified as at least 100 nS. The shunt coupling capacitors and series resonator capacitor are selected as optimizable elements.

The open-loop responses after optimization are given as the dashed traces in Figure 6-4 and the optimized element values are given near the bottom of the screen. After optimization the shunt coupling capacitors were adjusted to the nearest standard values and the series resonator capacitor was adjusted to maintain the phase zero crossing at 100 MHz. Notice the shunt capacitors increased which increased the phase slope and placed the zero crossing closer to the maximum phase slope.

Table 6-3 *Simulator circuit file for the MMIC oscillator. The OPTIMIZATION section of the WINDOW block has been manually added*

```
CIRCUIT
CAP 1 0 C=?lOO Q=1000 'Cl
CAP 2 3 C=?9.217 Q=lOOO 'C3
CAP 3 0 C=?lOO Q=lOOO 'C2
IND 1 2 L=330 Q=120 'L
IND 0 4 L=l e-06 Q=l e+06 'Ld
TWO 3 5 0 O=SP Z=50 F=MAR3.535 'MAR3
RES 4 5 R=270 'Rd
CAP 5 6 C=lOO
RES 6 0 R=50
DEF2P 1 5 Loop
WINDOW
Loop(50,50)
GPH S21 -20 20
GPH P21 -180 180
SMH S11
SMH S22
FREQ
SWP 90 110 101
OPT
99.9 100.1 S21>6 P21=0 S1 1 <-16 S22<-16 DLY>lOO
```

6.3.4 Noise Performance of the Example

The phase slope of the optimized oscillator open-loop response displayed in Figure 6-4 is approximately 36^{o} per megahertz. From the equations for loaded Q in Chapter 2, the loaded Q is found to be approximately 31.4. This is higher than the loaded Q of typical L-C oscillators found in the literature and provides good phase noise performance. At this point, we leave the analysis program =SuperStar=, and the noise estimation routine in =OSCILLATOR= is used to compute and display the SSB noise performance given in Figure 6-5. The SSB phase noise is outstanding for an L-C oscillator; -100 dBc/Hz at 1 KHz offset. The equations used to estimate the noise performance are given in Chapter 4.

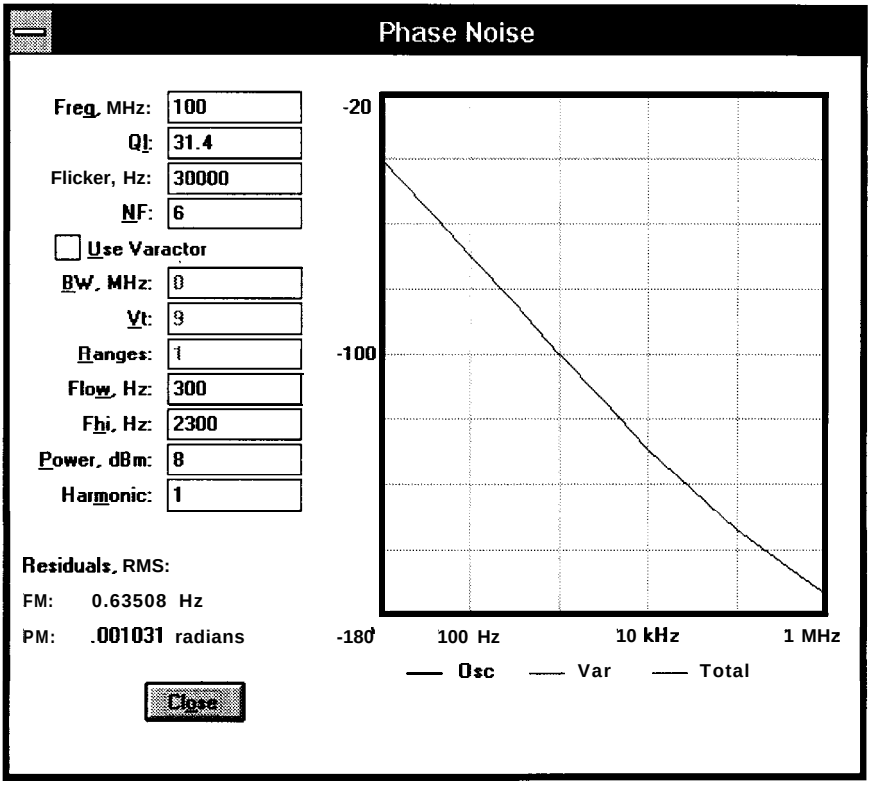

Figure 6-5 *=OSCILLATOR= program noise analysis screen with input data on the left and estimated SSB phase-noise graphed on the right.*

Important parameters are entered on the left of the noise analysis screen of =OSCILLATOR= as shown in Figure 6-5. The loaded Q from the =SuperStar= analysis is 31.4. The device flicker corner is estimated to be 30 KHz. The circuit noise figure is 6 dB. The varactor box is not checked, indicating that a varactor is not used to tune the frequency When a varatctor is used two additional traces appear on the noise analysis screen; one with varactor modulation noise and a third with the power sum of the oscillator and varactor modulation noise. The oscillator output power of 8 dBm is entered at the end of the input list.

Flow and Fhi entered near the end of the input list are the lower and upper baseband frequencies of interest in hertz, in this case 300 to 2300 Hz. =OSCILLATOR= integrates the SSB phase noise over this offset frequency range to predict the residual RMS FM and PM noise at 0.635 Hz and 0.00103 radians, respectively

Why do typical VCOs not achieve this phase-noise performance? To understand why we will use a third computer program.

6.4 SPICE Analysis of Oscillators

At this point we have used =OSCILLATOR= to create a 100 MHz L-C oscillator and used =SuperStar= to perform an open-loop analysis of oscillation criteria, the oscillation frequency, the loop cascade noise figure and the oscillator loaded Q. We used these parameters to estimate the phase-noise performance. Next we will use SPICE analysis to study oscillator starting, output level, harmonic content, and verify the oscillation frequency for steady-state operation in full limiting.

Table 6-4 *IsSpice 4 simulator net-list for the MMIC oscillator*

```
LOOP OSCILLATOR
*INCLUDE HPRF.LIB
CI 10 12OP
LI 1 2 330N
RQ 2 6 2.3
C2 6 3 8.82P
C3 3 0 120P
R1 1 4 270
C4 1 5 100P
R2 5 0 50
VSUP 4 0 12
XI 1 3 0 MSA0386
.TRAN .1N 1000N UIC
.FOUR 1 00meg V(5)
.PRINT TRAN V(5)
.PLOT TRAN V(5)
.end
```

The SPICE program we will use is IsSpice4 from Intusoft [3]. The circuit is still as shown in Figure 6-3 with the output of the cascade connected back to the input (node 1). Output is taken by connecting a 50 ohm termination to node 1 through a 100 pF coupling capacitor. The IsSpice4 net list is given in Table 6-4 which describes the circuit and specifies a transient analysis. RQ is a 2.3 ohm resistor to model the unloaded Q of the inductor as 90 at 100 MHz. The Mini-Circuits MAR3 MMIC amplifier is modeled using the HP MSA0386 SPICE model in the Intusoft RF library HPRF.LIB.

An Intusoft Scope program display of the voltage at node 5 across the 50 ohm termination is given in Figure 6-6. The sudden 1 volt

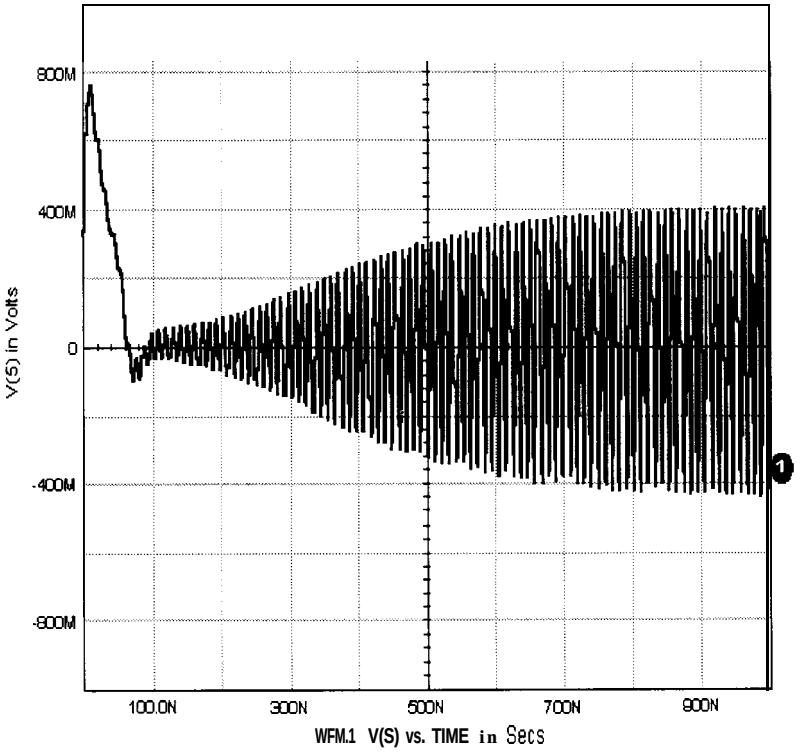

Figure 6-6 *IsSpice4 predicted oscillator starting waveform across the output* ***50*** *ohm load.*

rise in voltage just after t=O is due to start-up biasing transients. After approximately 50 nS, the circuit approaches the quiescent bias point and oscillation begins to build. In approximately 400 nS the level has reach 63% of the final value of 800 mV peak-to-peak. Full limiting and steady-state is reached in approximately 1 uS. Since the RMS voltage of a sinusoidal 800 mVp-p signal is 283 mV, the power delivered to the 50 ohm load is approximately 1.6 mW or 2.1 dBm.

Examination and interpolation of raw IsSpice4 data of the output voltage finds the period (voltage zero crossing to zero crossing) is 10.3 nS which corresponds to a frequency of 97 MHz. An IsSpice4 Fourier analysis of the output waveform predicts the 2nd, 3rd and 4th harmonics are -19.2, -44.7 and -45.4 dBc respectively

6.5 Loaded Q Limitation

Earlier we eluded to the fact that this circuit which has a high loaded Q is not usable as a broad tuning VCO. Analysis so far has still not revealed the reason. Shown in Figure 6-7 is an IsSpice4 analysis of the voltage at node 6, the connection of the resonator capacitor and inductor. The voltage at node 6 is over 10 Vp-p! This high voltage is the result of the transforming effect of the high loaded Q. The voltage at node 3, the input to the MAR3 amplifier, is very low in relation to the resonator voltage. Therefore most of the 10 volts appears across the resonator capacitor. Extreme care must be exercised in designing the tuning network so that the tuning varactor can deal with the high resonator voltage. Back-to-back tuning varactors are often used so when the voltage swing drive one varactor into forward conduction the opposite varactor is reversed biased. Using an amplifier with an input and output impedance lower than 50 ohms helps keep the resonator voltage lower, but element values and parasitics become a problem. This is a fundamental limitation of varactor tuned high-Q oscillators.

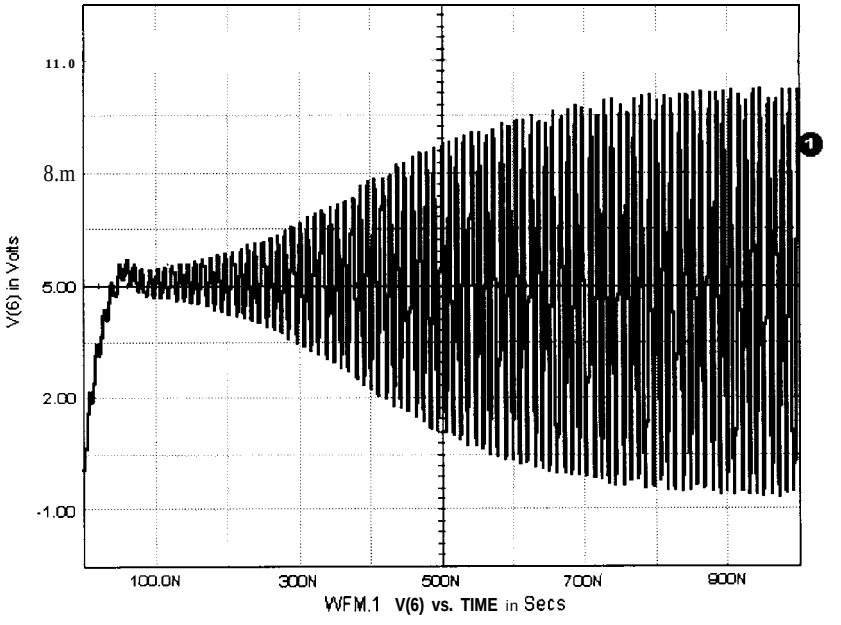

Figure 6-7 *IsSpice4 predicted waveform within the resonator.*

6.6 100 MHz Loop Oscillator Measured Data

The output spectrum of a prototype of this oscillator displayed using a Hewlett Packard HP8560E spectrum analyzer is given in Figure 6-8. The frequency span is 100 KHz (10 KHz/division) and the IF bandwidth (resolution bandwidth) is 1 KHz. The width of the carrier is the response of the analyzer IF filter and does not represent the character of the spectrum. Also, at the displayed offset frequencies the noise floor (above 20 KHz offset) is the noise performance of the analyzer and not the oscillator.

The oscillation frequency predicted by =SuperStar= and IsSpice4 are within 3 MHz of each other. The tolerance of the components used in the prototype are not nearly this tight and a prototype

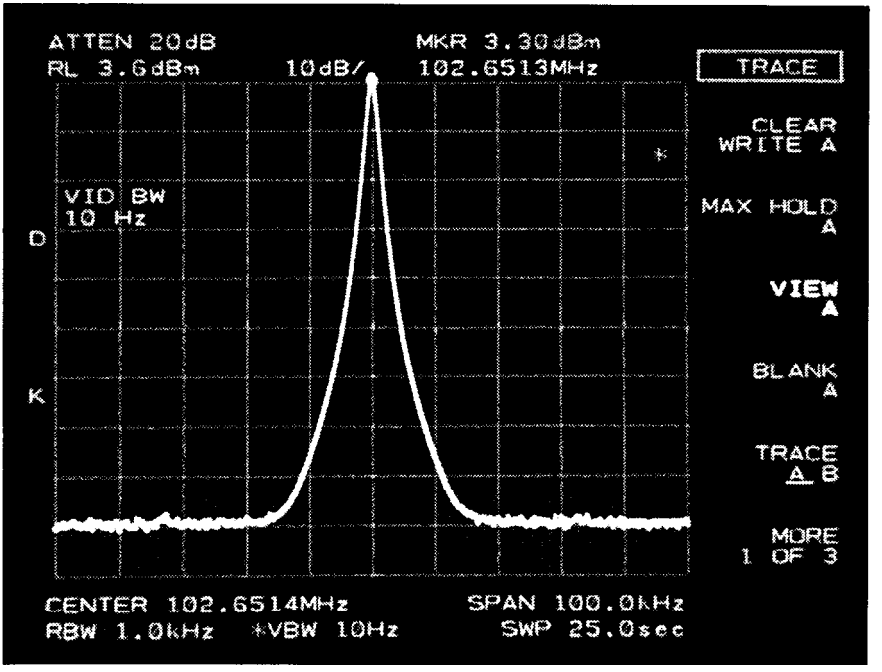

Figure 6-8 *Output spectrum of the 100 MHz oscillator for offsets to 50 KHz (5 KHz per division).*

oscillation frequency of 103.3 MHz (3.3% too high) is not unexpected.

The 3.3 dBm output level as measured by the spectrum analyzer is approximately 1.2 dB higher than the IsSpice4 predicted value of 2.1 dBm. The difference is less than the specified amplitude accuracy of the analyzer. The 2nd harmonic is -18 dBc, the 3rd is -42 dBc and the 4th is -43 dBc. These values are amazingly close to the predicted values.

The spectrum to 2.5 KHz offset is shown in Figure 6-9. The HP8560E IF bandwidth is 30 Hz which requires a correction factor of 10 log 30 = 15 dB. The analyzer IF filter noise bandwidth and detector characteristics require an additional correction factor of 2.5 dB. The displayed noise at 1 KHz offset (2 divisions)

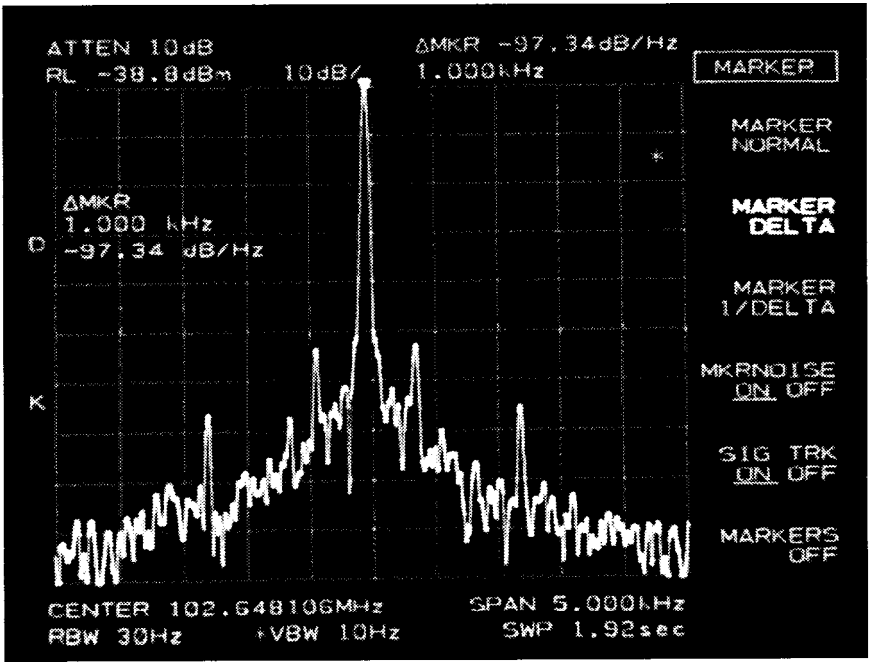

Figure 6-9 *Output spectrum of the 100 MHz oscillator for offsets to 2.5 KHz (500 Hz per division).*

after smoothing is approximately 85 dB. This value plus 15 dB minus 2.5 dB is 97.5 dBc/Hz, close to the -100 dBc/Hz predicted by =OSCILLATOR=. The marker at 1 KHz offset is set to read noise and the displayed value of -97.34 dBc/Hz is automatically corrected for analyzer bandwidth and detector characteristics.

6.7 Negative-Resistance Oscillator Computer Analysis

Negative resistance oscillator analysis was introduced in Chapter 2. We will investigate computer analysis techniques for these oscillators in this section. Recall from Chapter 2 that a bipolar common collector transistors may provide at its base negative resistance in series with capacitance. Since the capacitive reac-

tance may be relatively large it can significantly reduce VCO tuning range. The ideal transistor for a negative resistance VCO has a constant resistance versus frequency and a small capacitive reactance. Before beginning the design of the VCO it is appropriate to investigate the transistor in isolation.

6.7.1 Analysis Fundamentals

Consider the common-collector configuration shown in Figure 2-21. Shown on the left graph in Figure 6-10 is the display from =SuperStar= of the input reflection coefficient magnitude swept from 500 to 1000 MHz with a 50 ohm reference impedance. The lower, slightly lighter, trace is the magnitude, C_{11}, with the left vertical scale and the upper trace is the angle, P_{11}, with the right vertical scale. The transistor is a Motorola MRF559 biased at 5 volts Vce and 25 mA I_c. The emitter resistance is 270 ohms and

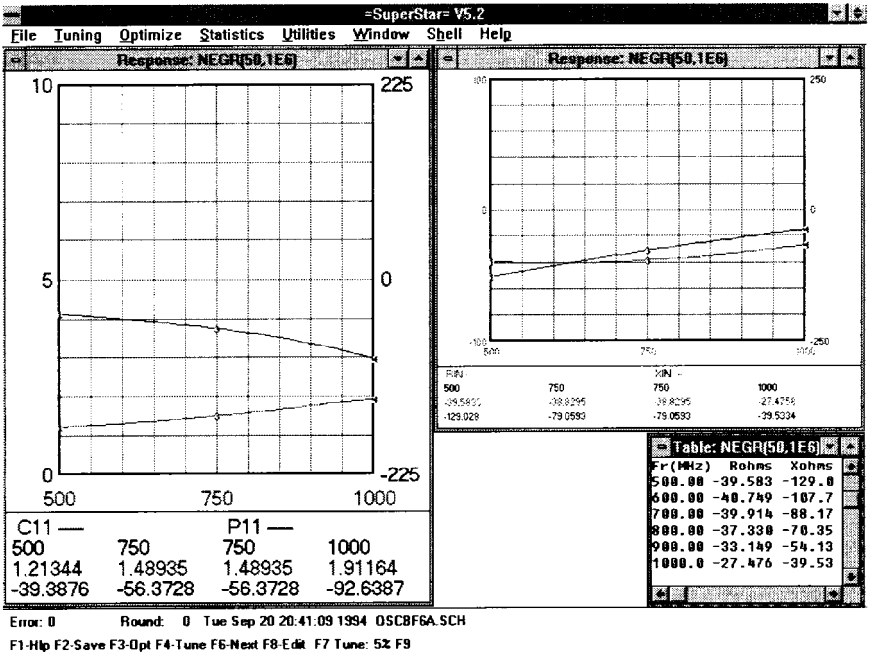

Figure 6-10 *=SuperStar= analysis of negative resistance transistor input characteristics.*

the emitter capacitance is 3.3 pF. The 270 ohm resistor is for biasing and the function of the 3.3 pF capacitor is described later.

The reflection coefficient increases from 1.21 at 500 MHz to 1.91 at 1000 MHz (notice the markers at the bottom of the graph.) The fact that the input reflection coefficient is greater than 1 indicates an incident wave is scattered back at greater amplitude than incident, the characteristic of a negative resistance. The angle ranges from -39.4' at 500 MHz to -92.6' at 1000 MHz.

Shown on the upper right in Figure 6-10 is the same input data displayed as Rin and Xin, the series resistance and reactance. This same data is also displayed in tabular form on the lower right. The negative resistance is relatively constant, from -27 to -41 ohms. The reactance is -129.8 ohms at 500 MHz, corresponding to a series capacitance of 2.45 pF, and -39.5 at 1000 MHz, corresponding to 4.0 pF.

Again referring to Figure 2-21, if the external tuning varactor is 2.45 pF, the effective series capacitance would be only 1.225 pF, resulting in a frequency 1.414 times higher than expected. One solution is to use very small tuning capacitance. This also increases the oscillator loaded Q. Unfortunately with small varactor capacitance, package and PWB parasitics limit the minimum capacitance which also decreases the tuning range. Therefore, device selection begs for large effective input capacitance.

6.7.2 Device Selection

Shown in Figure 6-11 are Rin and Xin. for four different bipolar transistors with grounded collectors, emitter resistance of 270 ohms and no emitter capacitance. The slightly lighter traces are the resistances with a vertical scale of -50 to 50 ohms. The reactances are plotted with a vertical scale of -500 to 500 ohms. On the upper left is a 2N3866 biased at 14 volts at 80 mA. On the upper right is a MRF559 biased at 5 volts and 25 mA (S-parameters from Motorola). On the lower left is an MRF901 biased at 6 volts and 15 mA (S-parameters from Motorola) and

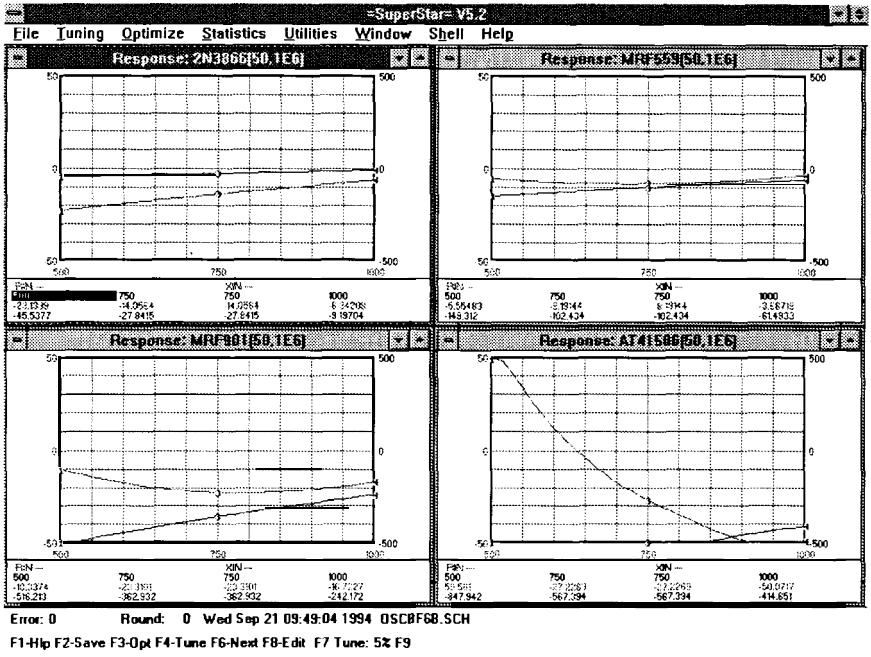

Figure 6-11 *Input resistance and reactance of four bipolar transistors in common-collector configuration. The transistor types are listed in the title bar of each graph.*

on the lower right is a Hewlett-Packard/Avantek AT41586 biased at 8 volts and 25 mA.

The resistances are relatively constant for the 2N3866, MRF559 and MRF901 transistors but not very negative for the MRF559. Below 650 MHz the resistance actually goes positive for the AT41586. The reactances at 500 MHz are -45 ohms, -149 ohms, -516 ohms and -948 ohms respectively for the 2N3866, MRF559, MRF901 and AT41586 transistors. The effective input capacitances are therefore 7.1 pF, 2.1 pF, 0.62 pF and 0.34 pF, respectively The lower capacitance values would severely restrict VCO tuning range.

The inescapable conclusion is that "higher performance" transistors with higher Ft and gain are the least suitable for negative resistance oscillators! This is clearly contrary to selection criteria for oscillators which use open-loop theory for design. This is because negative-resistance oscillators depend on internal feedback mechanisms to develop the negative resistance. These mechanisms rely on junction capacitance to provide this feedback. Older devices and devices designed for higher power typically have larger junctions and therefore junction capacitance.

The following common-emitter S-parameter criteria are helpful in selecting an active device for use in negative resistance oscillators, listed in order of importance.

(a) At low frequencies the common-emitter phase shift of bipolar transistors approaches 180'. However, for negative resistance oscillator devices, the angle of S_{21} at the lowest operating frequency should be 90^{o} or less.

(b) The magnitude of S_{21} should be as high as possible.

(c) The magnitude of S_{12} should be large as possible.

Higher F_t devices have a more ideal phase shift (closer to 180^{o}) which is inconsistent with requirement (a). This is why the AT41586 transistor has positive input resistance below 650 MHz even though it has higher S_{21} magnitude than the other devices.

In the next section we investigate the use of external components to make a given device more suitable for negative resistance oscillators.

6.7.3 Circuit Enhancements

Shown in Figure 6-12 are the input resistance and reactance for the AT41586 transistor with external capacitors. On the left is with 10 pF of capacitance to ground at the emitter. On the right is with 10 pF on the emitter and 2.2 pF to ground at the base. With just emitter capacitance, the input resistance ranges from -292 ohms to -90.8 ohms (lower trace) and the reactance ranges from -299 ohms to -30.8 ohms (upper trace). Notice the vertical

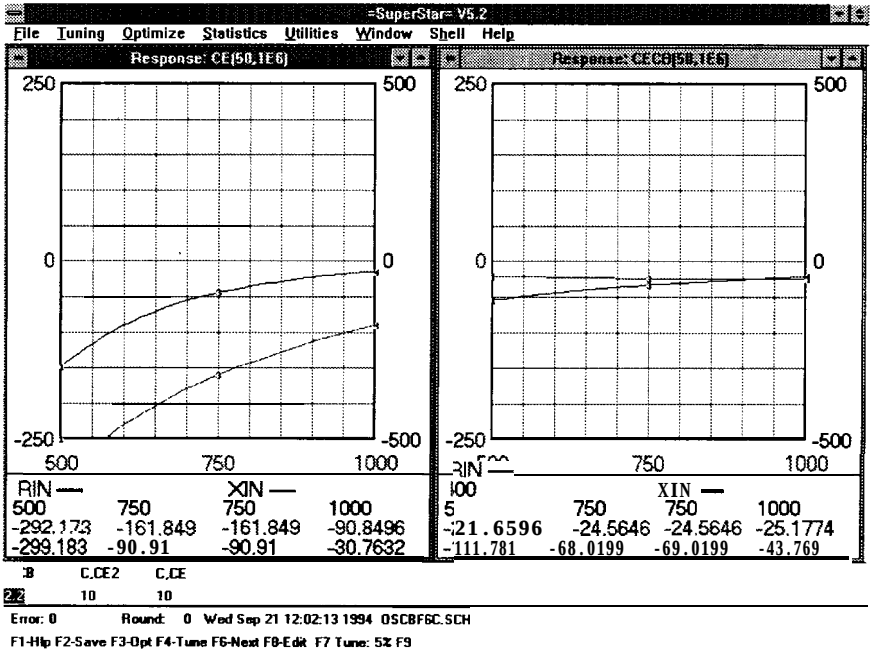

Figure 6-12 *Input resistance and reactance for the AT41586 transistor with* ***10 pF*** *emitter capacitance (left) and* ***10 pF*** *emitter capacitance and 2.2* ***pF*** *base capacitance.*

scales are changed from the previous figure. While the resistance is extremely negative across the band, at 500 MHz the -299 ohms reactance is only 1.06 **pF**. However, recall with no emitter capacitance the AT41586 input resistance is positive below 650 MHz and the capacitance is only 0.34 **pF**. Thus the emitter capacitor is absolutely necessary for oscillation below 650 MHz and also increases the effective series capacitance. The emitter capacitor is critical to negative resistance oscillator performance, particularly so for higher F_t devices. Design of these oscillators should always begin with review of the appropriate value for C_e. For a given device, higher C_e is generally required at lower frequencies. At still lower frequencies, a typical device becomes "too ideal" and

no value of C_e is incapable of producing negative resistance, at which point a lower F_t device should be selected.

On the right in Figure 6-12, 2.2 pF to ground at the base is included in addition to the 10 pF emitter capacitance. This shunt capacitance at the input has the effect of transforming down the magnitude of both the resistance and reactance. The negative resistance now ranges from -21.7 ohms to -25.1 ohms. The reactance at 500 MHz is reduced to -111.8 ohms with increases the input series capacitance to 2.85 pF from 1.06 pF. The shunt input capacitor is another tool for increasing the series capacitance, but can only be employed if the magnitude of the negative resistance is large.

In effect, external capacitance at the emitter and base causes a high F_t device to behave similarly to a less expense, low F_t device. However, use of external elements has the advantage of making oscillator performance less dependent on parasitics of the active device which improves temperature stability and manufacturing repeatability It is important to avoid and characterize the effects of lead and path inductance to ground for these external capacitors.

6.8 Broad Tuning UHF VCO Example

Shown in Figure 6-13 is the schematic of a complete negative resistance VCO. The power supply is assumed to be bypassed. Output power is taken at the collector so instead of directly grounding the collector at the supply, a 50 ohm resistor is used to develop output voltage. When a 50 ohm load is connected to the collector through the 100 pF coupling capacitor, the collector effectively "sees" about 25 ohms to ground at RF. This does effect the base R_{in} and X_{in} slightly and could have been included in the previous device analysis.

For biasing, the 50 ohm resistor drops only about a volt. The collector voltage is divided by the two 2700 ohm resistors to provide approximately 7 volts at the base. The additional drop of 0.65 volts across the base-emitter junction results in 6.35 volts at

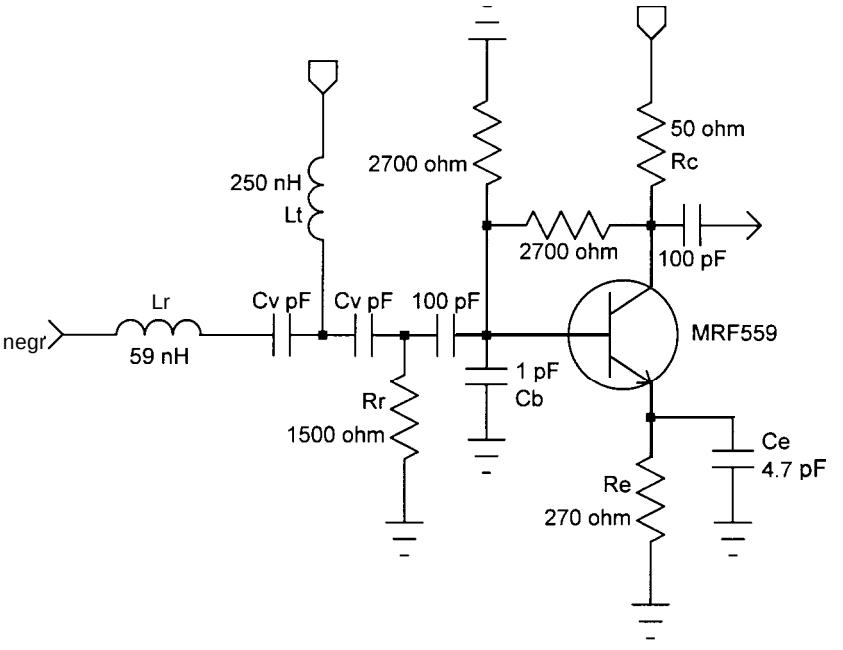

Figure 6-13 *Schematic of UHF VCO with biasing and resonator elements.*

the emitter which develops approximately 24 mA emitter and collector current.

An emitter capacitance of 4.7 pF is added and the base capacitance of 1 pF is actually PWB pad capacitance. The series 100 pF capacitance at the base decouples the base bias voltage from the varactor circuitry. The 1500 ohm resistor returns the right side of the right varactor to ground potential. While the oscillator is analyzed by looking through the resonator, the actual oscillator is constructed with the left side of the resonator inductor directly grounded. This returns the left side of the left varactor to ground potential. The back to back varactors are tuned via the 250 nH bypass inductor. Shown in Figure 6-14 is R_{in} and X_{in} looking into the resonator through the inductor lifted off ground. The solid

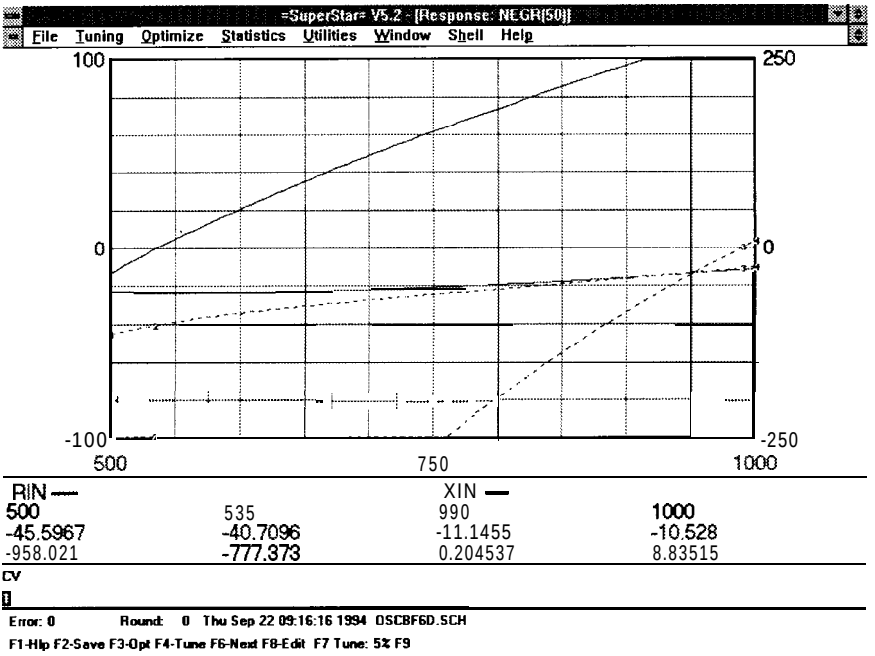

Figure 6-14 *=SuperStar= analysis of 500 to 1000 MHz negative resistance VCO.*

traces are with the varactor capacitance tuned to 6 pF and the dashed traces are with the varactors at 1 pF. Oscillation occurs when the net reactance in the resonator-transistor path is zero. This is 535 MHz at 6 pF and 990 MHz at 1 pF. Varactor capacitance of approximately 8 pF to 0.95 pF are required to tune from 500 MHz to 1000 MHz.

Two alternative methods of viewing the input of the oscillator are shown in Figure 6-15. On the left the linear input reflection coeffkient magnitude, C_{11}, and angle, P_{11}, are displayed. The solid traces are with the varactor capacitance at 6 pF and the dashed traces are with the capacitance at 1 pF. The input reference impedance is 15 ohms. The reflection coefficient magnitude peaks at approximately 4.5 with the capacitance at 6 pF. The

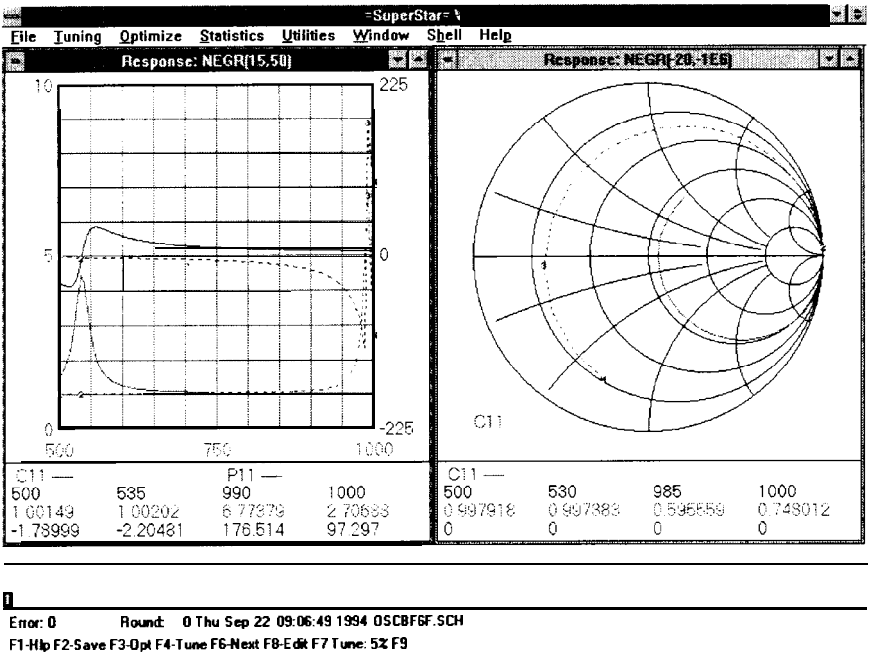

Figure 6-15 *Alternative formats for viewing the input characteristics of negative resistance oscillators.*

reflection coefficient angle is zero near this peak. The varactor tuned to 1 pF the reflection coefficient magnitude peaks at approximately 6.8 at 990 MHz where the angle is 180^{o}. These reflection coefficients correspond to the negative resistances displayed in Figure 6-14, -22 ohms at 535 MHz and -11 ohms at 990 MHz. Oscillation occurs at the frequency where the reflection coefficient angle is zero or 180^{o}.

To understand why oscillation can occur at reflection coefficient angles of either zero or 180^{o}, consider the right side of Figure 6-15. The same input characteristics are again displayed, this time on a Smith chart with -15 as the reference impedance. With a negative resistance specified as the normalizing impedance, negative input resistances display within the circumference of the chart. Negative resistances display outside a Smith chart with

the usual positive normalizing impedance. The two traces on the right in Figure 6-15 are again with the varactor tuned to 6 pF (solid) and 1 pF (dashed). They each cross the real axis of the Smith chart. At 535 MHz the resistance is -22 ohms and displays to the right of center (zero-degrees). At 990 MHz the resistance is -11 ohms and the real-axis crossing is left of center (180^o). Both occur at zero reactance and indicate the oscillation frequency. Whether the reflection coefficient angle is zero or 180^o depends solely on the arbitrary choice of the reference impedance.

At this point we have completed a steady-state analysis of the broadband VCO. Negative resistance is maintained across the band and the oscillation frequency versus tuning capacitance is easily predicted. Let's take this one step further and optimize component values in the oscillator to linearize the frequency versus tuning voltage.

6.8.1 Frequency Tuning Linearity

We will next attempt to optimize the linearity of the frequency versus tuning voltage curve of the VCO from 600 to 900 MHz. A A Loral Frequency Sources GC-15008 linear tuning varactor is selected[4]. GC-15003 capacitance versus voltage is given by the following expression from 2 to 20 volts.

$$C_v = \frac{C_o}{(1+sV)^2} \qquad 6.1$$

where s = 0.11 and C_o = 5.2 for the GC-15008.

Shown in Table 6-5 is the text portion of a schematic circuit file for =SuperStar=. We will attempt to linearize the tuning curve at four frequencies; 600, 700, 800 and 900 MHz. This is done by optimizing the phase zero crossing of S_{11} at these frequencies with varatctor voltages which are a linear progression. Four circuits which share all components except the varactor are defined in the schematic file. These four circuits use varatctor capacitance CV1, CV2, CV3 and CV4. The EQUATE block in the text portion of the schematic define these and the resonator

Table 6-5 *Text portion of a =SuperStar= schematic set-up for optimization of the tuning linearity of the VCO*

```
EQUATE
L=?66.77
Co=5.2
S=0.11
Voffset=2
K=?2.869
V1=Voffset
V2=V1+1 ● K
V3=V1+2*K
V4=V1+3*K
Cv1=Co/(1+S*V1)^2
Cv2=Co/(1+S*V2)^2
Cv3=Co/(1+S*V3)^2
Cv4=Co/(1+S*V4)^2
V=6.4
Cv=Co/(1+S*V)^2

WINDOW
CV1(5,50)
GPH S11 0 10
GPH P1 1 -225 225
FREQ
SWP 500 1000 101
OPT
599 601 S116 PII=O U11=.001

WINDOW
CV2(5,50)
GPH S11 0 10
GPH P1 1 -225 225
FREQ
SWP 500 1000 101
OPT
699701 S116 P11=0 U11=.001
WINDOW
CV3(5,50)
GPH S11 010
GPH P11 -225 225
FREQ SWP 500 1000 101
OPT
799 801 S116P11=0U1 1 =.001

WINDOW
CV4(5,50)
GPH S11 0 10
GPH P11 -225 225
FREQ
SWP 500 1000 101
OPT
899 901 S116 PII=O U11=.001

WINDOW
CV(5,50)
GPH S11 0 10
GPH P11 -225 225
FREQ
SWP 600 900 61
```

inductor, L, which can be optimized but which has an identical value for all circuits. The estimate for the original value is 75 nH. Co and S in the EQUATE block correspond to the GC-15008 varactor. Voffset is the minimum acceptible tuning voltage. This recognizes that the varactor equation is only valid above 2 volts. K is the linear voltage step between each frequency It insures

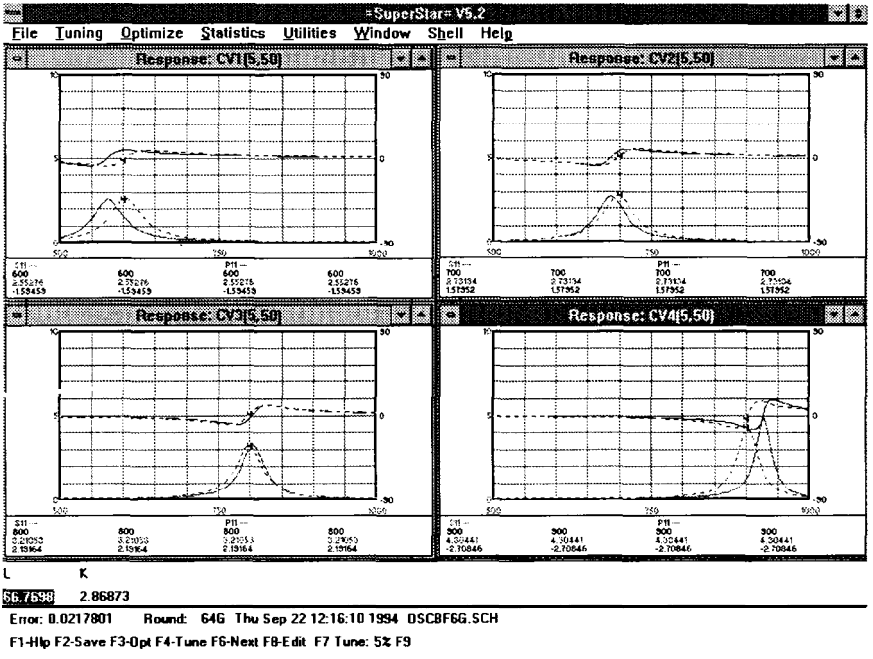

Figure 6-16 *Four frequency views of the VCO before (solid) and after (dashed) optimization to linearize the tuning.*

each voltage point is a linear progression from the previous voltage. Allowing it to be a variable sets the tuning rate. Voltage V1 through V4 then correspond to linearly increasing varactor voltages which are used to compute CV1 through CV4.

The reflection coefficient for these four circuits are displayed in Figure 6-16. The solid traces are the reflection coefficient magnitudes and angles before optimization. Notice that after optimization (dashed traces) the S_{11} are aligned at 600, 700, 800 and 900 MHz. The values of K and L after optimization are given at the bottom of the screen in Figure 6-16. With K= 2.869, the voltage at 900 MHz is 2+3*2.869=10.6 volts, well within the 20 volt maximum limit for the varactor equation.

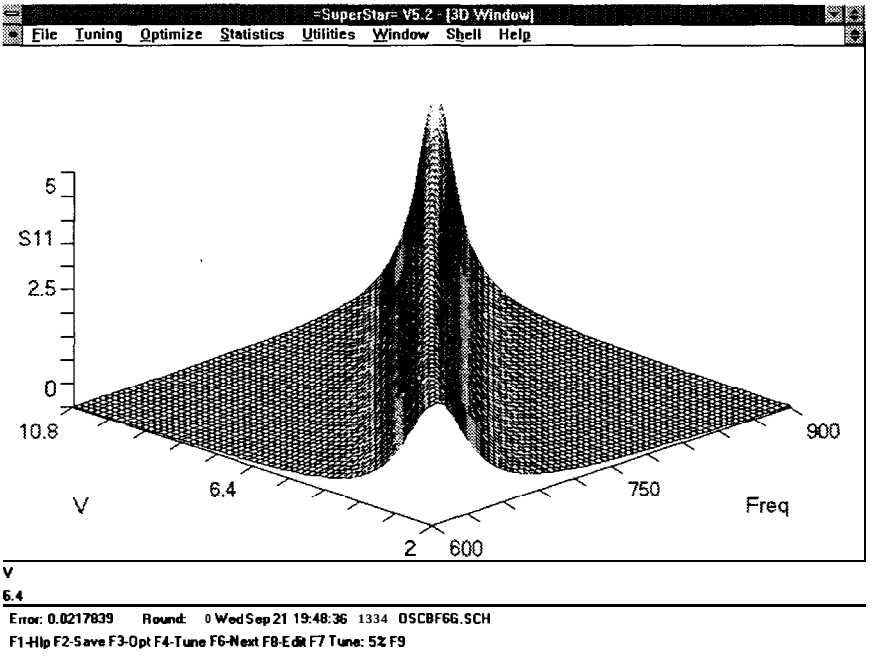

Figure 6-17 3-D *plot of the tuning linearity of the negative resistance VCO.*

Shown in Figure 6-17 is a 3-D plot of the input reflection coefficient after tuning linearity optimization. The fifth Window in Table 6-5 is used to generate this plot. The frequency sweep is from 600 to 900 MHz. The second independent axis of the 3-D plot is the varactor tuning voltage, V, which ranges from 2 to 10.8 volts. Looking along the peak response of S_{11}, the linearity of the tuning voltage curve becomes apparent.

6.9 SPICE Analysis of the UHF VCO

The oscillation criteria, negative resistance magnitude and flatness, effective series capacitance and tuning characteristics including linearity have been fully characterized using =SuperStar=. Next, as was done with the open-loop Bode analy-

Table 6-6 *IntuSoft ICAPI4 Spice net list for the negative resistance UHF VCO*

```
NEGATIVE-R OSCILLATOR
.MODEL MV120404 D(M=0.55 VJ=0.69 CJO=7.1P BV=43.33 IBV=1 ON)
*INCLUDE RF.LIB
Rp 0 10 3.3
Lp 10 1 59n
D11 2 MV120404
D2 4 2 MV120404
Vvar 3 0 9
Lt 2 3 250N
Rr 4 0 1500
cc45 100p
Cb 5 0 1 .0p
Rb 5 0 2700
Rbc 6 5 2700
Rc6750
Xl 6 5 8 MRF559
Ce 8 0 4.7p
Re 8 0 270
Cout 6 9 100p
Rload 9 0 50
Vsup 7 0 PULSE 0 15
.TRAN.1N 250N
.FOUR 760MEG V(9)
.PRINT TRAN V(9) V(1)
.end
```

sis, the starting and non-linear properties of this negative resistance oscillator are studied using SPICE analysis. The schematic of the oscillator under consideration is as before and is shown in Figure 6-13. The IntuSoft ICAP/4 SPICE file is given in Table 6-6. The transistor is from the ICAP/4 library for a Motorola MRF559 bipolar transistor. The varactor model is from the ICAP/4 library for a Motorola MV2101 varactor modified to approximately match the C-V curve of an Alpha Semiconductor SMV1204-104 varactor [5]. For the following SPICE analysis the varatctor is biased at 9 volts (the Vvar independent voltage source).

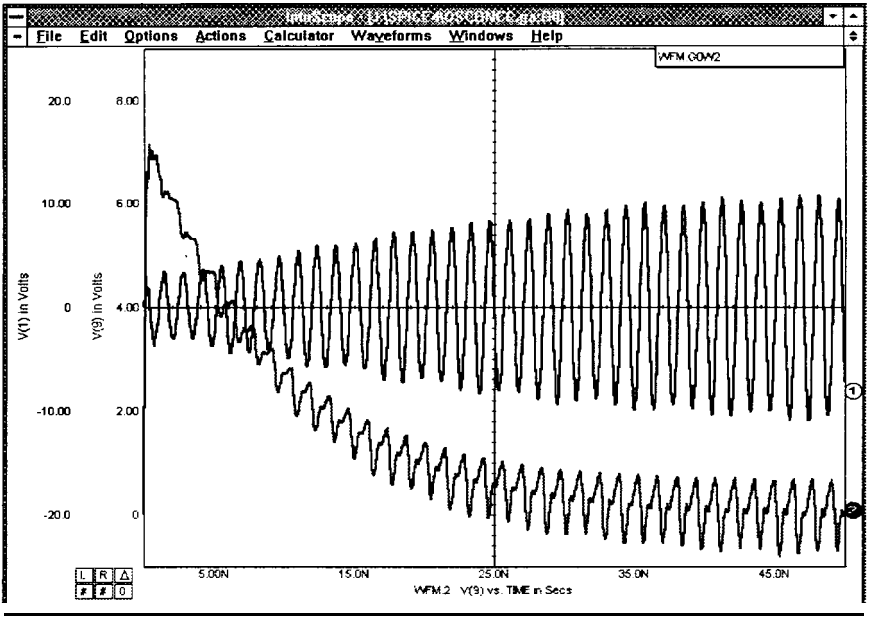

Figure 6-18 *Start-up transient analysis of the negative resistance oscillator.*

6.9.1 Oscillator Starting Time

The supply to the oscillator (Vsup) is pulsed on from $V = 0$ volts to V= 15 volts at $t = 0$ and the transient analysis is run to $t = 250$ nS. The IntuSoft Scope program is used to display the transient data from $t = 0$ to t= 50 nS as given in Figure 6-18. The center trace is the voltage at node 1, the ungrounded end of the resonator inductor. By 50 nS the voltage has risen to approximately 22 vp-p. Beyond 50 nS the voltage rises to approximately 25 vp-p steady-state. The second trace is the voltage developed across the 50 ohm load at node 9. The load is AC coupled so the steady-state average voltage is zero volts. When the oscillator supply is initially switched on at $t = 0$ bias network transients result in a voltage step in the load which diminishes as the output coupling capacitor charges. The steady-state load voltage is just under 2 vp-p.

Oscillator start-up is discussed in Chapter 3. Oscillator start-up theories are often based on noise. It is true that circuit thermal noise, when band limited by the resonator, is no longer white. Examination of a noise source transmitted through an oscillator resonator (acting like a filter) reveals a "fuzzy" sinewave. Components of this noise at the resonator frequency would build to reach the steady state oscillating condition.

However, the sudden application of the supply voltage to the oscillator circuit typically causes the resonator to ring and insures start-up with greater repeatability than would result from a small random process noise voltage. Therefore, it is often time constants in the bias supply network which are responsible for the starting characteristics of an oscillator. Figures 3-15 and 3-16 show no observable jitter on the leading edge. These waveforms are not a single stored sweep but are multiple sweeps of a

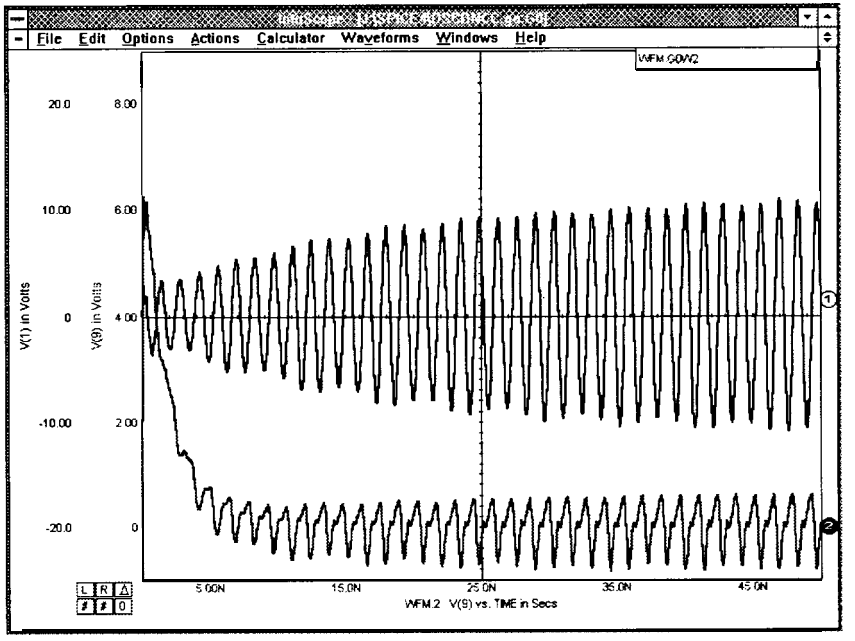

Figure 6-19 *Start-up waveforms of the VCO with output coupling capacitor reduced to 18pF.*

triggered oscilloscope. The absence of jitter in these photographs is testimony to the repeatability of starting and strongly suggests it is not based on a random process.

The transistor collector bias voltage rises as the coupling capacitor is charged through Rc and the load resistance. The 10 nS R-C time constant is evident in the load voltage plotted in Figure 6-18. In the SPICE starting waveforms shown Figure 6-19 the 100 pF coupling capacitor to the load is replaced with an 18 pF capacitor. The resulting output waveform approaches zero volts as expected approximately five time faster. Careful examination of the resonator voltage also reveals the steady-state oscillation level is reached more quickly This is because the collector voltage rises more quickly

It is evident that a number of factors contribute to oscillator starting time, including pararneters as mundane as bias network time constants and the values of coupling capacitors.

6.9.2 The Oscillator Spectrum

From Figure 6-19 we determine that approximately 18.75 cycles occur in 25 nS corresponding to a period of 1.33 nS and an oscillation frequency of 750 MHz. This information is used to specify a fundamental frequency of 750 MHz for a subsequent run including the SPICE ".FOUR" command to perform a Fourier series analysis. Inspection of the plots in Figure 6-19 reveals that V(9), the output waveform contains significant harmonic content while V(1), the voltage at the resonator is a purer sinewave. The

Table 6-7 SPICE Fourier analysis of the fundamental and harmonic components of the VCO output and resonator voltages

	V(9)		V(1)	
HARMONIC	Vpeak	dB	Vpeak	dB
Fundamental	0.664	0.0	14.7	0.0
2nd	0.387	-4.7	0.085	-44.8
3rd	0.098	-16.6	0.216	-36.7
4th	0.070	-19.5	0.152	-39.7

Fourier analysis determined the fundamental and harmonic peak voltages and the harmonics relative to the fundamental given in Table 6-7.

The fundamental peak voltage is 0.664 volts, corresponding to an output level of 6.4 dBm into a 50 ohm load. The harmonic levels at the output are very high. Current at the collector tends to flow as an impulse creating high harmonics. Lower F_t devices which do not support narrow impulses have better harmonic performance. Nevertheless this form of oscillator is naturally rich in harmonics.

The harmonic performance at the resonator is excellent. The second harmonic is -45 dB relative to the fundamental. This is because the resonator acts as a tracking filter. However, the impedance level within the resonator is high and direct coupling to a 50 ohm load kills oscillations. Therefore the output power available at the resonator is low. A linear, high impedance buffer coupled to the resonator provides excellent harmonic performance. Chapter 3 offers additional tips on controlling harmonics.

6.10 References

[1] *PC Products Technical Overview,* Eagleware Corporation, 1750 Mountain Glen, Stone Mountain, GA 30087, TEL (404) 939-0156, FAX (404) 939-0157, September, 1993.

[2] R.W. Rhea, *HF Filter Design and Computer Simulation,* Noble Publishing, Atlanta, GA, 1994, p. 239.

[3] *IsSpice4 Users Guide,* Intusoft, PO. Box 710, San Pedro, CA 90733, TEL (310) 833-0710, FAX (310) 833-9658, 1994.

[4] *Semiconductor Catalog 20,* Loral Microwave FSI Semiconductor Division, Chelmsford, MA, TEL (508) 256-8101, FAX (508) 937-3748, undated.

[5] *Semiconductor Devices: RF Through Millimeter* Wave, Alpha Semiconductor Devices Division, Woburn., MA, TEL (617) 935-5150, FAX (617) 935-4939, January 1992.

7

Circuits

In the next four chapters, the oscillator fundamentals discussed previously are applied to the design of a number of specific oscillators. The schematics, analysis of the Bode responses, circuit peculiarities, and performance of these oscillators will be studied.

Oscillators using L-C, transmission line, SAW, and piezoelectric resonators are investigated in detail. Each of these resonator media has advantages and disadvantages, with suitability for different oscillator applications. The range of examples is not intended to be inclusive, but representative of techniques which may be applied to satisfy specific oscillator requirements.

Each oscillator type is studied by a unified analysis approach, the open-loop cascade gain-phase plot (with two exceptions). The vagaries of different oscillator types have yielded to practical solutions developed over the years by countless contributors. A unified analysis of these practical designs will provide insight into oscillator behavior and prepare the reader for development of oscillators for new and unique applications.

Sixteen oscillator types, listed in Figure 7-1, are studied. Oscillator configurations that utilize capacitive tapping of a simple tank resonator are Colpitts oscillators. Oscillator configurations that utilize inductive tapping of the resonator are Hartley Clapp added a capacitor to the Colpitts [1]. The process of naming each variation or improvement to a classic design, as significant as they may be, soon gets out of hand. Giving correct credit is further complicated by the conversion of the classic vacuum tube designs to solid-state devices which bear little resemblance to the original active device. Oscillator types, other than those clearly

INPUTS — HELP & VALUES — ≡OSCILLATOR≡ Ver 1.0

TYPE=LCOL

TYPE	DESCRIPTION	FREQ MHz	STAB 1-10	TUNE %	NOISE Fo	SIMP 1-10	DEU 1-10
LCOL	LC COLPITTS	<50	3	67	3	10	FET
LCLP	Lc CLAPP	<50	4	30	4	9	FET
LBIP	LC BIPOLR AMP	30-300	3	lee	2	10	BIP
LHYB	LC HYBRID AMP	100-1200	3	lee	2	9	HYB
TUHF	T-LINE UHF UCO	300-2000	1	67	1	10	BIP
TUHX	T-LINE + XFMR	200-1200	2	lee	2	9	BIP
CBIP	CAVITY BIPOLR	300-2000	4	67	5	1	BIP
CHYB	CAVITY HYBRID	300-2000	4	67	5	1	HYB
SBIP	SAW 2-TERMINAL	200-1000	5	.02	6	3	BIP
SHYB	SAW 2-PORT HYB	200-1200	5	.05	6	3	HYB
SMOS	SAU 2-PORT nos	200-1000	5	.03	6	3	nos
XPRC	XTAL PIERCE SER	.1-20	8	.2	8	6	BIP
XCOL	XTAL COLPTS PAR	4-20	6	NIL	6	6	BIP
XHPF	XTAL HIGH PERF	1-20	9	.2	9	5	BIP
XOUR	XTAL OUERTONE	20-200	7	NIL	7	6	BIP
XNUL	XTAL & HULTPLR	50-600	7	.2	7	6	BIP

Figure 7-l *Sixteen oscillator types studied in the following chapters.*

resembling early classic configurations, are given names descriptive of the techniques used.

The parameters listed in the selection matrix are only guidelines. The advantage of oscillator design with computer simulation and analysis is that strict rules of design quickly and easily yield to new ideas which can readily be tested.

7.1 Frequency Range

The oscillators studied cover, without modification, a frequency range from submegahertz to about 2 GHz. All oscillators have at least L-C oscillator short-and long-term phase stability, so R-C oscillators are not included. The lower-frequency limit is determined primarily by the maximum inductor value the designer is willing to employ Although the upper frequency limit is stated as about 2 GHz, the upper frequency limit is determined by the

highest frequency at which the lumped, or semi-lumped, construction assumed is valid. Experienced microwave designers using hybrid, MMIC, or miniaturization techniques can extend these techniques to much higher frequencies.

The frequency range recommended for each oscillator type is the range for which that type is most often and successfully applied. For example, the L-C Clapp can be used above 50 MHz, but transistor parasitics are more easily dealt with at these frequencies by the oscillator referred to as the L-C bipolar type. The L-C bipolar can be used below 30 MHz, but the L-C Clapp is a simpler solution at the lower frequencies. When specific requirements suggest improvisation, by all means do so.

7.2 Stability

Long-term stability for each oscillator in the selection matrix is rated relatively with a number from 1 to 10, with 10 being the most stable. Long-term stability improves with increasing resonator loaded Q. High resonator loaded Q tends to reduce the effects of device to device, temperature, and aging variations of active-device reactances. Stability is then determined primarily by the temperature and aging characteristics of the resonator elements.

Power dissipation in the resonator can cause drift as the resonator warms up from a cold start. This is aggravated by higher-power oscillator operation (good for phase noise performance) and by greater resonator loss (higher loaded Q). Resonator components with lower-temperature coefficients reduce this problem.

7.3 Tuning Bandwidth

The maximum tuning bandwidth as a percentage of the center frequency is listed. A common misconception is that high loaded Q dictates a low tuning bandwidth. Loaded Q and tuning bandwidth are independent. As an analogy, consider narrow-band bandpass filters, which can be tuned over a frequency range far

in excess of the bandwidth at any particular frequency setting. The misconception is encouraged by SAW and bulk crystal resonators which have marvelously high Q and extremely poor tunability In this case, poor tunability results from an inability to change the resonator internal values. Tuning must be accomplished external to the resonator. External tuning could be much broader were it not for the static parallel capacitance, Co, of these devices.

A given oscillator configuration is capable of excellent high-Q operation over an octave when only one element in the resonator is tuned. An excellent example of high-Q oscillators with octave tuning are the cavity oscillators found in manually tunable signal generators. High-Q coaxial cavities with broadband tuning are tuned by changing the effective length of the cavity

If all resonator components are tuned, including coupling elements, for example, an oscillator can theoretically be tuned over extreme bandwidths. Practical problems do discourage high-Q broadband oscillator tuning. High loaded Q is achieved by loose coupling of the resonator, and looses are fairly high because loaded Q is a significant fraction of unloaded Q. Coupling values are therefore critical, and the loaded Q must not change significantly over the frequency range to be tuned. A coupling structure with this character must be used, or tuned coupling elements must be employed.

A practical problem with electronic tuning of high Q oscillators is high resonator voltage. As resonator loaded Q increases to 50% of the unloaded Q, the resonator voltage becomes high. Refer to Figure 2-7. The high resonator RF voltage can drive the varactor into forward conduction. High-power operation to improve phase noise performance aggravates the situation. Operation of the varactor with a larger reverse bias allows a higher RF voltage before forward conduction is reached. Unfortunately, a large reverse bias reduces the capacitance tuning range. A second solution involves using a dual back-to-back dual varactor configuration which reduces the effects of conduction as long as the RF voltage is less than the varactor reverse avalanche voltage.

7.4 Phase Noise

The relative phase noise performance of each oscillator type is also listed in Figure 7-l. This performance parameter closely matches the stability rating. Differences are found for the cavity and SAW oscillator types. The high-loaded Q of cavity and SAW oscillators results in excellent short-term stability but they possess poorer temperature-drift performance than that of quartz crystal oscillators. Very careful selection of cavity material and construction can improve the long-term stability

The phase noise of an oscillator is a strong function of the loaded Q. The loaded Qs assumed in Figure 7-l for each oscillator type are readily obtainable values using standard commercially available inductors, capacitors, and resonators. The assumed Q is specified in the detailed description of each oscillator. For critical applications, higher loaded Qs can be obtained by modifying the standard oscillator design.

7.5 Simplicity

This relative number is inversely proportional to the circuit complexity and cost. Complexity and cost is based on a somewhat arbitrary and subjective rating of 1 for resistors, 2 for capacitors, 3 for inductors, 5 for transistors, 10 for hybrids, 40 for bulk crystals, 100 for SAWS, and 200 for cavities. The sum for a circuit is normalized to 10 maximum. This approximate rating system is useful for quick comparisons. If cost or complexity requirements are critical, a more detailed comparison of actual schematics is advised.

7.6 General Comments

For each of the oscillators studied, a schematic with suggested resonator component reactances is given. Bias component values are determined using the techniques and equations given in Chapter 5. The schematic also gives resonator and bias component values for a typical oscillator as computed by the oscillator

synthesis program =OSCILLATOR=. A =SuperStar= circuit file written by =OSCILLATOR= and the resulting open-loop Bode or the reflection coefficient responses computed by =SuperStar= are also shown. Additional remarks concerning these programs and examples of oscillator design using the computer are given in Chapter 6.

Also given is the characteristic impedance recommended for the loop gain and phase analysis. This should result in S11 and S22 plots near the center of the Smith chart at the oscillation frequency. The actual best characteristic impedance is a function of the center frequency and the device selected for use. If S11 and S22 are not near the center of the Smith chart, raising or lowering the analysis characteristic impedance is recommended. The =SuperStar= circuit file written by the =OSCILLATOR= synthesis program uses the recommended characteristic impedance. The characteristic impedance specified in this file may be easily changed using the editor built into the =SuperStar= program.

One of the oscillator selection criteria was a desire for the characteristic impedance to be 50 ohms. This simplifies oscillator testing by allowing direct verification of the design loop gain and phase plot by measurement with common test equipment. This criterion was not always followed when an oscillator type was too common or useful to ignore. A measurement technique in this case might be to complete the design at the recommended impedance, and then as a final step, do the computer analysis at 50 ohms and compare the result with measured 50 ohm data.

The suggested reactances given for the resonator result in the given resonator loaded Q. Resonator values can be adjusted to decrease loaded Q (less critical stability and higher power) or to increase loaded Q (better stability). Guidelines for adjusting loaded Q are given for each oscillator.

Computer simulation allows great flexibility in the design. Ideas can be readily tested for their effect on oscillator performance. Custom oscillator designs are easily analyzed using these techniques.

7.7 Output Coupling

Specific output coupling component values are not given because they are a function of the design requirements. In addition, more than one output coupling location may be specified on the schematic. The text includes suggestions on the selection of the output coupling location.

When high output power is of primary interest and stability is less significant, tight output coupling is used. Coupling is taken through low-reactance elements to drive the load. If stability is of primary importance, a larger coupling reactance is used. For example, an element with 500 ohms or higher reactance is used to couple to a 50 ohm load. If a high-impedance buffer is used, the coupling reactance has little effect.

When tight coupling is employed, the Bode response analysis should include coupling of the output load. This is done by adding the coupling reactance and load in series from the chosen oscillator circuit location to ground. Additional details on output coupling are found in Chapter 2.

7.8 References

[1] J. K. Clapp, An Inductance-Capacitance Oscillator of Unusual Frequency Stability, *Proceedings of the IRE*, Vol. 36, 1948, pp. 356-358.

8

L-C Oscillators

Oscillators using resonators constructed from inductors and capacitors find wide application in electronic systems. L-C oscillators are more stable than R-C oscillators for both the long and the short term. As a consequence, L-C oscillators are almost exclusively used for general oscillator applications above the lower-frequency limit for which inductors are practical in size. Economic high quality capacitors are available for a wide range of values and seldom affect oscillator design as much as inductors. At low frequencies, the value of inductance required for reasonable reactance becomes large. Cores using magnetic materials help decrease the practical lower-frequency limit.

8.1 Capacitors

Capacitors used in the resonators of L-C oscillators should have a high Q and a stable temperature coefficient. Porcelain, ceramic, polystyrene, and silver mica capacitors are generally suitable, although silver mica capacitors can be somewhat erratic with temperature. At HF frequencies, polystyrene capacitors are an excellent choice. At VHF and higher frequencies, porcelain and ceramic are the best choices.

Ceramic material is available with a wide variety of temperature characteristics. The ceramic used in resonator capacitors should have an NPO or COG temperature characterization. Ceramic capacitors are available with a specified temperature characteristic, such as N750, N2200, and so on. N750 signifies a negative temperature characteristic of 750 parts per million per degree Celsius. Specified temperature characteristic capacitors

are used to compensate the known or measured temperature drift of inductors or of the entire oscillator.

The Electronic Industries Association maintains standards on capacitors [1]. For example, the EIA designation for a N750 capacitor is U2J. The capacitance required of coupling and bypass capacitors is large. To obtain large capacitance in a small size, a ceramic material with a very high dielectric constant is often used. Unfortunately, the temperature drift of these ceramics is often severe.

Shown in Table 8-1 is a sample of EIA capacitor designations. Except for the COG designator, the first character in the EIA code is the lower-temperature limit. The second character, a number, is the upper-temperature limit. The third character is the temperature tolerance over the specified frequency range.

It is obvious from Table 8-l that the temperature variation of certain capacitors is severe. The W suffix specifies that the capacitance at -55C may drop to 10% of the room temperature value. This can have a significant effect, even if the capacitor is used only for bypassing or coupling.

An important capacitor parasitic is lead inductance. The inductance of ceramic and silver mica capacitors with lead spacings of 0.2 to 0.25 inch, and with the leads trimmed very short, is typically 8 to 10 nH. The lead inductance of such a 10 pF capacitor causes a series resonance at approximately 500 MHz. As the operating frequency approaches the resonant frequency, the inductive reactance cancels some of the capacitive reactance, and

Table 8-1 *Sample of a Few EIA Temperature Designations for Capacitors*

	Temperature Range (°C)		Change with Temperature (%)	
EIA Code	Min	Max	Min	Max
COG	-55	125	-0.2	0.2
X7R	-55	125	-15	15
X5W	-55	85	-90	22
Y5F	-30	85	-7.5	7.5
Z5U	10	85	-56	22

the effective capacitance increases. Above the resonant frequency, the capacitor is actually inductive.

Capacitors with O.l-inch lead spacing, and trimmed leads, have approximately 3 to 5 nH of inductance. Chip capacitors typically have 1 nH or less of inductance.

Capacitor Q in the HF region is typically in the thousands. At VHF and higher frequencies, the Q is somewhat less, but usually larger than inductor Q, so the inductor in the resonator defines the resonator Q.

8.2 Inductors

The inductance in nanohenries of single-layer solenoid coils to about 1% accuracy is [2]

$$L(nH) = \frac{1000N^2R^2}{9R + 10L} \qquad 8.1$$

where

N = number of turns 8.2

R = radius to the center of the wire in inches 8.3

L = length of the solenoid in inches 8.4

For example, the inductance of a 22-turn coil with a radius of 0.15 inch and a length of 1 inch is approximately 960 nH.

To increase the inductance, or to facilitate tuning, the coil is sometimes wound on a cylindrical slug of magnetic material such as powdered iron or ferrite. The inductance of the solenoid increases proportionally to the effective permeability of the slug. Figure 8-l gives the effective permeability, μ_e, as a function of the material permeability, μ_o, and the cylinder shape [3]. For high material permeability, the effective permeability is largely a function of the length-to-diameter ratio.

An even more effective method of increasing inductance for a given physical size is to wind the coil on a toroid or pot core of

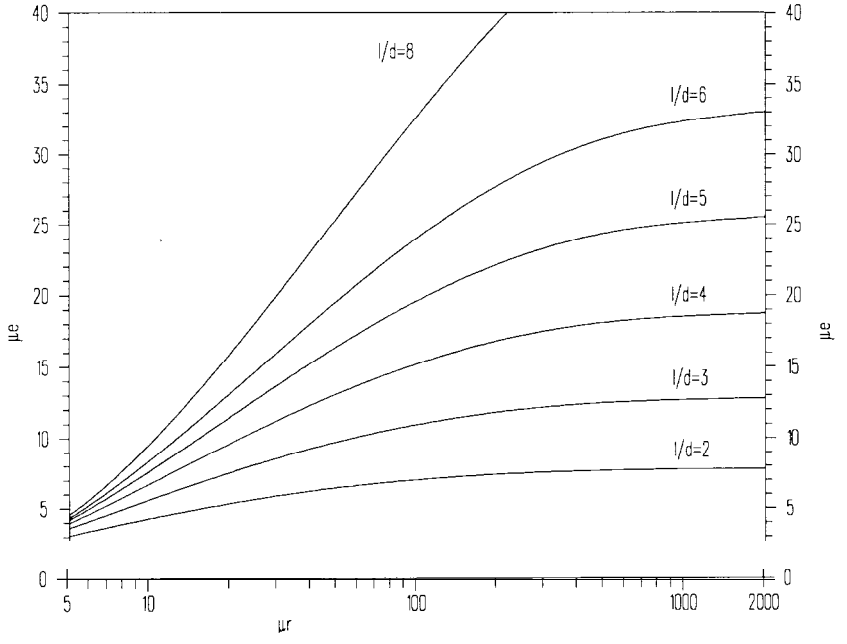

Figure 8-l Effective permeability for a solenoid inductor versus material relative permeability of a cylindrical core.

magnetic material. The effective permeability of these forms approaches the permeability of the material.

The inductance in nanohenries of a toroidal coil is

$$L(nH) = 11.7\mu_o\, tN^2\, log\, \frac{OD}{ID} \qquad 8.5$$

where

μ_o = material permeability 8.6

N = number of turns (passes through the center) 8.7

t = toroid thickness in inches 8.8

OD = toroid outer diameter 8.9

ID = toroid inner diameter 8.10

Using a magnetic material to increase coil inductance generally increases the temperature dependence of the inductance. The cylindrical core has the smallest effect on the temperature characteristics because the effective permeability is due primarily to the core shape. The temperature coefficient of toroidal and pot cores is almost identical to the temperature coeffkient of the material, which is often significant.

The prevalent inductor parasitic is often the unloaded Q. The approximate unloaded Q of single-layer solenoids with a length-to-diameter ratio of 2 and wound with copper wire is [2]

$$Qu = 240R\sqrt{f} \tag{8.11}$$

where

R = radius of the solenoid in inches 8.12

f = frequency in megahertz 8.13

Unloaded Q for other length-to-diameter ratios and more detailed inductor models are given in reference [2].

Another important inductor parasitic is the winding-to-winding distributed capacitance and stray capacitance to ground. For the solenoid this capacitance is approximately 1 pF per inch of solenoid radius. Therefore, for a given operating frequency there exists an upper limit on the usable solenoid size. The parasitic capacitances of larger solenoids become significant, increasing the effective inductance and reducing the Q. At still higher frequencies, the coil resonates and then becomes capacitive.

A reasonably conservative air solenoid maximum radius in inches is

$$R_{max} = \frac{15}{f} \tag{8.14}$$

The maximum unloaded Q as a function of frequency is therefore

$$Q_{u\,max} = \frac{3600}{\sqrt{f}} \qquad 8.15$$

These relations are only approximate.

The maximum coil size at lower frequencies is quite large. To obtain higher unloaded Q in smaller coils at low frequencies, toroids and pot cores are often utilized, although temperature drift may become a problem. At VHF and higher frequencies, higher unloaded Q is achieved by using distributed (cavity or transmission line) resonators.

8.3 L-C Colpitts Oscillator

This L-C Colpitts JFET circuit is the simplest oscillator studied. The schematic for a 19 to 19.8 MHz example is given in Figure 8-2. It is a natural choice for low-cost and low-power tunable or fixed-frequency requirements to about 50 MHz. The approximate loaded Q of this oscillator with the resonator reactance values suggested in the schematic is about 25. A =SuperStar= computed cascade open-loop Bode response is shown in Figure 8-3. With the tuning capacitor, C_1, at 33.17 pF the phase zero crossing is near 19.4 MHz (markers 2 and 6). The zero crossing occurs slightly higher in frequency than the loop gain peak. Both S11 and S22 are realtively well matched as shown in the Smith chart plot. The open loop cascade is terminated with 150 ohms as indicated in the title bar of the computed response.

The solid traces are with a resonator inductor (L=2200 nH) with a very high unloaded Q. The dashed responses are with an inductor unloaded Q of 100. Notice with finite inductor Q a drop in loop gain and a slight reduction in the phase slope (loaded Q). Both S_{11} and S_{22} shift slightly to the left (lower impedance) with finite inductor Q. At this point a more accurate assessment of the loop would be obtained by reducing the terminating impedance.

Element values were chosen based on the following equations:

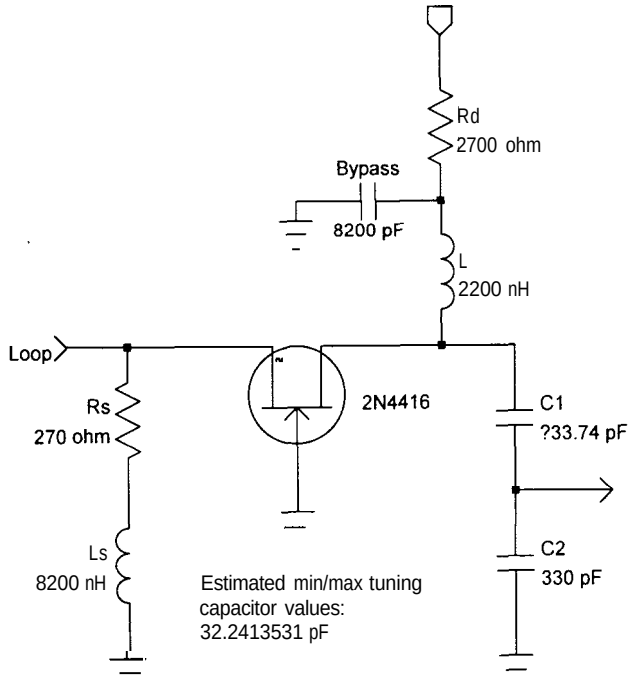

Figure 8-2 A *19.4 MHz Colpitts oscillator.*

$$L = \frac{258}{2\pi f} \qquad 8.16$$

$$C_1 = \frac{1}{480\pi f} \qquad 8.17$$

$$C_2 = \frac{1}{48\pi f} \qquad 8.18$$

The loaded Q for the element values above is approximately 25.

The bias element values were found using the equations in Section 5-8 with a supply voltage of 20.4 volts, a drain-source voltage of 14 volts, a drain current of 2 mA and a gate-source voltage of 0.5 volts. The 8200 nH source inductor decreases

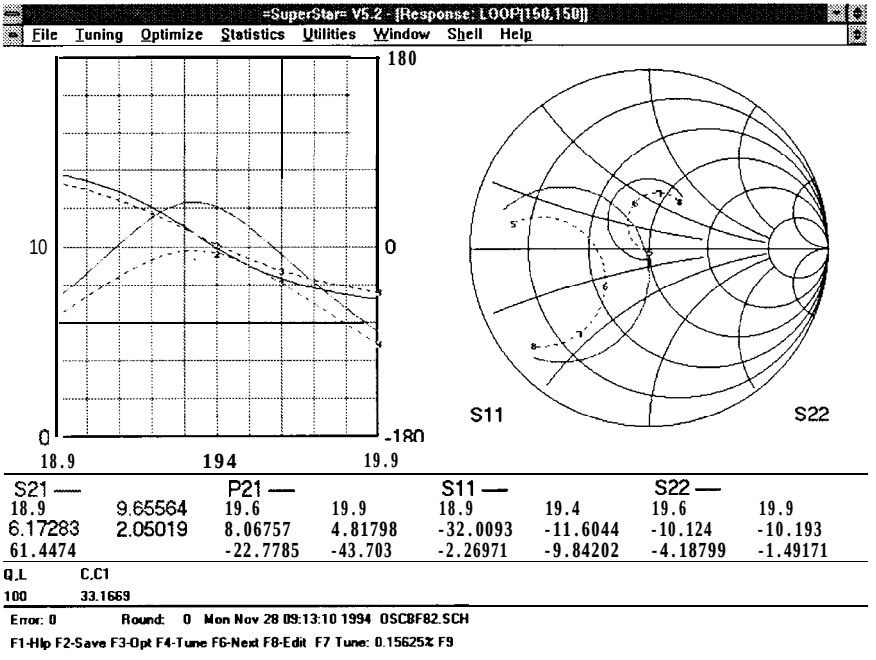

Figure 8-3 *Open loop response and matches for a 19.4 MHz oscillator with very high inductor Q (solid) and an inductor Q of 100 (dashed).*

loading by the source resistor. In this case, the 270 ohm source resistance is greater than the 150 ohm impedance level, and removing the source inductor decreases the loop gain only by about 1.5 dB. This is a good trade-off for a low-cost design, particularly if little tuning is required which might further decrease the loop gain. Lower drain currents and devices with higher *Vgs* requirements increase the source resistance.

The frequency is tuned from 19 to 19.8 MHz with C1 tuned from 34.84 to 31.72 pF. For this narrow tuning range the loop gain, loop phase and match characteristic change little. The tuning bandwidth of this circuit is approximately 100% (3: 1 in frequency) with some degradation of gain, phase and match. A wider tuning range, particularly down in frequency, is achieved by tuning the inductor instead of tuning the capacitor C1.

Increased loaded Q is achieved by increasing C2 and decreasing C1, or by decreasing ***L*** and increasing both C1 and C2. For a given inductor Q, increased loaded Q naturally results in less loop gain.

8.3.1 Output Coupling

The output is usually taken from the JFET source. A suggested coupling reactance at the source for a 50 ohm load is 300 to 700 ohms. The drain is at a high impedance. Very light coupling must be used if energy is taken at this point. Refer to Chapter 2 for additional details on coupling techniques.

8.4 L-C **Clapp Oscillator**

This oscillator [4] is very similar to the previous Colpitts JFET circuit. The resonator inductor is replaced with a series L-C network. The schematic is given in Figure 8-4. For a given inductor value, this circuit has a higher loaded Q than that of the Colpitts oscillator.

The element values are

$$L = \frac{300}{2\pi f} \qquad 8.19$$

$$C_1 = \frac{1}{340\pi f} \qquad 8.20$$

$$C_2 = \frac{1}{36\pi f} \qquad 8.21$$

$$C_3 = \frac{1}{232\pi f} \qquad 8.22$$

These resonator values result in a loaded Q of approximately 35. The loaded Q can be increased by increasing ***L*** and decreasing C3, or by decreasing C1 and increasing C2. Bias components are found using the techniques discussed for the Colpitts circuit.

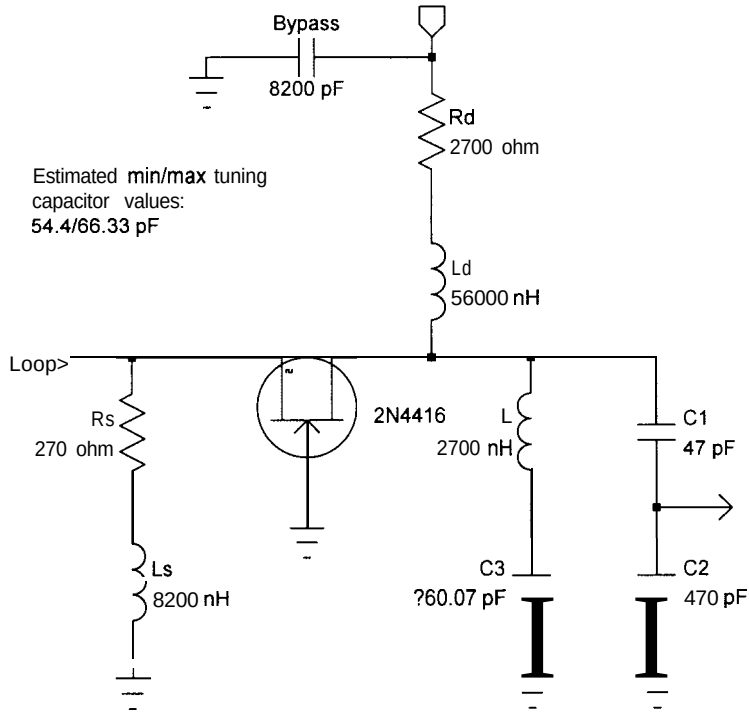

Figure 8-4 *Schematic of a 20 MHz Clapp oscillator.*

The =SuperStar= computed open loop responses and matches are shown in Figure 8-5. The terminating impedances are 100 ohms. Notice the phase slope is steeper than the previous Colpitts which is associated with the higher loaded Q. As before, the solid traces are with high resonator inductor Q and the dashed responses are with an inductor Q of 100. The higher loaded Q results in a more significant gain loss for a given inductor Q.

8.4.1 Tuning

The Clapp is normally tuned with C3. The tuning characteristics are quite different from those of the Colpitts. The cascade loop gain remains relatively constant as the frequency is tuned lower

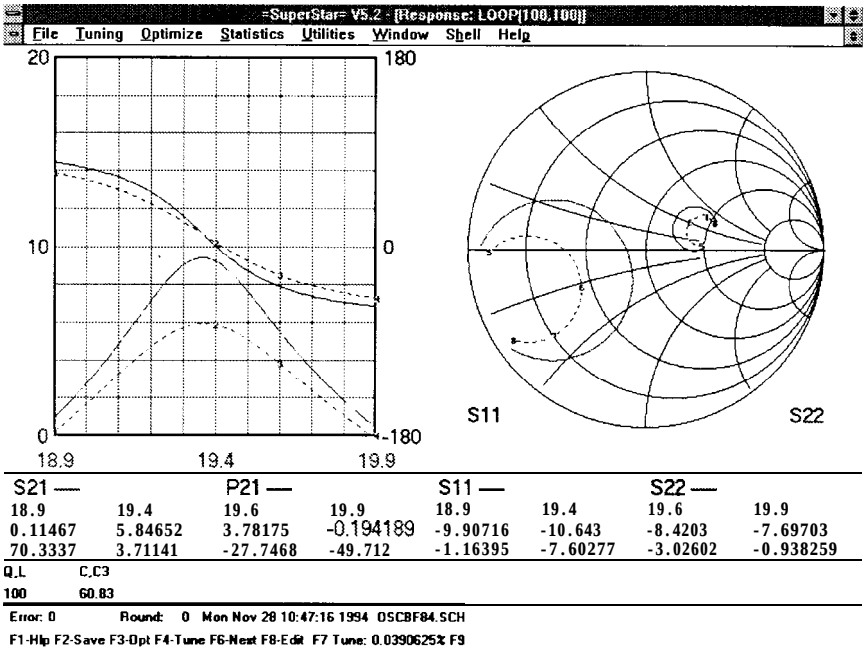

Figure 8-5 *Loop responses and matches for a 20 MHz Clapp oscillator.*

by increasing C3. The frequency reaches a lower limit as C3 becomes large. When using varactors to tune the oscillator, this effect can be used to linearize the frequency versus voltage curve, since the capacitance change in varactors is generally greatest at largest capacitance. Also, the RF voltage across C3 decreases as C3 increases. This helps compensate for the problem of varactor forward conduction when the resonator RF voltage swing exceeds the tuning voltage (this occurs at lower frequencies).

With a capacitance ratio of 10 to 1, the tuning range is approximately 40% of the center frequency The tuning range can be much wider if the inductance is tuned. An inductance ratio of 7 to 1 provides a tuning range of approximately 100% with the resonator reactances given.

8.4.2 Output Coupling

The output is usually taken from the FET drain. The coupling reactance for a 50 ohm load is 300 to 700 ohms. Refer to Chapter 2 for details on coupling techniques.

8.4.3 Circuit Vagaries

The drain choke in this circuit should have at least 50 times the reactance of the resonator inductor. Caution must be exercised in the selection of this inductor to make certain that it does not series resonate. Parallel resonance in the drain choke is acceptable, since it increases the effective reactance of the choke. At the high end the recommended frequency range and with high-loaded Q, the lead inductance of C2 can become troublesome. If the C2 lead inductance and capacitance resonate near or just above the operating frequency, the effective reactance can be quite low. The resulting high loaded Q can increase the resonator loss and the loop gain can drop below unity

8.4.4 Operating Frequency

The JFET Colpitts and Clapp oscillators are best suited for operation below 100 MHz. With typical VHF JFETs, at higher frequencies the input impedance develops a negative real component and the loop cascade becomes unstable. Careful device selection and a series input resistor help manage this problem.

8.5 **L-C Bipolar Transistor Oscillator**

This L-C bipolar oscillator using a shunt-C coupled resonator is an excellent choice for frequencies up to 500 MHz, perhaps higher. It works well over a wide frequency range for a wide range of operating conditions. Similar versions constructed with hybrid amplifiers is studied next. SAW and bulk crystal resonator forms of this basic configuration are studied later. The schematic of a

300 MHz example is given in Figure 8-6. The open loop responses and matches are given in Figure 8-7

A series resonator, *L* and C3, is coupled with shunt capacitors C1 and C2. When the reactance values of C1 and C2 are lower than the input and output impedance of the transistor amplifier, the phase shift of the resonator is approximately 180^{o} at the peak amplitude response frequency The loaded Q with the reactance formulas given below is about 22 through much of the frequency range, but decreases with typical VHF/UHF transistors to about 12 at 500 MHz. The loaded Q of this configuration is readily adjustable to higher or lower values. Increasing C1 and C2 increases the loaded Q. Increasing *L* and decreasing C3 also increases the loaded Q. This degree of freedom in C3 is helpful when limited values of tuning varactors are available.

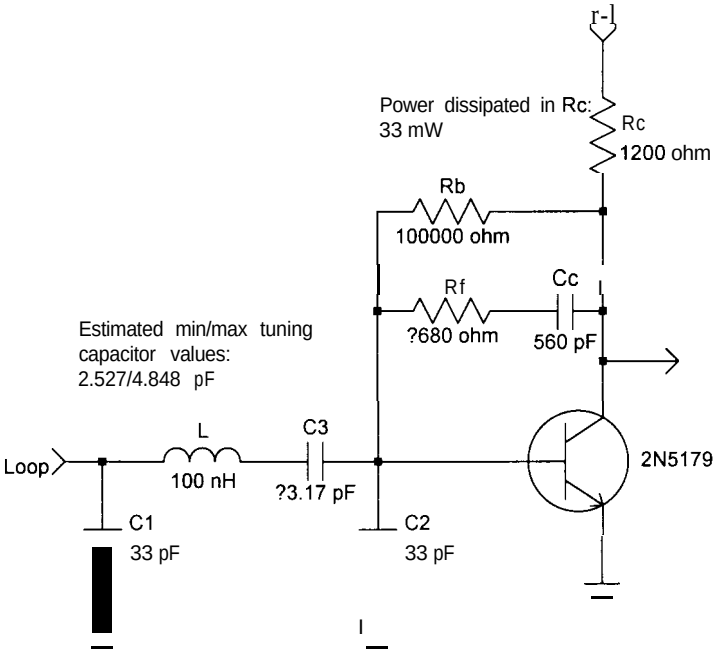

Figure 8-6 *Schematic of a 300 MHz L-C bipolar oscillator.*

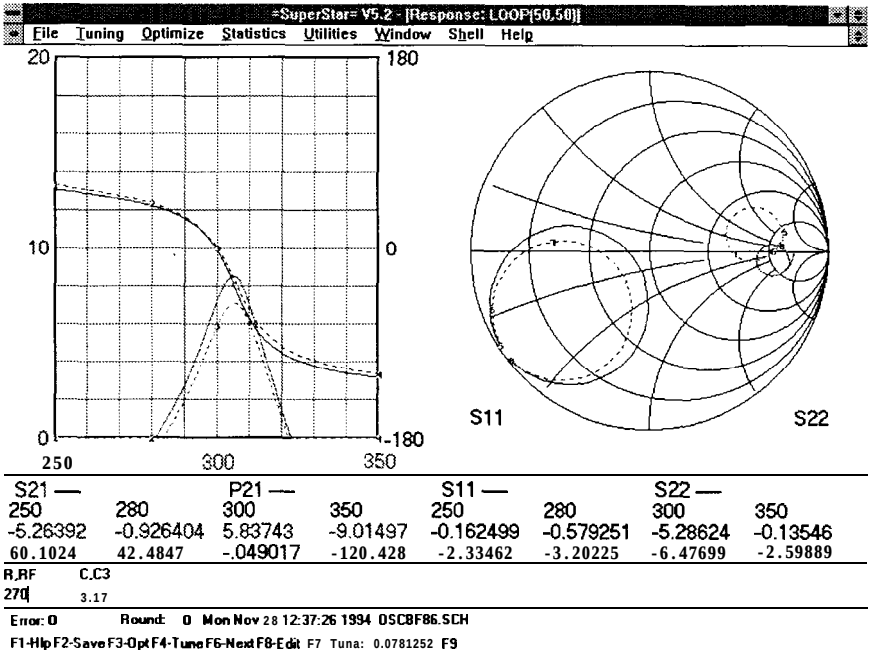

Figure 8-7 *Open loop responses and matches for a 300 MHz L-C bipolar oscillator.*

The element values are

$$L = \frac{190}{2\pi f} \qquad 8.23$$

$$C_1 = \frac{1}{48\pi f} \qquad 8.24$$

$$C_2 = \frac{1}{48\pi f} \qquad 8.25$$

$$C_3 = \frac{1}{300\pi f} \qquad 8.26$$

$$R_f = 680 \text{ ohms} \qquad 8.27$$

The impedance level of this configuration is near 50 ohms, so the predicted open-loop gain and phase performance can easily be

verified using a network analyzer. The impedance level is adjustable by proper design of the transistor amplifier. This is discussed in more detail later.

8.5.1 Tuning

The frequency is tuned with C3 or ***L.*** The tuning bandwidth is approximately 100% with a C3 capacitance ratio of 10 to 1. C3 begins to have little effect as it approaches the effective series capacitance of C1 and C2. This is normally not a problem with reasonable loaded Qs because C3 is less than C1 and C2. This effect can be used to advantage to linearize the frequency versus tuning voltage curve when using a varactor, if lower loaded Q is acceptable. The tuning range is slightly improved when tuning is done with the inductor, ***L.***

The resonator behaves much like a single section filter. The function of the coupling capacitors is to decouple the resonator from the 50 ohm characteristic impedance of the transmission path. A high loaded Q is obtained with reasonable inductor values when shunt coupling capacitors are used. If a simple series resonator with no coupling capacitors is used, the phase shift at resonance is zero-degrees instead of 180^{o}.

This configuration has a disadvantage when tuned. As the resonant frequency is changed by tuning C3, the reactances of the coupling capacitors change. This increases the loaded Q as the frequency is tuned higher. Since the loaded Q is a function of frequency, the loop gain tends to drop off as the frequency is increased. This reduces the output power as the oscillator is tuned higher. A modified configuration, which uses shunt coupling inductors, eliminates this problem. It also increases the tuning range when the tuning element is C3. However, minimum inductor designs are generally less costly The use of coupling inductors may be justified when wide tuning is required. The coupling capacitors are simply replaced with inductors of the same reactance. Mixing the coupling elements, with one capacitor and one inductor, results in a zero-degree phase shift at resonance.

8.5.2 Coupling Capacitor Inductance

Relatively large values of coupling capacitors are used for high loaded Q. At higher operating frequencies, the parasitic lead inductance of these capacitors becomes significant. With only 1 nH of total inductance in the ground path, the 33 pF coupling capacitors in Figure 8-6 resonate at 876 MHz, less than three times the operating frequency of that oscillator. This is low even for chip capacitors and is hopeless for leaded capacitors. Use of several parallel capacitors helps manage this problem. Nevertheless, parasitic inductance typically limits the upper frequency of high loaded Q oscillators of this type.

8.5.3 Controlling the Phase

Best performance is achieved when the open-loop gain crosses zero-degrees near the maximum phase slope. This oscillator configuration satisfies this condition well, through about 200 MHz, when using VHF/UHF transistors. Management of the phase response may be required at higher frequencies. This is discussed in detail in Chapter 2 and in the next example, the L-C hybrid oscillator. The open-loop Bode response analysis of this 300 MHz example reveals that the phase zero crossing does not occur at maximum phase slope. There is about 40^{o} of excess phase. As a consequence, the gain margin is about 1.5 dB less than the peak gain. These margins are acceptable. However, any additional phase shift will begin to reduce oscillator performance.

A higher Ft transistor with less phase shift at 300 MHz helps this problem. Decreasing the coupling capacitors from 33 pF to 18 pF, and increasing the resonator inductance to 240 nH to retain the same loaded Q, results in a more optimum design. C3 in this case is reduced to 1.32 pF.

8.5.4 The Bipolar Amplifier

The amplifier stage shown in Figure 8-6 and the responses in Figure 8-7 includes a shunt feedback resistance of 680 ohms. The shunt feedback tends to stabilize the amplifier by reducing the low-frequency gain. It also reduces the input and output impedance of the common-emitter configuration, providing a better match to 50 ohms. This simple configuration is suitable for most applications.

The dashed responses in Figure 8-7 are with the 680 ohm shunt feedback resistor reduced to 270 ohms. This reduces the input and output impedance (shift left on the Smith chart) and reduces the loop gain.

The amplifier gain can be further reduced, the phase shift brought closer to 180°, and the input and output impedance brought closer to 50 ohms by including series feedback in the emitter. Emitter degeneration also improves linearity and discourages class-C oscillation conditions [5]. Equations relating the gain and match of amplifiers with feedback are given in Section 1.7.

Bipolar transistors are available for a wide range of applications and operating conditions. The selection can be based on cost, noise figure, special voltage and current requirements, output power level, and so on. For example, if the transistor is selected and biased for high power levels, the resulting oscillator output level is high. Best noise performance is achieved by selecting a device with low noise at relatively high collector currents and operating the oscillator at a relatively high power level. Refer to Chapters 3 and 4. Additional methods of biasing are given in Chapter 5.

8.6 **L-C Hybrid Oscillator**

This oscillator is similar to the shunt-C coupled L-C bipolar configuration with an MMIC (monolithic microwave integrated circuit) amplifier is substituted for the bipolar amplifier. The

active device is therefore slightly more expensive, but external bias components are eliminated. The MMIC approach has several advantages, including smaller size and operation to higher frequencies. The schematic of a 600 to 730 MHz example using a Mini-Circuits MAR2 is shown in Figure 8-8 and the open loop responses and matches are given in Figure 8-9. The solid traces are with the tuning capacitor at 1.85 pF (oscillation at 600 MHz) and the dashed traces are with the capacitor tuned to 1.15 pF (oscillation at 730 MHz). The loaded Q of the series inductor is 100.

Small and inexpensive hybrid and MMIC devices are available from several manufacturers. Hybrids are constructed using film or lumped elements on a small insulating substrate. The simplest forms are a common-emitter bipolar with series and shunt feedback. A base-to-ground resistor and a collector choke may be included for biasing [6]. MMICs are constructed using a semiconductor substrate. The typical MMIC uses series and shunt feedback applied to a Darlington-connected transistor pair [7]. Using two transistors, which has little cost impact on MMICs, increases the gain- bandwidth product prior to inclusion of series and shunt

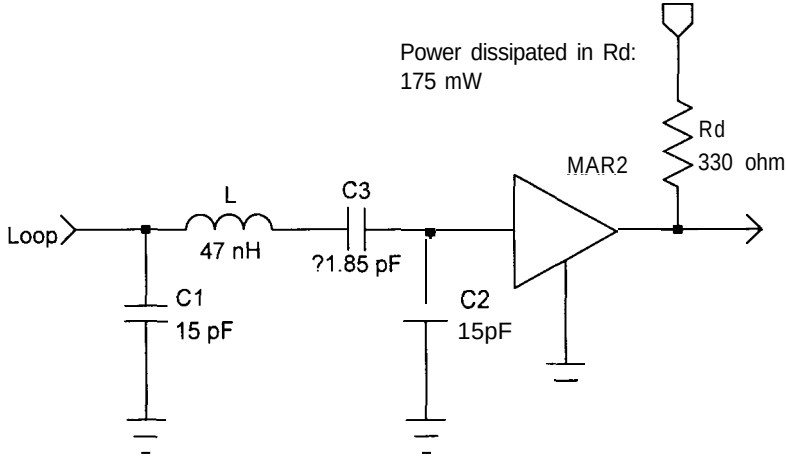

Figure 8-8 *Schematic of a* 600 *to* 730 MHz L-C *hybrid oscillator.*

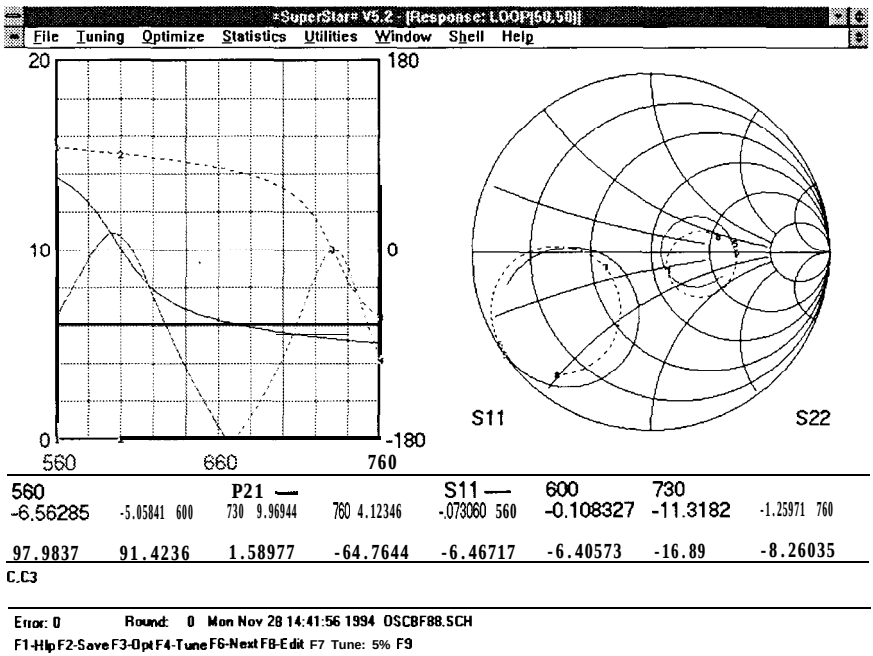

Figure 8-9 Open loop responses and matches for the 600 to 730 MHz L-C shunt-C coupled MMIC oscillator.

feedback. The resulting gain-bandwidth and input and output matches are generally better than those of single-transistor hybrids.

Both hybrids and MMICs have internal bias networks. Application of these devices typically requires only an output resistor and/or choke to the supply and input and output coupling capacitors. When the device operating voltage, *Vd,* and current, Id, are given, the required output-to-supply resistance is

$$R_d = \frac{V_{cc} - V_d}{I_d} \qquad 8.28$$

Dissipation is often significant in Rd. It is

$$P_{Rd} = I_d^2 R_d \qquad 8.29$$

Some of the signal is also dissipated in Rd. The gain loss is given by [3]

$$loss(\text{dB}) = 20 \log \frac{Rd}{Rd+25} \qquad 8.30$$

assuming that the device is matched well to 50 ohms. The loss increases with decreasing *Rd.* If the loss is objectionable, an RF choke may be added in series with *Rd.*

One factor that limits the upper frequency limit of this and the L-C bipolar transistor oscillators is the transmission phase shift. Ideally, the phase shift should be 180^{o}. This shift, when combined with a resonator phase shift of 180^{o}, results in a cascade open-loop phase shift of zero-degrees. The amplifier phase shift decreases from 180^{o} at low frequency Table 8-2 gives the gain and phase shift versus frequency for 10 dB gain amplifiers constructed using a Motorola 2N5179 bipolar transistor with feedback, a Motorola LT4785 bipolar transistor with feedback, several Mini-Circuits MAR series MMICs, a Motorola MWA220 hybrid, and an Avantek MSA-0285 MMIC. The phase shifts of the 2N5179 and LT4785 amplifiers were determined by circuit simulation using =Super-Star=. These amplifiers were designed using =SuperStar= to determine the optimum values for the series and shunt feedback

Table 8-2 *Gain and Phase Shift of Broadband Amplifiers*

	Bias	100MHz	500MHz	1000MHz
Device	V mA	G(dB) ϕ	G(dB) ϕ	G(dB) ϕ
2N5179	6 5	10.0 150°	6.0 92°	4.5 6°
LT4785	8 25	10.0 175°	10.0 154°	10.0 129°
MAR2	5 25	13.0 174°	12.8 156°	12.5 131°
MAR3	5 35	13.0 174°	12.8 152°	12.5 128°
MAR4	5 50	8.2 174°	8.2 156°	8.1 135°
MAR6	4 16	20.1 171°	18.7 138°	16.4 107°
MAR9	8 35	7.7 166°	7.4 159°	7.3 142°
MSA0285	3 55	12.6 175°	12.3 157°	11.9 135°
MWA220	5 25	10.8 166°	11.4 104°	9.4 -5°

resistors. A peaking inductor was used to improve the 2N5179 amplifier phase and gain flatness.

The hybrid and MMIC devices are available for a wide range of output levels. As discussed in Chapter 3, oscillator output level is directly related to the output capability of the amplifier device. Amplifier output power capability is proportional to 20 times the log of the device operating current. An approximate relationship for the power output at 1 dB compression is

$$P_o(dBm) = -24 + 20 \log Ic \qquad 8.31$$

From this we see that the devices listed in Table 8-2 are suitable for oscillator output levels of approximately -10 to +10 dBm.

As the phase shift departs further from 180^o the cascade phase zero crossing departs further from the maximum phase slope. This decreases the loop phase margin and noise performance of the oscillator. It is feasible to add phase shift with a delay network or transmission line until zero-degrees is achieved again. However for a given delay the extra phase shift increases with frequency Ultimately this reduces the oscillator tuning range.

8.7 References

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[2] R.W. Rhea, *HF Filter Design and Computer Simulation,* Noble Publishing, Atlanta, GA, 1994, pp. 59.

[3] *Stackpole Ceramag Ferrite Cores,* The Stackpole Corporation, St. Marys, PA, undated, p. 9.

[4] J. K. Clapp, An Inductance-Capacitance Oscillator of Unusual Frequency Stability, *Proceedings of the IRE,* Vol. 36, 1948, pp. 356-358.

[5] Anzac Division of Adams Russel, Amplifier Application Notes, Microwave Journal, October 1982, pp. 130-136.

[6] *Motorola RF Deuice Data,* 3rd ed., MWA110/120/130 Wideband Hybrid Amplifier Data Sheet, Motorola, Phoenix, AZ, 1983, pp. 5-88 to 5-95.

[7] *Si MMIC Cascadable Amplifiers,* Avantek Application Information, Avantek, Santa Clara, CA, undated.

9

Distributed Oscillators

As the operating frequency is increased, oscillator phase noise performance degrades. Oscillators with improved phase noise require higher loaded Q. Higher loaded Q requires higher unloaded Q, and for L-C oscillators, this means increased inductor physical size. There is an upper limit on inductor size before distributed self-capacitance and stray capacitance to ground become a problem. A potential solution to this problem is to use distributed (transmission line) resonators which may be larger and therefore have higher unloaded Q than inductors.

Recall from Chapter 8 that the maximum unloaded Q of inductors as a function of frequency in megahertz is approximately

$$Q_{u\ \max} = \frac{3600}{\sqrt{f}} \qquad 9.1$$

In practice this expression is optimistic at low frequencies and pessimistic at high frequencies. Above several hundred megahertz, higher unloaded Q can be obtained using transmission line resonators. For a given volume, transmission lines have an unloaded Q similar to that of inductors. However, transmission lines at a given frequency can be physically larger than an inductor. The upper frequency of transmission lines is limited by high-order moding. The unloaded Q and upper frequency limit for representative quarter-wave transmission line resonators are given in Table 9-l. The transmission line unloaded Q and moding frequency limits are computed using the physical model transmission line program, =TLINE= [l], The unloaded Qs are with copper or silver metallization and the stated dielectric material, and include both conductor loss and dielectric loss.

Table 9-1 *Best unloaded Q and maximum frequency for representative transmission lines*

Construction	Q at 100 MHz	Q at 1000 MHz	Maximum Freq. (GHz)
Coax, 50 Ω, Cu metal			
0.141 -in.-OD semirigid, PTFE	120	370	34
0.25in.-OD, air	240	770	21
1 .O-in.-OD, air	970	3100	5
Coax, ceramic loaded, Ag metal			
0.156-in profile, ε_r=38.6	200	300	2
0.238-in profile, ε_r=38.6	250	400	2
0.477-in profile, ε_r=38.6	500	1100	1
Microstrip, Cu metal			
50 Ω, 0.062-in. thick, PTFE-glass	140	350	19
100 Ω, 0.062-in. thick, PTFE-glass	100	280	19
50 Ω, 0.025-in. thick, alumina	25	75	47
Stripline, Cu metal			
80 Ω, air, 0.5-in. ground to ground, 25-in.-wide, .062-in.-thick bar	600	1900	10

A drawback of transmission line resonators is long physical length at frequencies below several gigahertz. Loading a coaxial line with a dielectric material reduces the physical length by the square root of the relative dielectric constant. The length reduction is substantial with high dielectric constant materials. Modern materials with relative dielectric constants of 90 and higher now have excellent temperature and loss characteristics.

A quarter wavelength coaxial resonator in air at 984 MHz is approximately 3 inches long. When loaded with ceramic with a relative dielectric constant of 38.6, a quarter wavelength resonator is only 0.48 inches long. Above several gigahertz ceramic loading results in resonators which are too short to be practical!

The loss in ceramic loaded resonators is primarily conductor loss. The unloaded Q of the ceramic (the inverse of the loss tangent) is typically higher than the unloaded Q due to conductor loss. The optimum ratio of the coaxial outer to inner conductor diameters

for minimum loss is independent of the dielectric constant. However, the impedance is inversely proportional to the square root of the dielectric constant. Therefore with high dielectric constant materials the transmission line impedance is very low, typically 5 to 15 ohms.

It is important to recognize that the primary advantage of ceramic loading is resonator length reduction. The unloaded Q of these resonators is no higher than a longer non-ceramic resonator. A second advantage is rigidity which can reduce oscillator acoustic (vibration) noise.

The unloaded Qs given in Table 9-1 are theoretical and safety factors are not included. If loaded Qs approaching the unloaded values are used the actual unloaded Q should be measured or a safety factor should be applied.

Oscillators should be designed for loaded Qs of 10% to 70% of the unloaded resonator value. Lower loaded Qs are selected for higher output power or less critical applications. Higher loaded Qs are selected for best phase noise performance. As the loaded Q approaches the unloaded Q, the resonator loss becomes excessive. This limits the maximum loaded Q and is the reason that loaded Qs are seldom greater than 70% of the unloaded Q.

An additional factor limiting the maximum loaded Q is resonator voltage in varactor tuned circuits. The voltage impressed across a varactor coupled to a high Q resonator can be very high. This is discussed in Chapter 2.

9.1 Negative Resistance UHF Oscillator

This oscillator is evaluated by negative resistance analysis. The author feels this design approach offers less insight into circuit behavior than does the open loop cascade analysis. However, the one-port negative resistance method is particularly useful for broad tuning VCOs in the UHF and microwave frequency range. Fundamentals of negative resistance oscillator analysis are given in Chapter 2.

For this oscillator configuration, the transistor is operated common-collector. The resonator is a series-tuned base network consisting of Ct and an inductor or transmission line for the positive reactance element. The analysis is done by looking through the transmission line. The oscillator is formed by grounding the input port. This design is the basis of many commercially available VCOs.

This VCO works well to 2000 MHz using discrete components, can be pushed to several gigahertz using hybrid construction techniques. At lower frequencies capacitance must be added from the base to emitter and the emitter capacitance must be increased. Below a few hundred megahertz the L-C bipolar or hybrid oscillator is recommended. The schematic for a 750 to 1150 MHz VCO is shown in Figure 9-l. The circuit file includes Cc, a 1.5 pF capacitor to model load coupling at the emitter.

The Motorola MRF559 transistor is biased at Vce = 10 volts and Ic = 25 mA. The grounded collector bias configuration used here

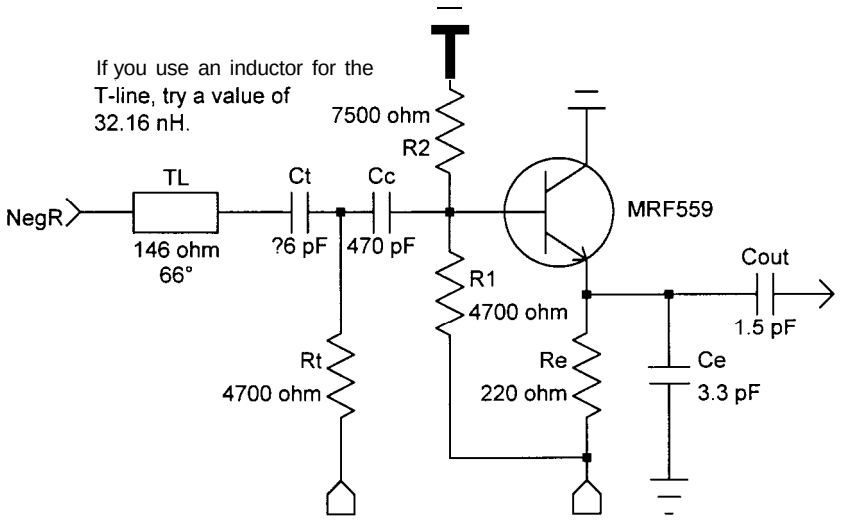


Figure 9-1 Schematic of a 750 to 1150 MHz VCO.

uses only three resistors and offers excellent stability However, it required a negative supply when an NPN bipolar transistor is used. To form the oscillator the point labeled "NegR" is grounded. The tuning voltage is applied to the varactor via a 4700 ohm resistor. As discussed in Chapter 4, the thermal noise voltage developed in this resistor will tune (modulate) the VCO and degrade the phase noise. Because the RF impedance at the base is low, the 4700 ohm resistor could be reduced somewhat to decrease the noise voltage. The best performance is achieved by replacing this resistor with an inductor.

The input reflection coefficient magnitude, C_{11}, and angle, P_{11}, are given on the left in Figure 9-2. The solid curve that crosses zero-degrees phase at 750 MHz is the phase of S_{11}. The second solid curve below the first is the magnitude of the input reflection

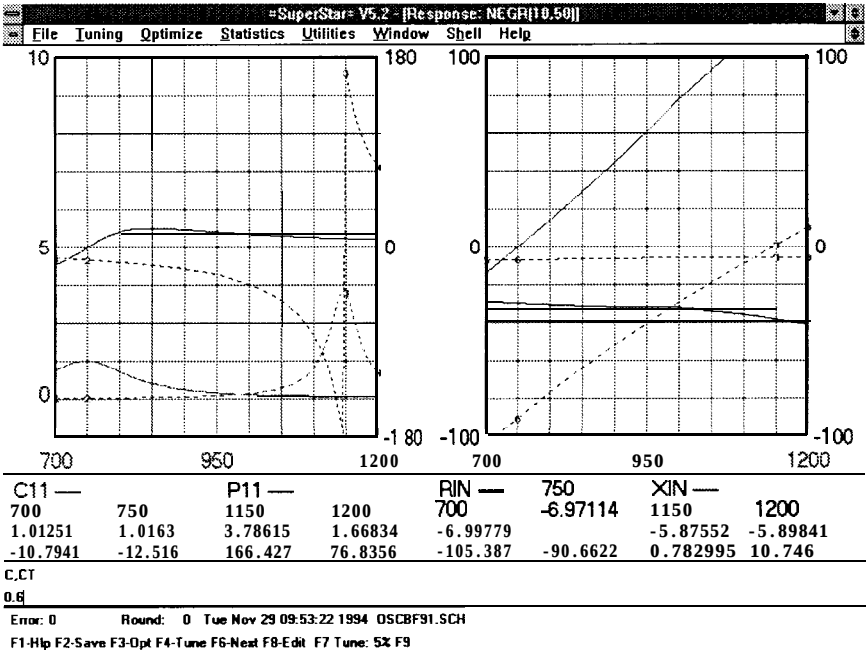


Figure 9-2 *Input reflection coefficient magnitude and phase (left) and the input resistance and reactance (right).*

coefficient. C_{11}, plotted on a scale of 0 to 10, is 2.0. The input reference impedance is 10 ohms. These solid curves are obtained with the tuning capacitor Ct at 6 pF. When Ct is tuned to 0.6 pF, the dashed curves are obtained. The phase of C_{11} crosses 180^o at 1150 MHz. The magnitude of C_{11} for this condition is 3.8. The fact that oscillation occurs when the reflection coefficient phase is either zero or 180^o is explained in Chapter 2. The formula given there can be used to find the effective negative resistance and reactance given the magnitude and angle of C_{11} and the 10 ohm reference impedance. The resistance and reactance are plotted on the right in Figure 9-2. Again the solid traces are with Ct at 6 pF and the dashed traces are with Ct at 0.6 pF. The sloped traces are reactance and the flatter traces are resistance. The frequency where the reactance is zero corresponds to the frequency where the reflection coefficient angle is zero or 180^o. The negative resistance is approximately -30 ohms at the lower frequencies but only -6 ohms at the higher frequencies.

The element values are determined using the following guidelines. First, the network effective input capacitance is determined using the techniques outlined in Section 2.18. The added emitter capacitance is adjusted to the maximum value which maintains ample negative resistance. C_{eff} ranges typically from 7 pF for VHF transistors down to 2 pF for UHF transistors but is increased with larger values of emitter capacitance. The maximum value of the resonator capacitor or varactor is 1 to 3 times C_{eff}. Smaller values are used for better phase noise and larger values for better tuning linearity.

The transmission line characteristic impedance is then

$$Z_o = \frac{1}{2\pi f_l C_{net} \tan\theta_e} \qquad 9.2$$

where

$$C_{net} = \frac{C_t C_{eff}}{C_t + C_{eeff}} \qquad 9.3$$

$$\theta_e = 45 \text{ to } 70^o \qquad 9.4$$

f_l = lower operating frequency 9.5

Short transmission lines result in an impracticably high line impedance. If the resulting line impedance is too high, a larger C_{net} must be realized. This may require using a lower Ft transistor, or adding a transformer as is done in the next oscillator type. Line lengths greater than 70^o create problems on the high-frequency end of the tuning range. Using a smaller value of resonator capacitance solves this problem.

The loaded Q of negative resistance oscillators is typically less than 5 and this circuit defies attempts at improving the Q. When used as a broadband varactor-tuned VCO, the low loaded Q does not limit phase noise performance significantly because varactor modulation noise predominates, particularly at higher offset frequencies.

9.1.1 Circuit Vagaries

Despite the popularity of this oscillator, it is touchy to design. Performance is highly dependent on the transistor type. Certain component values are critical. If the designer understands and manages these vagaries, this oscillator is the best choice for UHF broadband VCO applications.

The maximum useful capacitance value of Ct is limited by the effective input capacitance, C_{eff}. Values of Ct greater than C_{eff} do not further lower the operating frequency The unsuspecting designer is left wondering why the tuning range is low. Increasing the transmission line Z_o and using a lower capacitance varactor is one solution. The limited tuning range is often used to advantage to improve the tuning linearity If the value of varactor capacitance is selected properly, C_{eff} naturally compensates for the increased rate of change of varactor capacitance at lower reverse bias.

This oscillator actually works best when lower Ft transistors are used. The circuit can be envisioned as a series-tuned Clapp, with internal transistor base-to-emitter capacitance and collector

(ground)-to-emitter capacitance acting as a voltage divider. Microwave transistors with little internal capacitance do not work well except at the high end of the useful range of this oscillator type. Older and higher-power devices, such as the 2N3866, 2N5109, and LT1001A, often work well. The MRF559 is often a good choice. Higher Ft devices required increased capacitance added at the emitter. Experimentation with device selection and careful circuit simulation are strongly advised. At the low end of the frequency range, adding external base-to-emitter capacitance is sometimes necessary,

If bias conditions result in a emitter resistance below about 200 ohms, an RF choke may be required in series with the resistance. This choke must be free of any resonances in the operating frequency range.

9.1.2 L-C Resonator Form

A variation on this circuit is the substitution of an inductor for the transmission line. This technique is used to reduce oscillator size, and is often used in commercially available VCOs. An L-C resonator gives a broader tuning range for a given tuning capacitance ratio. The inductor value is chosen so that the reactance at the upper frequency limit is

$$X_L = Z_0 \tan\theta_e \qquad 9.6$$

The frequency dependence of transmission lines greater than 20^o long is different from that of inductors, so the exact inductor value is determined by circuit simulation or empirically

9.1.3 Output Coupling

The output can be taken from several points. The inductor or transmission line can be tapped. As the tap is moved toward the transistor, more power is coupled out. If the tap is too close to the transistor, the loading reduces the oscillation margin, and the operating frequency becomes more load dependent.

The output can be taken by capacitive coupling at the emitter. Because some additional capacitance at the emitter increases C_{eff}, this is an effective method. However, too large a capacitor loads the circuit and oscillation is extinguished. The reactance, Xc, of the coupling capacitor is nominally 150 ohms or greater.

A third output coupling method is to add a low resistance in series with the collector to ground. Fifty ohms is typical. The output is then taken directly at the collector. This is a thermal disadvantage since the transistor case is no longer connected directly to ground.

Tapping the transmission line or inductor results in the lowest level of output harmonics and gives a flat output level versus frequency tuning. Taking power from the collector generally results in high harmonic levels.

9.1.4 Advantages

Because the negative resistance oscillator uses a series-tuned resonator, the varactor lead inductance becomes a part of the resonator. This is an advantage over varactor-tuned oscillators using parallel resonators. The base coupling capacitor inductance and transistor base inductance are also absorbed.

The collector case of the transistor can be directly grounded, which results in excellent thermal properties for this oscillator. Since this circuit works well with power transistors (lower Ft), this configuration makes an excellent power oscillator. Also, the output level of this configuration is relatively flat with frequency tuning.

The negative resistance VCO has been used in a configuration that includes a frequency multiplier [2-4]. Push-pull and push-push configurations are used to double and triple the oscillation frequency, resulting in higher-frequency outputs with suppression of the fundamental. Winch [3] reported operation with 6 to 10 milliwatts of output from 14 to 17 GHz.

9.15 Circuit Variations

Shown in Figure 9-3 is a common-collector VCO with a positive supply voltage. This VCO uses back-to-back varactors in the resonator. It requires the use of an additional resistor or inductor as a ground return for the tuning voltage on the second varactor. This reduces the voltage swing across each varactor. For a given varactor capacitance it also reduces the total external series capacitance by a factor of two which reduces the deleterious effects of C_{eff} and requires a larger resonator inductance which improves the loaded Q.

The voltage across the resonator in common collector VCOs is reduced by reducing the emitter bias voltage. This VCO uses an inductor at the emitter instead of a resistor to minimize the voltage at the emitter. The lack of emitter resistance increases the bias sensitivity to temperature variation. This is compensated for in this VCO by deriving the base drive voltage for R_1

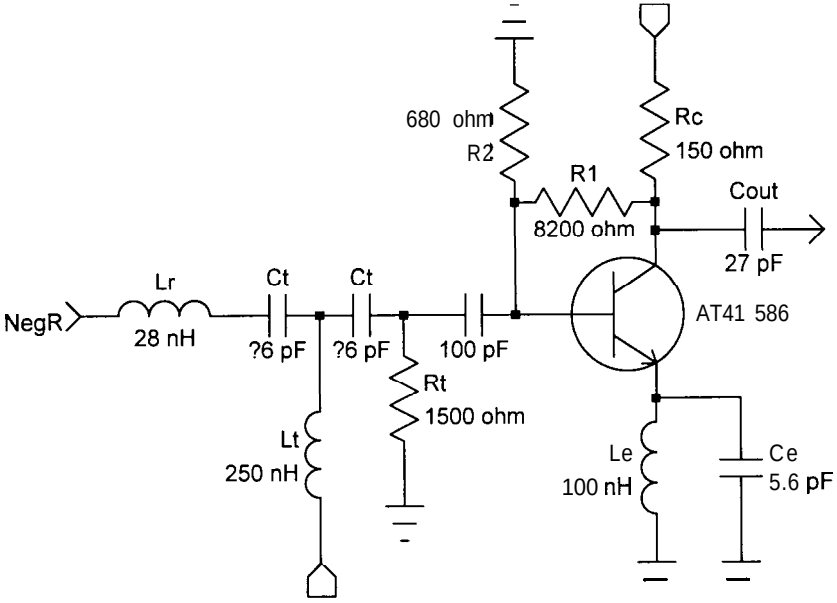


Figure 9-3 900 - 1400 MHz common-collector VCO.

and R2 after the collector resistor Rc. A potential increase in the collector current drops the collector voltage which reduces the base drive and counters the increased collector current.

Because Rc is larger than the 50 load resistance, most of the power available at the collector is delivered to the load. The output level and efficiency of this VCO is better than the previous VCO. However, the load pulling is worse because of the tight coupling.

Harmonic energy is high at the collector. The second harmonic in this VCO with a high Ft device such as the Hewlett-Packard AT41586 is only a few decibels below the fundamental.

Shown in Figure 9-4 is another variation of the common collector VCO. The output is taken from the resonator. A two-winding

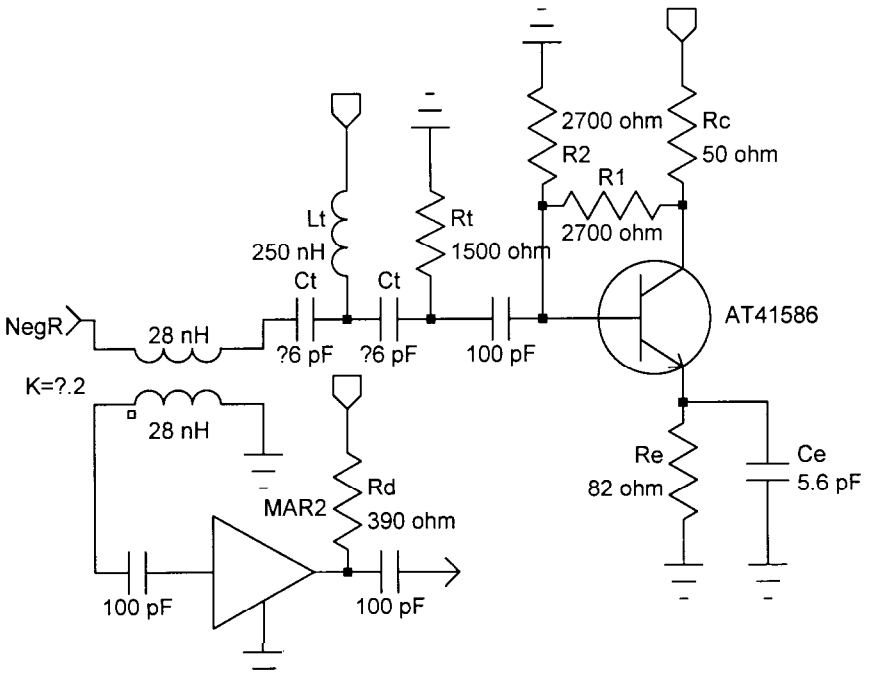


Figure 9-4 *Common-collector VCO with output coupling at the resonator and output buffering.*

transformer with loss coupling (K=0.1 to 0.4) is used to keep the 50 ohm load from absorbing the negative resistance and killing the oscillation. Coupling directly to the resonator also significantly degrades load pulling performance so a Mini-Circuit MAR2 MMIC buffer has been added.

The advantage of coupling at the resonator is excellent harmonic performance. The second and higher harmonics are down 25 dB or better with this configuration. This performance is achieved because the resonator acts as a narrow filter which tracks automatically with the oscillation frequency

9.2 Negative Resistance Oscillator with Transformer

The loaded Q of conventional negative resistance oscillators is typically less than 5 and they defy attempts at improving the Q. One method for increasing the loaded Q is to add a transformer in the base network. The oscillator studied in this section uses this technique.

The schematic of a 450 to 550 MHz example with a typical turns ratio of 1 to 4 is given in Figure 9-5. Higher impedance ratios further increase the loaded Q and C_{eff}, but if the transformer ratio is too high, transformer parasitics make oscillator susceptible to spurious oscillations. For a given resonator the loaded Q is increased by the impedance ratio. The increased C_{eff} results in a broader tuning range, particularly if the maximum value of the varactor approaches the original value of C_{eff} without a transformer. The ratio of the maximum to minimum frequency for this oscillator approaches the square root of the varactor capacitance ratio. Since this configuration is similar to that of the previous oscillator, the comments in the preceding section apply R_{in} and Xin with Ct = 2.7 pF (solid curves) and Ct = 1.54 pF (dotted curves> are given in Figure 9-6.

The element values are found using the guidelines given for the previous oscillator type with C_{eff} increased by the impedance ratio. The higher C_{eff} value of this oscillator with a transformer generally results in more practical component values. However

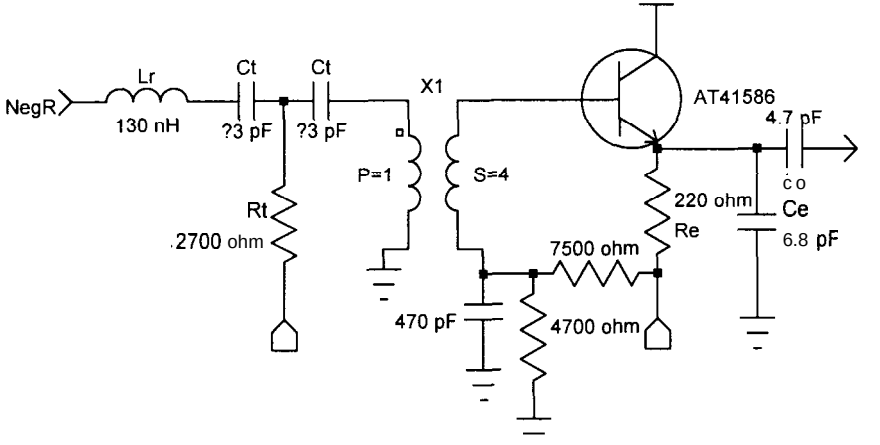


Figure 9-5 Common collector VCO with impedance transformer.

the negative resistance is divided by the impedance ratio so loss resistance must be managed more carefully.

9.3 Bipolar Cavity Oscillator

The schematic of a bipolar cavity oscillator [5] configuration is given in Figure 9-7. The transmission line resonator is usually a coaxial cavity A planar line such as stripline or microstrip can be used, but C1 and C2 have a very low reactance and inductance of the chip capacitors and the via hole to ground may be overwhelming. Also, unless a thick substrate is used, the unloaded Qs of stripline and microstrip are small.

The frequency is determined by the transmission line, C1, C2, and Ct, and to a lesser extent by reactive loading of the coupling inductors and the transistor. The transmission line length is just over 90^{o} long. C1 and C2 have a very low reactance, which decouples the transistor amplifier and results in a high loaded Q. The design does not require the coupling inductors, ***L,*** but physi-

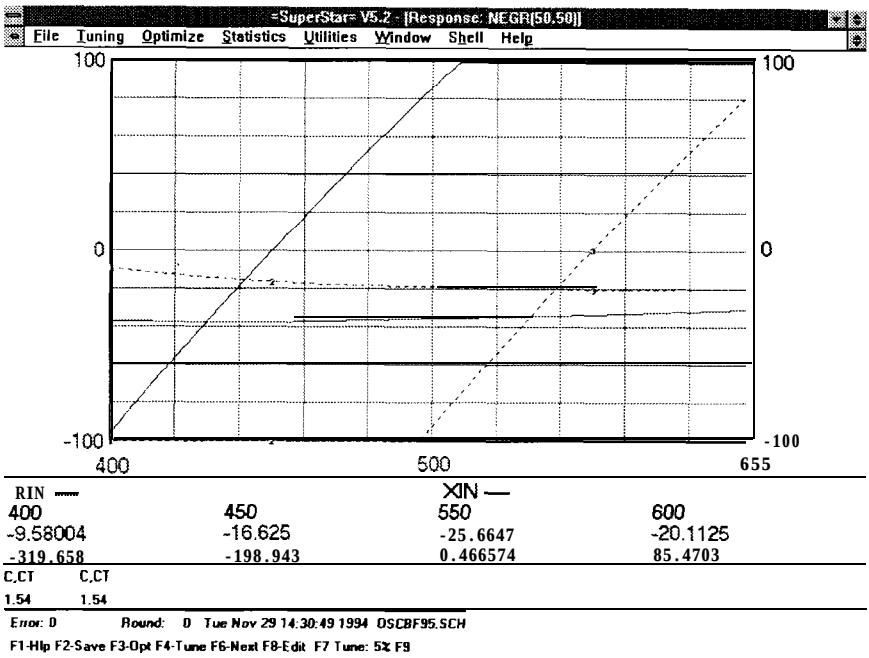


Figure 9-6 *R_{in} and X_{in} for the 450 to 550 MHz common collector VCO with an impedance transformer.*

cal construction without a method of dealing with lead inductance is very difficult at UHF and microwave frequencies. One method of construction for this configuration is shown in Figure 9-8. C_1 and C_2 are realized using flat plates separated by dielectric material, such as mica, Teflon, or another dielectric. The reactances of C_1 and C_2 are very low, and construction using leaded capacitors is generally unworkable. A possible exception is using many capacitors in parallel for a lower-frequency oscillator. The inductors L_1 and L_2 must be near the cavity cold end to avoid significant magnetic coupling via the loops formed by these inductors. Output coupling is taken from the cavity via a magnetic loop as shown, or via capacitive probe into the upper end of the cavity

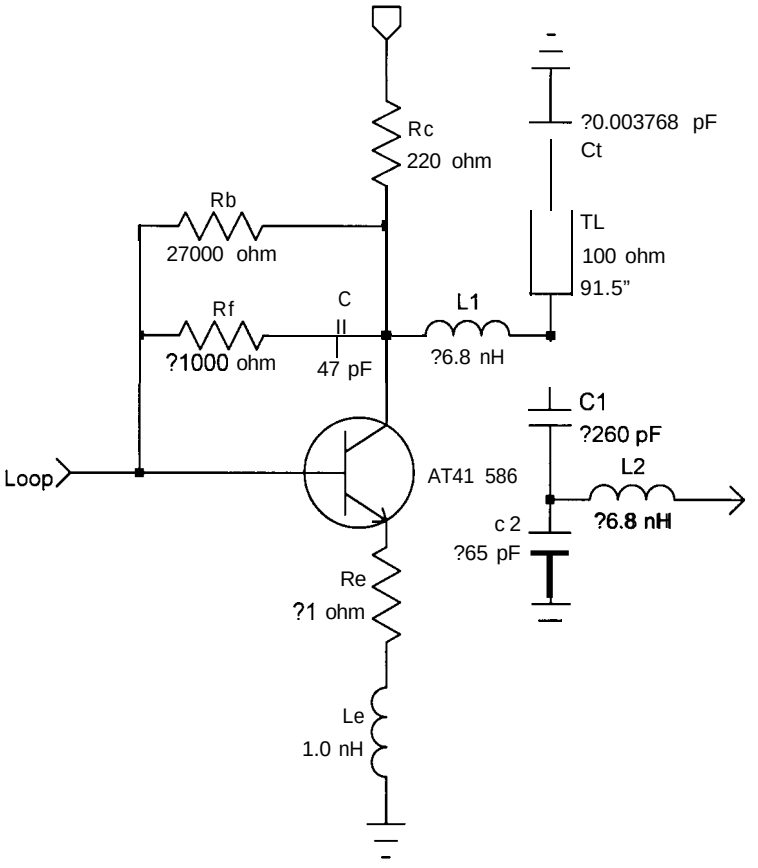


Figure 9-7 *High loaded Q coaxial cavity oscillator with a bipolar amplifier.*

9.3.1 Tuning

Narrow-band tuning can be accomplished using a trimmer screw or manufactured piston protruding into the cavity at the end opposite C_1 and C_2. In the L-C designs studied earlier, the resonator unloaded Q was determined primarily by the inductor, with capacitors Qs much higher. With high unloaded Q cavities, caution must be exercised when adding a tuning capacitor. A

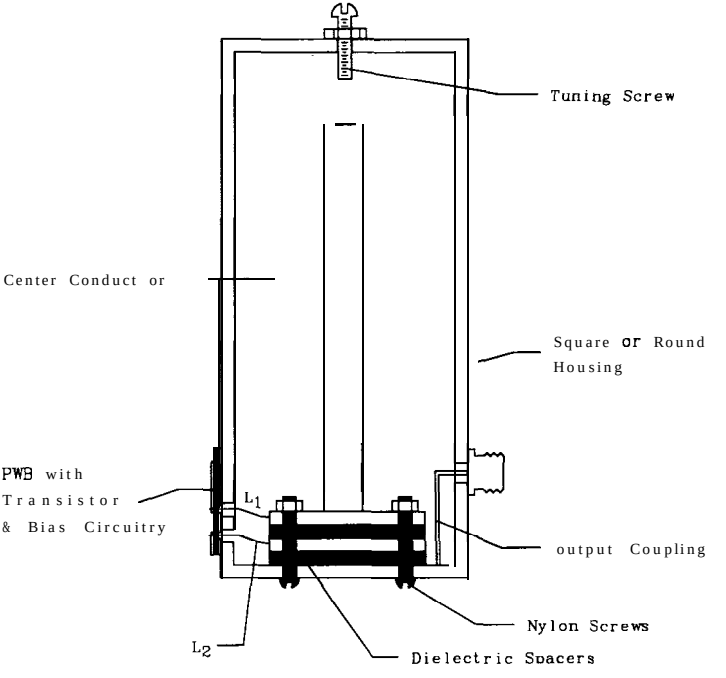


Figure 9-8 Construction of coaxial cavity bipolar oscillator.

small amount of tuning with a post rarely decreases the unloaded Q. If wide bandwidth tuning is required, the best approach is to adjust the length of the center conductor. If possible, threads should be placed near the open end of the line, where RF currents are lower. The adjusting screw mechanism is therefore within the center conductor.

Electronic varactor tuning can be added, but if tuning over more than a very narrow bandwidth is attempted, the stability is lowered severely, and the justification for the use of a cavity is questionable. The coaxial cavity oscillator is sometimes phase locked to a reference for improved long-term stability In this case, a varactor is used to tune the center frequency just enough to overcome temperature and long-term drift in the resonator. The high Q and power level typical in this oscillator result in high

resonator voltages, another reason that varactor tuning bandwidth is limited.

9.3.2 Example

The open-loop Bode response and matches for the 1100 MHz oscillator in Figure 9-7 are given in Figure 9-9. The solid traces are before optimization and the dashed responses are after optimization. The original element values shown in Figure 9-8 were found using the following relations with a loaded Q of 500.

$$L1 = L_2 = 8\times10^{-9}\left(\frac{1\times10^{9}}{f}\right)^{1.5} \qquad 9.7$$

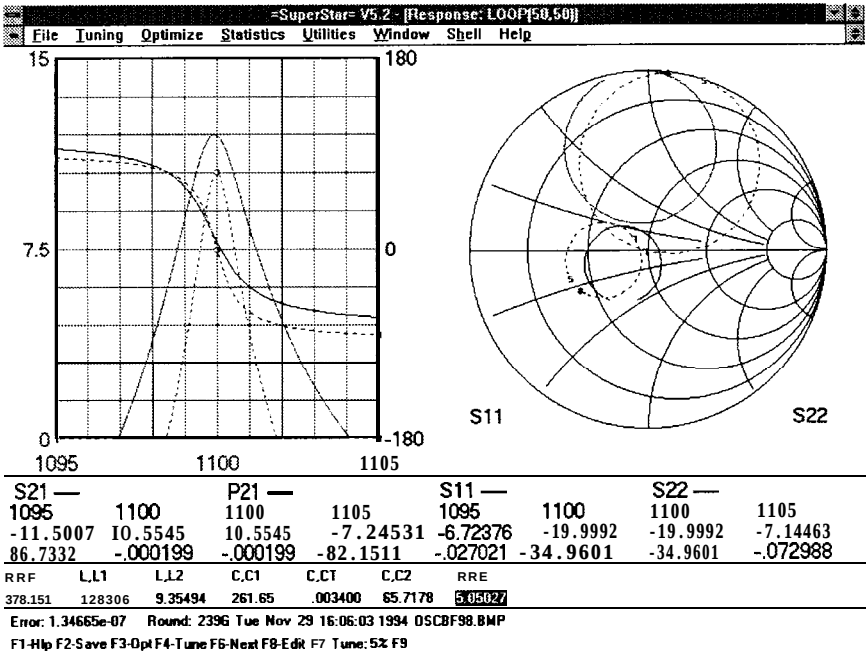


Figure 9-9 *Open loop gain and phase responses (left) before optimization (solid) and after optimization (dashed). The matches are given on the right.*

$$C_2 = \left(\frac{3.2 \times 10^{-3} Q_L}{f} \right)^{1/2} \quad 9.8$$

$$C_1 = 4C_2 \quad 9.9$$

$$\theta_e = 90 + \tan^{-1} \frac{X_{TRL}}{100} \quad 9.10$$

where

θ_e = transmission line electrical length in degrees 9.11

$$X_{TRL} = \frac{60}{Q_L^{1/2}} \quad 9.12$$

The phase zero crossing can be adjusted toward the maximum phase slope by adjusting L_1 and L_2. A disadvantage of this configuration is the difficulty of verifying the design by measurement. Although S_{11} and S_{22} are near 50 ohms, it is physically difficult to gain access to the network with connectors.

The original element values were optimized in =SuperStar= to the objectives listed in Figure 9-10. Also listed is the =SuperStar= Window block which specifies the desired parameters to plot and the desired sweep frequency

The original gain margin in Figure 9-9 is 12.5 dB. This is more than necessary so the objective is to increase the phase slope (which increases the loaded Q) by optimizing for a higher group delay at the expense of gain if required. Although the match was originally acceptible, improved matches were also requested. Finally the phase was optimized to zero-degrees at the desired oscillation frequency, 1100 MHz. The results after optimization are given as the dashed responses in Figure 9-9. The final element values are listed at the bottom on the computer screen in Figure 9-9. The final phase slope is approximately 100^o/MHz which corresponds to a loaded Q of 960.

Loss associated with finite transmission line resonator Q was not included in the TRL element in this analysis. To avoid the loop gain from falling below unity, the unloaded line Q must be several

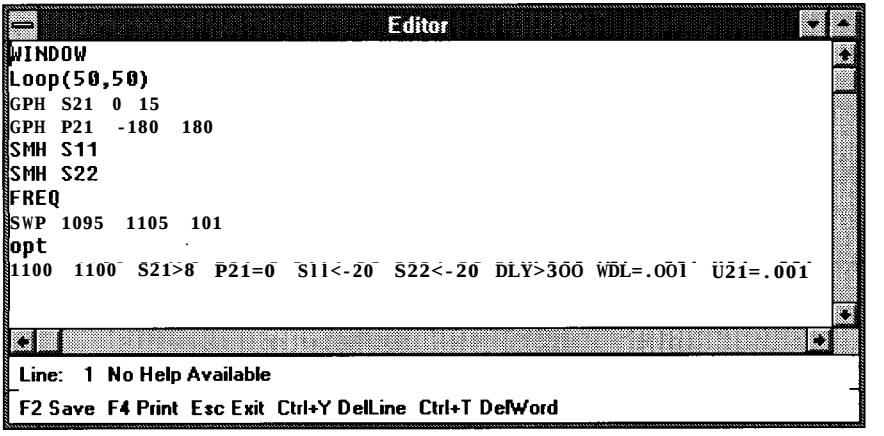


Figure 9-10 *=SuperStar= output display specifications and optimization goals for the coaxial cavity oscillator.*

times greater than 960. The unloaded Q of a coaxial cavity with an outer diameter of 1 inch is over 3500.

9.4 Hybrid Cavity Oscillator

The bipolar cavity oscillator is economical of materials, but it has the disadvantage of being difficult to verify by measurement. Because the transistor is embedded in or adjacent to the cavity, there is not a convenient point for opening the loop and measuring the Bode response. The hybrid cavity oscillator shown in Figure 9-11 consists of separate amplifier and resonator sections which may be tested individually or in cascade. The amplifier and cavity resonator may each have their own RF connectors. This high-performance oscillator can therefore be built from prepackaged connectorized components. The additional electrical length associated with the component packages and connectors is dealt with by adding a section of 50 ohm transmission line until the phase shift returns to zero-degrees. This limits the tuning bandwidth somewhat, but a tuning bandwidth of 50% is readily achieved. This oscillator design has the distinct advantage that each component can be independently specified, tested, and opti-

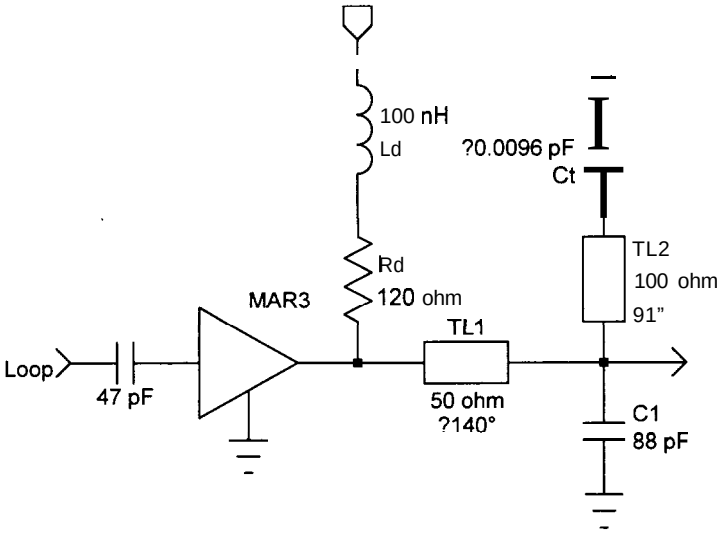


Figure 9-11 *Coaxial cavity oscillator with an MMIC amplifier.*

mized. The designer is left with an excellent characterization and understanding of oscillator behavior.

The open-loop Bode response and matches for the 810 MHz oscillator are given in Figure 9-12. The well-matched character of the Mini-Circuits MAR3 MMIC is evident from C_{11} and C_{22}. In this case, a 140^{o} length of transmission line is required to return the phase shift to zero-degrees. The frequency is tuned by the same methods as those discussed for the bipolar cavity oscillator.

Suggested element values are

$$C_1 = \left(\frac{3.2 \times 10^{-3} Q_L}{f} \right)^{1/2} \qquad 9.13$$

$$\theta_e = 90 + \tan^{-1} \frac{X_{TRL}}{100} \qquad 9.14$$

where

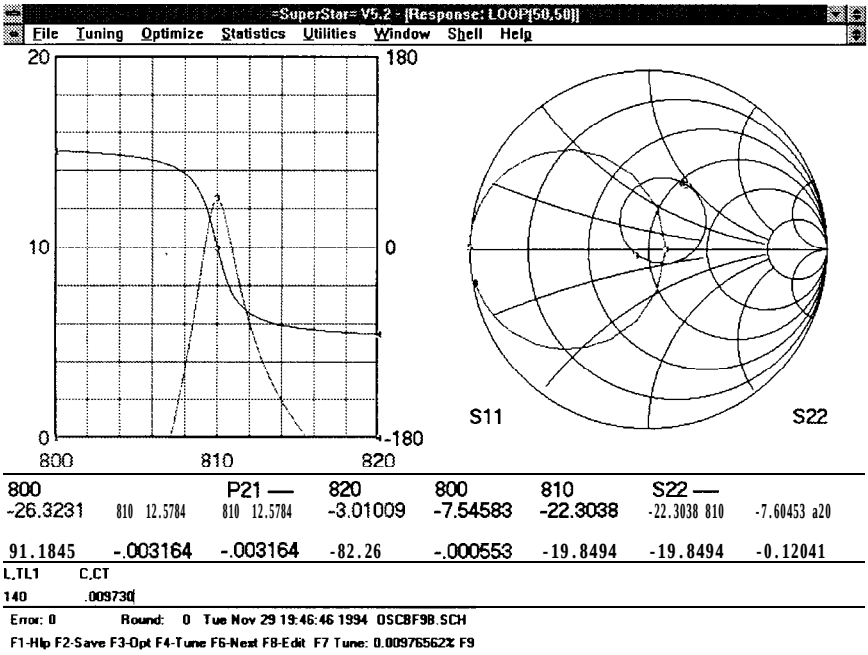


Figure 9-12 *Open loop gain and phase responses (left) and matches (right) for a coaxial cavity oscillator with an MMIC amplifier.*

θ_e = transmission line electrical length in degrees 9.15

$$X_{TRL} = \frac{50}{Q_L^{1/2}} \qquad 9.16$$

Although this oscillator is identified as an MMIC cavity oscillator, the same technique can be applied to oscillators using other active device forms. Any type of amplifier can be used. The technique is simply a direct application of the fundamental process of designing oscillators by analyzing the open loop response.

9.5 References

[1] Eagleware Corporation, 1750 Mountain Glen, Stone Mountain, GA 30087, (404) 939-0156.

[2] G. Hodowanec, Microwave Transistor Oscillators, *Microwave Journal,* June 1974, pp. 39-42,69.

[3] R. G. Winch, Oscipliers: K-Band VCOs You Build with Bipolars, *Microwaves,* November 1977, pp. 62,66-67.

[4] John R. Bender and Colman Wong, Push-Push Extends Bipolar Frequency Range, *Microwaves & RF,* October 1983, pp. 91-92, 94,96,98.

[5] Carl F. Klein, Microwave Oscillator Design, *Frequency Technology,* November 1969, pp. 13-19.

10

SAW Oscillators

High-Q oscillators up to 200 MHz are built using bulk quartz crystal resonators. For UHF and microwave frequencies, transmission line and cavity oscillators offer higher Q than L-Cdesigns, but they are larger SAW resonators fill the need for small high-loaded-Q oscillators in the frequency range 200 to 1,200 MHz. Typical unloaded Qs are 6,000 to 12,000.

SAW resonators are commercially available in both two-terminal and two-port forms. As with bulk quartz crystals, tuning is difficult. The operating frequency is set at the time of manufacture, so SAWs must be tooled and stocked for each oscillator frequency requirement.

The shunt capacitance, Co, of SAW resonators is proportionally smaller than the parallel capacitance of bulk crystal resonators. Therefore, the SAW oscillation frequency can be pulled farther. This advantage is somewhat mitigated by the fact that the initial tolerance and stability are poorer, and often a significant portion of the pulling range is required just to "net" the oscillator frequency Additional information on SAW resonators is given in Section 2.15. Three different oscillator configurations using SAW resonators are considered next.

The bipolar SAW oscillator uses a common-emitter amplifier configuration and a two-terminal SAW resonator. It is a cost-effective design. The hybrid and dual-gate MOSFET oscillators use two-port SAW resonators. The hybrid SAW design results in an excellent characterization of oscillator performance and is the best choice if frequency pulling is required. The dual-gate MOS-

FET design has had widespread application, and can be used with 0^o or 180^o resonators by reversing the transformer leads.

10.1 SAW Bipolar Oscillator

This oscillator uses a two-terminal 180^o SAW resonator cascaded with a simple common-emitter bipolar amplifier. The schematic for a 637 MHz oscillator is shown in Figure 10-l. Similar circuits are found in several references [1-3].

Suggested element values are

$$C_3 = \frac{1}{66\pi f} \qquad 10.1$$

$$C_2 = \frac{C_1}{2} \qquad 10.2$$

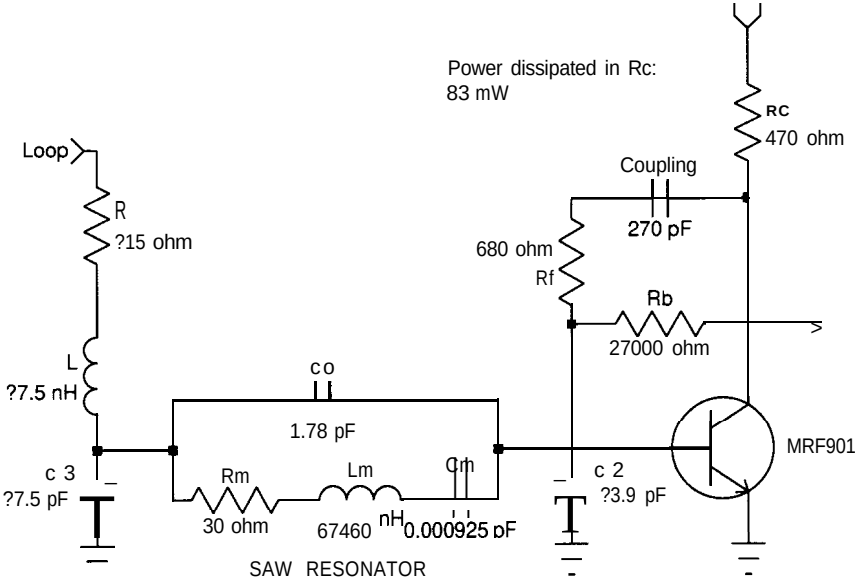


Figure 10-l A 637 *MHz two-terminal SAW oscillator using a common-emitter bipolar transistor.*

$$L = \frac{5}{f} \qquad 10.3$$

The characteristic impedance is approximately 50 ohms. The phase response zero crossing is adjusted using the inductor, L. C3 and C2 adjust the loaded Q, with increasing capacitance increasing the loaded Q. Adjusting the ratio of C3 and C2 may yield an improved match of S11 and S22 to Z_O.

The open-loop Bode response is shown in Figure 10-2. The phase response has two zero crossings. This characteristic is a result of Co of the SAW resonator. The phase zero crossing at the higher frequency occurs near the SAW parallel resonance where there is little transmission and therefore poses no threat as an oscillation frequency ambiguity. Notice the oscillation frequency (marker 3

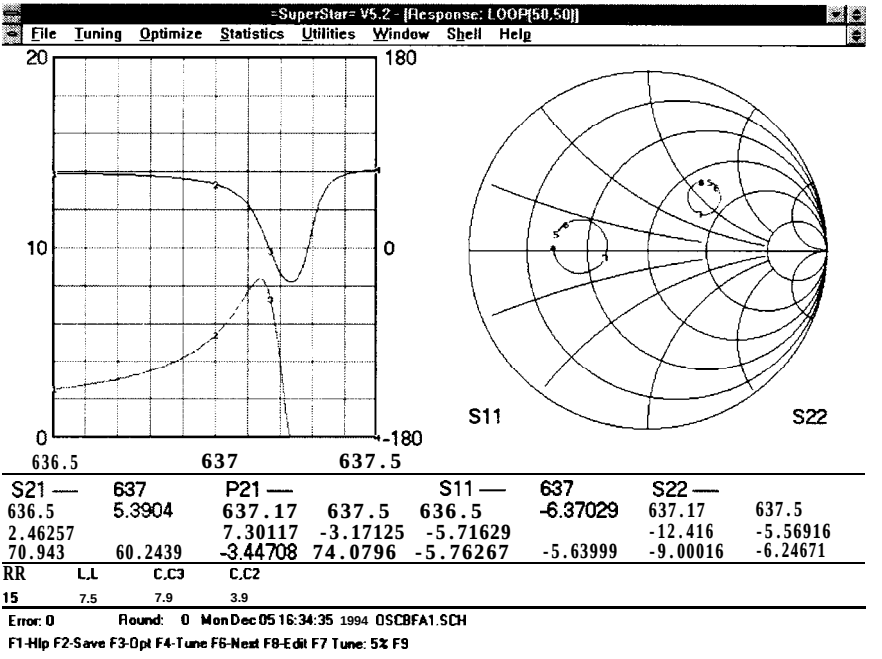


Figure 10-2 *Open loop gain and phase responses (left) and matches (right) for the 637 MHz two-terminal SAW oscillator.*

at 637.17 MHz is higher than the resonant frequency of the SAW (637.127 MHz).

Temporarily modifying the simulator file to plot the group delay yields a value of 2200 nS. This corresponds to a loaded Q of 4404. The unloaded Q of the SAW resonator (X_{Lm}/R_m) is 9002.

This oscillator can be temperature compensated by tuning C2 with a varactor driven by a temperature-dependent voltage source. The temperature stability of the SAW oscillator is improved by almost an order of magnitude [3] using this technique. SAWs, as well as bulk crystal resonators, have a frequency versus temperature curve with a "turnover" temperature point where the temperature coefficient is zero. The turnover temperature is a function of the crystal cut. Typical SAW oscillator Q, temperature stability, aging, and initial manufacturing tolerance are about an order of magnitude worse than those of bulk crystals.

10.1 .l Output Coupling

Output is normally taken from the collector. Fairly tight coupling can be used such as a coupling reactance of 100 ohms. If tight coupling is used, the coupling reactance and load should be added to simulate the effect of the loading on the gain margin. More stable operation is obtained with somewhat looser coupling. The output can be taken at C3 for lower harmonic levels, but looser coupling should be used.

10.2 SAW Hybrid Oscillator

This oscillator uses a two-port zero-degree SAW resonator. As with the hybrid cavity oscillator, a transmission line section is added to adjust the open-loop phase-response zero crossing so that it occurs at maximum phase slope. This oscillator, as with the L-C hybrid oscillator, consists of individual elements, each of which is well matched to 50 ohms. Therefore, performance verification by measurement of open-loop parameters is straightforward. The schematic of a 300 MHz SAW oscillator of this type is

shown in Figure 10-3. The added transmission line in this case is 94^{o} long.

10.2.1 Tuning

The center frequency may be tuned slightly with the input inductor, *L*. A more effective tuning method is adjustment of the transmission line phase length. A meander line is trimmed, or an electrically tunable phase shift network is used. Consider Figure 10-4. The open loop-Bode response is given for the 300 MHz SAW oscillator with the nominal transmission line length of 94^{o}.

In Figure 10-5, the length of the transmission line cascaded with the amplifier and resonator is adjusted from 149 (solid curves) to 39 (dashed curves). The oscillation frequency as predicted by the phase zero crossing ranges from 299.94 MHz to 300.06 MHz. Notice that neither the gain (on the left) or the group delay responses (right) change with transmission line length. Because of this, the gain margin at 299.94 MHz (marker 2) is only 1.7 dB and the gain margin at 300.06 MHz (marker 3) is only 2.3 dB.

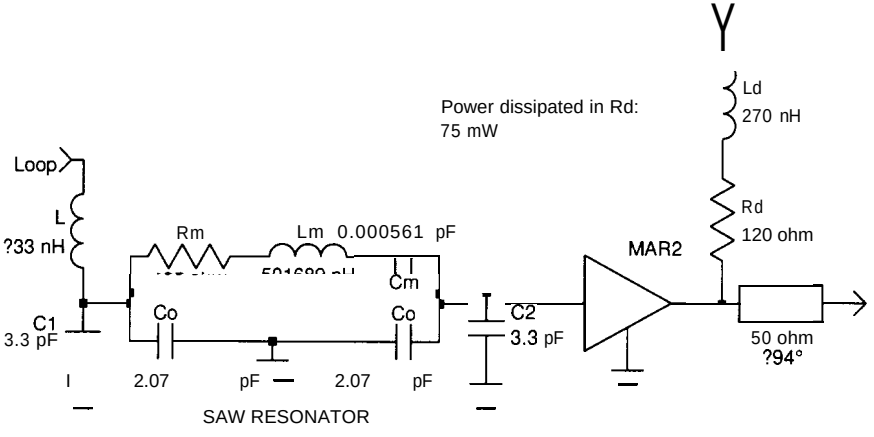


Figure 10-3 *Two-port SAW oscillator using a Mini-Circuits MMIC amplifier.*

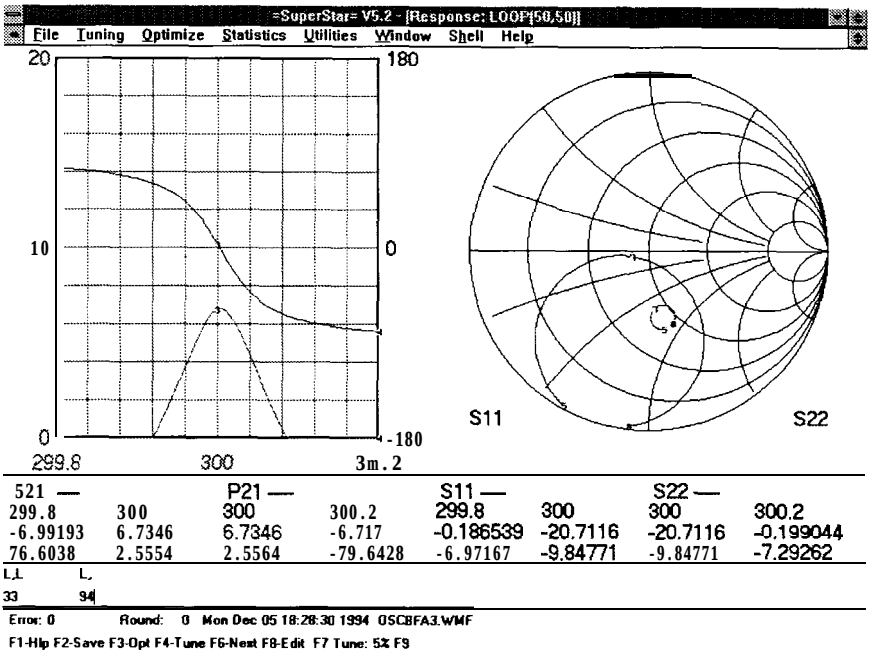


Figure 10-4 *Open loop gain and phase responses (left) and matches (right) for the two-port* **SAW** *oscillator.*

Wider tuning results in inadequate gain and loss of oscillation. With less gain margin less output level is expected as the frequency is tuned above or below the nominal frequency

The group delay at the nominal frequency (marker 8) is 3720 nS. This corresponds to a loaded Q of 3506. The group delay (and therefore the loaded Q) at the tuning extremes is one-third the group delay at the nominal frequency This is a direct consequence of operating off the peak slope of the loop phase response. Since the phase noise performance is proportional to the loaded Q squared, a drop of approximately 10 dB in the phase noise performance at these tuning extremes is expected.

When the resonator frequency is tuned, as with L-C and cavity resonators, the peak delay tracks with or near the phase zero crossing and the loaded Q does not degrade with tuning. SAW

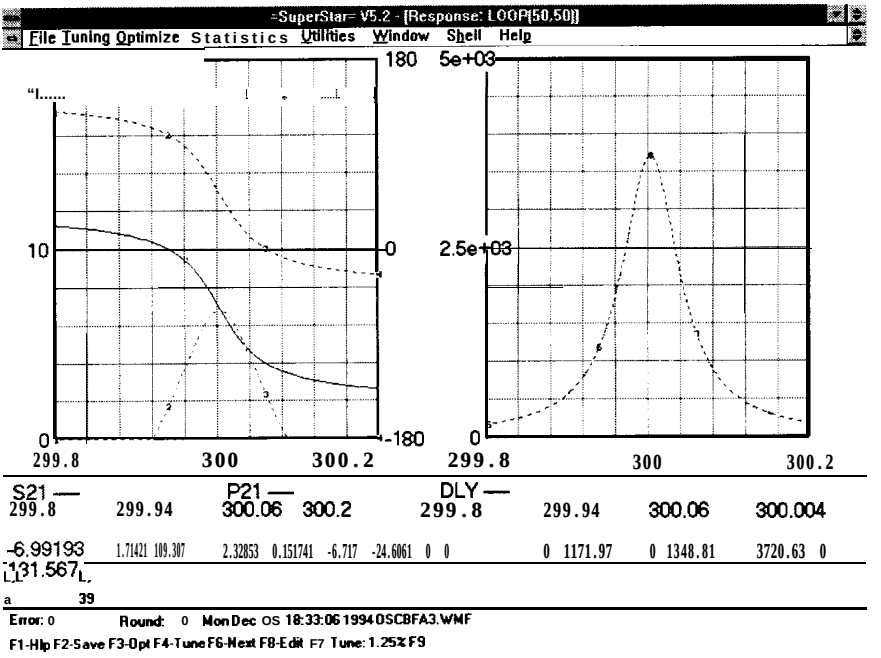


Figure 10-5 Open loop gain and phase (left) and group delay (right) with the transmission line length adjusted from 149 (solid) to 39 (dashed).

and bulk crystal resonator element values are set at the time of manufacture, and pulling the frequency of these oscillators by tuning external elements results in lower loaded Qs.

10.2.2 Element Values

Suggested element values are

$$C = \frac{(R_r - 1)^{1/2}}{2\pi f(R_m + 30)} \qquad 10.4$$

If C > Co, then C1 = C – Co, else C1 = 0 10.5

$$C_2 = C_1 \tag{10.6}$$

$$L = \frac{(R_m + 30)(R_r - 1)^{1/2}}{2\pi f R_r} \tag{10.7}$$

$$\theta_e = 115^{\circ} - 0.067 \times 10^{-6} f \tag{10.8}$$

where

$$R_r = \frac{R_m + 30}{50} \tag{10.9}$$

The characteristic impedance is approximately 50 ohms. The loaded Q is adjusted with C_1 and C_2. Increasing C_1 and C_2 increases the loaded Q. Increasing C_1 and C_2 also increases the operation frequency slightly, reduces the loop gain, and reduces the required length of the transmission line.

Decreasing the inductor, L, increases the loaded Q. L can also be used to adjust the input match, S_{11}. Decreasing L increases the required transmission line length.

10.2.3 Output Coupling

Output is normally taken at the output of the MMIC. The remarks on coupling in the SAW bipolar oscillator also apply to this configuration.

10.3 SAW Dual-gate FET Oscillator

One of the more common SAW oscillators uses a dual-gate MOS-FET [illegible]
Figure 10-6. The open-loop response and matches for this oscillator are given in Figure 10-7.

The series resonant frequency of the SAW used in this example is 949.836 MHz. As can be seen, the Bode phase response zero crossing occurs at 950.02 MHz, 184 kHz igher. Adding shunt capacitors to ground at the input and output of the SAW resonator

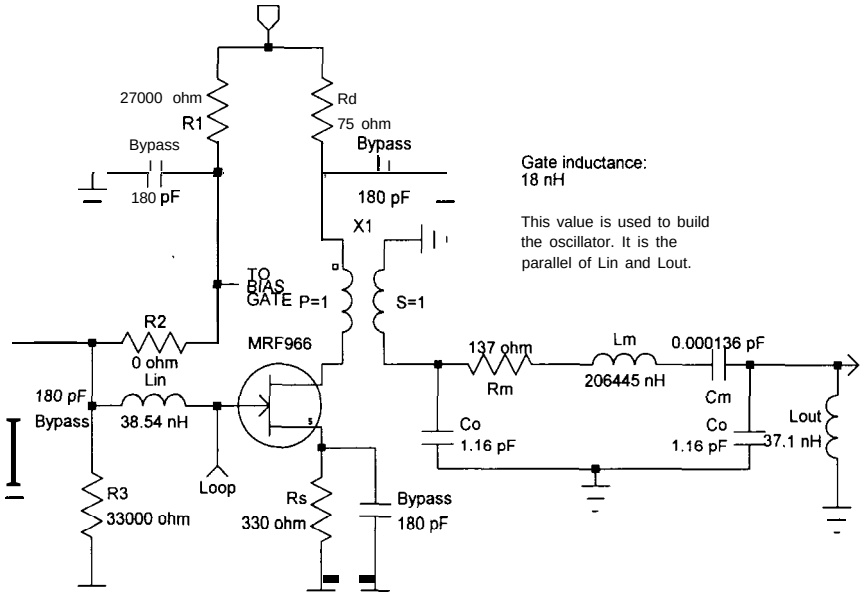


Figure 10-6 950 *MHz* SAW *oscillator with a MOSFET active device.*

pulls the operating frequency closer to the resonant frequency of SAW and increases the loaded Q. Unfortunately, it also decreases the already low loop gain. The loaded Q computed from the 229 KHz 3 dB bandwidth of the gain response is approximately 4148.

The input impedance of MOSFETs is capacitive with a high resistive component. In this case an analysis reference impedance of 1000 ohms. This makes verification of the loop characteristics by network analyzer measurement more difficult. However, adjustment of the reference impedance to the actual value improves the match for computer analysis. Notice the expanded polar plot of the loop matches in Figure 10-7 where the radius of the chart is 20 dB return loss.

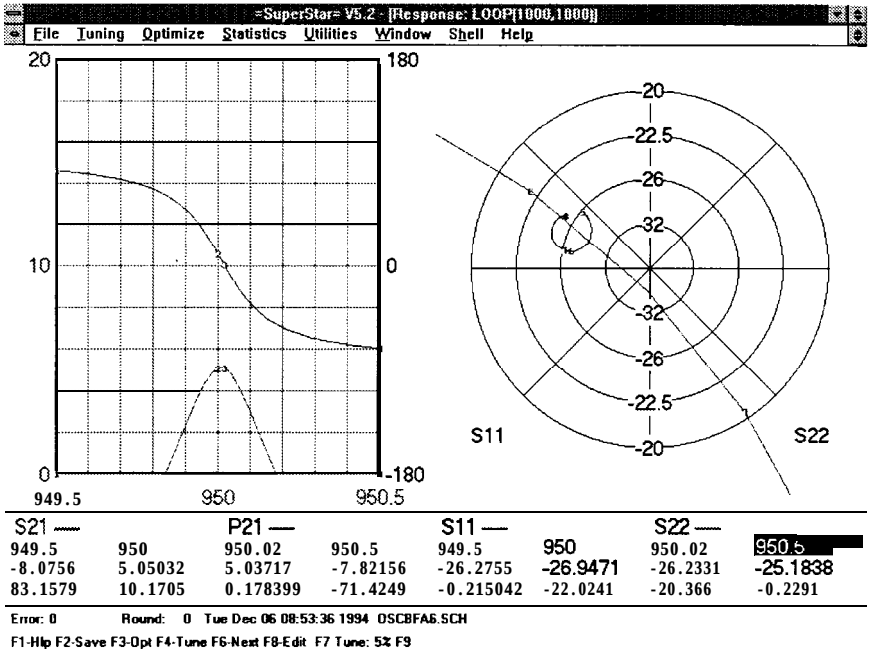


Figure 10-7 *Open loop gain and phase responses (left) and matches (right) for the 950 MHz SAW oscillator using a MOSFET device.*

The capacitive component of the MOSFET input impedance is tuned out with the inductor L_{in}. The output of the loop is also capacitive which is tuned out with L_{out}. In the final oscillator, *Lin* and *Lout* are combined to form a single inductor with a value equal to the parallel combination of *Lin* and *Lout. The* inductor is split for analysis to give a good match for S11 and S_{22}. The drain transformer can generally be replaced with an inductor of high reactance. The loop gain can be increased by reducing the reactance of this inductor, but the loaded Q is reduced.

Historically, this oscillator has been constructed using a transformer, and the circuit is "tweaked" by adjusting the coupling of the primary and secondary windings. Using a transformer has the advantage that either a zero-degree two-port SAW resonator

can be used, or by reversing the sense of the transformer, a 180 two-port resonator can be used.

10.3.1 Element Values

In the oscillators studied previously, a design independent of the active device parameters was an important goal. This naturally results in an oscillation frequency that is insensitive to device variations and changes with time and temperature. It also simplifies design and results in designs that work well with a wide variety of devices. Oscillator designs with high unloaded Q resonators such as SAW and bulk quartz crystal require less device independence.

The element values and the optimum analysis impedance of the MOSFET SAW oscillator are significantly affected by device parameters. To find element values, the MOSFET input and output admittances, Yin and Y_{out}, are determined. The admittances can be read from data sheets or computed from S11 and S_{22}.

If

$$Y_{\text{in}} = G_{\text{in}} \pm jB_{\text{in}} \tag{10.10}$$

then

$$Z_{\text{o}} = \frac{1}{G_{\text{in}}} \tag{10.11}$$

$$L_{\text{in}} = \frac{1}{2\pi f B_{\text{in}}} \tag{10.12}$$

Z_o is the Bode response analysis impedance. Then

$$L_{\text{out}} = \frac{Z_{\text{o}}}{2\pi f(2\pi f\, Z_{\text{o}} C_{\text{o}} - \text{Q})} \tag{10.13}$$

where

$$Q = \left(\frac{Z_o}{R_t} - 1\right)^{1/2} \qquad 10.14$$

$$Y_{out} = G_{out} \pm jB_{out} \qquad 10.15$$

$$Y_t = B_{out} + 2\pi f C_o \qquad 10.16$$

$$R_t = \frac{R_m + G_{out}}{G_{ut}^2 + Y_t^2} \qquad 10.17$$

When these formulas are used the analysis is exactly matched to Z_o. Ideally, the oscillator is trimmed for maximum output by adjusting the inductor, *L*, which is the final parallel combination of *Lin* and *The* oscillator is often trimmed by spreading or compressing the transformer windings.

10.3.2 Output Coupling

The output is taken from the MOSFET drain. A high coupling reactance is used to avoid loading the high impedance at the drain. A coupling reactance of 300 to 500 ohms is typical.

10.4 References

[1] W. J. Tanski, UHF SAW Resonators and Applications, Proceed*ings 34th Annual Frequency Control Symposium,* IEEE, May 1980.

[2] C. Bennett, SAW Resonator Stabilized Oscillator, *Proceedings 37th Annual Frequency Control Symposium,* IEEE, 1983, pp. 405-409.

[3] J. Ladd, C. Abdallah, and T. O'Shea, A Temperature Compensated L-Band Hybrid SAW Oscillator and Resonator Filter, *Proceedings of the 1984 Ultrasonics Symposium,* IEEE, 1984.

[4] F. H. Perkins, Technique Aids SAWR Oscillator Design, *Microwaves & RF,* March 1984, pp. 153-155,182-183,185.

11

Quartz Crystal Oscillators

Oscillators using quartz crystal resonators are the epitome of phase noise and stability performance. Marvelously high loaded Q oscillators of small size and low cost are easily designed and built using the quartz crystal. Crystal oscillators were invented in the 1920s [1]. By the 1930s, several designs had ***been*** *published and patented. Crystal resonator and oscillator development was intense during and after World War II. During the 1950s, the art encompassed harmonic operation at VHF frequencies. Today, crystals are a common component of nearly all consumer commercial, and defense systems.*

Crystal Oscillator Circuits [1] is an excellent reference on crystal oscillator design. It contains a plethora of practical circuits, tips, and techniques. The number of different crystal oscillator circuits in use is phenomenal. In this chapter, five crystal-controlled oscillators are studied which are representative of many available choices. The first is the Pierce. The author recommends it as the oscillator of choice for standard fundamental mode applications. The second, a fundamental parallel mode Colpitts is included with less enthusiasm because of its popularity The third example is a high-performance crystal oscillator with excellent short-and long-term stability characteristics. It was first proposed by Driscoll and has been used in several variations. The fourth is a Butler overtone oscillator useful for VHF applications. The fifth oscillator, a Butler derivative, is operated at either fundamental or overtone, and includes a built-in frequency multiplier. This form includes improvements developed by the author.

11.1 Pierce Crystal Oscillator

The Pierce is an excellent fundamental-mode-series resonant crystal oscillator circuit. The bipolar transistor 15 MHz Pierce oscillator shown in Figure 11-1 works well with AT-cut crystals from about 600 kHz up to 20 or 30 MHz, the practical fundamental-mode limit. Other quartz crystal cuts can be used for frequencies below 600 kHz. The Pierce can be designed to work with overtone crystals by replacing Cl with a parallel resonant tank to ensure operation at the desired overtone. R, Cl, the resonator, and C2 form a selective phase shift network with approximately 180^{o} of phase shift. Unfortunately, the open-loop impedance of this oscillator is greater than 50 ohms, so verification of the open-loop gain and phase response is more difficult.

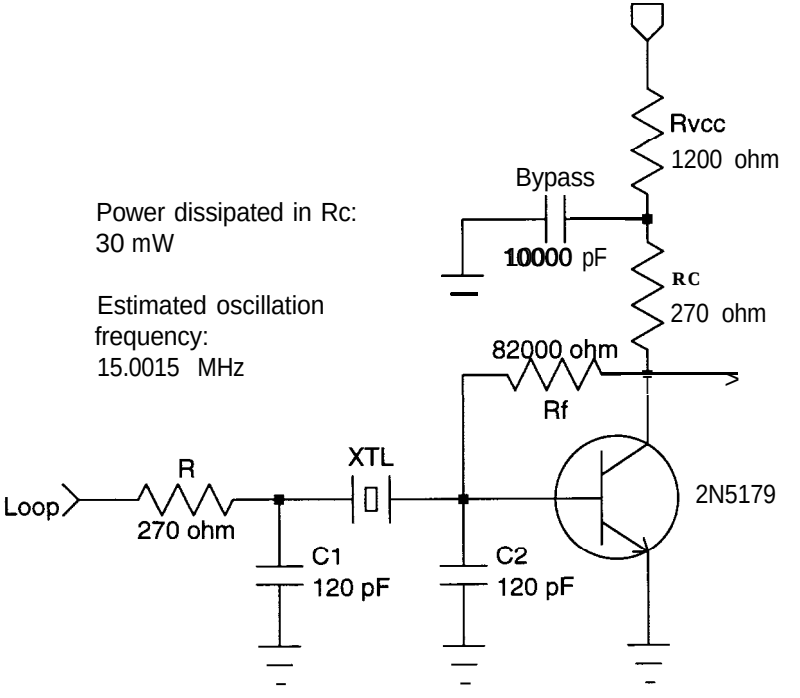


Figure 11-l *A* ***15 MHz*** *quartz crystal fundamental-mode Pierce oscillator.*

The Pierce oscillates just above the series resonant frequency of the crystal. If necessary, the Pierce can be operated exactly at series resonance by adding an additional R-C phase shift network in the transmission path. The oscillation frequency approaches the series resonant frequency as Cl and C2 are increased. A capacitor may be placed in series with the crystal to tune the oscillation frequency Decreasing the value of this capacitor increases the oscillation frequency A large capacitance value results in the lowest possible oscillation frequency for given shunt coupling capacitors. This frequency is slightly higher than the crystal-series resonant frequency As the value of this series capacitor approaches the crystal parallel capacitance, Co, the loop gain falls off significantly Pulling is considered in detail in Section 2.13.

11.1.1 Loaded Q

Shown in Figure 11-2 are the open-loop gain, phase and group delay responses of the 15 MHz Pierce oscillator. The crystal parameters used for this analysis were Co = 4.18 pF, Cm = 0.01275 pF, Lm = 8.83 mH and *Rm* = 27 ohms. The solid curves are the responses with Cl and C2 values of 120 pF The open-loop gain peaks just over 16 dB near the phase zero crossing at 15.0012 MHz (marker 3). The delay at f_o is approximately 3.8 $\times 10^5$ nS which corresponds to a loaded Q of 17,900. The unloaded Q of the crystal resonator computed by dividing the motional inductor reactance by the 27 ohm series resistance is 30,800. The loaded Q is therefore 58% of the unloaded Q.

The dotted responses in Figure 11-2 result when C_1 and C_2 are increased to 270 pF. The phase zero crossing is closer to the series resonant frequency of 15 MHz. The loop gain drops to about 6 dB. The delay increases to 4.87 x 10^5 nS, which corresponds to a loaded Q of 22,900. This is 74% of the unloaded Q.

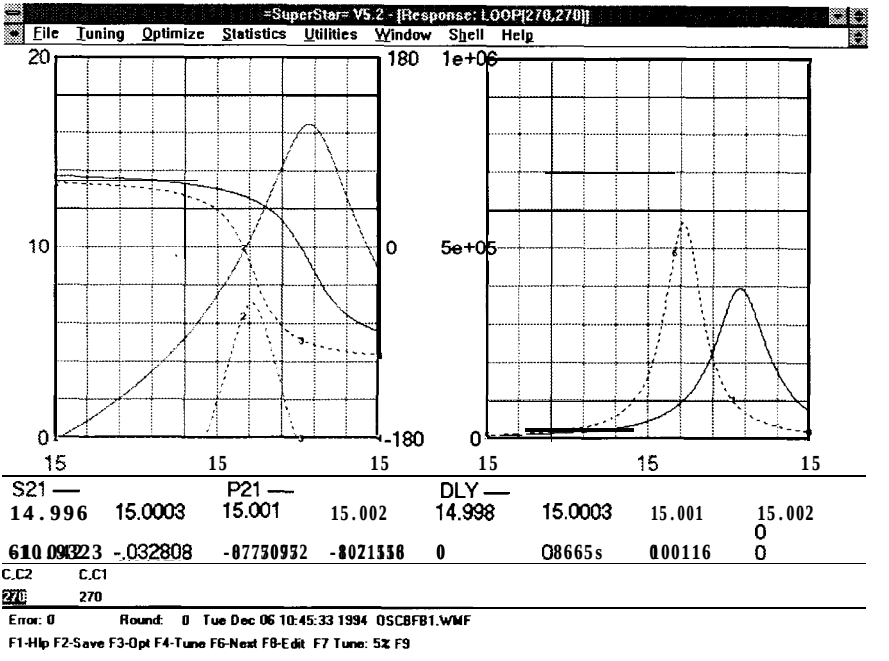


Figure 11-2 *15 MHz Pierce crystal oscillator open loop gain and phase responses (left) and group delay (right) with 120 pF shunt coupling capacitors (solid traces) and 270 pF coupling capacitors (dashed traces).*

11.1.2 Element Values

The nominal value of C_1 and C_2 is

$$C_1 = C_2 = \frac{2000 \times 10^{-12}}{1 + 10^{-6} f} \qquad 11.1$$

R and R_c are then

$$R = R_c = \frac{3}{2\pi f C_1} \qquad 11.2$$

11.1.3 Dissipation

The transistor should be biased at a quiescent power level of 10 mW or less to avoid damage to the quartz resonator. For best aging characteristics, the power level should be much lower than this. Refer to Section 2.12. The voltage across the crystal in this circuit is about 0.2 to 0.6 volt peak to peak for Vce = 5 volts and I_c = 1 to 2 mA. This bias is suitable for best phase noise performance. As the oscillator power level is reduced to improve aging characteristics, it often becomes necessary to add a buffer to amplify the oscillator output. The lower oscillator power level and the buffer both increase the phase noise at larger carrier offset frequencies.

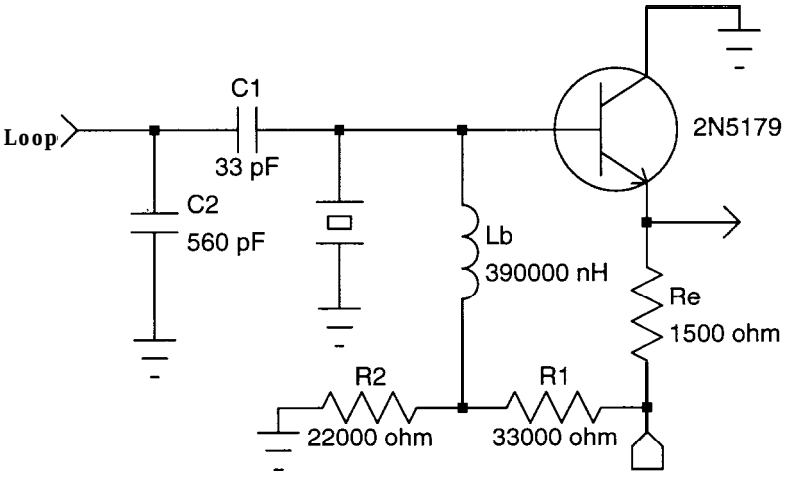
The resistor R is sometimes not included in the Pierce oscillator. This increases the loop gain, but it also significantly increases the dissipation in the crystal. When R is excluded, the transistor quiescent power level should be 1 mW or less to avoid possible crystal damage.

11.2 Colpitts Crystal Oscillator

The Colpitts crystal oscillator is a parallel resonant circuit for fundamental-mode crystals. The bipolar transistor amplifier is an emitter follower and voltage gain is developed by a capacitive-tap impedance transformer. A 5 MHz example is shown in Figure 11-3. The series combination of C_1 and C_2, in parallel with the effective transistor input capacitance, form the crystal loading capacitance. The crystal parameters used for this analysis were C_o = 4.18 pF, Cm = 0.01275 pF, *Lm = 79.5* mH and *Rm* = 45 ohms.

11.2.1 Limitations

The gain and phase responses (left) and matches (right) are given in Figure 11-4. Notice the presence of two phase zero crossings. The zero crossing at the lower frequency (marker 2) occurs at the series resonant frequency of the crystal and the gain is well below unity so it does not represent a oscillation frequency ambiguity



F'igure 11-3 *Schematic of a 5 MHz Colpitts crystal oscillator.*

Unfortunately, the phase slope at the desired zero crossing (marker 4) is lower than the maximum phase slope (marker 3). This problem is difficult to correct in the Colpitts crystal oscillator. It is a fundamental performance limitation of this configuration. Also examination of S11 and S22 on the right in Figure 11-4 reveals poor input and output matching.

Although this circuit is simple and economic of components, the operation mode is fairly complex. The transistor operates in the active region during a small fraction of the oscillation period; therefore, crystal loading is dynamic. For these reasons, the Pierce crystal oscillator is a preferred circuit. The Colpitts crystal oscillator circuit is included here because of its widespread use.

The Colpitts crystal oscillator may be netted by adjusting C_1 or by placing a reactance in series with the crystal. Because of the difficulty of retaining phase slope at the phase zero crossing, the Pierce crystal oscillator is a better choice when substantial pulling is required.

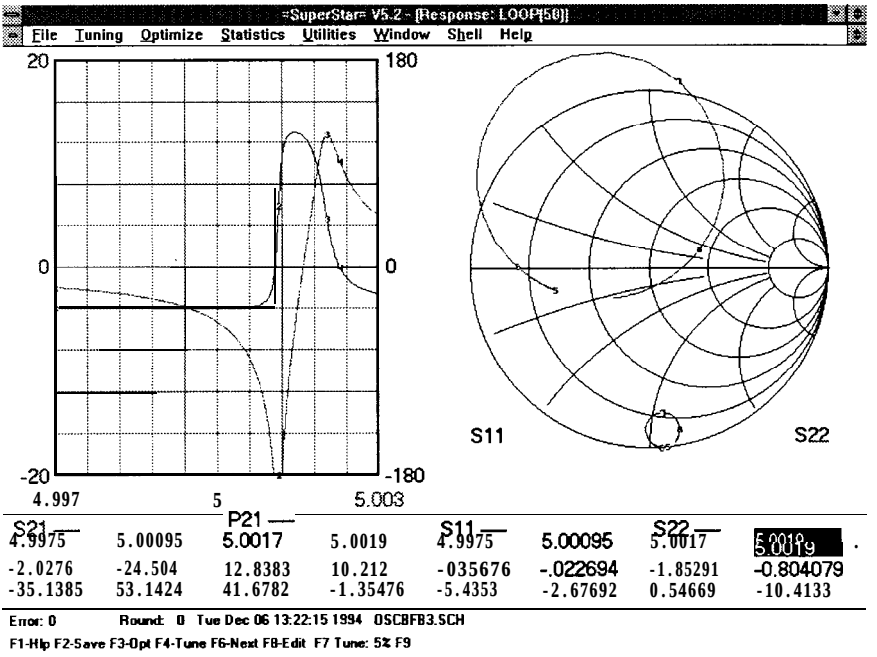


Figure 11-4 *Open loop gain and phase responses (left) and matches (right) for the 5 MHz Colpitts oscillator.*

11.2.2 Element Values

Nominal values are

$$C_2 = \frac{60 C_{\text{load}}}{f} \tag{11.3}$$

$$C_1 = \left(\frac{1}{C_{\text{load}}} - \frac{1}{C_2} \right)^{-1} \tag{11.4}$$

where

$$\text{Cload} = \text{desired crystal load capacitance} \tag{11.5}$$

The load capacitance is generally specified as 32 pF, or perhaps 20 pF at the higher end of the frequency range. The best analysis

impedance is approximately 100 ohms, although 50 ohms may be acceptable at the higher end of the frequency range.

The emitter resistor is generally large because the emitter current is low to avoid excess dissipation in the quartz crystal. Therefore, it is seldom necessary to add an emitter inductor.

11.2.3 Comments

The Colpitts crystal oscillator configuration requires a high crystal load resistance, particularly at lower frequencies, where the crystal resistance is higher. For operating frequencies lower than about 1 MHz, a JFET should be substituted for the bipolar transistor.

The high crystal load resistance requirement dictates that R_1, R2, and Lb be as large as possible. R_1 in parallel with R2 should be at least 12 kΩ, and preferably greater. The common node of these components should not be bypassed.

11.3 High-Performance Crystal Oscillator

The crystal oscillator configuration shown in Figure 11-5 is due to Driscoll [2]. Although more complex than single-stage crystal oscillators, it exhibits excellent performance characteristics. All resistors in the circuit except R_8 are bias resistors. R_8 stabilizes the common base transistor. The configuration is a cascade amplifier with the crystal in series with the emitter of the input common-emitter transistor, Q_1. The high-impedance output of the common-base output transistor, Q_2, is transformed down to the moderate input impedance of Q_1 via the phase shift network consisting of C_1, L, and C_2. Driscoll described two similar configurations of this oscillator. The configuration given here avoids the use of a tapped inductor.

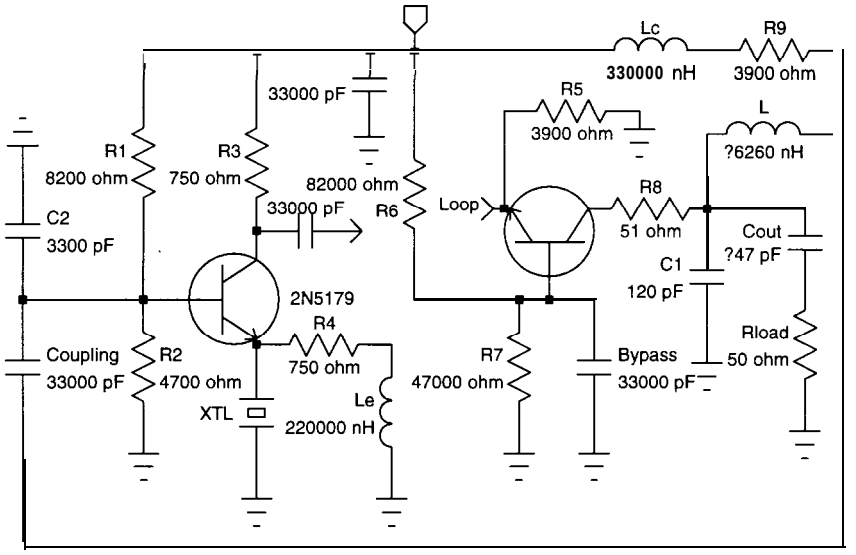


Figure 11-5 *Schematic of the Driscoll high-performance crystal oscillator.*

11.3.1 Performance

The excellent performance of the Driscoll crystal oscillator is attributable to:

(a) High loaded-Q

(b) Limiting in a second stage isolated from the crystal

(c) Moderate power level with low crystal dissipation

High loaded Q is critical to low-noise oscillator performance. The emitter of the grounded base transistor presents a low impedance to the collector of the first transistor which lowers the effective resistance in series with the crystal. This maximizes the cascade loaded Q. The majority of the resistance in the emitter of Q_1 at resonance is the series resistance of the crystal. Therefore, the loaded Q of this oscillator approaches the unloaded Q of the crystal.

The bias current in Q2 is set at a fraction of the current in Q_1. As oscillation builds, limiting first occurs in Q2, and Q1 remains in a linear active mode. Since Q1 never saturates or cuts off, the load impedance presented to the crystal remains low for the entire oscillation period. Linear operation of the sustaining stage minimizes up-conversion (modulation) of the baseband noise on the carrier.

As discussed earlier, the requirements of moderate power level for best phase noise performance and low crystal dissipation for best aging characteristics are conflicting requirements. The Driscoll crystal oscillator provides a moderate power level, typically 3 to 6 dBm, with low crystal dissipation, typically 50 to 100 μW.

11.3.2 Low-Frequency Overtone Crystals

The highest unloaded crystal Q in the HF region (2.5 to 15 MHz) is achieved by using a lower-frequency quartz crystal and operating at the third or fifth overtone. The resulting series resistance is greater but the motional inductance is increased significantly and more than compensates for the higher resistance. The higher series resistance is an advantage with the Driscoll oscillator since a given effective series resistance in Q1 will degrade the unloaded Q even less.

A typical high-precision 5 MHz fifth-overtone crystal resonator in a vacuum-sealed glass holder might have a resistance of 120 ohms and a motional inductance of 8 henries. This is an unloaded Q of over 2 million. A more economical 5 MHz fundamental-mode crystal might have a series resistance of 35 ohms, a motional inductance of 110 mH, and an unloaded Q of about 100,000.

11.3.3 Example

The open loop responses of the 5 MHz Driscoll oscillator given in Figure 11-5 are given in Figure 11-6. The gain and phase are given on the left and the group delay is given on the right. The sweep frequencies are from 4.999975 to 5.000025 MHz or which

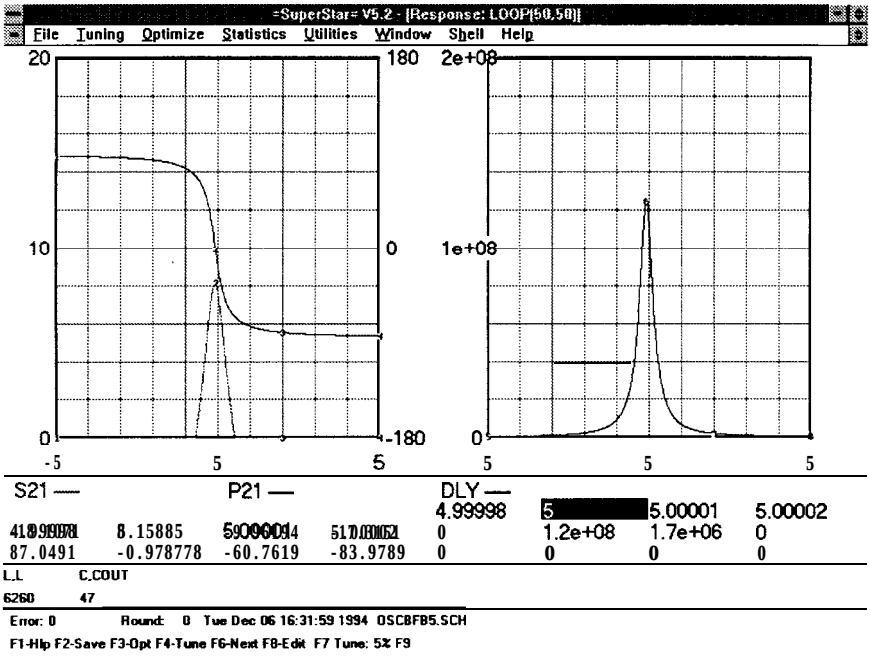


Figure 11-6 *High-performance 5 MHz Driscoll oscillator gain and phase responses (left) and group delay (right).*

is only 5 Hz per division! This exceeds the display resolution of the =SuperStar= simulator program which indicates start and stop frequencies of 5 MHz. However, the resolution of crystal parameters in =SuperStar= is approximately one tenth of a part per million which is more than adequate for analysis of crystal circuits.

The capacitor Cl has been tuned so that the phase zero crossing occurs near the maximum phase slope. Notice that the gain peak occurs at the maximum phase slope and that the phase zero crossing (oscillation frequency) is at the series resonant frequency The open-loop gain at the phase zero crossing is about 10 dB. The open-loop analysis includes a 50 ohm output load coupled to the limiting stage collector via a 47 pF capacitor. This is fairly heavy coupling considering the high impedance at the collector of

a common base bipolar. This reduces the gain margin several decibels.

The crystal used in this example has the following parameters:

overtone = 5 11.6

Rs = 120 ohms 11.7

Lm = 8 henries 11.8

Cm = 0.0001266515 pF 11.9

Co=5pF 11.10

The series resonant frequency, computed from ***Lm*** and ***Cm,*** is 4.9999996 MHz. The unloaded crystal Q is

$$Q_u = \frac{\omega L_m}{R_s} = 2.09 \times 10^6 \qquad 11.11$$

The group delay displayed on the right in Figure 11-6 is .128 seconds (1.2838 nS)! The loaded Q computed from the group delay is

$$Q_l = \frac{\omega t_d}{2} = 2.01 \times 10^6 \qquad 11.12$$

which is 96% of the unloaded Q. This Driscoll oscillator circuit realizes a loaded Q nearly equal to the unloaded Q of this low frequency fifth overtone crystal and achieves phenomenal loaded Q.

11.3.4 Element Values

The elements L, C_1, and C_2 transform the high-impedance output of the common-base stage Q_2 to the lower input impedance of Q_1. Nominal values are

$$C_1 = \frac{1}{500\pi f} \qquad 11.13$$

$$L = \frac{125}{\pi f} \qquad 11.14$$

$$C_2 = \frac{1}{20\pi f} \qquad 11.15$$

The Q of this network is moderately high and the network must be tuned. C_1, or a portion of C_1, is a trimmer capacitor. Alternatively, L may be tuned. The total capacitance at C_1 includes capacitive loading from the output coupling network. C_1 is therefore reduced by the parallel equivalent capacitance of the output coupling network. The values given above are approximate, and it may be necessary to adjust these values during circuit analysis to achieve optimum results.

The emitter resistance of Q_1 should be at least 200 ohms. The inductor in series with this resistor should have a reactance of about 10 times the resistor value.

11.3.5 Frequency Pulling

The frequency can be adjusted with variable reactance in series with the crystal. An inductive reactance lowers the oscillation frequency, and a capacitive reactance increases the operating frequency A series L-C network provides netting of the frequency both up and down. The pullability is very low because of the extreme Q. The circuit above is pulled up in frequency approximately 7 Hz with a 36 pF capacitor in series with the crystal. This lowers the loop gain about 2 dB, assuming a capacitor Q of 800. An 18 pF capacitor pulls the frequency approximately 13 Hz with a decrease in loop gain of about 4 dB. These frequency pulling figures were determined by modifying the simulation program circuit file to include a series capacitor with a Q of 800.

11.3.6 Phase Noise

The phase noise performance of the high-performance crystal oscillator is outstanding. Driscoll published the SSB phase noise

for a similar 5 MHz oscillator using a third overtone BT-cut quartz crystal resonator. The reported phase noise is plotted in Figure 11-7. The bias levels for this oscillator were Ic = 10 mA and *Vce* = *9* volts for Q_1 and I_c = 0.5 mA and *Vce* = *9* volts for Q2. The reported output power level, taken via a coupling capacitor at the collector of Q2 was 4 dBm. The SSB phase noise was approximately -147, -152, -160, and -166 dBc/Hz for offset frequencies of 100,300, 1000, and 10,000 Hz respectively

The power level of a single-stage near-class-A oscillator is generally less than 25% (the maximum efficiency of class-A amplifiers) of the quiescent dc power level. The signal power level in the sustaining stage, Q_1, is well below 25% of the quiescent dc power level because limiting in the output stage, Q2, reduces the drive to Q_1.

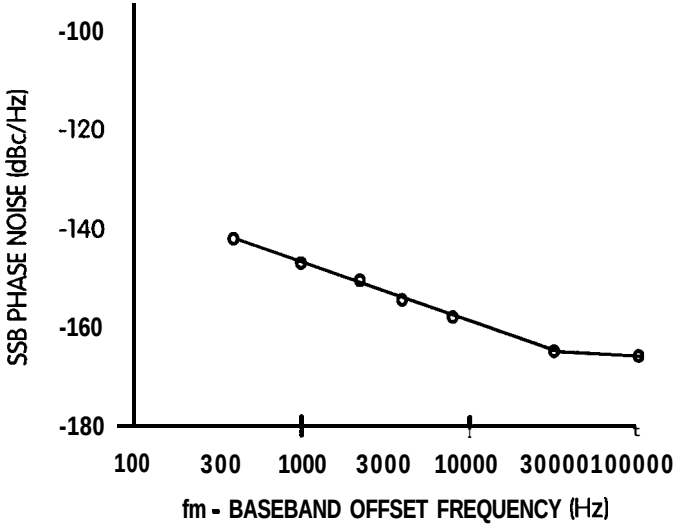


Figure 11-7 *Phase noise performance of the Driscoll oscillator.*

The SSB phase noise reported by Driscoll is consistent Leeson's equation and varactor modulation noise with the following oscillator parameters:

frequency = 5 MHz 11.16

Q_l > l,000,000 11.17

flicker corner = 8000 Hz 11.18

NF=5dB 11.19

sustaining stage signal power = -6 dBm 11.20

The crystal dissipation in the circuit reported by Driscoll was 85 μW, which suggests good aging performance. Typical single-stage crystal oscillators with a restricted power level to retain good aging performance typically have ultimate S/N ratios at least 10 dB worse than the -166 dBc/Hz reported by Driscoll.

11.3.7 AM-to-PM Conversion

A premise of oscillator design based on the linear open-loop Bode response is that limiting has a small or predictable effect on the phase shift of the amplifier. Driscoll gave the measured open-loop phase versus input drive level for the cascade amplifier used in the high-performance oscillator. Only about 1^o of phase change was measured from linear operation to over 17 dB of gain compression.

11.4 Butler Overtone Crystal Oscillator

The Pierce and Colpitts crystal oscillators can be operated on an overtone of the crystal resonator. The oscillator should be modified to ensure operation on the desired overtone. For example, C_1 in the Pierce circuit is changed to a parallel L-C resonant at just below the desired overtone frequency The net reactance is therefore capacitive at the desired overtone frequency The reactance of the parallel L-C is sufficiently low at the fundamental and

other overtone frequencies to discourage oscillation on the incorrect frequency

A common collector 120 MHz Butler 7th overtone crystal oscillator is shown in Figure 11-8. This configuration is a popular and effective overtone crystal oscillator. The author feels this configuration is less temperamental than the common-base version of the Butler. The amplifier is an emitter follower. The crystal resonator is driven by the emitter and is coupled to the higher-impedance base via a capacitive tap. The inductor, ***L,*** resonating with Cl and C2 and the transistor input capacitance, ensures operation on the desired overtone.

The Bode response and matches for the 120 MHz example are given in Figure 11-9. The open-loop gain, after tuning of ***L,*** is approximately 5.7 dB. Both S11 and S22 on right of center on the Smith chart indicating the input and output impedances are

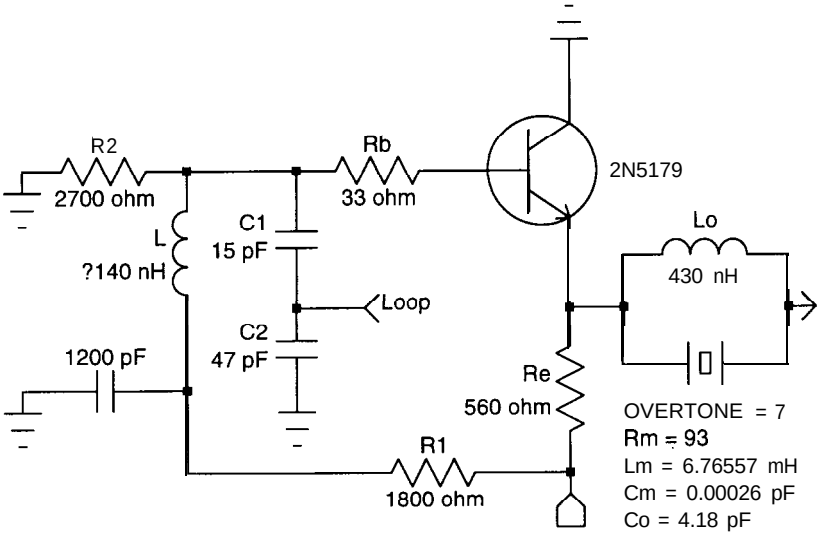


Figure 11-8 ***Schematic for a 120 MHz Butler overtone oscillator.***

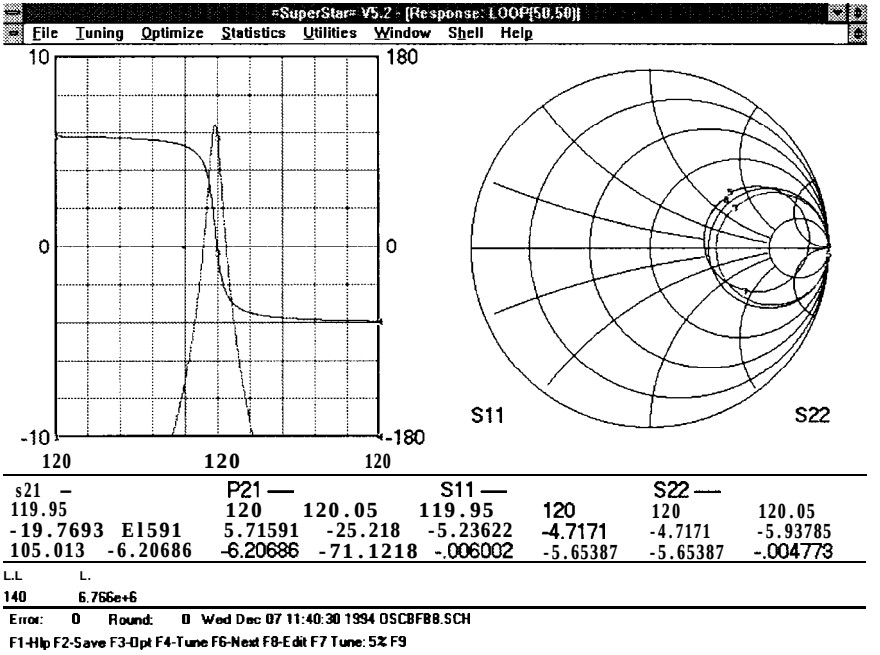


Figure 11-9 Bode response and matches of the 120 MHz Butler oscillator.

higher than 50 ohms. Changing the analysis reference impedance to 120 ohms reveals the loop gain is closer to 8 dB.

11.4.1 Pulling

The frequency is pulled slightly by tuning *L*. This also adjusts the offset of the phase response and the gain margin. Small amounts of netting may be accomplished this way, but larger deviations should be accomplished by reactance in series with the crystal.

The pullability of crystals is inversely proportional to the square of the overtone. Therefore, overtone oscillators are not a good choice when large deviations are required.

11.4.2 Circuit Tips

Higher loss resistance in overtone crystals, lower gain margins for VHF operation, and parasitic component effects conspire to make overtone oscillator design more critical than fundamental-mode oscillator design. A few circuit tricks applied to the Butler considerably tame the temperamental nature of overtone oscillators.

Notice that the topology is similar to that of the negative resistance VCO oscillator, Excluding the crystal, the grounded collector and floating emitter suggest that a series-tuned circuit on the base would invite oscillation. Indeed, inductance associated with the base lead of Q1 and the leads of C_1 and C2 form a series L-C to ground. The resonant frequency is generally in the VHF region, and parasitic oscillation frequently occurs in the region 200 to 800 MHz. This problem can be eliminated by placing a resistor in series with the base. This resistor absorbs the negative resistance associated with the undesired mode but has little effect on the desired Butler mode because of the high input impedance at the base of Q_1. A value of 27 to 68 ohms generally works well.

Even with a capacitive tap at the input to Q_1, the open loop input impedance can be very high. When L is tuned for a phase zero crossing near the maximum phase slope, the input impedance is often very capacitive. This situation can be improved by placing a resistor in parallel with L. A value of 1800 to 3300 is recommended. A smaller value reduces the gain margin but can be used with high-gain transistors. A larger value has little effect.

The reactance of the ***Rm-Lm-Cm*** arm of the crystal resonator model becomes very large off-resonance, which would open the feedback path of the Butler circuit and prevent oscillations. However, the crystal parallel capacitance, Co, provides a feedback path with sufficiently low reactance to be troublesome, particularly for overtones of 5 or higher. Co has little effect near resonance because of the low impedance of the crystal motional arm. As L is tuned off the crystal resonant frequency, oscillation can occur at the resonant frequency of L, C_1, and C2. Since this frequency is near the desired crystal frequency, it may be difficult

to ascertain if the oscillation is crystal controlled. Frequency jumps may be observed as L is tuned. This problem can be eliminated by placing an inductor, Lo, in parallel with the crystal. The inductor is chosen to resonate with C_0 at the desired operation frequency Lo provides a feedback path at frequencies well below resonance of Lo and C_0, but the network of L, C_1, and C_2 prevents oscillation at these frequencies.

11.5 Butler Oscillator-Multiplier

The Butler oscillator-multiplier is similar to the Butler overtone oscillator except that output is taken at the collector, which is grounded via a parallel resonant L-C network. The L-C network is tuned to a desired harmonic of the oscillation frequency The highly nonlinear behavior of the Butler/Colpitts type of oscillator configuration enhances the harmonic content of the current flowing through the collector of Q_1.

The Butler configuration is used so that oscillation can be at either a fundamental or an overtone crystal frequency The oscillator-multiplier configuration is useful for

(a) Extending the frequency range of crystal-controlled oscillators

(b) Increasing the deviation or modulation of 20 MHz and higher crystal-controlled oscillators

The practical upper frequency limit of overtone bulk quartz crystal oscillators is about 200 MHz. By taking output at a harmonic of an overtone oscillator, the frequency range can be extended to 600 MHz or higher. The Butler/Colpitts circuit generates a significant amount of harmonic energy, and the resonant output network enhances the signal level at the desired output frequency

Because the pullability of crystal oscillators is inversely proportional to the square of the overtone, significant deviation or frequency modulation of VHF crystal-controlled oscillators is very difficult. By operating the oscillator on the fundamental mode of

the crystal and taking output at a harmonic of the oscillation frequency, this problem is circumvented.

The disadvantages are reduced output level at the desired frequency and spurious harmonic signals above and below the desired frequency The level of the spurious signals is reduced by decreasing ***Lout*** and increasing C_{out}, which increases the loaded Q of the output resonator. At higher operating frequencies it is difficult to achieve high loaded Q because ***Lout*** becomes vanishingly small and C_{out} becomes large. Additional filtering of the output is required for many applications.

11.5.1 Example

A 20 MHz fundamental-mode oscillator with output taken at 120 MHz is shown in Figure 11-10. The desired output, 120 MHz, has the same frequency as that of the Butler overtone oscillator example shown in Figure 11-8. However, in this case, the crystal operates in the fundamental mode at 20 MHz. Although the values are different, the circuit topology is almost identical to the Butler overtone oscillator. An exception is the peaking inductor, ***Lpeak,*** in the base of Q_1. ***Lpeak*** resonates with C_1 and C_o to enhance the feedback, and therefore the gain of the amplifier, at the desired output frequency ***Lpeak*** can be adjusted to the optimum value by observing the desired output and the other 20 MHz harmonics on a spectrum analyzer. The optimum value Of L_{peak} maximizes output at the desired frequency and reduces the output level of 20 MHz harmonics above and below the desired frequency

The open loop responses for the oscillator-multiplier are evaluated at the oscillation frequency Responses for this example are given in Figure 11-11. Again, ***L*** is adjusted for a phase zero crossing near maximum phase slope. A high gain margin, resulting in a greater degree of limiting, enhances nonlinear behavior and results in greater harmonic content. Sustaining high peak currents requires transistors with high gain and high Ft at collector currents several times the quiescent bias current.

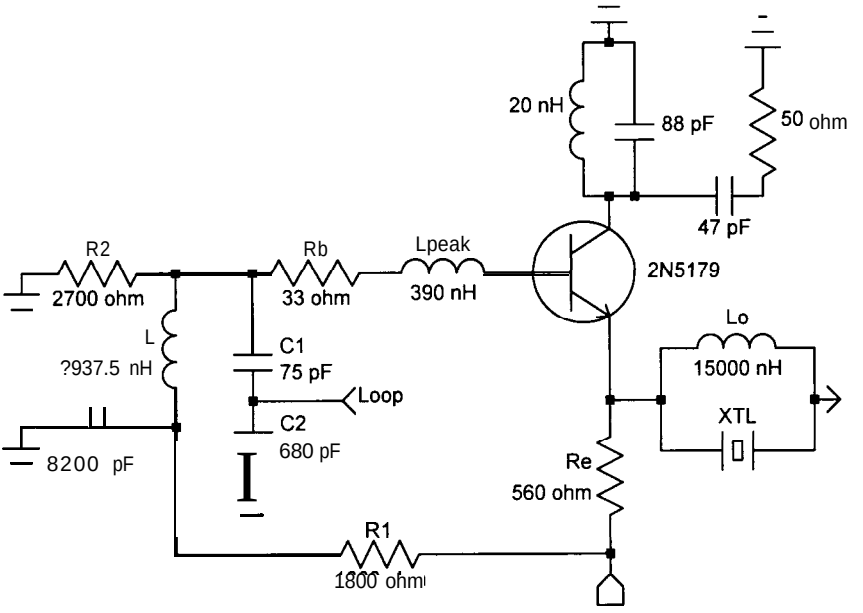


Figure 11-10 *Butler overtone oscillator with frequency multiplier.*

The circuit tips suggested for the Butler overtone oscillator apply to this circuit as well, particularly when this circuit is operated with overtone crystals. If the oscillation frequency is on the crystal fundamental, *Lo* is not necessary

11.5.2 Modulation

The crystal frequency may be pulled by reactance in series with the crystal. This method may also be used to modulate the frequency of the crystal oscillator. The very high unloaded Q of the quartz crystal, even in the fundamental mode, prevents large deviation and fast deviation rates. As the deviation or the deviation rate is increased, the modulation sidebands become unsymmetrical. This is readily observed using a spectrum analyzer.

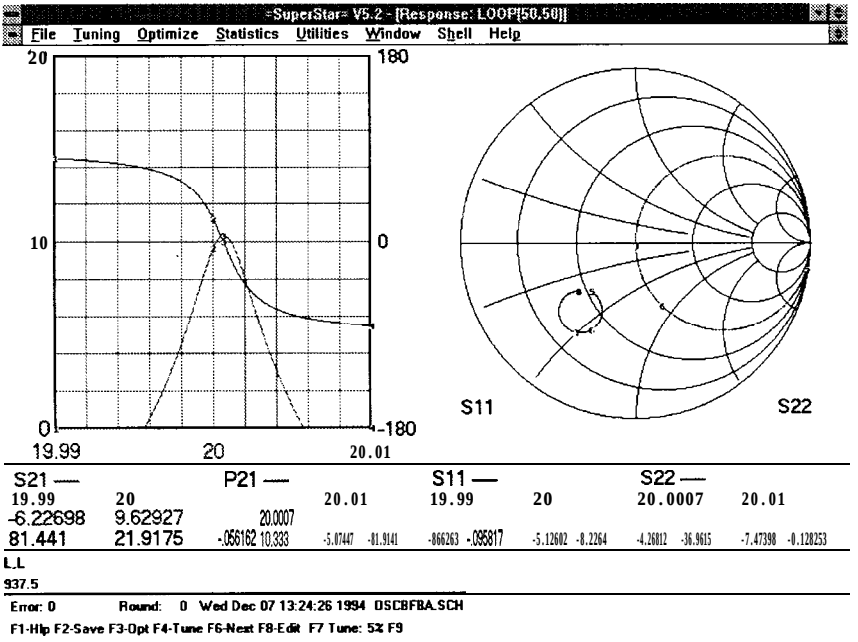


Figure 11-11 *Open loop gain and phase responses (left) and matches (right) for the 20 MHz oscillator with multiplier.*

However, VCXOs are a natural choice for narrow-band systems requiring stable sources. Typical applications might be phase-locking a crystal oscillator to a system reference frequency or a narrow channel telemetry link.

A varactor in series with the crystal can be used to modulate the oscillator. FSK modulation can be applied to the oscillator-multiplier using the circuit in Figure 11-12. This circuit was developed by the author for use in a 300 MHz wireless security system. Over 1 million of these units were produced. The transistor Q_2 is used to switch the capacitor C_t in or out of the circuit. When Q_2 is saturated, Ct is effectively shorted and oscillation occurs near the series resonant frequency of the crystal. When Q2 is off, the oscillation frequency is pulled up an amount dependent on the value of Ct. The value of Ct therefore establishes the deviation.

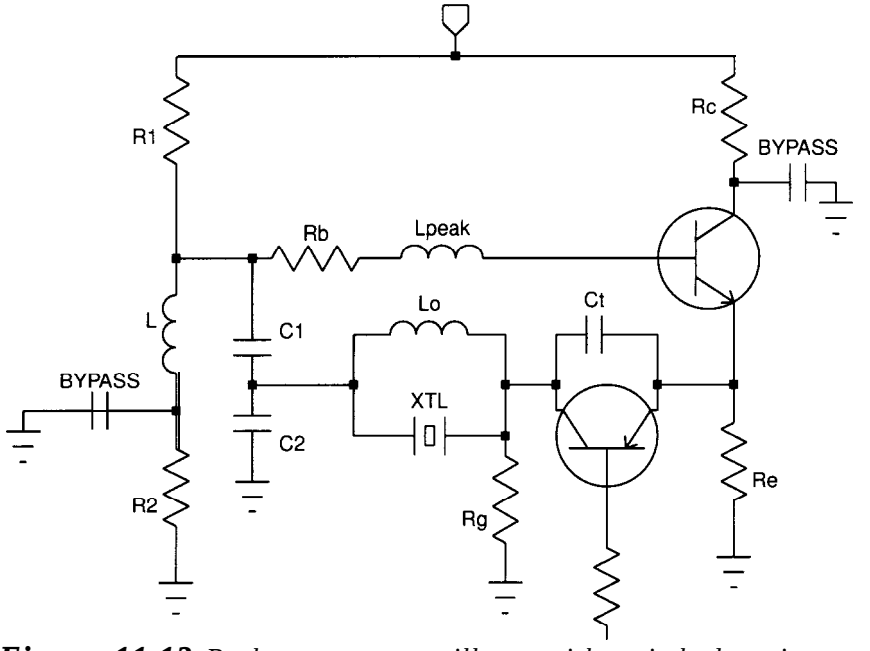


Figure 11-12 *Butler overtone oscillator with switched tuning capacitor for FSK modulation.*

A PNP transistor is used for Q_2. Rg is typically 10 kΩ and the base resistor is 1.8 kΩ. When a modulation voltage that is more positive than the emitter voltage of Q1 is applied, transistor Q2 is off. When a modulation voltage less than the emitter voltage of Ql is applied, such as a logic low, Q2 is on.

11.6 References

[1] Robert J. Matthys, *Crystal Oscillator Circuits,* John Wiley & Sons, New York, 1983.

[2] Michael M. Driscoll, Two-Stage Self-Limiting Series Mode Type Quartz-Crystal Oscillator Exhibiting Improved Short-Term Frequency Stability, *IEEE Transactions on Instrumentation and Measurement,* June 1973, pp.130-138.

12

Case Studies

*This Chapter utilizes the principles presented earlier to study oscillators from the **designer's** perspective. For each case we begin with a specification, discuss the design qualitatively and then proceed with the actual design. Each case is an oscillator which satisfies a typical application requirement.*

12.1 Assumed Specifications

Certain characteristics are unnegotiable in good oscillator designs. Failure to achieve these basic objectives is an indication of design flaws which often manifest themselves in unpredictable and undesirable ways. Achieving these basic objectives is an indication of design quality Among these desired objectives are the following.

The output level and frequency should change smoothly with supply variation from the start of oscillations up to a supply voltage which threatens device thermal, voltage or current failure. Neither the output level or operating frequency should jump or make sudden changes with smooth changes in the supplies.

There should be no discrete frequency components in the output spectrum other than the desired output, integer harmonics of the desired output or harmonics of the line frequency In addition, reasonable levels of electromagnetic interference from external sources are to be expected in the spectrum. For example, the author's lab is within sight of a 50 KW AM broadcast station operating at 750 KHz and sidebands at this offset are often observed in oscillator outputs.

Other undesired spectral components are fractional harmonics of the desired output such as 1/2, 1/3 or 1/4. These arise from parametric pumping of tuning capacitors or active device junction capacitance. Periodic variation of capacitance mathematically can be shown to develop negative resistance at sub-harmonics of the fundamental period. This is the basis of varactor diode parametric amplifiers used for low noise applications before the advent of low noise transistors. Negative resistance at sub-harmonic frequencies can lead to undesired spectral components in oscillators at those frequencies.

Another unnegotiable characteristic is that the output frequency should change smoothly and monotonically with tuning voltage. Monotonic means that a tuning voltage change in one direction results in a frequency change in one direction.

Also, oscillation should not fail at any tuning voltage which the system may apply to the oscillator. It is even more desirable that oscillation not fail with a tuning voltage from 0 volts up to the reverse breakdown of the varactor. However this requirement is usually more stringent than absolutely required. High loaded Q results in high RF voltage across the varactor and in certain applications a minimum tuning voltage greater than 0 volts may be required to avoid forward conduction in the varactor.

Certain other specifications are self-evident. A proposed oscillator should be designed and tested to operate over the range of environmental specifications. Important oscillator operating and storage environmental specifications include temperature, shock and vibration.

Vibration is an often overlooked requirement. Oscillators are typically susceptible to vibration induced phase noise. These problems can be severe in mobile and airborne applications. Even fan bearing noise in fixed instruments can introduce noise. “Dropping a 0.5 inch steel ball on the oscillator cover from a height of 4 inches shall not cause the system to lose lock” is a typical type of specification to manage these problems. Inductor vibration, wire on ferrite cores (even for chokes) and small capacitance changes induced by package vibration are common culprits.

12.2 **Low-Noise 91 O-920 MHz VCO**

This requirement is a low noise 915 MHz VCO tuned +/-3 MHz. The specifications are

Vsupply	+ 13.6 volts
Imax	<40mA
Power output	>3dBm
Load impedance	50 ohms
Harmonics	<-10dBc
Frequency	912 - 918 MHz
Tuning Voltage	0- 12volts
SSB phase noise	
1 KHz offset	**-85** dBc/Hz
10 KHz offset	-110 dBc/Hz

12.2.1 Initial Observations

The relatively high supply voltage and supply current, the relatively low output level and no output level flatness specification make realization of the amplitude characteristics straightforward. A harmonic specification of -10 dBc is not overly tight but warrants consideration.

The first specification to cause concern is the frequency specification: 912 to 918 MHz. The 6 MHz tuning bandwidth is only 0.66%. Narrow tuning per se is not a problem but it indirectly implies a tight frequency tolerance. Can the oscillator achieve this stability from unit to unit and with temperature. On standard PWB materials this would definitely require adjustment unit to unit and might be difficult to maintain over temperature. This problem could be resolved by having the varactor tune much wider than necessary to correct for all sources of frequency error. A detailed noise analysis is required to determine whether varactor modulation noise precludes extra tuning range.

12.2.2 Noise Analysis

Shown in Figure 12-1 is a noise estimation screen from the program =OSCILLATOR= [1]. The center frequency and all other specifications except the loaded Q were entered. The proposed active device is a Mini-Circuits MAR3 MMIC amplifier which draws 35 mA at the nominal operating voltage. A device flicker corner of 3 KHz was estimated and the noise figure (6 dB) was read from the Mini-Circuits data book [2]. To allow some margin for the frequency range and tuning voltage the oscillator is designed to tune 10 MHz with a 5 volt tuning swing. The MAR3 is easily capable of +3 dBm output and the oscillator output level was later measured to be 5.4 dBm midband.

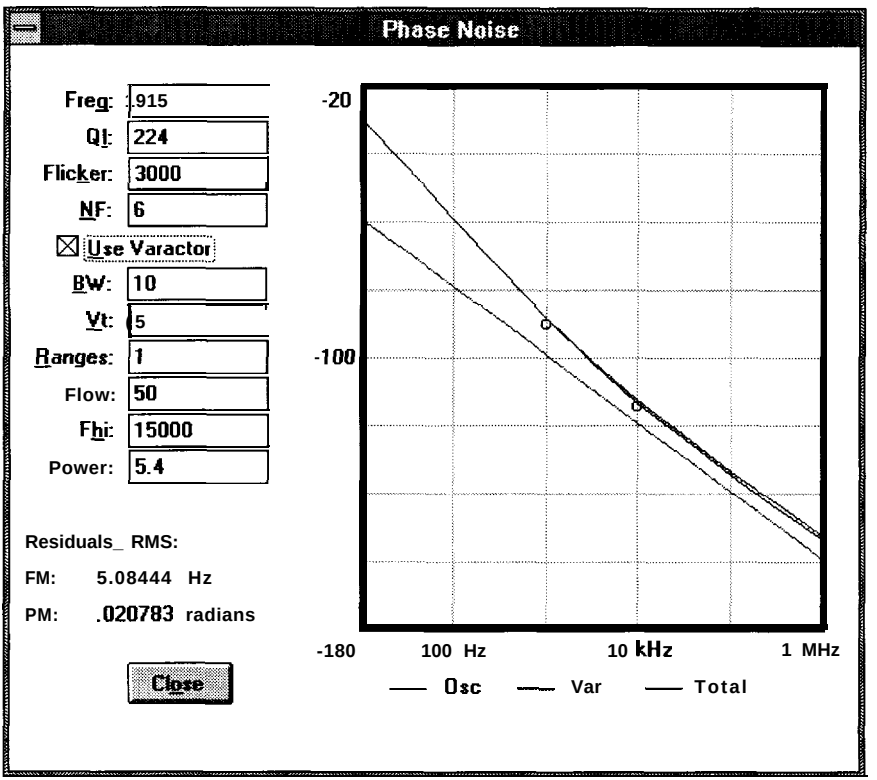


Figure 12-1 *Phase noise estimation screen from the =OSCILLATOR= program.*

It would seem that noise figure would be an important parameter for achieving the desired noise performance. However, whether we use a discrete amplifier design with an expensive low noise transistor or an easy-to-use and inexpensive MAR3 the difference in circuit noise figure is only a few decibels. As is typical in a given application the only parameters at our disposal which have a significant impact on the noise performance are the loaded Q and the output power. Higher output power requires higher supply current. Therefore, the loaded Q was increased until the SSB phase noise performance plotted exceeded the specification (-85 dBc/Hz at 1 KHz and -110 dBc/Hz at 10 KHz) with 5 dB of margin. The required loaded Q is 224. To avoid significant resonator insertion loss an unloaded Q much higher than this is required. A Trans-Tech standard profile TEM mode coaxial resonator [3] loaded with ceramic material with a relative dielectric constant of 38.6 (material 8800) was selected. The unloaded Q of this resonator is over 400.

12.2.3 Proposed Oscillator

A schematic of the proposed oscillator is given in Figure 12-2. The Mini-Circuits MAR3 is cascaded with a top-C coupled coaxial resonator. Small (size 0805, 0.3 pF) AVX chip capacitors [4] lightly couple to the resonator to achieve the desired loaded Q. The low impedance of the high dielectric resonator reduces the normally high voltage swing which would appear across a high loaded Q resonator. This and the low value of capacitance in series with the varactor help reduce the voltage across the varactor. The varactor is a Metelics MSV34-075-E28 [5].

The 5 nH inductor (a short loop of wire) at the output of the MAR3 tunes out the output capacitive reactance of the MAR3 and the 4 pF load coupling capacitor so the phase shift through the cascade at the resonator frequency is zero degrees. The output is coupled to a 50 load through a 4 pF capacitor at the MAR3 output. The sole biasing elements are the 270 ohm resistor and the 47 pF bypass capacitor. With a device operating voltage of 5 volts and a supply voltage of 13.6 volts the operating current is just less

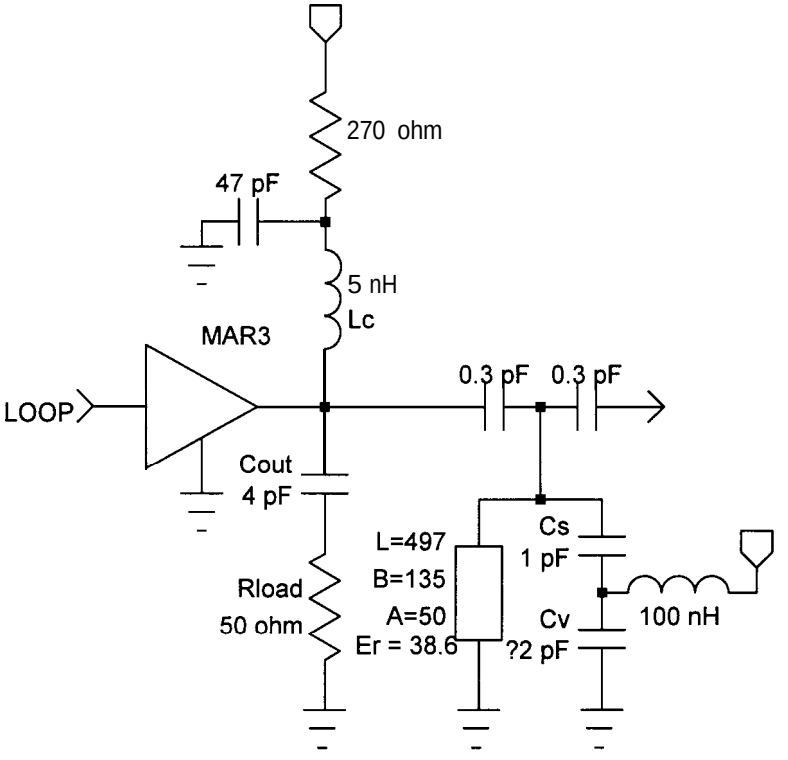


Figure 12-2 *912 to 918 MHz VCO using a ceramic loaded TEM mode coaxial resonator and an MAR3 MMIC amplifier.*

than the nominal 35 mA of the MAR3 and well within the 40 mA specification.

The open loop gain and phase responses and the group delay are given in Figure 12-3. The solid traces are with the varactor at 3.4 pF and the dashed traces are with the varactor at 1.1 pF. During the design process the coupling capacitors were reduced until the group delay was over 77 nS. This corresponds to a loaded Q of 221.

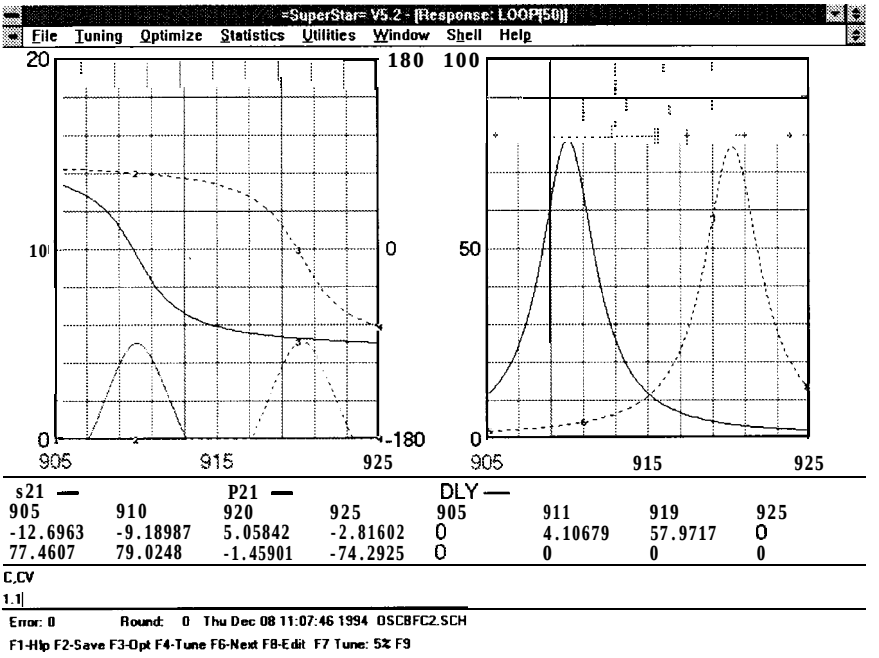


Figure 12-3 *Open loop gain and phase responses (left) and group delay (right) for the 912 to 918 MHz VCO. The solid traces are with the tuning varactor at 3.4pF and the dashed responses are at 1.1 pF.*

12.2.4 Test Results

The circuit was constructed and the data in Table 12-1 was taken using a 13.6 volt battery for the supply There is approximately 2 MHz of tuning margin. The tuning sensitivity is approximately 2 MHz/volt between 0 and 2 volts and 1 MHz/volt between 2 and 4 volts. At the upper end of the band it is 0.5 MHz/volt. The output level varies less than 1 dB over the entire tuning range.

Given in Table 12-2 is the SSB phase noise performance at 0 volts and 13.6 volts. This data is also placed as circles on the =OSCILLATOR= SSB phase noise plot in Figure 12-1. Agreement is excellent.

Table 12-1 *Measured output frequency, level and 2nd harmonic level vs. tuning voltage for the coaxial resonator VCO*

Vt (volts)	fo (MHz)	Po (dBm)	2nd (dBc)
0	909.9	4.8	-14
2	913.8	5.1	-14
4	915.8	5.3	-14
6	917.3	5.4	-14
8	918.5	5.4	-14
10	919.4	5.4	-14
12	920.2	5.6	-14

12.3 Ultra Low Cost 939 MHz VCO

This requirement is for a low cost VCO which tunes 939 ±25 MHz. The specifications are

Vsupply	-9.8 volts
Isupply	<10 mA
Power output	>-3 dBm
Load impedance	50 ohms
Harmonics	<-6 dBc
Frequency	939 ±25 MHz
Vtuning	0 to -9.4 volts
SSB phase noise	
>I 0 KHz	<-70 dBc

Table 12-2 *Measured SSB phase noise performance of the coaxial resonator VCO*

vt (volts)	fm (Hz)	SSB phase noise (dBc/Hz)
0	1000	-90
0	10000	-115
13.6	1000	-90
13.6	10000	-114

12.3.1 Reducing the Cost

For this application cost is of extreme concern. We begin our considerations with the relatively simple UHF VCO schematic in Figure 9-l. To minimize cost we question the purpose and need for every component in this design. We take advantage of the fact that a short run on a PWB looks inductive when it is terminated to ground and looks capacitive when it is open terminated. At 939 MHz these runs are short, consume little space and may replace inductors and small values of capacitance. The final result is a UHF VCO constructed with a PWB, three resistors, one varactor, one transistor and no capacitors! The tuning voltage even supplies power to the oscillator! The schematic is given in Figure 12-4.

An inherent advantage of the negative supply common-collector VCO in Figure 9-l is that all connections to the power supply are through a high RF resistance path. This means that bypass capacitors are not required on the supply line which saves a capacitor in this case.

The function of C_{out} in Figure 9-l is twofold; to isolate the DC resistance of the load resistor from the emitter and to transform the load resistance to a higher value to avoid loading the emitter to heavily The collector is grounded directly with this common-collector negative power supply configuration. Recall from previous discussions that the output may be taken directly from the collector. Therefore we DC ground the collector with a printed trace which has 7.5 nH of inductance to ground and take output directly at the collector. No capacitor is required because the DC voltage is zero. The inductance provides a finite impedance across which the output is developed.

The purpose of Cc in Figure 9-l is to isolate the base bias voltage from the varactor tuning voltage. The left side of the transmission line resonator in Figure 9-l is grounded in the final oscillator so no other return components are required. However we do need a high impedance component to deliver a tuning voltage to the varactor. At this point an unusual technique is considered. Both Cc and Rt in Figure 9-l are eliminated if the base bias voltage is

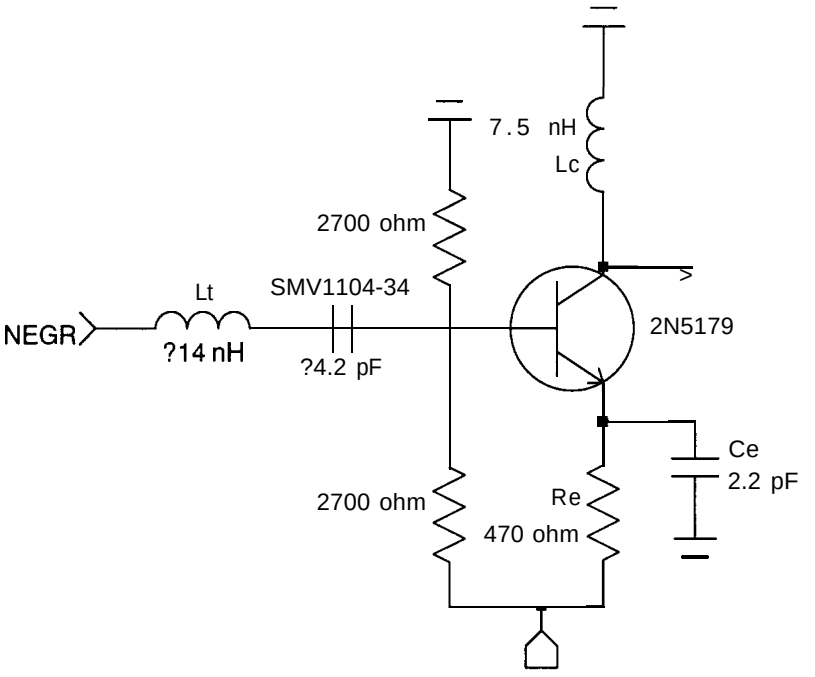


Figure 12-4 *Ultra low cost VCO design. Lo Lt and Ce are realized as printed elements.*

used to bias the varactor. The bias network establishes the base voltage at approximately 50% of the supply voltage. Therefore the base voltages changes with the supply voltage. The narrow tuning range of this requirement possibly could be satisfied with a supply voltage range narrow enough to not disturb other oscillator specifications.

The simulated input resistance and reactance for this design are given in Figure 12-5. The solid responses are with the varactor at 4.2 pF and the dashed responses with the varactor at 2.7 pF. The required voltage range for an Alpha SMV1104-34 varactor [6] is approximately 3 to 4.5 volts.

The emitter capacitor can be realized as a 300 mil square pad on 62 mil thick G-lO/FR-4 board with a dielectric constant of ap-

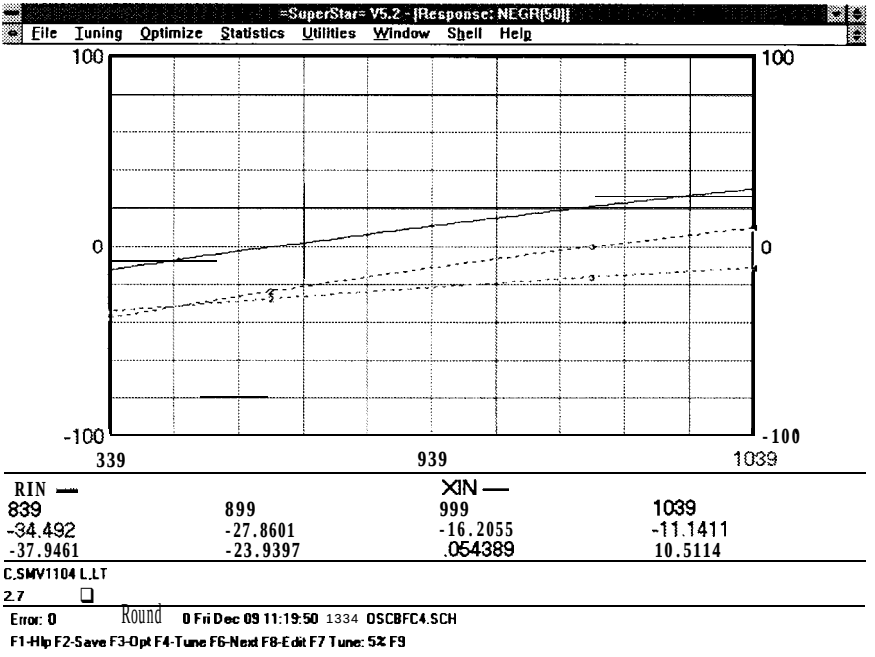


Figure 12-5 *Input resistance and reactance for the low cost VCO. Solid traces are with the varactor at 4.2 pF and dashed responses are at 2.7 pF.*

proximately 4.8 to 5.4. The collector inductor can be realized as a 10 mil wide 450 mil long straight line or loop. The resonator inductor is a 10 mil wide 680 mil long line. This is the only critical line length and must be carefully controlled.

12.3.2 Test Results

A prototype was built and the characteristics given in Table 12-3 were measured. The output level exceeds -3 dBm with a supply voltage from 6 to 9.5 volts and the tuning range over this supply range is 893 to 964 MHz. The frequency sweeps somewhat wider than expected for this varactor apparently because without a varactor the frequency increases with an increasing supply volt-

Table 12-3 *Measured output frequency, level and 2nd harmonic level vs. tuning voltage for the ultra low cost VCO*

vt (volts)	fo (MHz)	Po (dBm)	2nd (dBc)
4	836.2	-8.9	-20.7
5	866.2	-5.2	
6	893.2	-3.0	-20.5
7	917.9	-1.7	
8	939.2	-1.0	-24
9	958.2	-1.7	
10	974.9	-6.0	-33

age. Previous considerations of this VCO configuration suggested the harmonic levels when taking power at the collector might be fairly high. In this case the harmonic performance is excellent. This is probably because the 2N5179 transistor has less gain at 1.8 GHz than the microwave transistors used earlier. Also harmonics are generated in this circuit by short duration current spikes of relatively high current. The 2N5179 device gain decreases significantly at current levels above 20 mA.

The noise performance of this circuit at *Vs* = ***6.8*** volts is given in Table 12-4. Notice that it easily satisfies the specified SSB phase noise.

Table 12-4 *Measured SSB phase noise performance of the ultra low cost VCO*

VS (volts)	fm (Hz)	SSB phase noise (dBc/Hz)
6.8	10000	-83
6.8	100000	-102
6.8	1000000	-119

12.3.3 Varactorless VCO

The tuning sensitivity of the low cost VCO is approximately 20 MHz/volt at the nominal operating voltage of 8 volts. When the supply voltage is changed the device junction capacitances also change and tune the oscillator. If the required tuning range is less then even the varactor may be removed and replaced with a fixed capacitor. The resulting VCO characteristics with a 3.3 pF fixed capacitor are given in Table 12-5. The tuning sensitivity without the varactor is reduced to approximately 5 MHz/volt. The output level is somewhat higher suggesting that losses in the varactor reduce oscillator limiting and the resulting output level.

12.3.4 One Transistor, Resistor and Capacitor VCO

The ultimate in VCO simplicity is given in Figure 12-6. This 900 MHz VCO uses one transistor, one resistor and one capacitor. All other components are printed elements. The design is similar to the varactorless design in the previous section except the positive supply must be bypassed to RF ground. This is accomplished with a capacitive transmission line stub. Despite the simplicity it is a practical design when positive and negative supplies are available.

Table 12-5 *Measured output frequency, level and 2nd harmonic level vs. tuning voltage for the ultra low cost VCO*

vt (volts)	fo (MHz)	Po(dBm)
5	901.9	-8.7
6	906.1	-3.2
7	911.4	-0.5
8	916.6	+1.5
9	921.7	+3.0
10	926.6	+4.1

12.4 Low Harmonic, Low Load Pull VCO

This requirement is for a 500 to 900 MHz VCO with all harmonics less than -20 dBc and with low load pulling. The specifications are

Vsupply	11 volts
Isupply	cl 00 mA
Power output	>7 dBm
Frequency	500 - 900 MHz
Tuning voltage	0 - 11 volts

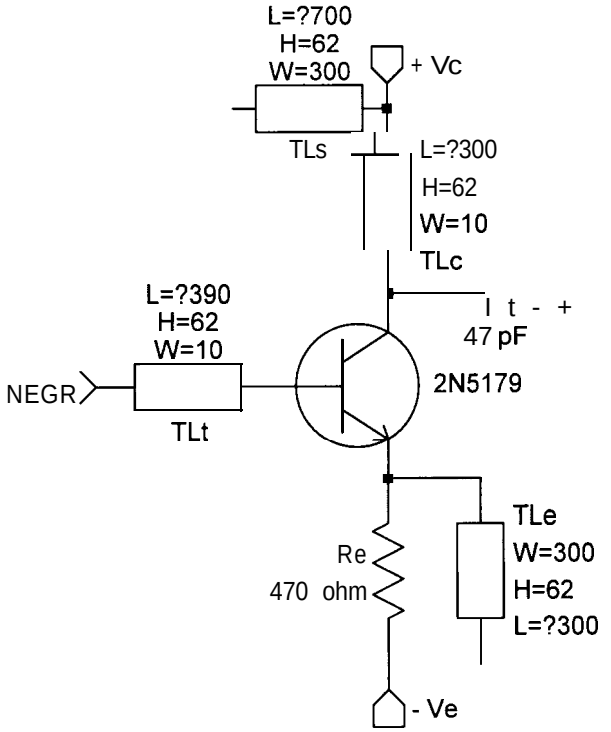


Figure 12-6 *VCO constructed using one transistor, resistor and capacitor. The remaining components are printed on the PWB.*

Harmonics	<-20 dBc
Load impedance	50 ohms
Pulling, R.L. = 12 dB	<1 MHz/volt
Residual PM	
30 Hz - 64 KHz	<0.2 radians

More than adequate power supply characteristics and tuning voltage range are available for the required output level and frequency range. Therefore, the specifications which drive this design are the harmonic and specification pulling specifications. The phase noise is specified as residual PM. This is addressed later.

12.4.1 Harmonic Performance

In Section 3.6 the harmonic performance of an open-loop cascade oscillator design is discussed. Factors that effect harmonic performance are identified. In Section 6.9.2 the harmonic performance of a negative resistance oscillator was simulated using Spice. These discussions illustrate that harmonic performance of -20 dBc is aggressive and without attention -6 to -10 dBc is typical. When an oscillator is used to drive a non-linear device such as a mixer these higher harmonic levels are typically not a problem. When improved harmonic performance is required the two most useful techniques are external filtering and the choice of the point within the oscillator for output coupling.

12.4.2 Output Filtering

Filtering the output spectrum is most useful for narrow tuned oscillators. When the tuning bandwidth is an octave or more a fixed filter is useless because the second harmonic when the oscillator is tuned low is within the required output passband. Narrow tuned oscillators avoid this difficulty and simple filters are generally adequate. As the required tuning bandwidth widens the filter order become progressively higher. This is illustrated in Table 12-6. Given is the required filter order versus the

needed additional harmonic attenuation and the oscillator tuning bandwidth as a percentage of a full octave. The required order is given for both 0.25 dB ripple Chebyshev lowpass filters and bandpass filters with a conventional lowpass to bandpass transformation[7]. The percentage of octave tuning is defined as

$$tuning\ \% = 100\%\left(\frac{fu}{fl} - 1\right) \qquad 12.1$$

No margins are allowed for passband tolerance or loss in the filter so the passband of the filter should be designed slightly wider and a somewhat higher filter order used. It is evident from Table 12-6 that with wide tuning the required filter order becomes extreme.

The rigorous definition of order in filters is the degree of the denominator in the polynomial in s (jw) which defines the transfer approximation. For all-pole lowpass filters such as the Cheby-

Table 12-6 *Required filter order versus oscillator tuning bandwidth (percentage of octave tuning). A 0.25 dB ripple Chebyshev response is assumed*

Atten		10%	25%	50%	65%	80%	90%
10	BP	0.98	1.38	2.11	2.75	3.93	5.80
	LP	2.74	3.16	4.15	5.16	7.07	10.22
20	BP	1.32	1.84	2.82	3.68	5.25	7.75
	LP	3.66	4.22	5.55	6.89	9.45	13.66
30	BP	1.65	2.33	3.55	4.64	6.61	9.76
	LP	4.61	5.31	6.99	8.68	11.90	17.21
40	BP	1.99	2.81	4.28	5.60	7.98	11.78
	LP	5.57	6.41	8.44	10.48	14.37	20.78
50	BP	2.36	3.29	5.02	6.56	9.35	13.80
	LP	6.53	7.51	9.89	12.28	16.83	24.34
60	BP	2.68	3.77	5.75	7.52	10.72	15.82
	LP	7.48	8.61	11.33	14.08	19.30	27.90

shev the order of a lowpass filter is equal to the number of reactors (inductors or capacitors) in the filter. After the filter is transformed into a bandpass the degree of the denominator is doubled. Nevertheless, in Table 12-6 and much of the filter literature, the order of a bandpass filter is defined as the order of the lowpass prototype from which it is derived. The conventional bandpass transformation results in two reactors (an inductor and a capacitor) for each reactor in the lowpass prototype. So in terms of filter economy, for a given order listed in Table 12-6 the lowpass is favored over the bandpass by a factor of two.

Because we are attempting to filter harmonics a lowpass filter is suggested. For reasons discussed in reference [7], this does not necessarily lead to the most economic filter. For example, in the present case 80% tuning bandwidth and 14 dB of attenuation requires an eighth order lowpass versus a fifth order bandpass. An eighth order lowpass requires only 8 reactors while a fifth order bandpass requires 10 reactors, so the lowpass is favored. However, for narrow tuning bandwidth the bandpass is heavily favored.

Also, notice from Table 12-6 that narrow bandwidth requires significantly lower order filters. A method of reducing the required filter order to suppress harmonics is to use a narrow bandwidth filter and tune the passband with the oscillation frequency This has two disadvantages. It requires varactors in the filter and tracking the frequency of the filter and oscillator can be difficult.

12.4.3 Resonator Coupling

Both of these difficulties can be overcome with a clever technique. The resonator in an oscillator is essentially a first order filter. However, when the oscillator is designed with a high loaded Q, the effective bandwidth of this filter is very narrow. The advantages are twofold. Tracking is assured and additional varactors are not required because the same resonator is used for oscillation and for filtering. This technique is implemented by coupling energy directly from the resonator.

The oscillator given in Figure 12-7 to solve the current specification uses this technique. It is the now familiar common-collector negative resistance VCO with the resonator inductor being a transformer. The inductance of each winding is similar to that of the conventional uncoupled inductor.

This technique has disadvantages. Coupling directly to the frequency determining element of the oscillator worsens load pulling. Small changes in the load can significantly affect the operating frequency and output level. This technique is risky in

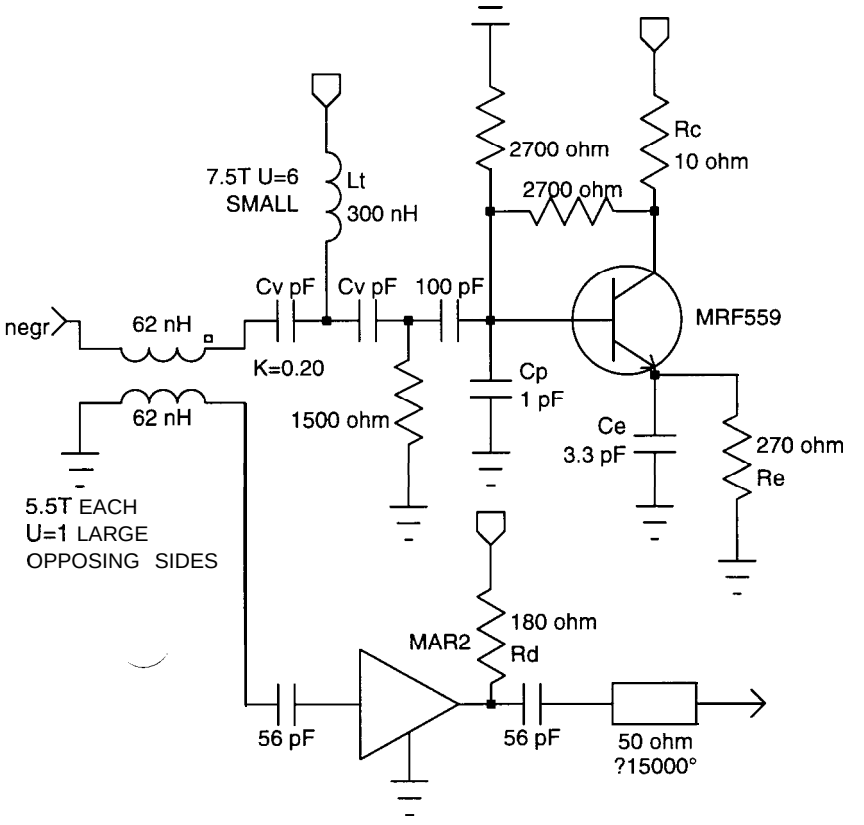


Figure 12-7 500-900 MHz VCO with improved harmonic and load pulling performance.

this application because the second specification driving the design is a tight load pulling specification. To overcome this difficulty, loose coupling is used. In this case a transformer coupling coefficient, K, of 0.2 is selected. This results in relatively low output level.

12.4.4 Buffering

A Mini-Circuits MAR2 MMIC amplifier buffers the transformer coupled output signal. This both increases the low output level and further improves the load pulling. Using an MMIC amplifier offers low cost, flat gain, amplifier stability, a well defined impedance to the transformer and a good output match. The load pulling is improved because the reverse isolation of the MAR2 exceeds the forward gain by approximately 5 dB in this frequency range.

To simulate the load pulling performance a very long 50 ohm transmission line drives a 29.9 ohm output termination. This resistance is a return loss of 12 dB in a 50 ohm system. Small changes in the long line length rotates the phase of the mismatch though all possible angles. A Monte Carlo run with 50 samples of random line length are given in Figure 12-8. The vertically slanted traces are the negative resistance oscillator input reactance and the horizontal traces are the input resistance. The oscillator is tuned to mid-range. Notice the expanded frequency range of 1 MHz per division used to emphasize the load pulling. The load pulling is fo.43 MHz, well within the specification.

12.4.5 Measured Performance

The circuit in Figure 12-7 was constructed and the tuning characteristics are given in Table 12-7. At a supply voltage of 11 volts the supply current is 52 mA. The 500 - 900 MHz range is covered with a tuning voltage of approximately 0.5 to 8.5 volts. The output level over that range is 8.3 to 10 dBm. The worst harmonic

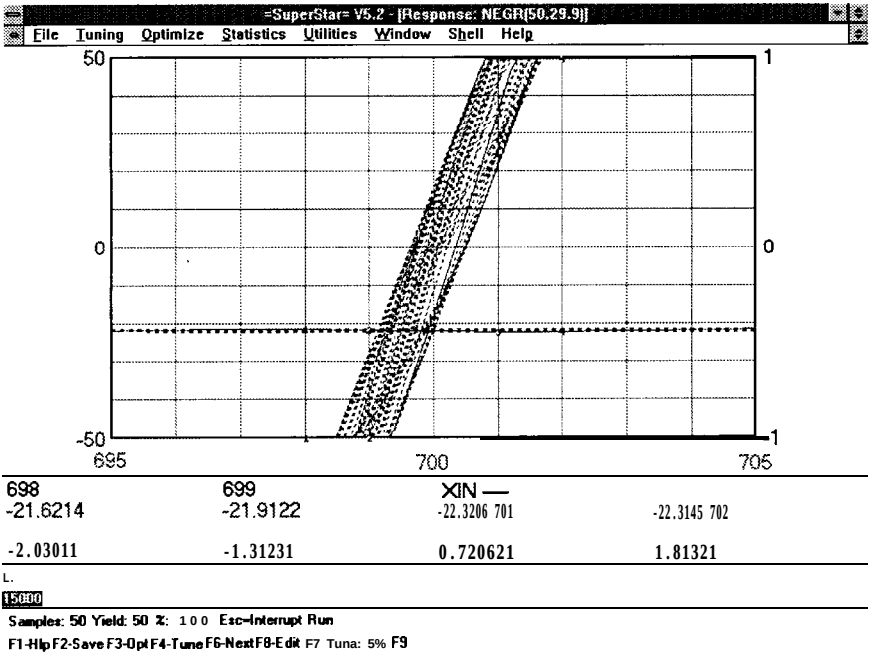


Figure 12-8 *Monte Carlo run demonstrating load pulling. The vertically slanted traces are the negative resistance oscillator input reactance and the horizontal traces are the input resistance.*

performance is at the low end of the frequency range but is within specification.

The current level in the VCO is approximately 17 mA and the MAR2 current drain is 35 mA, slightly higher than expected. The MAR2 output resistor could be increased slightly to drop the current drain.

As an experiment, the MRF559 emitter resistor was increased to 1000 ohms. This drops the oscillator bias current to 5 mA and reduces the oscillator output level presented to the MAR2. The output level after the MAR2 was reduced by about 4 dB and was less flat. All harmonics were improved by about 6 dB to worst

Table 12-7 *Measured frequency, output level, 2nd and 3rd harmonic level vs. tuning voltage for the low-harmonic VCO*

Vt (volts)	fo (MHz)	Po (dBm)	2nd (dBc)	3rd (dBc)	4th (dBc)
0	472.5	8.7	-20.6	-22.7	-33.0
1	527.5	9.8	-21.5	-21.1	-27.1
2	583.8	10.0	-29.3	-22.3	-26.3
3	645.0	9.8			
5	757.3	9.2	-27.5	-29.7	
7	851.3	8.5			
9	911.3	8.2	-25.5	-31.8	
11	947.5	7.0			
13	977.5	5.2	-30.8		

case levels of -*26* dBc. This suggests that with the original 470 ohm MRF559 emitter resistance the oscillator output was driving the MAR2 into gain compression which increased harmonics but had the advantage of flattening the output level.

12.4.6 Noise Performance

The measured SSB phase noise is given in Table 12-8. The residual PM could be measured directly with a modulation analyzer. Because a modulation analyzer was unavailable the following technique was used. The noise analysis algorithm in =OSCILLATOR= [1] was used to estimate the SSB phase noise performance. The accuracy of this analysis was increased by adjusting oscillator parameters in that program so that the program estimated noise performance match measured SSB phase noise data. The residual noise integration algorithm in =OSCILLATOR= then determined the residual PM as displayed in Figure 12-9. The 0.12 radians value is well within specification.

The VCO tuning sensitivity in the actual circuit is 58 MHz/volt at 3.02 volts where the phase noise performance was measured. The tuning sensitivity required to match the measured noise data was 500/22 or ***22*** MHz per volt. This suggests that the effective

Table 12-8 *Measured SSB phase noise performance of the low harmonic VCO*

VS (volts)	fm (Hz)	SSB phase noise (dBc/Hz)
3.02	10000	-97
3.02	100000	-118

noise resistance in the SMV1204-109 varactor used in this VCO is lower than the 3200 ohms assumed for varactors in the =OSCILLATOR= noise algorithm.

12.5 Higher Power Oscillator

This requirement is a fixed tuned oscillator at 837 MHz with a minimum of +20 dBm output. It has a relatively loose frequency tolerance and each unit is mechanically tuned during manufacture. Electronic tuning is not required.

The specifications are

Vsupply	+13.6 ±1 volts
Isupply	<50 mA
Frequency @ 13.6 volts	837 ±5 MHz
Pushing	< 2 MHz/volt
Power output	> 20 dBm

12.5.1 Initial Considerations

The driving specification for this application is the output level which must exceed +20 dBm. The available supply power at 12.6 volts and 50 mA maximum is 630 mW. The required output level is 100 mW minimum which requires at least 16% efficiency. While this is within the theoretical limits of class-A operation it does not leave much margin for tolerance. Therefore we will

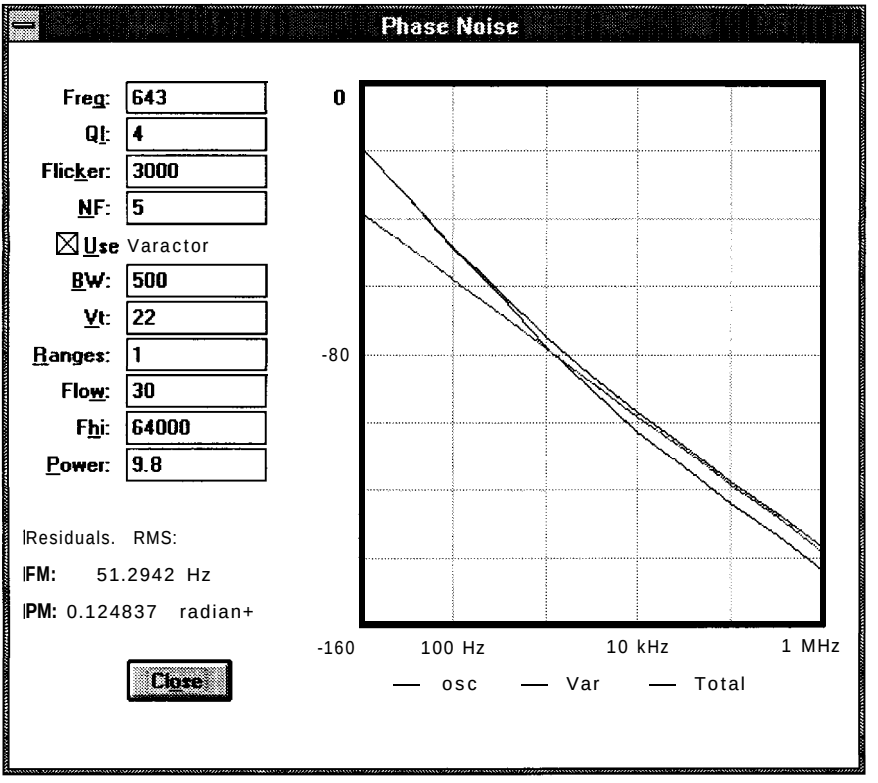


Figure 12-9 *Predicted SSB phase noise and residual FM and PM performance of the low harmonic VCO.*

employ a bias configuration which is between class-A and class-C to improve the efficiency

The operating class and quiescent bias power are primarily responsible for the output level regardless of the oscillator type. Therefore, for the sake of variety we will use a common base negative resistance configuration. A proposed schematic is given in Figure 12-10.

The bias scheme is simple and uses two resistors. A more complex bias scheme is needed if greater temperature and device to device bias stability is required. The large collector to base bias resis-

tance provides little base drive so the quiescent collector current is modest. However, notice that the total resistance in the collector/emitter supply to ground path is quite low, only 10 ohms. Therefore the peak collector current during RF drive is limited primarily by the MRF559 transistor. The combination of modest quiescent current and nearly unlimited peak current results in higher operating efficiency than class-A biasing.

A final value of 27K ohms was selected for the base drive resistor. Higher values of resistance improve efficiency but tend to result in instability at certain supply voltage levels. This is likely the result of device characteristic changes during signal build-up transition from very low bias to class-C operation.

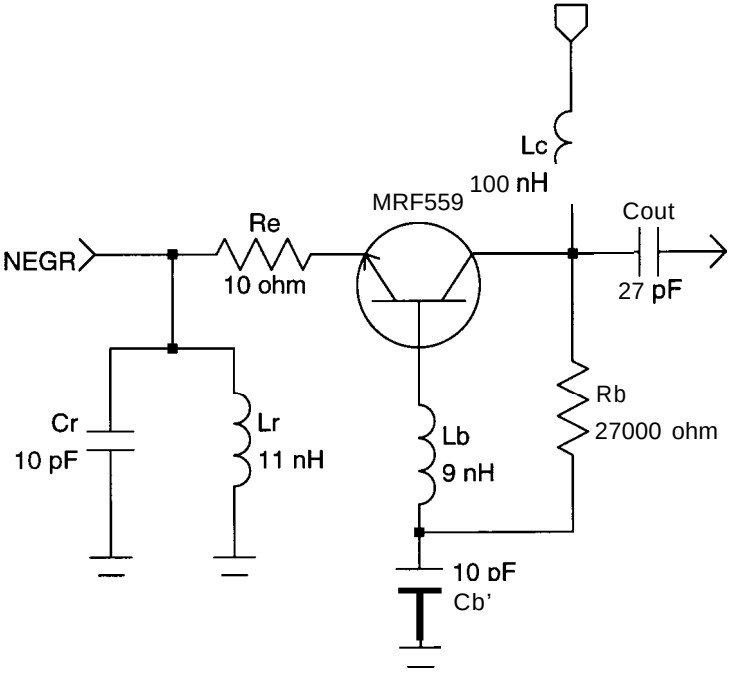


Figure 12-10 *Schematic of the high output level oscillator.*

Unlike previous oscillator examples the supply is inductively coupled to the collector instead of resistibly coupled. Therefore the entire dissapative load at the collector is the output load resistance. This heavy coupling results in degraded load pulling performance but increased operating efficiency

The base choke, ***Lb,*** is used to develop negative conductance at the emitter. As discussed in Section 2-26, the common base configuration limits along a constant susceptance curve of an admittance Smith chart. It therefore uses a parallel resonant circuit.

Given in Figure 12-11 on the left are the negative resistance and reactance looking into the emitter across the parallel resonator. On the right in Figure 12-11 is S11 plotted on an impedance Smith chart with a normalized resistance of -50 ohms.

12.5.2 Measured Results

A prototype unit was constructed and the measured characteristics are given in Table 12-9. The output characteristics were well behaved with instabilities or sudden changes with supply voltages from 5 volts where oscillation begins through 20 volts where device dissipation limits are approached. The DC supply power to output power efficiency improves with increasing supply voltage to 35% for supply voltages above 17.5 volts. At a supply voltage of 20 volts the output level is +26.2 dBm or 417 mW. At the specified 13.6 ± 1 volts supply range the output level is +21.4 to 22.2 dBm, well above the +20 dBm specification limit. The efficiency in this range is approximately 30%.

For a supply range of 7.5 to 20 volts the frequency change is only 4.5 MHz. This excellent pushing performance is indicative of a high quality design. At the specified operating voltage pushing is only 0.5 MHz/volt.

Although unspecified, the second harmonic and SSB phase noise performance are also given in Table 12-9. Particularly interesting is the noise performance. Notice the SSB phase noise at 10 KHz offset improves with increasing output and tracks with the output

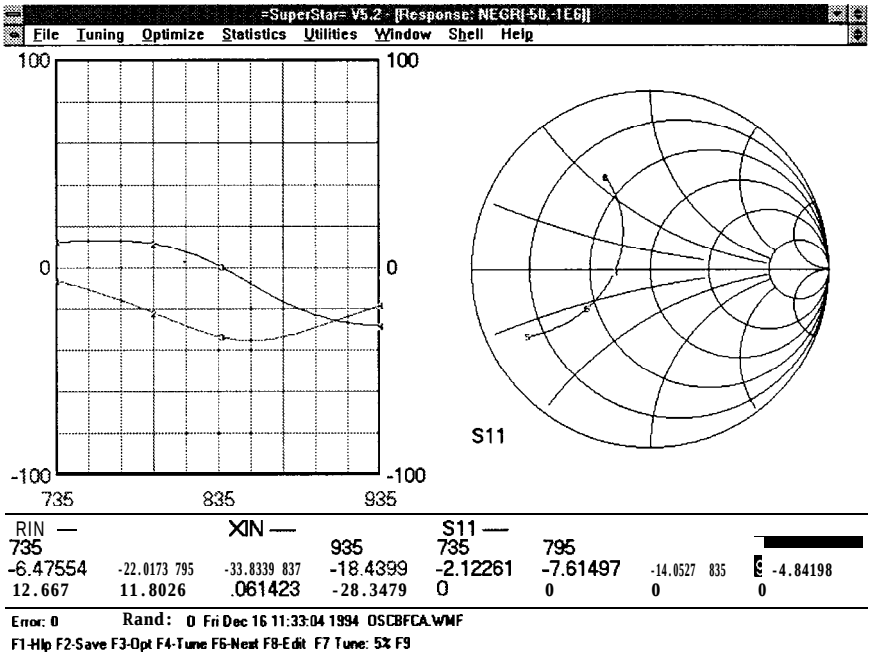


Figure 12-11 *Simulated input resistance and reactance (left) and* S_{11} *(right) for the high output level negative resistance oscillator.*

level within a few decibels up to a supply of *+15* volts just as predicted by Leeson's equation. Above 15 volts the SSB phase noise performance begins to decrease with increasing level. This is very likely the result of degraded device noise figure with increasing collector current.

12.6 References

[1] =OSCILIATOR= Operation Manual, Eagleware Corporation, 1750 Mountain Glen, Stone Mtn, GA, 30087, 1994, TEL (404) 939-0156, FAX (404) 939-0157.

Table 12-9 Measured characteristics of the high output level oscillator

Vs(volts)	Is(mA)	Po(dBm)	η(%)	fo(MHz)	2nd(dBc)	φ-noise(dBc/Hz)
5.0	18	5.0	4	840.5	-24.5	-86
7.5	21	15.0	20	833.3	-21.5	-97
10.0	30.	18.9	26	834.1	-17.0	-101
12.5	38	21.3	28	835.2	-16.8	-105
15.0	44	23.3	32	836.7	-17.0	-107
17.5	50	24.9	35	837.5	-17.3	-102
20.0	60	26.2	35	837.8	-18.0	-95

[2] RF/IF Designers Handbook, Mini-Circuits, 13 Neptune Avenue, Brooklyn, NY, 11235, 1992, TEL (718) 934-4500, FAX (718) 332-4661.

[3] Coaxial Resonators and Inductors, Trans-Tech, Inc., 5520 Adamstown Road, Adamstown, MD, 21710,1990, TEL (301) 695-9400, FAX (301) 695-7065

[4] AVX Corporation, PO. Box 867, Myrtle Beach, SC, 29577, TEL (803) 448-9411

[5] State-of-the-Art Microwave Diodes, Metelics Corporation, 975 Stewart Avenue, Sunnyvale, CA, 94086, 1991, TEL (408) 737-8181, FAX (408) 733-7645

[6] Semiconductor Devices: RF Through Millimeter Wave, Alpha Semiconductor Devices Division, 20 Sylvan Road, Woburn, MA, 01801,1992, TEL (617) 935-5150, FAX (617) 935-4939

[7] R. W. Rhea, *HFFilter Design and Computer Simulation,* Noble Publishing, Atlanta, GA, 1994, pp. 146

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