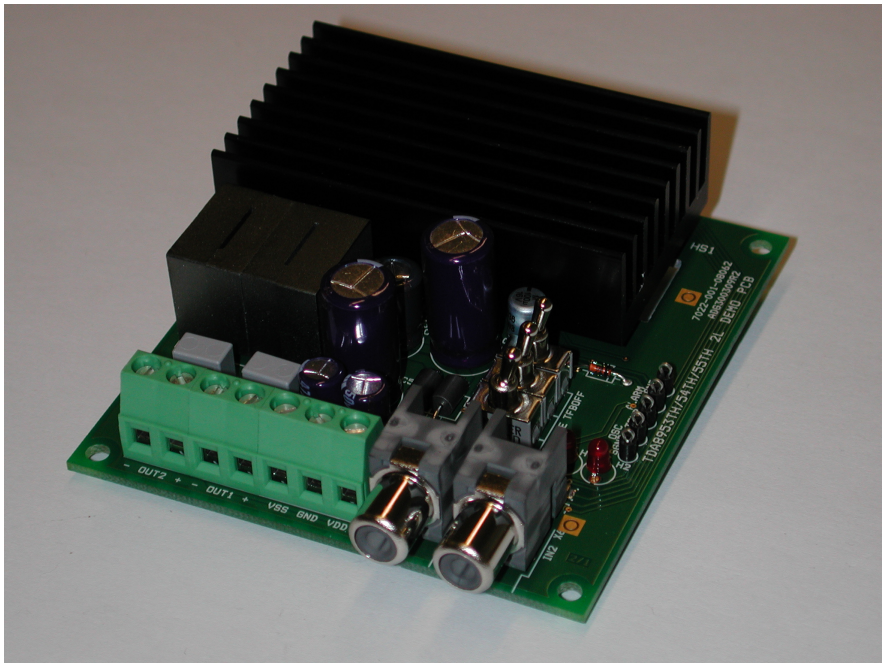
UM10373_1

TDA8953TH/54TH/55TH 2L demo PCB symmetrical supply

Rev. 0.1 — 2009-09-15 **User manual**



Document information

Info	Content
Keywords	Class-D amplifier, High efficiency, Switch Mode Amplifier
Abstract	*This User Manual describes the TDA8953TH/54TH/55TH double layer high power Class-D amplifier demonstration PCB, which can be stuffed with either the TDA8953TH, TDA8954TH or TDA8955TH NXP Semiconductors' devices, depending on the output power requirements and the need for diagnostic functionality.* *These pin-to-pin compatible devices are intended for high power applications and deliver a typical output power of 2 x 210 W_{RMS} for the TDA8953TH and TDA8954TH or 2 x 150 W_{RMS} for the TDA8955TH respectively in Single Ended (SE) configuration or 420 W_{RMS}, for the TDA8953TH and TDA8954TH and 300 W_{RMS} for the TDA8955TH respectively in Bridge Tied Load (BTL) configuration.* *The demonstration PCB can be used either in stereo Single Ended (SE) or in mono Bridge Tied Load (BTL) configuration, operating from a symmetrical supply with a wide voltage range:* *TDA8953TH/54TH/55TH: ±12.5V…±42.5V* *The TDA8953TH/54TH/55TH family utilizes advanced limiting and protection features, such as selectable Thermal Fold Back and cycle-by-cycle current limiting, to avoid audio holes (interruptions) during normal operation. Furthermore it contains special control logic for pop free switch on/off and standby-mode for power saving regulations.* *An application designed around this family of devices is a very robust, high performance solution with a small form factor.*

Revision history

Rev	Date	Description
0.1	2009-09-15	Preliminary version

Contact information

For additional information, please visit: http://www.nxp.com

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1. Introduction

This User Manual describes the TDA8953TH/54TH/55TH high power Class-D amplifier double layer demonstration PCB that is suitable for pin-to-pin compatible *TDA8953TH*, *TDA8954TH* or *TDA8955TH* NXP Semiconductors' devices. Extension "TH" is referring to the HSOP24 package.

The demonstration PCB can be used either in stereo Single Ended (SE) or in mono Bridge Tied Load (BTL) configuration operating from a symmetrical supply with a wide voltage range.

The necessary information for a quick start-up of the demonstration PCB is given in chapter 2. Chapter 5 show the results of the audio performance characterization. Schematic, BOM and layout is provided in chapter 6, 7 and 8.

Features

- Wide symmetrical supply voltage range
- Single Ended (SE) or Bridge Tied Load (BTL) output configuration
- Very high power capability
- Low THD+N
- Low noise
- AC-coupled differential inputs
- High efficiency
- Selectable Thermal Fold Back and current limiting to avoid audio interruptions
- Low power consumption in standby-mode
- Fixed frequency
- Diag functionality for Protections and Temperature (not for *TDA8953TH*)

Table 1. Selection table

Device	TDA8953TH	TDA8954TH	TDA8955TH
Supply range (V)	±12.5…±42.5	±12.5…±42.5	±12.5…±42.5
Typical supply voltage (V)	±41	±41	±37
Typical output power SE (W_{RMS})	2 x 210[1)]	2 x 210[1)]	2x150W[1)]
Typical output power BTL (W_{RMS})	1 x 420[2)]	1 x 420[2)]	1x300W[2)]
Iocp (A)	12.5	12.5	9.2
DIAG TEMP	NO	YES	YES
DIAG ALARM	NO	YES	YES

[1)] Note: Load: 4Ω
[2)] Note: Load: 8Ω

2. Setup demonstration PCB

Figure 1 is showing the TDA8953TH/54TH/55TH double layer demonstration PCB with screw terminals for connecting the power supply and speaker cables. The audio input signal must be applied using the cinch inputs.

External clock input

Test pin X6 can be used as input for an external clock. Test pin X7 should be used to connect the corresponding ground reference.

Specification of the external clock signal:

High level: 5V

Low level: 0V

$f_{osc(ext)}$: 500k – 1000kHz

Duty cycle: 10-90%

Rise time typical 50ns

Note: power stage switching frequency equal to $f_{osc(ext)}/2$

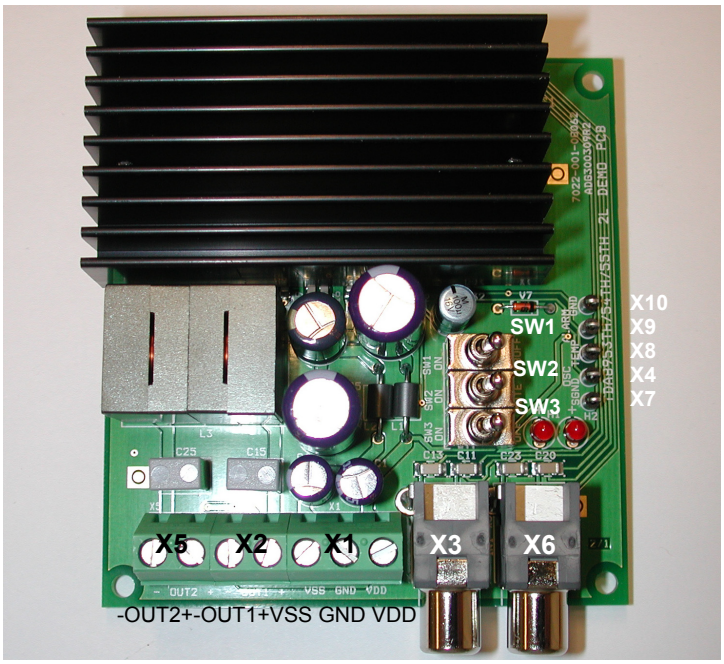


Fig 1. Setup demonstration PCB

2.1 I/O connector

Table 2. Input/output connector assignment

REF	TYPE	Pin	Label	Description
X1	Terminal block, screw	1	V_{SS}	Negative supply line
		2	GND	Ground
		3	V_{DD}	Positive supply line
X2	Terminal block, screw	1	OUT2 +	Ground
		2	OUT2 -	Active output 2
X3	Cinch plug	1	IN1	Input 1
		2	GND	Ground
X4	Test pin	1	Ext osc	External clock input
X5	Terminal block, screw	1	OUT1 +	Active output 1
		2	OUT1 -	Ground
X6	Cinch plug	1	IN2	Input 2
		2	GND	Ground
X7	Test pin	1	SGND	Signal ground
X8	Test pin	1	Temp alarm	Temp alarm
X9	Test pin	1	Diag alarm	Diag alarm
X10	Test pin	1	GND	GND

2.2 Jumper

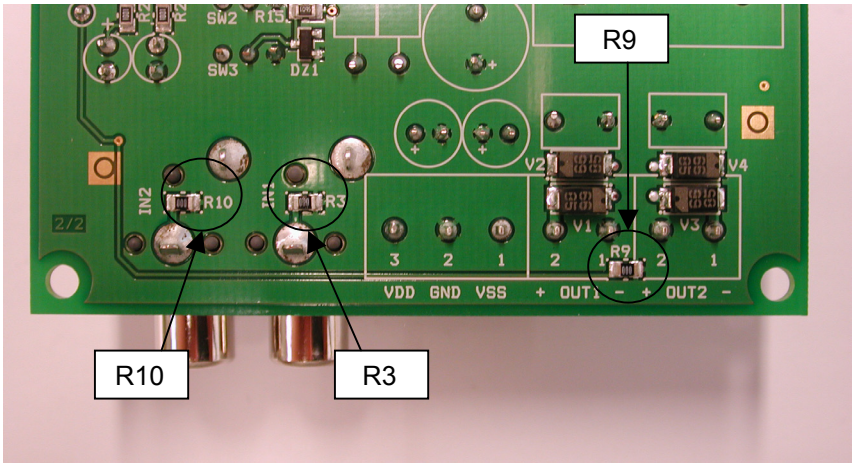


Fig 2. Jumper location demonstration PCB

Table 3. Jumper assignment

REF	TYPE	Description
R3	0Ω resistor	Jumper connection to ground
R9	0Ω resistor	Jumper connection to feedback ground. (FBGND)
R10	0Ω resistor	Jumper connection to ground

When the input source is properly grounded to the ground reference of the power supply on set level, it is necessary to remove jumpers R3 and R10 to avoid ground loops that can create noise issues.

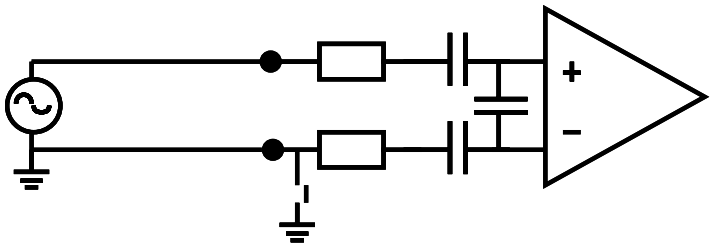


Fig 3. One ground reference on set level

2.3 Mode selection

Use the switches SW1, SW2 and SW3 to enter respectively standby, mute or operating mode.

Table 4. Modes

Mode	SW1	SW2	SW3
STANDBY	Don't care	Don't care	OFF
MUTE	Don't care	MUTE	ON
OPERATING With thermal foldback	ON	ON	ON
OPERATING without thermal foldback	TFB OFF	ON	ON

1. STANDBY mode
   The STANDBY mode is incorporated to reduce the power consumption.
2. MUTE mode
   In MUTE mode, the stabilizer will be enabled (internal logic biased). The power stage is enabled and starts switching. The gain is reduced to zero
3. OPERATING mode with thermal foldback
   In the OPERATING mode, the gain of the device is gradually increased to 30 dB per channel to avoid pop-noise due to DC output offset voltage (see figure 5). The complete start-up sequence will take less than 500 ms in a typical application. Thermal foldback is active.
4. OPERATING mode without thermal foldback
   In the OPERATING mode, the gain of the device is gradually increased to 30 dB per channel to avoid pop-noise due to DC output offset voltage (see figure 5). The complete start-up sequence will take less than 500 ms in a typical application. Thermal foldback is disabled.

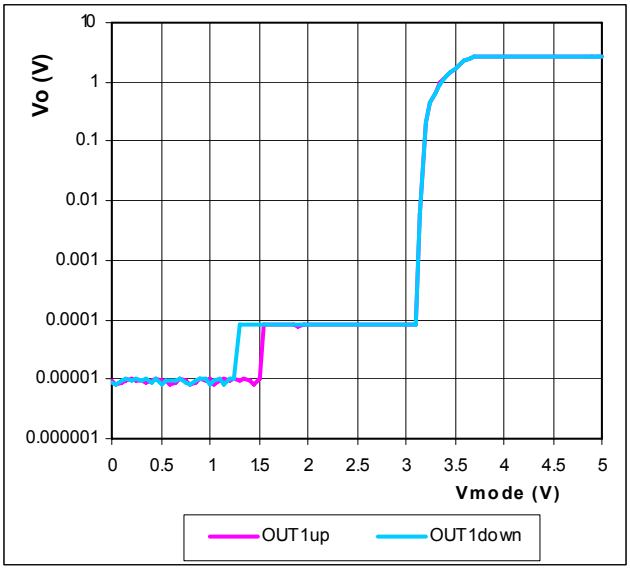


Fig 4. Output voltage vs. mode voltage

Vi: 100mVrms

2.4 Diagnostic

The TDA8954TH and TDA8955TH are both equipped with advanced diagnostic circuitry that shows activity of the protections (DIAG ALARM) or a temperature warning above 139°C (DIAG TEMP). The demo board is equipped with two LED's that show activity of both diagnostic lines. There are also two test points (X9 for DIAG ALARM, X8 for DIAG TEMP) that can be used to monitor the diagnostic lines with an oscilloscope. It is recommended to filter the two DIAG lines with a 100 Ohm resistor and 1nF capacitor to the local ground of the uC. The figure below shows how the diag circuitry can be connected to the uC on set level.

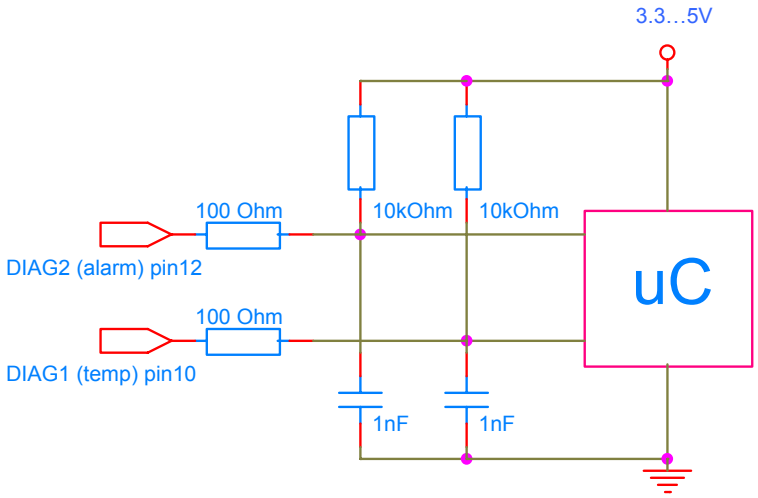


Fig 5. Recommended filtering of DIAG ALARM and DIAG TEMP

2.5 Speaker configuration and impedance

For a flat-frequency response (second order Butterworth filter) it is necessary to change the low pass filter components L3 and C15/C25 according to the speaker configuration and impedance. The table below is showing some practical example values for a resonance frequency of 50kHz:

Table 5. Filter component values

Configuration	Impedance (Ω)	L3 (μH)	C15 / C25 (nF)
SE	3 – 6	15	680
	4 – 6	22	470
	6 – 8	33	330
BTL	6 – 12	15	680
	8 – 12	22	470
	12 – 16	33	330

The boards are standard equipped with 15μH and 680nF for 2 x 4Ω SE or 1 x 8Ω BTL.

3. Limiting and protection features

The TDA8953TH/54TH/55TH devices utilize two advanced limiting features, respectively the Thermal Fold Back and cycle-by-cycle current limiting, to avoid audio holes (interruptions) during normal operation.

The Thermal Fold Back feature will reduce gradually the output power until the global junction temperature reaches the threshold level of 154°C (OTP). Therefore the amplifier junction temperature will always stay within the Safe Operating Area.

In addition to these limiting features the device has several protection features that makes the TDA8953TH/54TH/55TH family very robust during a fault condition.

The following protections are incorporated:

- Window Protection WP
- Under Voltage Protections UVP
- Over Voltage Protection OVP
- Unbalance Protection UBP
- Over Current Protection OCP
- Over Temperature Protection OTP
- Clock protection

4. Design considerations

4.1 Sil-Pad

For the optimal Sil-Pad selection three properties are of importance:

- Low thermal impedance
- Electrical insulation (package is referenced to VSS, heat sink needs to be grounded for good EMC performance)
- Gap filling properties to fill up the possible airspace present between the heat sink and IC to maximize the heat conducting area (SP1500ST and SP300P)

The sil pad listed below is recommended:

Type	Thickness (inch)	Thermal impedance (°C-in^2/W)[1)]
Sil-Pad 1500ST	0.008	0.37 – 0.20

[1)] Depending on pressure. Range: 10 – 200 PSI

4.2 Heat sink

The type number and brand of the used heat sink is: SK178, Fisher Elektronik. The length of the heat sink is: 62.5mm. This results in an R_{th} value of 5.5 K/W, (see below).

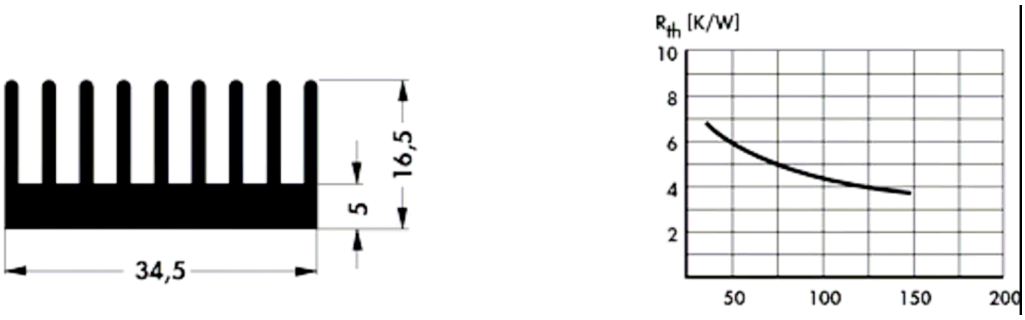


Fig 6. Heat sink SK495 dimension and Rth value as function of length

For mechanical stability and optimal EMC performance the heat sink is mounted with screws to the pcb. The heat sink is connected to the ground plane with 10Ω (R3) for a defined potential. It is also possible to AC-coupled the heat sink to the pcb. Therefore R3 needs to be removed and C35 (100nF) needs to be placed.

5. TDA8953TH/54TH performance

5.1 Quick performance figures TDA8953TH/54TH

Following low pass filter components are used for the measurements:
L1 = 15µH (*TOKO*) C6, C7 = 680nF, f_i=1kHz,T_{amb} = 25°C, internal clock 100nF across R8.

Table 6. Performance figures

Symbol	Parameters	Conditions	Typical	Unit
Po	RMS output power			
		R_L=3Ω SE , V_p=±39V, THD+N=0.5%	190	W
		R_L=3Ω SE , V_p=±39V,THD+N=10%	236	W
		R_L=4Ω SE , V_p=±41V, THD+N=0.5%	172	W
		R_L=4Ω SE , V_p=±41V, THD+N=10%	215	W
		R_L=8Ω BTL, V_p=±41V, THD+N=10%	430	W
THD+N	Total Harmonic Distortion and Noise	f_{IN}=1kHz, V_p=±41V, 22Hz-20kHz AES17 brick wall filter		
		R_L=3Ω SE, V_p=±39V, P_O =1W, f_i=1kHz	0.03	%
		R_L=3Ω SE, V_p=±39V, P_O =10W, f_i=1kHz	0.02	%
		R_L=3Ω SE, V_p=±39V, P_O =1W, f_i=6kHz	0.05	%
		R_L=3Ω SE, V_p=±39V, P_O =10W, f_i=6kHz	0.04	%
		R_L=4Ω SE, V_p=±41V, P_O =1W, f_i=1kHz	0.03	%
		R_L=4Ω SE, V_p=±41V, P_O =10W, f_i=1kHz	0.02	%

Symbol	Parameters	Conditions	Typical	Unit
		R_L=4Ω SE, V_p=±41V, P_O =1W, f_i=6kHz	0.05	%
		R_L=4Ω SE, V_p=±41V, P_O =10W, f_i=6kHz	0.08	%
		R_L=8Ω BTL, V_p=±41V, P_O =1W, f_i=1kHz	0.03	%
		R_L=8Ω BTL, V_p=±41V, P_O =10W, f_i=1kHz	0.006	%
		R_L=8Ω BTL, V_p=±41V, P_O =1W, f_i=6kHz	0.01	%
P	Power dissipation	Total application in idle, V_p=±41V	7.3	W
		TDA8954TH in idle, V_p=±41V	3.75	W
		R_L=4Ω; f_i=1kHz, V_p=±41V, P_o=2 x 210W	460	W
η	Efficiency total application	R_L=4Ω; f_i=1kHz, V_p=±41V, P_o=2 x 210W total application	91	%
		R_L=4Ω; f_i=1kHz, V_p=±41V, P_o=2 x 210W TDA8954TH	93	%
$G_{V(cl)}$	Closed loop voltage gain	V_i = 100mV_{rms}, R_i = 5.6kΩ, 2 x 4Ω SE	28.9	dB
$V_{n(o)}$	Noise output voltage	R_i = 5.6kΩ, cinch inputs shorted, int clock, V_p=±41V		
		R_L=3Ω SE, operating	155	μV
		R_L=3Ω SE, mute	87	μV
		R_L=4Ω SE, operating	165	μV
		R_L=4Ω SE, mute	96	μV
		R_L=8Ω BTL, operating	175	μV
		R_L=8Ω BTL, mute	105	μV
α_{cs}	Channel separation	P_o = 1W	-67	dB
f_{osc}	Oscillator frequency	R8 = 30kΩ	338	kHz

5.2 Performance curves TDA8953TH/54TH

Supply voltage: ±39V for SE 3Ω, ±41V for SE 4Ω and 8Ω BTL,
External clock frequency (when applied): 650kHz

Measurement bandwidth: 22Hz – 20kHz AES17

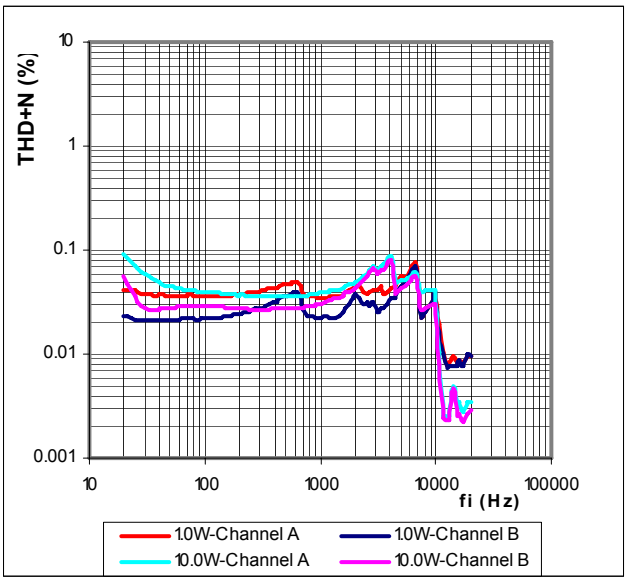


Fig 7. THD vs. Frequency, SE 3Ω, int clock

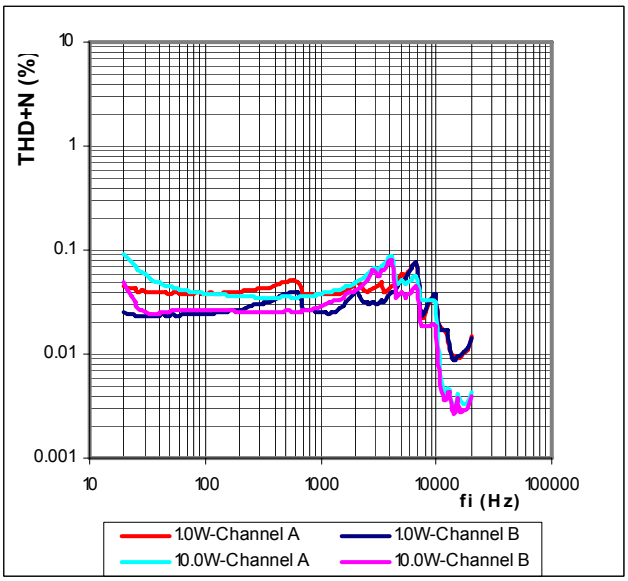


Fig 8. THD vs. Frequency, SE 3Ω, ext clock

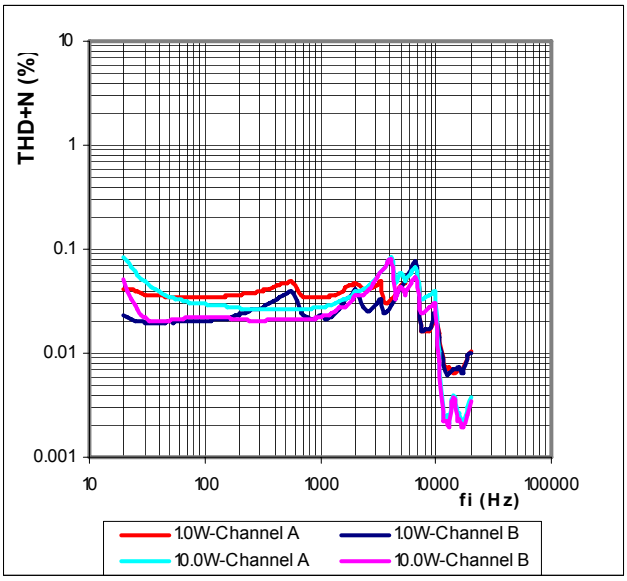


Fig 9. THD vs. Frequency, SE 4Ω, int clock

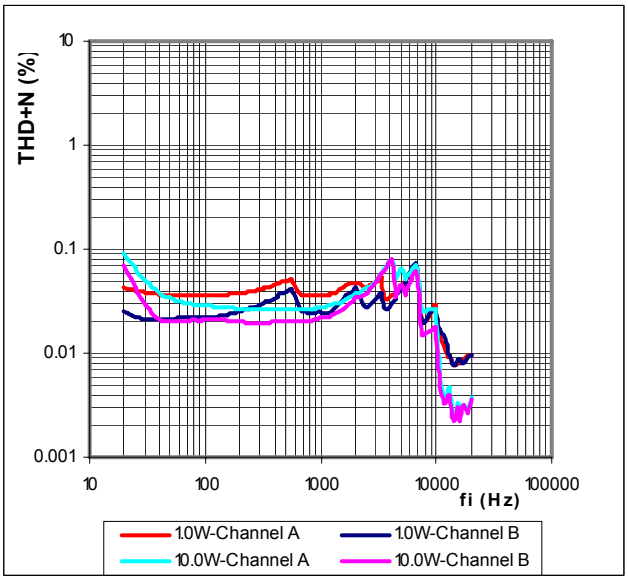


Fig 10. THD vs. Frequency, SE 4Ω, ext clock

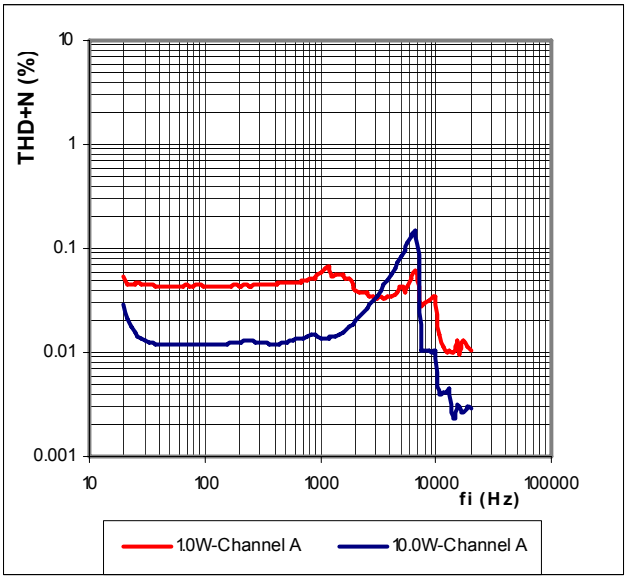


Fig 11.THD vs. Frequency, BTL 8Ω, int clock

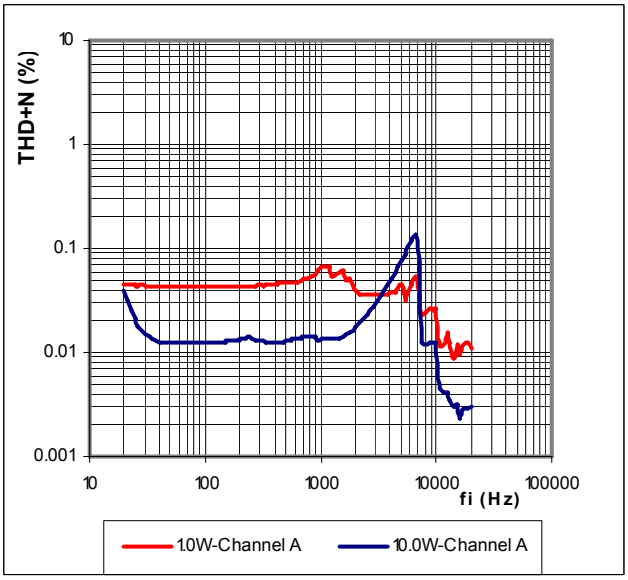


Fig 12.THD vs. Frequency, BTL 8Ω, ext clock

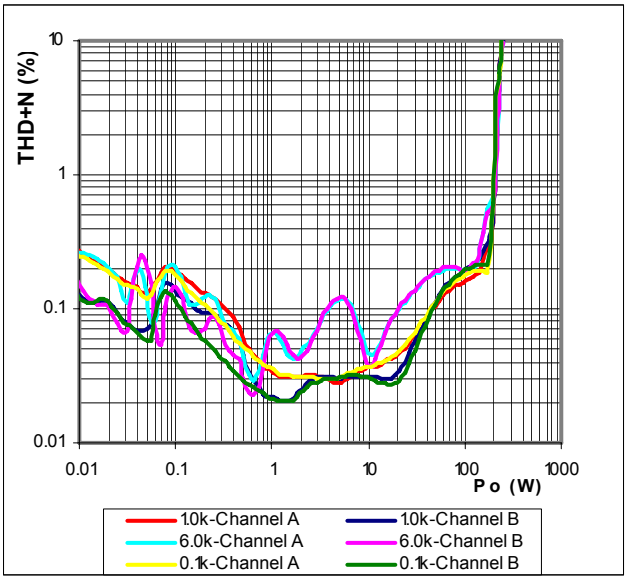


Fig 13.THD vs. Po, SE 3Ω, int clock

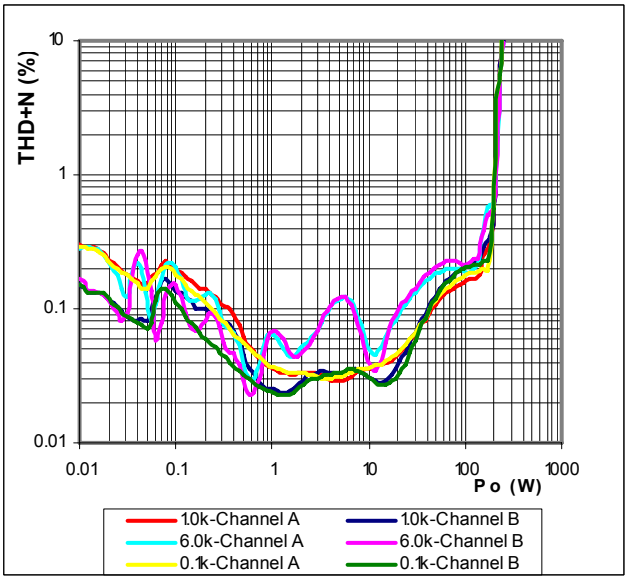


Fig 14.THD vs. Po, SE 3Ω, ext clock

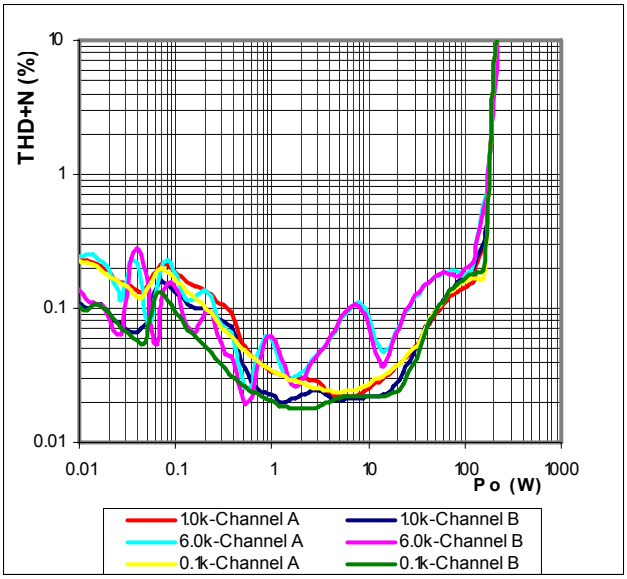


Fig 15.THD vs. Po, SE 4Ω, int clock

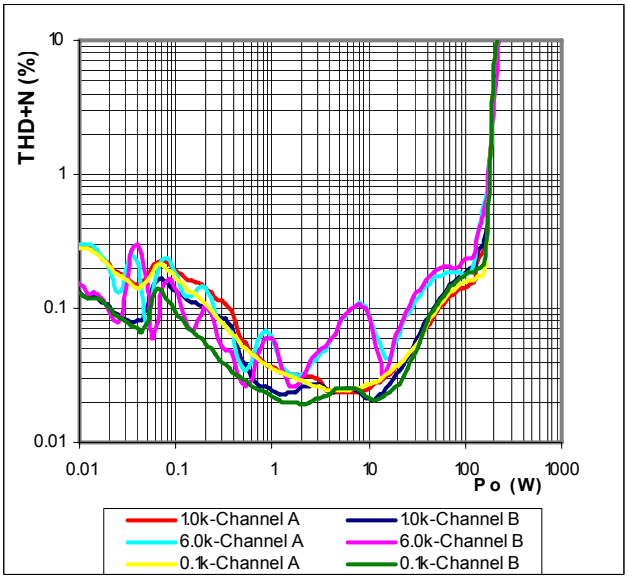


Fig 16.THD vs. Po, SE 4Ω, ext clock

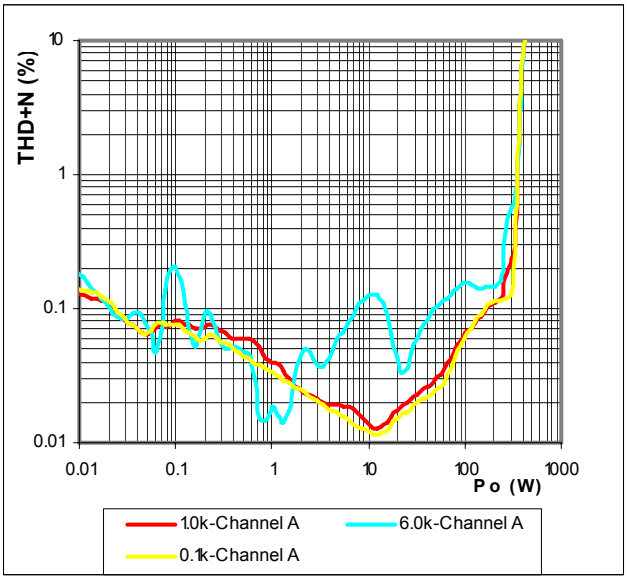


Fig 17.THD vs. Po, BTL 8Ω, int clock

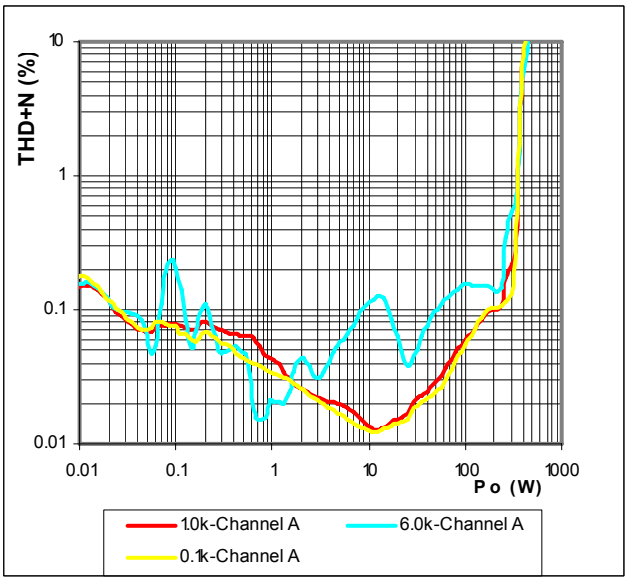


Fig 18.THD vs. Po, BTL 8Ω, ext clock

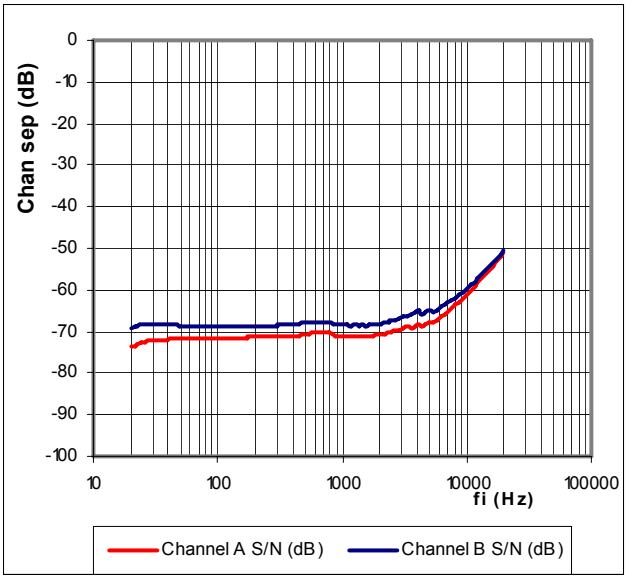


Fig 19.Channel separation, SE 3Ω, int clock, 1W

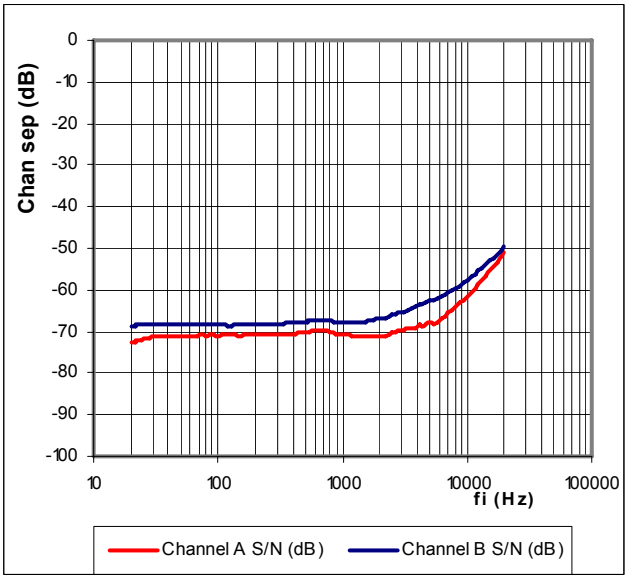


Fig 20.Channel separation, SE 3Ω, ext clock, 1W

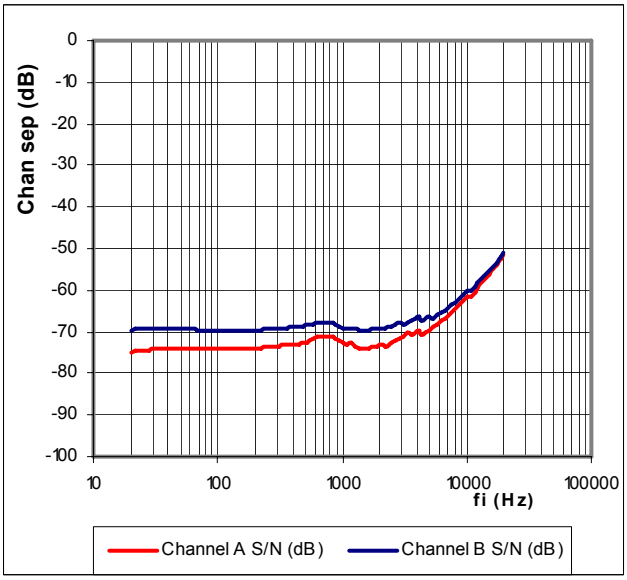


Fig 21.Channel separation, SE 4Ω, int clock, 1W

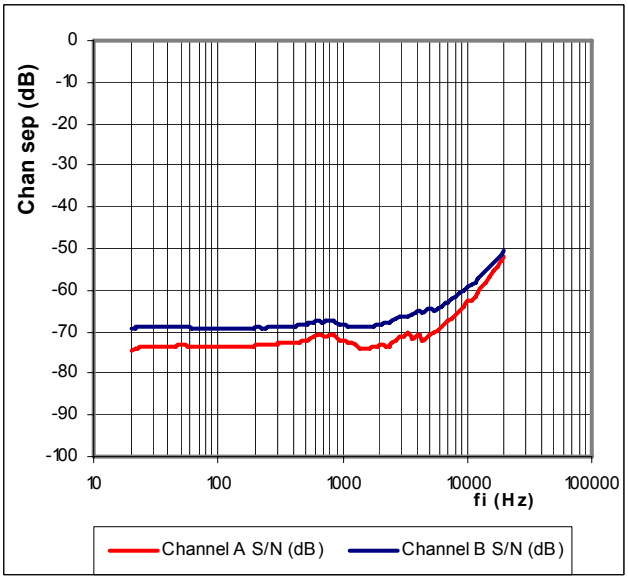


Fig 22.Channel separation, SE 4Ω, ext clock, 1W

Supply voltage: ±41V
Measurement bandwidth: <10Hz – 500kHz
L=15uH, C=680nF Vin=100mV

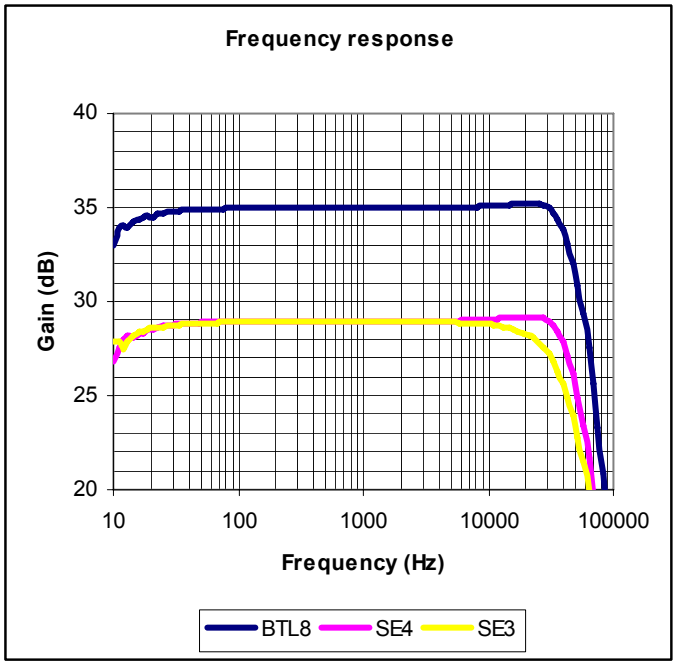


Fig 23.Frequency response

5.3 Output power performance TDA8953TH/54TH

Po vs. time

The selected heat sink and Sil-Pad are chosen to fulfill the following target:
- Rated power of 2x210W (2 x 4Ω SE) for at least 10s (after 30min in idle) at Vp=±41V
- 1/4 rated power, which is 2 x 52.5W (2 x 4Ω SE) after 10 min.

3Ω SE 1x Prated and 1xPrated/8 is also tested.

External clock frequency: 650kHz
Sil-Pad used: Sil-Pad 1500ST
Heat sink used: SK495

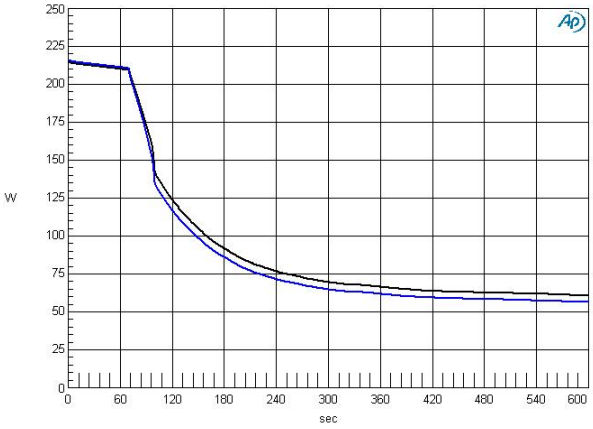


Fig 24.Po/chan vs. time TDA8954TH/N1B ±41V, 4Ω 2xPrated

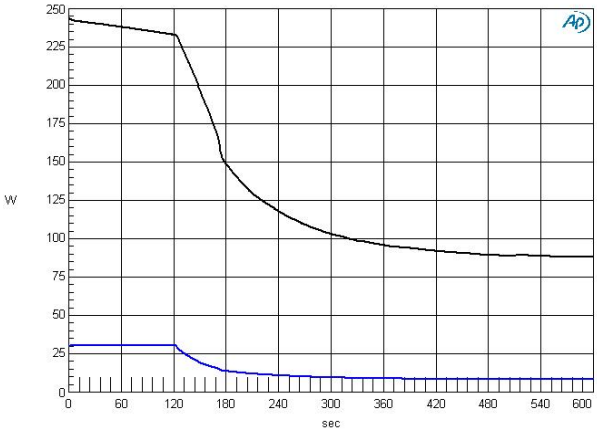
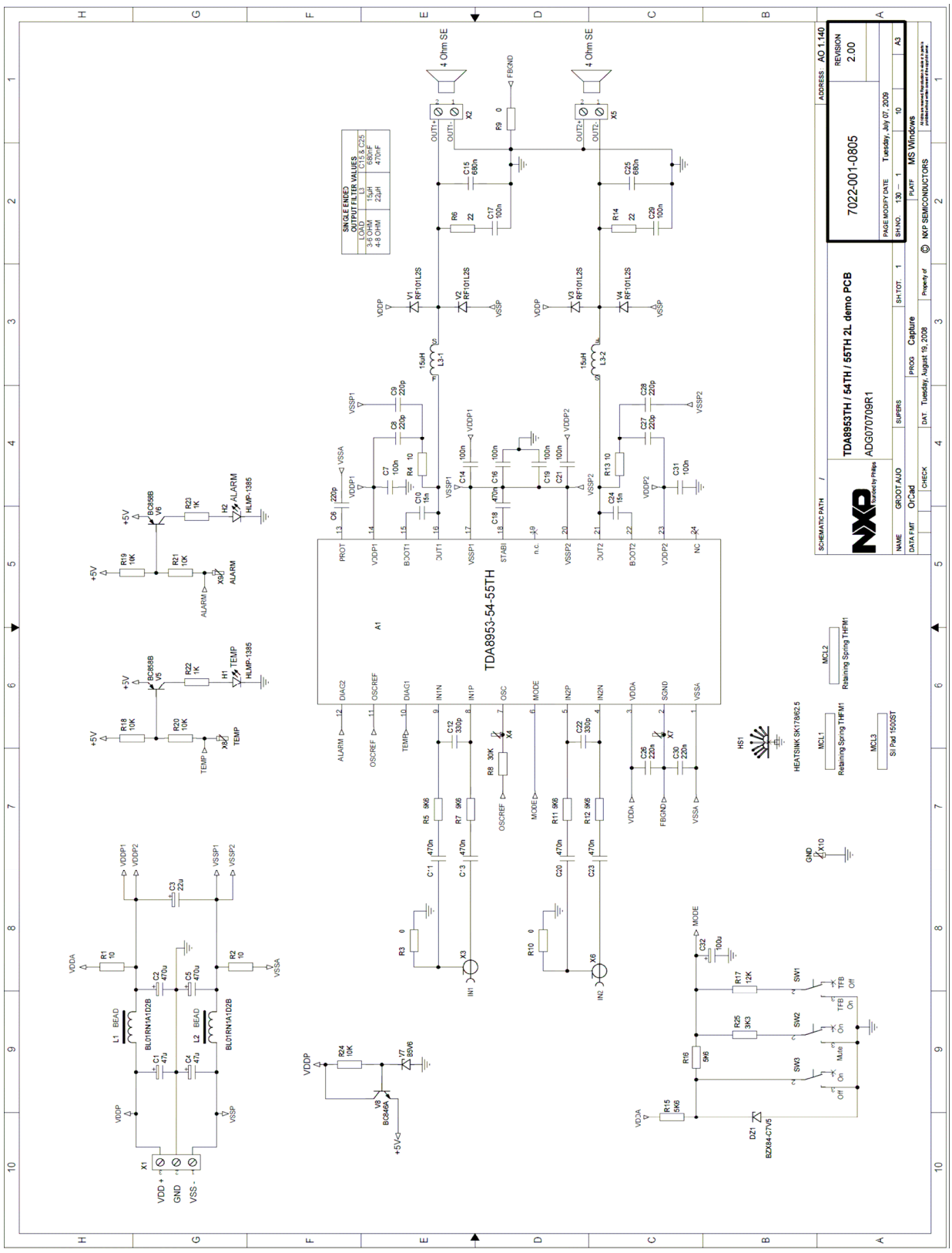


Fig 25.Po/chan vs. time TDA8954TH/N1B ±39V, 3Ω 1xPrated 1xPrated/8

6. Schematic – 7022-001-0805



7. Bill Of Materials – 7022-001-0805

Item #	Part Reference	Description	Manufacturer	Manufacturer Part Number	PCB Footprint
1	A1				HSOP24-SOT566-3
2	C1 C4	47u/20%/50V	Panasonic	ECA1HM470	EV6.3_11_2.5MM
3	C2 C5	470u/20%/50V	Panasonic	ECA1HM471	EV10_20_5MM
4	C3	22u/20%/100V	Panasonic	EEUFC2A220	EV8_11.5_3.5MM
5	C6	220p/2%/50V	Philips	2222 861 74221	C0805
6	C7 C16 C19 C31	100n / 10% / 50V	Phycomp / Yageo	2238 580 15649	C0805
7	C8 C9 C27 C28	220P / 5% / 100V	AVX	08051A221JAT2A	C0805
8	C10 C24	15n / 10% / 50V	Philips	2222 580 15638	C0805
9	C11 C13 C20 C23	470n/10%/16Vdc	AVX	1206YC474KAT1A	C1206
10	C12 C22	330p/2%/50V	Philips	2222 861 74331	C0805
11	C14 C17 C21 C29	100n/10/100V	Kemet	C1206F104K1RAC	C1206
12	C15 C25	680n / 10% / 63V	BC components	2222 370 11684	MKT_2E_4
13	C18	470n / 10% / 50V DC	Kemet	C0805F474K5RAC	C0805
14	C26 C30	220n / 10% / 50V DC	Kemet	C0805C224K5RAC	C0805
15	C32	100u / 20% / 16V	BC components	2222 036 55101	EV5.5_12_1E
16	DZ1	BZX84-C7V5	NXP	BZX84-C7V5	SOT23
17	H1 H2	Led / HLMP-1385/RED	Hewlett Packerd	HLMP-1301-G0000	F078C
18	HS1	HEATSINK SK178/62.5	Fisher Elektronic	SK178/62.5	HEATSINK-SK178-62.5
19	L1 L2	Bead Inducto- BL01RN1A1D2B	Murata	BL01RN1A1D2B	CHOKE BL01
20	L3	Dual Coil 15uH	TOKO	DAEPWG-M255	TOKO-DAEPW
21	MCL1 MCL2	Retaining Spring THFM1	Fisher Electronik	THFM1	CABLE-TIE-MOUNT
22	MCL3	Sil Pad 1500ST (Insulator)	The Bergquist Company	Sil Pad 1500ST	
23	R1 R2	10E / 1% / 0.1W	Philips	2322 734 61009	R0805
24	R3 R9 R10	0E / 5% / 0.125W	Phycomp	2322 730 91002	R0805
25	R4 R13	10E / 2% / 0.25W	Welwyn	WCR 1206 10R 2%	R1206
26	R5 R7 R11 R12 R15 R16	5K6 / 1% / 0.1W	Philips	2322 734 65602	R0805
27	R6 R14	22E / 5% / 1W	Yageo	2322 702 70229	R2512
28	R8	30K / 1% / 0.1W	Philips	2322 734 63003	R0805
29	R17	12K / 1% / 0.1W	Philips	2322 734 61203	R0805
30	R18-R21 R24	10K / 1% / 0.1W	Philips	2322 734 61003	R0805
31	R22 R23	1K / 1% / 0.1W	Philips	2322 734 61002	R0805
32	R25	3K3 / 1% / 0.1W	Philips	2322 734 63302	R0805
33	SW1-SW3	Switch SPDT ATE1D	Knitter	SPDT ATE 1 D	SWITCH ATE1
34	V1-V4	RF101L2S/1A/200V	Rohm	RF101L2S	SOD106
35	V5 V6	BC858B	Infineon	BC858B	SOT23-BEC
36	V7	BZX79-B5V6	Philips	9331 668 20113	DO35_3E
37	V8	BC846A	Philips	7322 079 92581	SOT23-BEC
38	X1	Vertical PCB Mounted Screw Terminal MKDS 1.5/3-5.08I 3P	Phoenix	1715734	SCREW-TERMINAL-1715XXX-5.08PITCH-3P
39	X2 X5	Vertical PCB Mounted Screw Terminal MKDS 1.5/2-5.08I 2P	Phoenix	1715721	SCREW-TERMINAL-1715XXX-5.08PITCH-2P
40	X3 X6	Phono Conn Black WBTOR-1	Lumberg	WBTOR1 BLACK	PHONE-CONN-RCA
41	X4 X7-X10	Isolated Testpin	Vero Electronic	20-2137D	ISO-TESTPIN

8. PCB layout – 7022-001-08062

Double layer PCB 75mm x 80mm

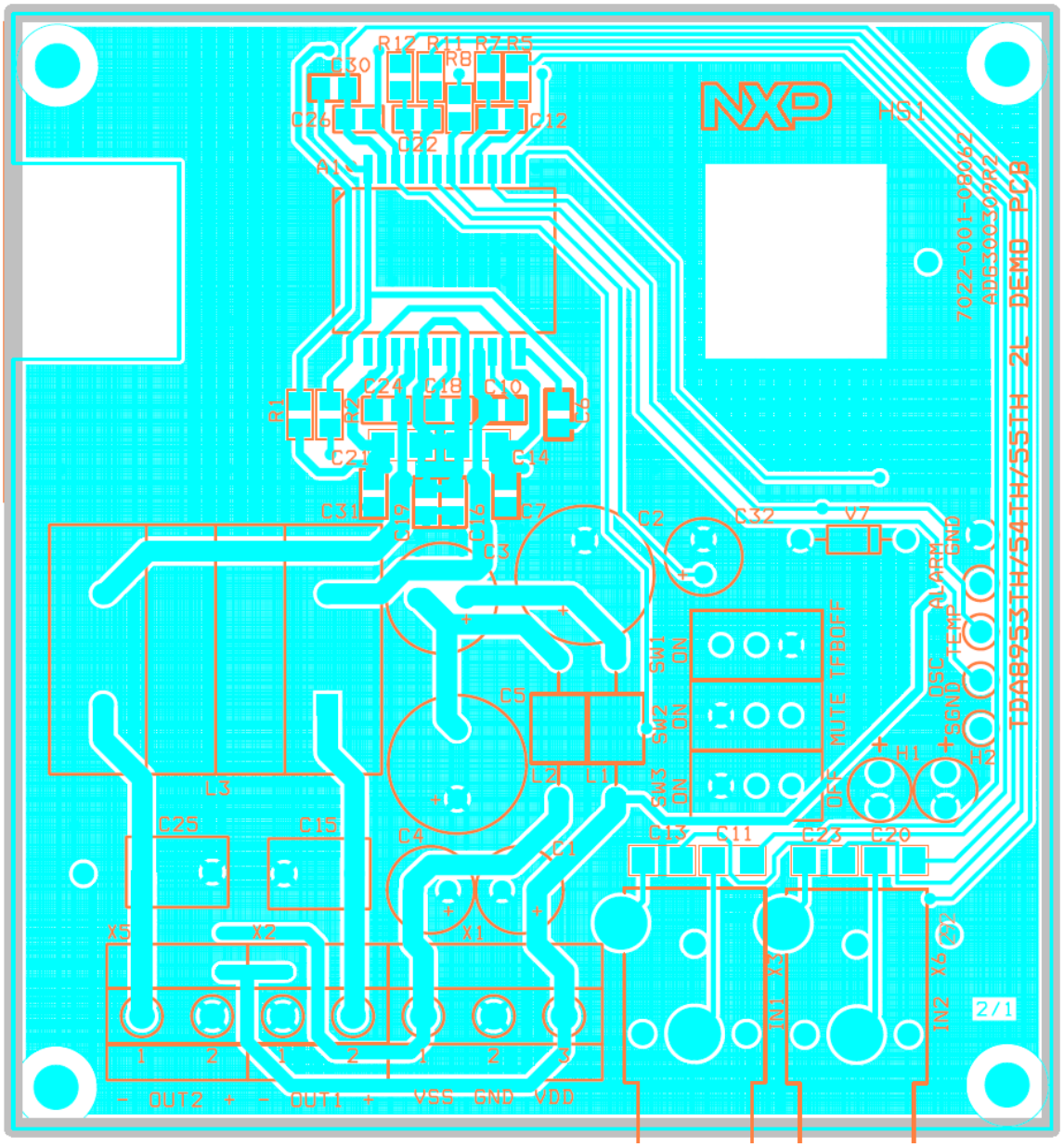


Fig 26.Top layer (top view)

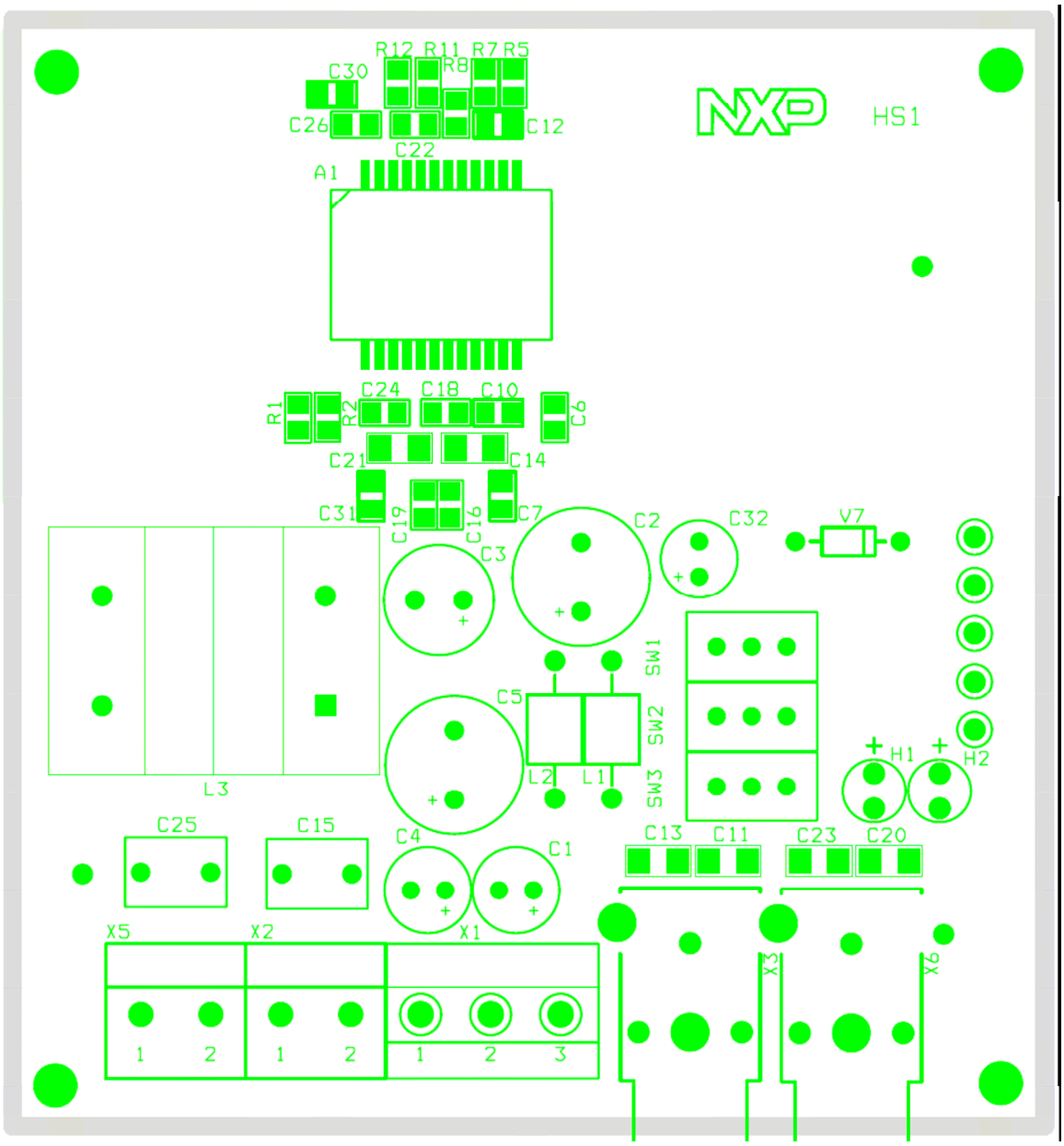


Fig 27.Assembly top (top view)

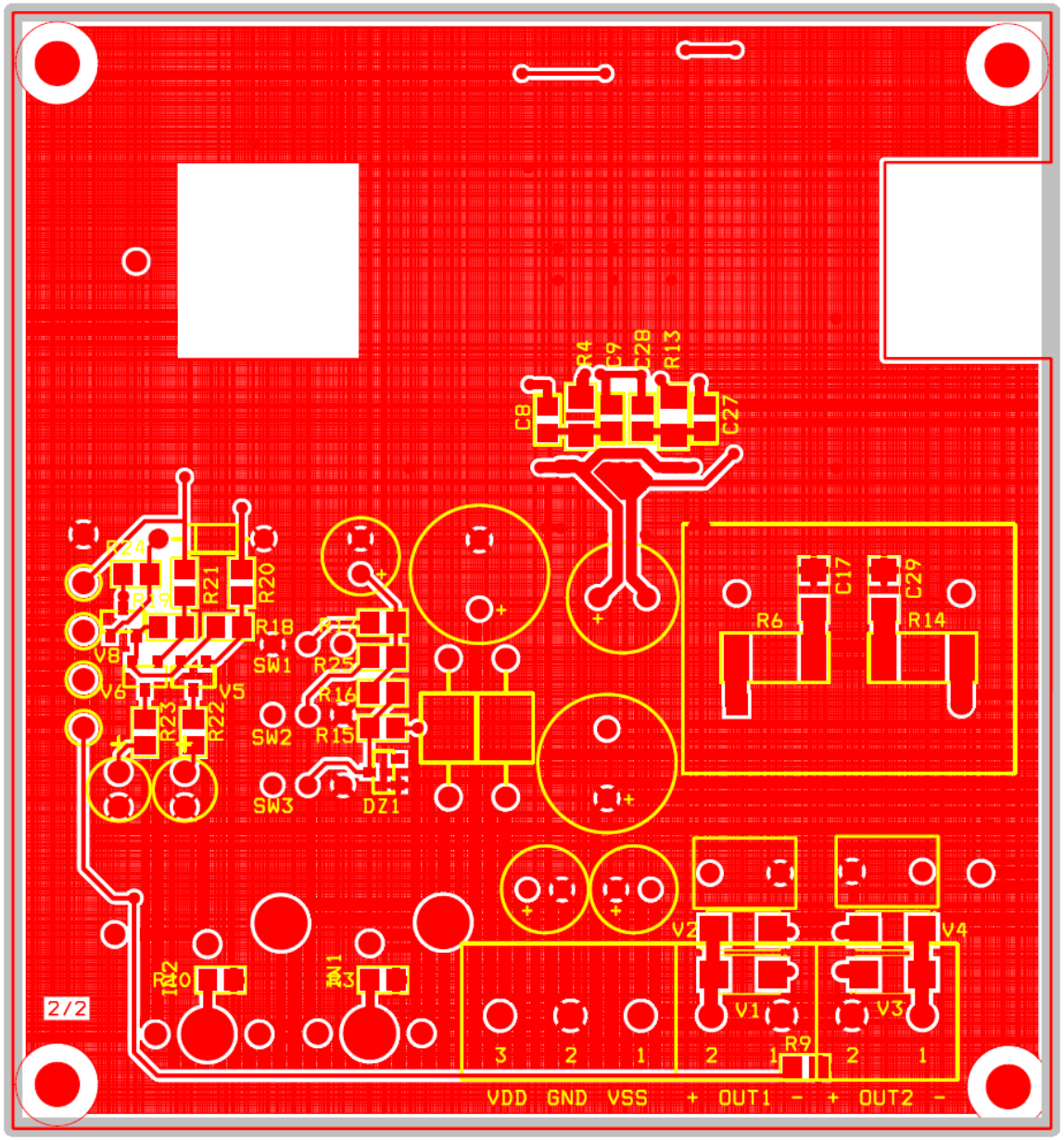


Fig 28.Copper bottom layer (Bottom view)

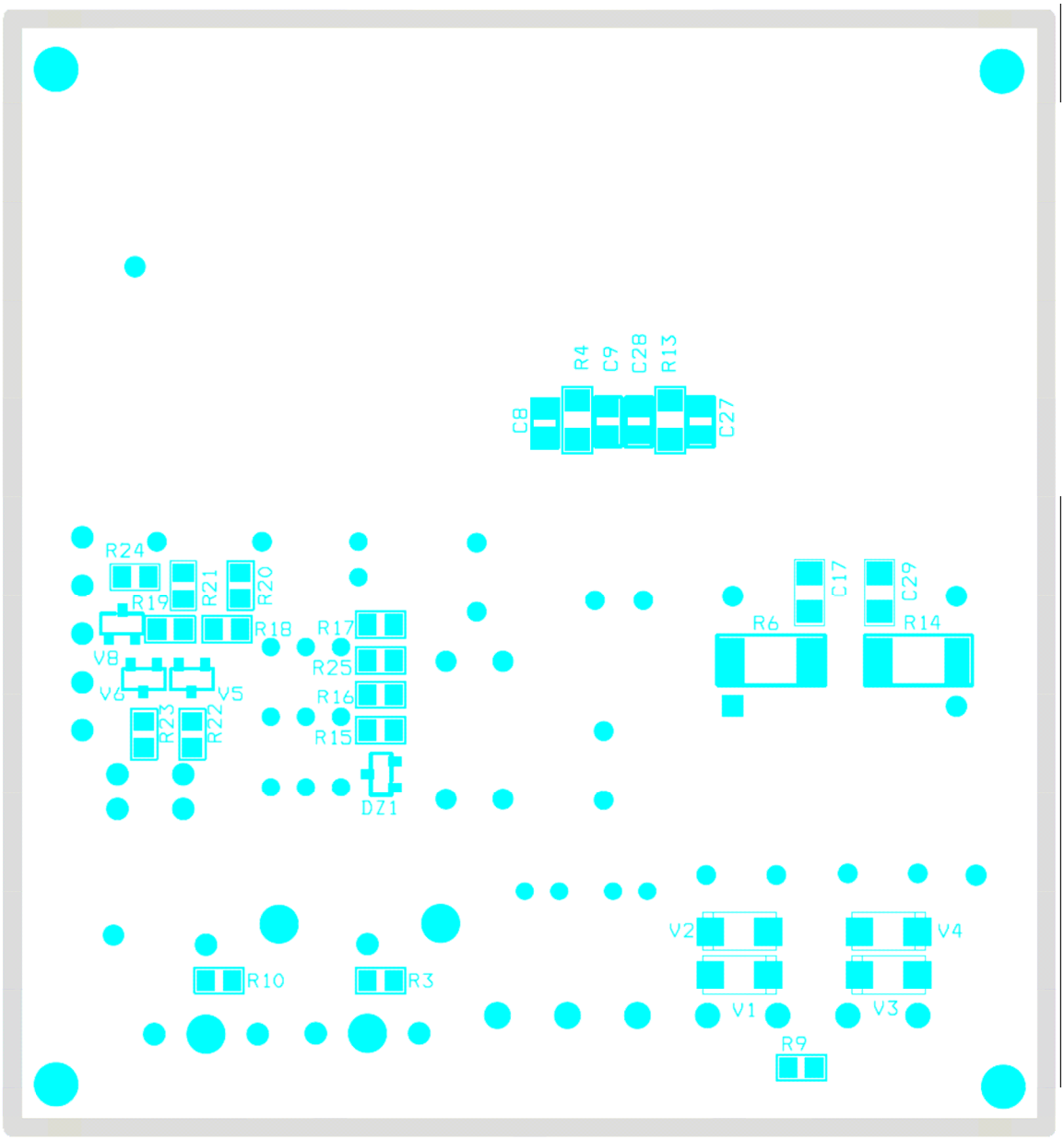


Fig 29.Assembly bottom (Bottom view)

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10. Contents